

Specification for Approval

PRODUCT NAME : RGS08096016BW001
PRODUCT NO.: 9913701000
PART NUMBER: PMO13701

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2005. 12. 29	
A01	<ul style="list-style-type: none"> ■ Transfer from X version ■ Add the information of module weight ■ Modify lifetime specification ■ Add the operating conditions for different luminance ■ Add the panel electrical specification ■ Modify the CIE specification ■ Modify the reliability test conditions ■ Add the packing specification 	2006. 03. 20	Page 5, 6, 7, 8, 15, 17 & 21
A02	<ul style="list-style-type: none"> ■ Modify features ■ Modify lifetime specification ■ Modify panel electrical specifications – current, power consumption, luminance, CIE tolerance & contrast setting 	2006. 07. 31	Page 4, 6 & 8

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Blue monochrome Small Molecular Passive Organic Light Emission Diode.
- Panel matrix : 96*16
- Driver IC : SSD0300
- Excellent Quick response time : 10 μ s
- Extremely thin thickness for best mechanism design : 1.65mm.
- High contrast : 500:1
- Wide viewing angle : 160°
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral Interface and I²C interface.
- Wide range operating temperature : -40 to 70 °C
- **Anti-glare polarizer.**

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x 16 (H)	dot
2	Dot Size	0.2 (W) x 0.2 (H)	mm ²
3	Dot Pitch	0.22 (W) x 0.22(H)	mm ²
4	Aperture Rate	83	%
5	Active Area	21.1 (W) x 3.5 (H)	mm ²
6	Panel Size	26 (W) x 9.2 (H)	mm ²
7	Panel Thickness	1.65 ± 0.1	mm
8	Module Size	26 (W) x 23.2 (H) x 1.65 (D)	mm ³
9	Diagonal A/A size	0.8	inch
10	Module Weight	0.84 ± 10%	gram

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	$T_a = 25^{\circ}\text{C}$	
Supply Voltage (V_{CC})	8	16	V	$T_a = 25^{\circ}\text{C}$	
Operating Temp.	-40	70	$^{\circ}\text{C}$		
Storage Temp	-40	85	$^{\circ}\text{C}$		
Humidity		85	%		
Life Time	6,800	-	Hrs	140 cd/m ² , 50% checkerboard	Note (1)
Life Time	8,000	-	Hrs	120 cd/m ² , 50% checkerboard	Note (2)
Life Time	9,600	-	Hrs	100 cd/m ² , 50% checkerboard	Note (3)

Note:

(A) Under $V_{CC} = 10\text{V}$, $T_a = 25^{\circ}\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 140 cd/m² :

- Contrast setting : 0x8A
- Frame rate : 85Hz

(2) Setting of 120 cd/m² :

- Contrast setting : 0x76
- Frame rate : 85Hz

(3) Setting of 100 cd/m² :

- Contrast setting : 0x5D
- Frame rate : 85Hz

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

($V_{SS}=0V$, $V_{DD}=2.25$ to $3.3V$, $T_a=25^{\circ}C$)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Logic operating voltage	-	2.4	2.7	3.5	V
V_{CC}	OLED operating voltage	-	9.5	10	10.5	V
V_{IH}	High logic input voltage	-	$0.7V_{DD}$	-	V_{DD}	V
V_{IL}	Low logic input voltage	-	V_{SS}	-	$0.3V_{DD}$	V
V_{OH}	High logic output voltage	$I_{OH} = -0.1mA$	$0.85V_{DD}$	-	V_{DD}	V
V_{OL}	Low logic output voltage	$I_{OL} = +0.1mA$	V_{SS}	-	$0.15V_{DD}$	V
I_{IL}	Input leakage current	$V_{IN}=V_{DD}$ or V_{SS}	-1.0	-	+1.0	μA

Note 1: $V_{DD}=2.7V$; $V_{CC}= 10V$; Frame rate=85Hz ; No panel attached.

Note 2: The V_{CC} input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		3	4	mA	All pixels on (1)
Standby mode current		0.2	0.4	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		30	40	mW	All pixels on (1)
Standby mode power consumption		2	4	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	100	120		cd/m ²	Display Average
Standby mode Luminance		10		cd/m ²	Display Average
CIE _x (Blue)	0.10	0.14	0.18		x, y (CIE 1931)
CIE _y (Blue)	0.20	0.24	0.28		
Dark Room Contrast	500:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

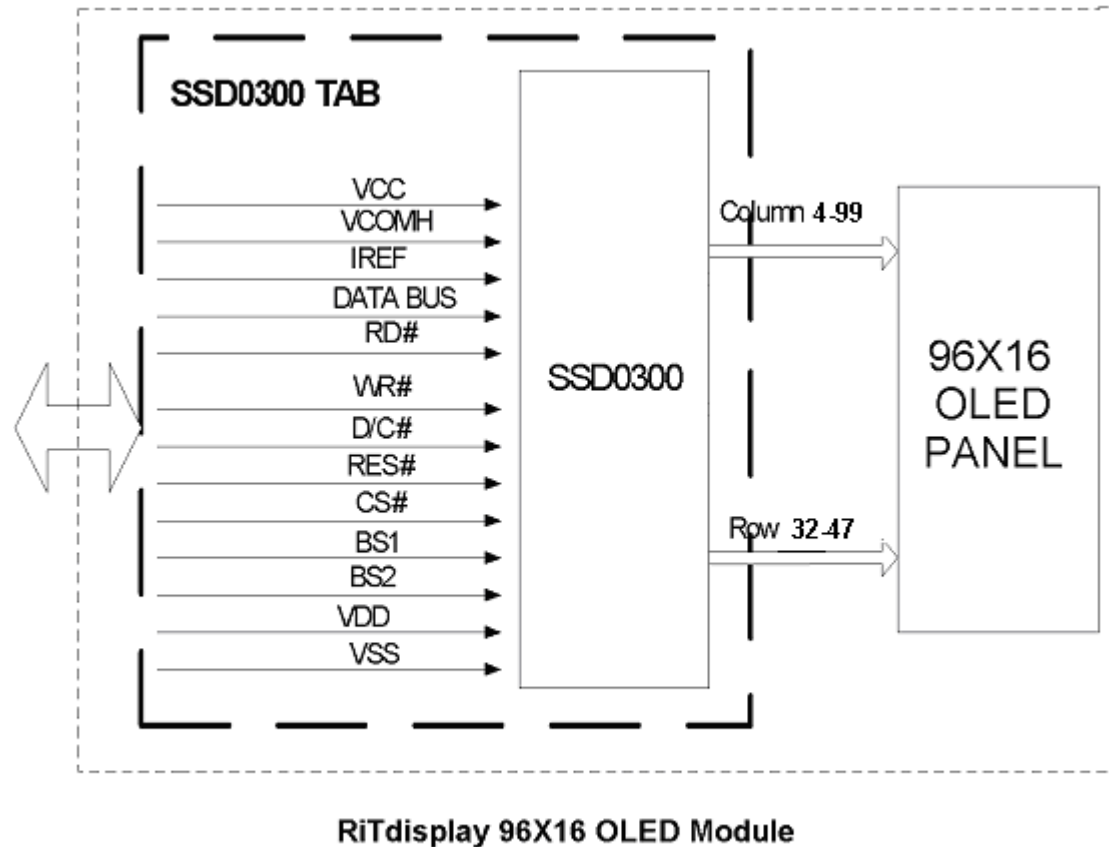
- Driving Voltage : 10VDC
- Contrast setting : 0x76
- Frame rate : 85Hz

(2) Standby mode condition :

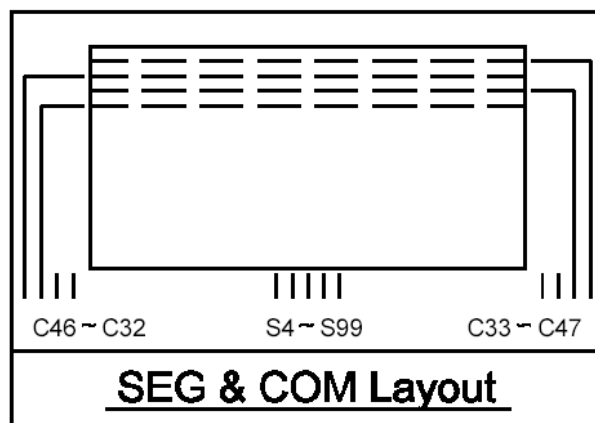
- Driving Voltage : 10VDC
- Contrast setting : 0x04
- Frame rate : 85Hz

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

Pin No.	Pin Name	Description
1	NC	No connection.
2	VSS	This is a ground pin.
3	TEST5	Reserved pins. No connection and should be left open.
4	TEST4	
5	TEST3	
6	TEST2	
7	TEST1	
8	NC	No connection.
9	NC	No connection.
10	NC	No connection.
11	VDD	Voltage source input for logic circuit.
12	BS1	MCU interface selection input. In I ² C mode, it should be pulled logic high.
13	BS2	MCU interface selection input. In I ² C mode, it should be pulled logic low.
14	NC	No connection.
15	CS#	It should be tied to VSS.
16	RES#	Hardware reset signal input pin. Low active.
17	D/C#	It serves as SA0 (slave address bit). It should be tied to logic high or low when slave address was defined.
18	WR#	It should be tied to VSS.
19	RD#	It should be tied to VSS.
20	D0	SCL; Serial clock input pin for I ² C interface application.
21	D1	SDA; Serial data input/output pins. D2 and D1 serve as SDA _{out} and SDA _{in} . They should be tied together in I ² C interface application.
22	D2	
23	D3	They should be tied to VSS.
24	D4	
25	D5	
26	D6	
27	D7	
28	IREF	A resistor should be connected between this pin and V _{ss} .
29	VCOMH	A capacitor should be connected between this pin and V _{ss} .
30	VCC	Voltage source input for OLED operating.
31	NC	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed.

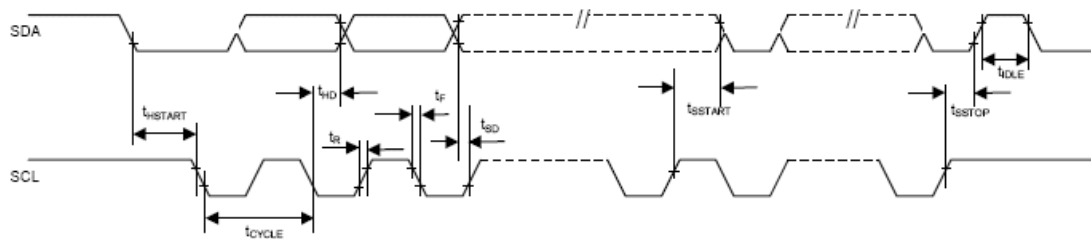
The size of the RAM is $104 \times 48 = 4992$ bits.

		OUT	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG101	SEG102	SEG103	SEG104
COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7	PAGE 0	D0													
		D1													
		D2													
		D3													
		D4													
		D5													
		D6													
		D7													
COM8 COM9 COM10 COM11 COM12 COM13 COM14 COM15	PAGE 1	D0													
		D1													
		D2													
		D3													
		D4													
		D5													
		D6													
		D7													
COM16 COM17 COM18 COM19 COM20 COM21 COM22 COM23	PAGE 2	D0													
		D1													
		D2													
		D3													
		D4													
		D5													
		D6													
		D7													
COM32 COM33 COM34 COM35 COM36 COM37 COM38 COM39	PAGE 4	D0													
		D1													
		D2													
		D3													
		D4													
		D5													
		D6													
		D7													
COM40 COM41 COM42 COM43 COM44 COM45 COM46 COM47	PAGE5	D0													
		D1													
		D2													
		D3													
		D4													
		D5													
		D6													
		D7													

7.5 INTERFACE TIMING CHART

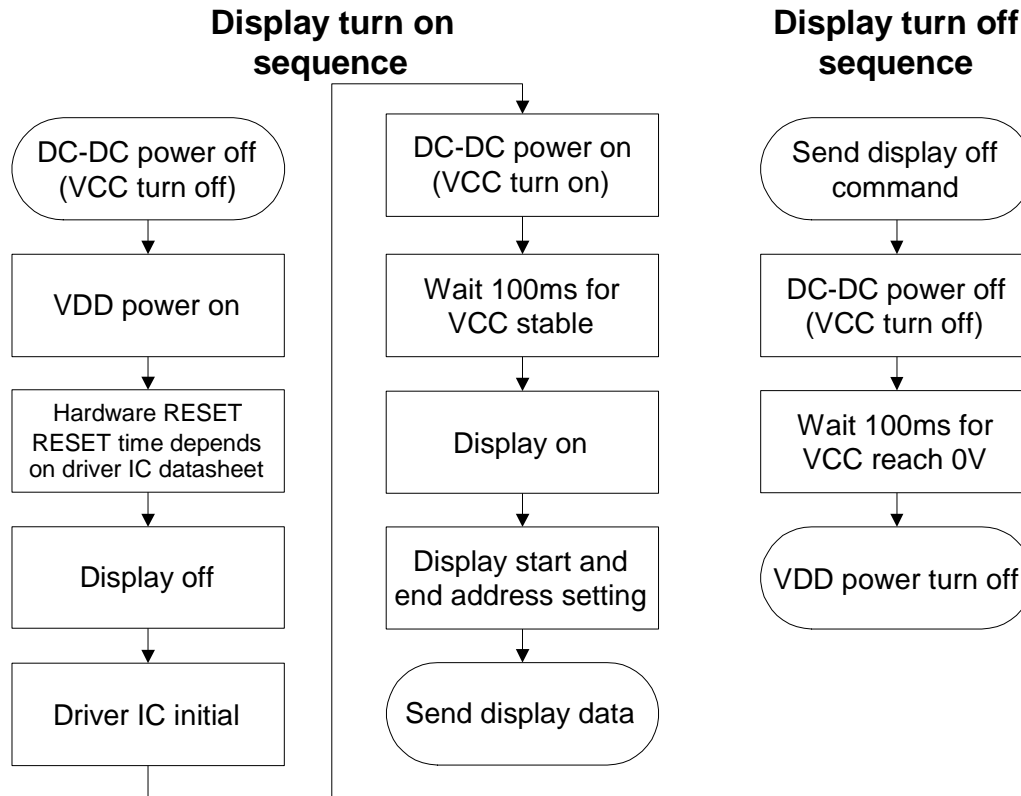
I²C Interface Timing Characteristics ($V_{DD}-V_{SS}=2.4$ to $3.5V$, $T_A=-40$ to $85^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us



8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



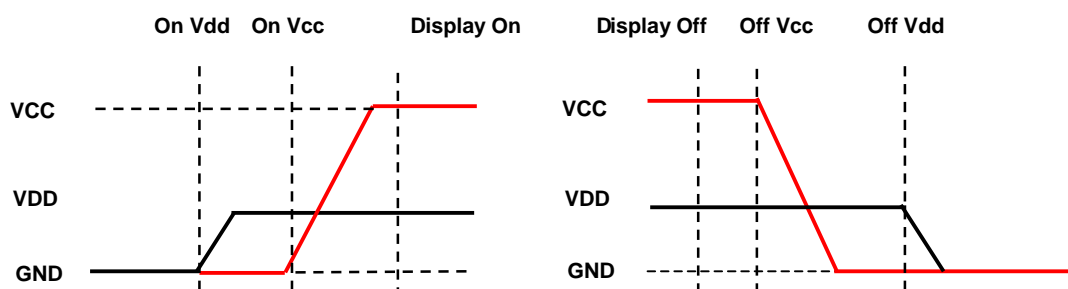
To protect OLED panel and extend the panel lifetime, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources turn on/off.

Power up Sequence:

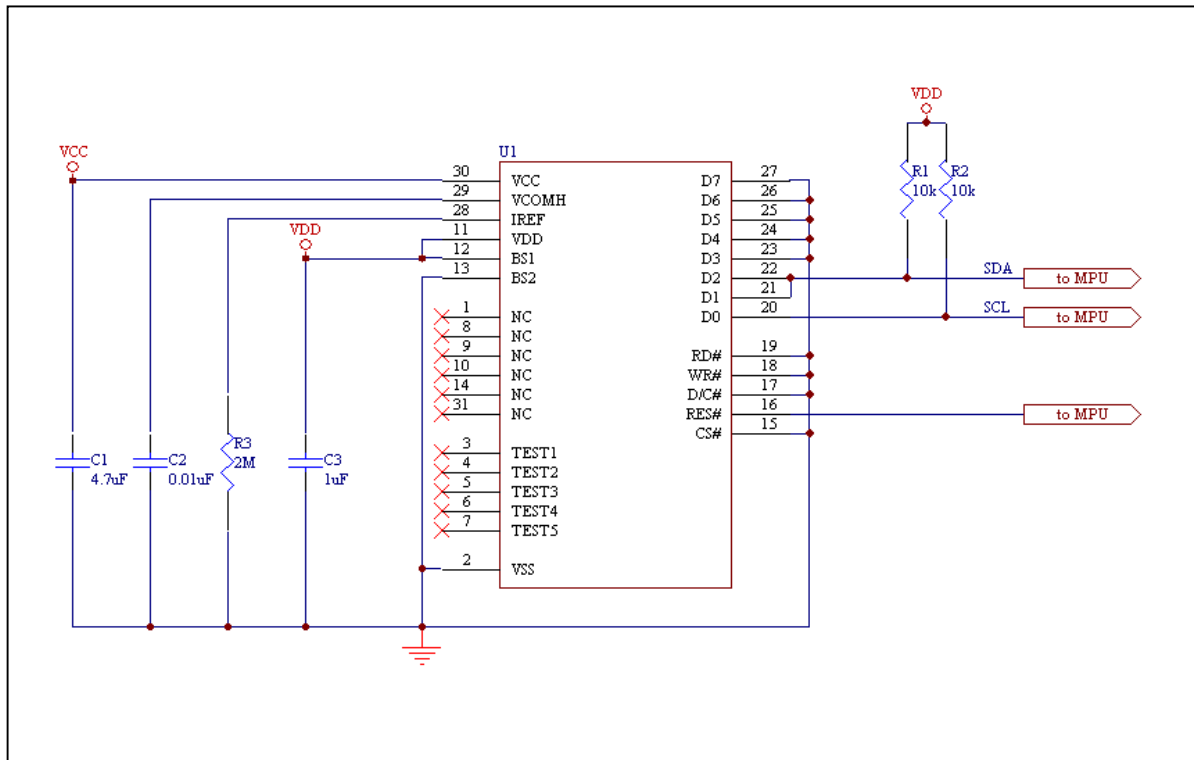
1. Power up Vdd
2. Hardware RESET
3. Send display off command
4. Power up Vcc
5. Delay 100ms (when Vcc is stable)
6. Send Display on command

Power down Sequence:

1. Send Display off command
2. Power down Vcc
3. Delay 100ms (When Vcc is reach 0 and panel is completely discharges)
4. Power down Vdd



8.2 APPLICATION CIRCUIT



8.3 COMMAND TABLE

Please reference the IC data sheet.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within $\pm 50\%$ of initial value.

[illegible]

11. PACKING SPECIFICATION

Revision	Date	Note
01	12/27/2005	Packing Tray Instruction

① P13701 Module
P/N: 9613071000
Face Down
旋轉放置

② Packing Tray
330x270x11mm, t=0.7mm
P/N: 3008000054

③ EPE Cover Foam
279.6x226.6x1mm
P/N: 3002000075

④ 4G 矽膠乾燥劑 (不織布)
P/N: 30000000500

⑤ 真空包裝袋 ONY/LDPE
480x285x90mm
P/N: 30030000012
抽真空6秒, 壓力170

⑥ Antistatic Bubble Bag
420x(350+450)mm
P/N: 30030000013

⑦ Pizza Box
345x285x88mm, B浪
P/N: 30010000005

⑧ 單色 Carton
385x305x203mm, AB浪
P/N: 30000000009

⑨ Label
P/N: 30060000000
x1 pcs

⑩ Label
P/N: 30060000000
x2 pcs

Item	Part No.	Description	QTY
1	9613071000	P13701 Module Assy	640
2	3008000054	Tray 330x270x11mm, PET, t=0.7mm	24
3	3002000075	EPE Cover Foam 279.6x226.6x1mm	40
4	30000000500	4G 矽膠乾燥劑 (不織布)	10
5	30030000012	真空包裝袋 480x285x90mm	2
6	30030000013	Antistatic Bubble Bag 420x(350+450)mm	2
7	30010000005	Pizza Box 345x285x88, B浪	2
8	30000000009	單色 Carton, 385x305x203mm	1
9	30060000000	Label	3
10	30080000125	封箱膠帶, W=48mm, L=910cm	

General		Tolerance		CONFIDENTIAL		Scale		Unit		Sheet		PROJECT CODE	
Length (mm)	Width (mm)	Height (mm)	Tolerance (mm)	M.E.	E.E.	Module	Spec.	mm	1/1	Approved	REVISION	Part Name	Revision
0 ~ 8	±0.1	±0.2	±0.3	Iven Lee	Paul Chang	Module	Spec.	mm	1/1	Approved	01	Packing Tray Instruction	01
8 ~ 25	±0.2	±0.3	±0.4									9913701000	01
25 ~ 50	±0.3	±0.4	±0.5										

RiTdisplay Corporation

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

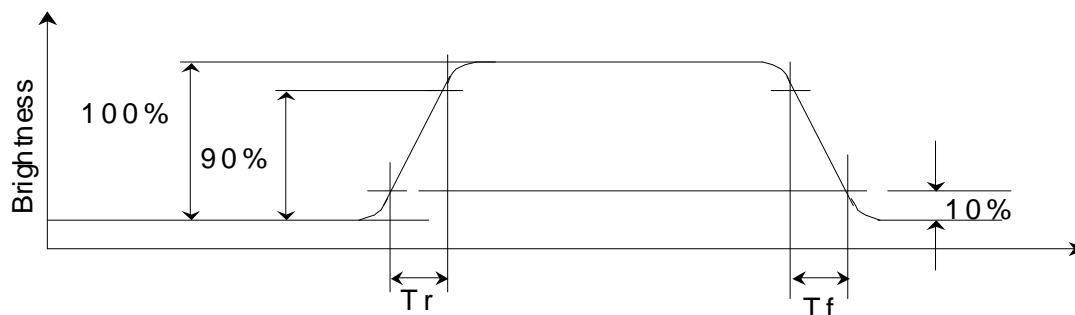


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

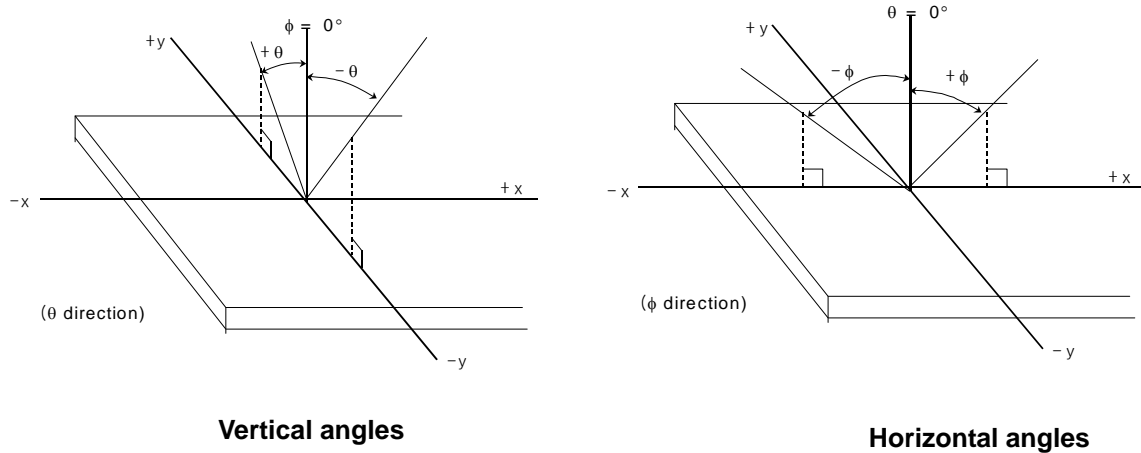
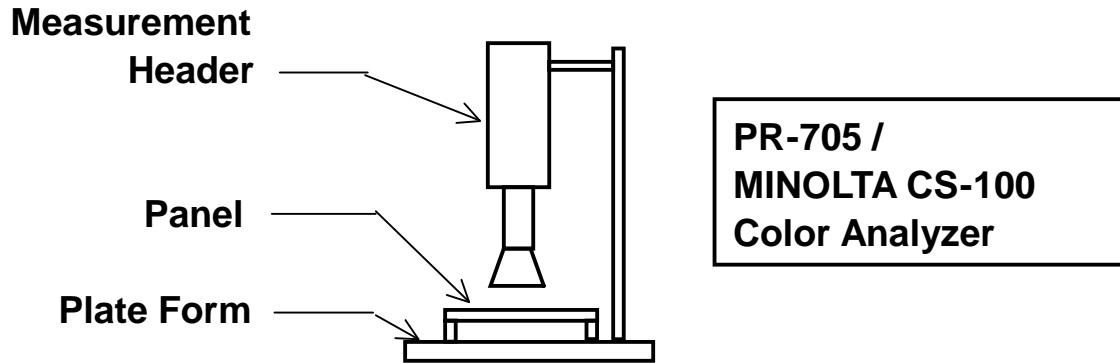


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

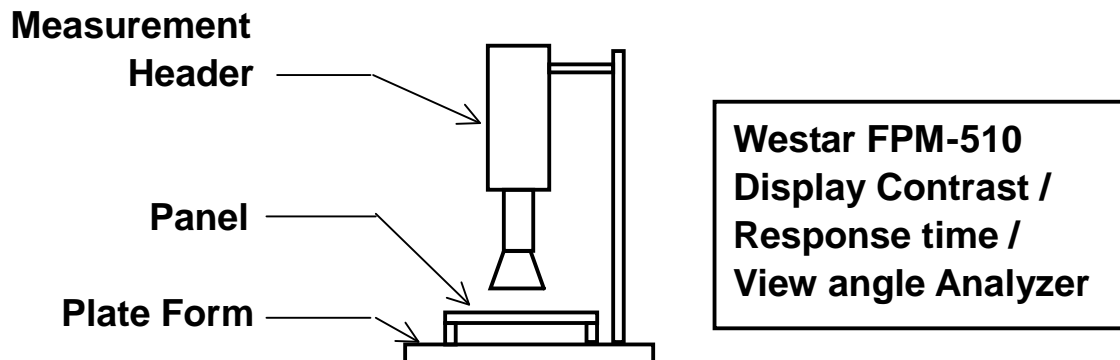
A. LUMINANCE / COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

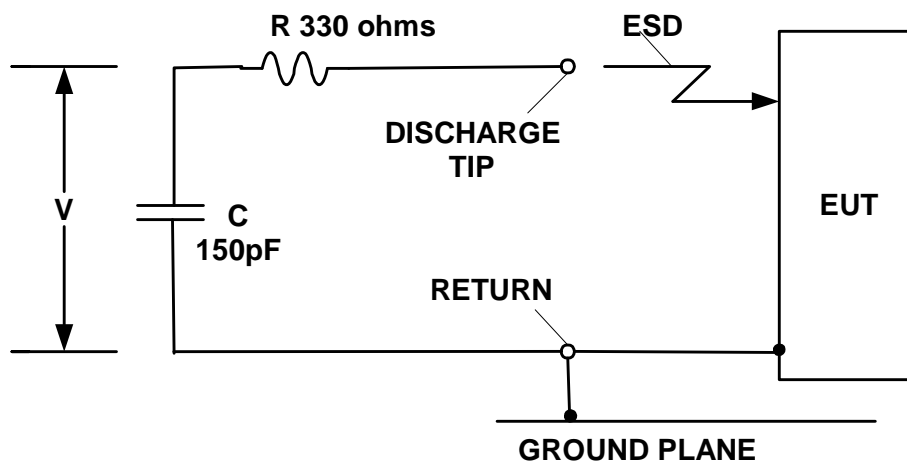


B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.