SoC Real Time Clock (RTC)

IP Core

Initial Register Specification

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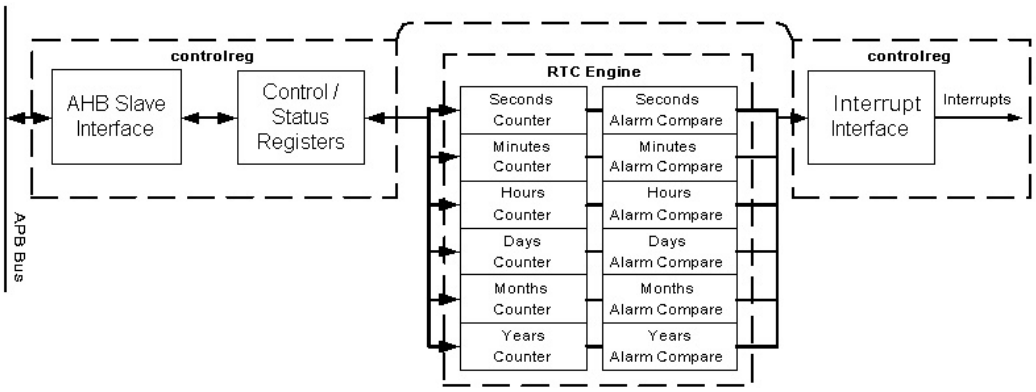
Features

- Clock / Calendar (BCD Format)
  - Seconds
  - Minutes
  - Hours
  - Days
  - Months
  - Years
- Alarm Mode for each “Time Unit”.
- Repeat Alarm Mode for each “Time Unit”.
- AMBA APB Interface.
- Interrupt control for Alarms.



General Description

The **SoC-RTC** is a clock-calendar IP core that keeps track of the “Time of Day”. The core is organized as a series of BCD counters that counts Seconds, Minutes, Hours, Days, Months and Years (Time Units).

The RTC seconds counter time base is generated from a programmable divisor of the system clock. The divisor should be set to generate a 1Hz clock enable signal to the seconds counter. This divisor can also be used to adjust the clock accuracy by periodically adding or subtracting values from the divisor. Calibration accuracy is controlled by software.

Each of the Time Units can be loaded by writing BCD information to the proper Time Unit register. The RTC will immediately load the new time and will continue to count.

The Core can also be loaded with an Alarm Compare value for each Time Unit that will generate an interrupt when that Time Unit reaches the compare value. A Repeat Alarm function is also available. When enabled, this function will cause an interrupt at the terminal count of each Time Unit counter. For example, if the Repeat Alarm bit (bit 7 or Seconds Alarm Register) for the Seconds counter is set, the RTC engine will generate an interrupt every second when the counter rolls over from 59 to 00.

Testmode bits for each Time Unit counter enable the counter to be clocked by the secondsClk in order to speed testability. This can also be used to incrementally update the RTC.

The testRstN bit enables the RTC counters to be reset under software control. Otherwise the RTC counters are free running and do not reset upon system reset.

The **SoC-RTC** operates as a slave device on the AMBA APB bus. Each register is accessed by simple APB bus transactions.

The **SoC-RTC** package includes Verilog source and simulation test-benches.

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Register Descriptions

Note: seconds, minutes, etc. are BCD.
Bits [7:4] represent 10s (10-99)
Bits [3:0] represent 1s (0-9)

Register	Bits	Offset Address	R/W	default	Bit Description
Seconds Ctr		**0x00**	**R/W**	**0x00**	
Seconds 00-50	6:4				Read actual seconds BCD value, write to update new seconds BCD value.
Seconds 0-9	3:0				
					Counts from 00 to 59
Minutes Ctr		**0x04**	**R/W**	**0x00**	
Minutes 00-50	6:4				Read actual minutes BCD value, write to update new minutes BCD value.
Minutes 0-9	3:0				
					Counts from 00 to 59
Hours Ctr		**0x08**	**R/W**	**0x00**	
Hours 00-20	5:4				Read actual hours BCD value, write to update new hours BCD value.
Hours 0-9	3:0				
					Counts from 00 to 23
Days Ctr		**0x0C**	**R/W**	**0x01**	
Days 00-30	5:4				Read actual days BCD value, write to update new days BCD value.
Days 0-9	3:0				
					Counts from 01 to 28,29,30 or 31
Months Ctr		**0x10**	**R/W**	**0x01**	
Months 00-20	4				Read actual months BCD value, write to update new months BCD value.
Months 0-9	3:0				
					Counts from 01 to 12
Years Ctr		**0x14**	**R/W**	**0x00**	
Years 00-20	7:4				Read actual years BCD value, write to update new years BCD value.
Years 0-9	3:0				
					Counts from 00 to 99
RTC ctrl		**0x18**	**R/W**	**00**	
	5:0				testmode – Used to speed up Time Unit counters for test.
	7				testRstN – Used to reset the Time Unit counters under software control.
Clk Divisor		**0x1C**	**R/W**		
	31:0			0x01	Clock Divisor for generating a 1Hz enable to the Seconds Counter

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Seconds Alarm		**0x20**	**R/W**	**0x00**	
Repeat	7				When set, generates an interrupt every second.
Seconds 00-50	6:4				BCD Alarm Compare value used to generate an interrupt on a seconds counter match.
Seconds 0-9	3:0				
Minutes Alarm		**0x24**	**R/W**	**0x00**	
Repeat	7				When set, generates an interrupt every minute.
Minutes 00-50	6:4				BCD Alarm Compare value used to generate an interrupt on a minutes counter match.
Minutes 0-9	3:0				
Hours Alarm		**0x28**	**R/W**	**0x00**	
Repeat	7				When set, generates an interrupt every hour.
Hours 00-20	5:4				BCD Alarm Compare value used to generate an interrupt on a hours counter match.
Hours 0-9	3:0				
Days Alarm		**0x2C**	**R/W**	**0x00**	
Repeat	7				When set, generates an interrupt every day.
Days 00-30	5:4				BCD Alarm Compare value used to generate an interrupt on a days counter match.
Days 0-9	3:0				
Months Alarm		**0x30**	**R/W**	**0x00**	
Repeat	7				When set, generates an interrupt every month.
Months 00-20	4				BCD Alarm Compare value used to generate an interrupt on a months counter match.
Months 0-9	3:0				
Years Alarm		**0x34**	**R/W**	**0x00**	
Years 00-20	7:4				BCD Alarm Compare value used to generate an interrupt on a years counter match.
Years 0-9	3:0				
INT control		**0x38**	**R/W**	**0x00**	
	5				Enable Year Alarm interrupt.
	4				Enable Month Alarm interrupt.
	3				Enable Day Alarm interrupt.
	2				Enable Hour Alarm interrupt.
	1				Enable Minute Alarm interrupt.
	0				Enable Second Alarm interrupt.

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INT status	0x3C	RO	0x00	
5				Year Alarm interrupt status
4				Month Alarm interrupt status
3				Day Alarm interrupt status
2				Hour Alarm interrupt status
1				Minute Alarm interrupt status
0				Second Alarm interrupt status
INT clear	**0x40**	**WO**	**0x00**	**LCD Control Register**
5				Clear Year Alarm interrupt.
4				Clear Month Alarm interrupt.
3				Clear Day Alarm interrupt.
2				Clear Hour Alarm interrupt.
1				Clear Minute Alarm interrupt.
0				Clear Second Alarm interrupt.

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