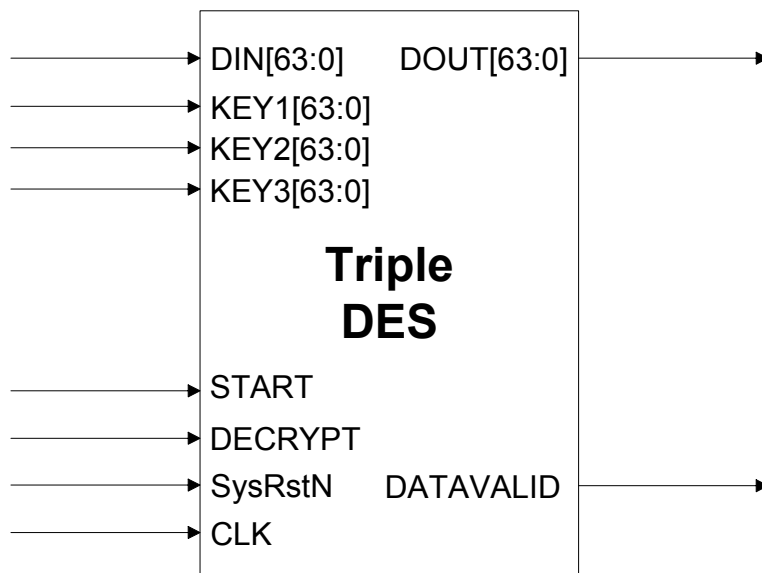


Features

- FIPS 46-3 Standard Compliant
- Encryption/Decryption performed in 48 cycles (ECB mode)
- Up to 168 bits of security
- For use in FPGA or ASIC designs
- Verilog IP Core

Applications

- Secure video
- Electronic Funds Transfer
- Encrypted Storage Data
- Secure communications



General Description

The **SoC-IP-2003** core is a complete implementation of the Triple Data Encryption Standard (TDES) documented in the U.S. Government publication FIPS 46-3.

The **SoC-IP2003** TDES core is a block cipher, working on 64 bits of data at a time. It is built upon the **SoC-IP2002** DES core. Key length is 56 bits. Encoding and decoding operations are performed in only 48 cycles, in Electronic Codebook (ECB) mode. Other modes are available.

The **SoC-IP2003** core can be used in wired, wireless secure data applications.

IP Package

The **SoC-IP2003** TDES core package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and AMBA AHB/APB interfaces are also available.