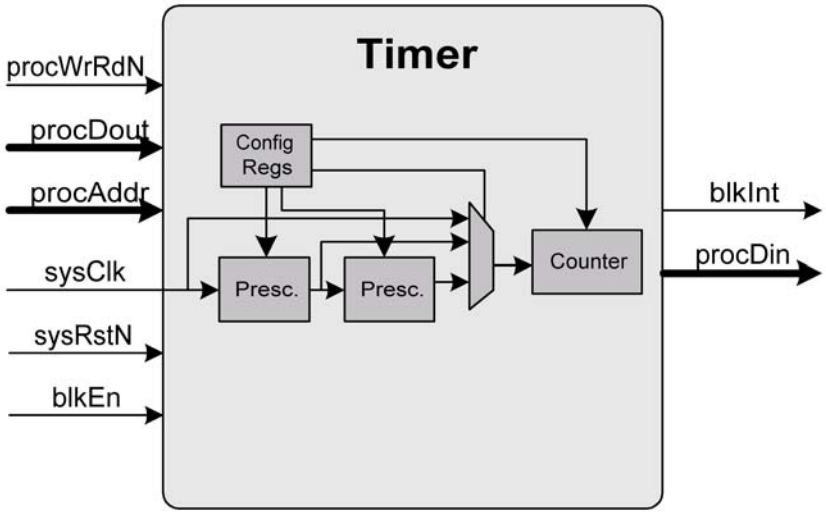
Features

- *16 bit counter/timer*
- *Two 4-bit pre-scalers*
- *Configurable*
- *Free running or periodic mode*
- *Interrupt output*
- *Standard uP bus interface*
- *Included in PiP-EC Embedded Controller Verilog IP*
- *Testbench and Bus Functional Model available as an option.*



General Description

The ***SoC-IP1001*** is a programmable 16-bit counter/timer. Although the ***SoC-IP1001*** was designed for the time-base generator for the ***PiP-EC Pre-Integrated IP™***, it can be used in any application requiring a timer. The timer function is necessary for any embedded microprocessor based SoC that is running a Real Time Operating System (RTOS). The ***SoC-IP1001*** contains a generic bus interface to a single cycle access microprocessor bus.

The ***SoC-IP1001*** Timer module is a sixteen bit down counter with a selectable prescaler. Prescale values of 1, 16 and 256 can be selected. The prescaler extends the timer's range at the expense of precision. The Timer provides two modes of operation that provide a free running value and also periodic interrupts.

The Timer contains several configuration registers that can be written and read by the processor. Two 4-bit prescalers precede a 16-bit counter. The counter can be clocked at either the input clock rate, or a choice of 2 prescaled rates. The counter can be loaded with a value from a preload register. The counter can optionally generate an interrupt.

IP Package

The ***SoC-IP1001*** Timer package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

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