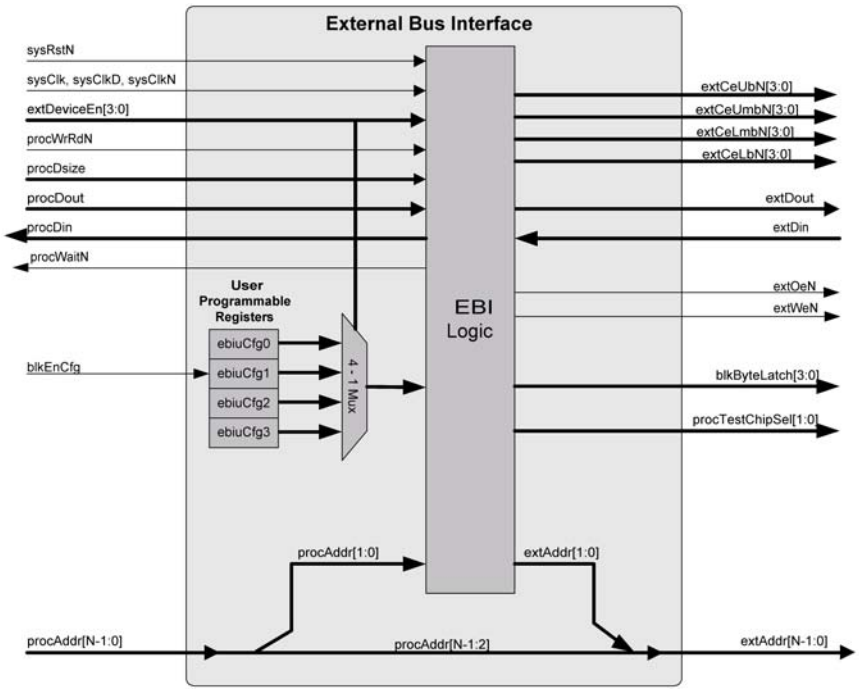
IPC-1003 External Bus Interface

Features

- *Configurable External Bus Interface*
- *Scalable number of external devices*
- *Programmable access times*
- *Independent 8, 16, or 32 bit data interface*
- *Byte, 16 bit half-word and 32 bit word accessible*
- *ARM7TDMI™ compatible*
- *Single cycle external bus access selectable*
- *Single cycle processor bus access*



General Description

The ***SoC-IP1003*** External Bus Interface is a configurable module designed to interface an ARM7TDMI™ microprocessor bus to a generic External Bus. The external bus interface (EBI) allows the processor to transmit and receive data to and from external devices, one or more of which may be memory. External memory can be SRAM, Flash, etc. The user can configure (or program) the ***SoC-IP1003*** to the proper number of read & write wait states and the memory size to allow proper communication. The ***SoC-IP1003*** allows word, half-word, and byte width addressing to 32-bit, 16-bit, and 8-bit external devices.

The ***SoC-IP1003*** interfaces the processor with up to 4 external devices. The Verilog source was designed to allow the user to easily scale the EBI to allow for more than 4 devices. Each device has a configuration register. The 2 LSBs of the processor address bus are modified depending on the type of access specified by the processor and the capabilities of the device (as programmed into the configuration register). The EBI logic performs this and other tasks such as:

- breaks down device enables into upper, upper middle, lower middle, & lower bank chip enables
- steers data bytes or halfwords onto appropriate data bits
- sequences multi-byte or multi-halfword read and write operations
- puts the processor in a wait state until the access completes

SoC Solutions LLC
3200 Peachtree Industrial Blvd.
Suite 301,
Duluth, Georgia, 30096
770-680-2500
www.socsolutions.com

VP-EC Virtual Platform™

IP Package

The ***SoC-IP1003*** External Bus Interface package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

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3200 Peachtree Industrial Blvd.
Suite 301
Duluth, Georgia 30096
www.socsolutions.com
Telephone (770) 680-2500
Fax (770) 680-2501
email: info@socsolutions.com