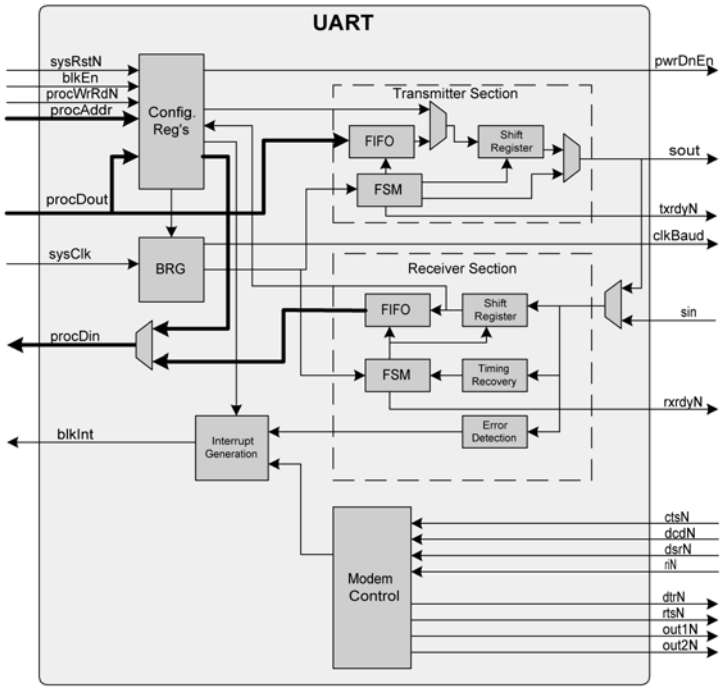
IPC-1005 UART

Features

- *16450/16550 Compatible*
- *16 byte transmit FIFO*
- *16 byte receive FIFO*
- *Modem control*
- *Programmable baud rate generator*
- *Prioritized interrupt system*
- *Line status and error checking (parity and framing errors)*
- *2 Direct Memory Access Modes*
- *Loopback Mode*
- *Included in PiP-EC Embedded Controller Verilog IP*



General Description

The ***SoC-IP1005*** is a 16450/16550 compatible Universal Asynchronous Receiver/Transmitter (UART). The ***SoC-IP1005*** allows the user to configure, send data, and/or receive data. It contains a baud rate generator that can be configured to generate a wide range of baud rates depending on the system clock frequency and the programmable divisor latch. The baud rate generator also generates the clkBaud output signal which can be used to provide a timing reference to external receivers. The ***SoC-IP1005*** has 16 byte internal FIFOs for both receive and transmit modes.

There are 12 internal registers for monitoring and control of the UART functions. Status information can be read at any time during operation. The ***SoC-IP1005*** contains a microprocessor bus interface that is compatible with an ARM7TDMI™ bus or can be easily interfaced to other standard processor buses.

The ***SoC-IP1005*** has a prioritized interrupt system which can generate five types of interrupts: receiver line status, received data available, character timeout, transmitter holding register empty, and modem status. The ***SoC-IP1005*** can transfer parallel data via two direct memory access modes (DMA) and has a loopback mode for on chip diagnostics.

IP Package

The ***SoC-IP1005*** UART package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

3200 Peachtree Industrial Blvd.
Suite 301,
Duluth, Georgia, 30096
770-680-2500
www.socsolutions.com