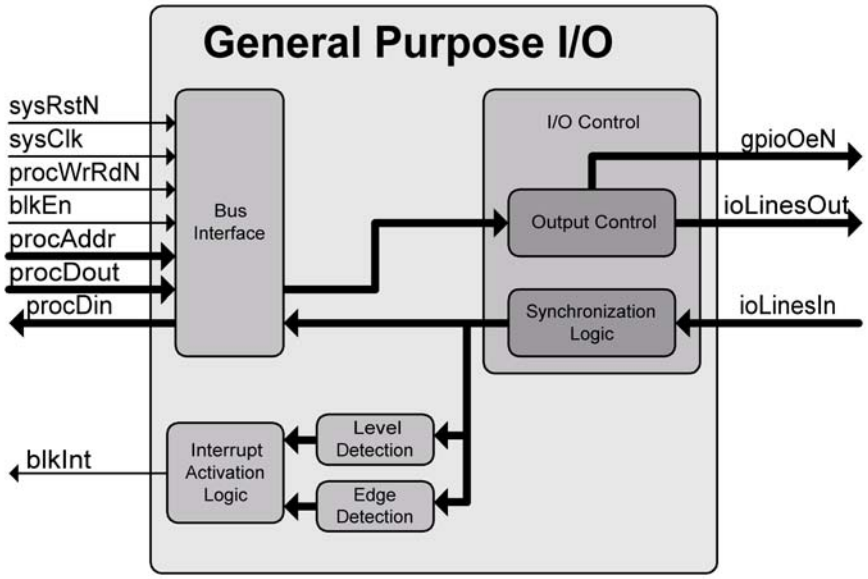
IPC- 1007 General Purpose I/O

Features

- *Configurable I/O lines*
- *Scalable*
- *Interrupt output*
- *Selectable level sensitive or edge triggered interrupt system*
- *Supports asynchronous inputs*
- *Standard uP bus interface*
- *Included in PiP-EC Embedded Controller Verilog IP*
- *Testbench and Bus Functional Model available as an option.*



General Description

The ***SoC-IP1007*** is a configurable General Purpose I/O module with a scalable set of up to 32 I/O lines. All lines can be configured independently of each other, with any combination of inputs and outputs. This module can be used in a wide variety of applications where simple I/O control is needed.

The ***SoC-IP1007*** provides synchronization logic for its inputs in order to safely connect with asynchronous inputs or inputs from other clock domains. Optionally the GPIO module can be configured to generate an interrupt on a high level, low level, positive edge, negative edge, or either edge of any general purpose input line. Each input line has a dedicated interrupt enable set and interrupt enable clear register. Each line configured as an output also has dedicated set and clear registers for simple output control. If interrupt capabilities are not required, the GPIO can be conditionally compiled without interrupt capabilities to save gates.

All signals needed to implement a bidirectional bus are provided by the ***SoC-IP1007***.

IP Package

The ***SoC-IP1007*** General Purpose I/O package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

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