IPC-1002 Interrupt Controller

Features

- *Programmable Interrupt Controller*
- *Scalable (from 1 to 32 interrupts)*
- *Optional programmable interrupt*
- *ARM7TDMI™ compatible*
- *Easily cascaded to support more interrupts*
- *Separate interrupt enable set and clear mechanisms*
- *Included in PiP-EC Embedded Controller Verilog IP*
- *Testbench and Bus Functional Model available as an option.*

General Description

The ***SoC-IP1002*** is a programmable interrupt controller designed to interface to an ARM7TDMI™ microprocessor core. Although the ***SoC-IP1002*** was designed for the interrupt control for the ***PiP-EC Pre-Integrated IP™***, it can be used in any ARM7TDMI™ application requiring an interrupt controller. The interrupt function is necessary for any embedded microprocessor based SoC that is running a Real Time Operating System (RTOS). The ***SoC-IP1002*** contains a microprocessor bus interface that is compatible with an ARM7TDMI™ bus or can be easily interfaced to other standard processor buses.

The ***SoC-IP1002*** Interrupt Controller is fully scalable to support 1 to 32 interrupt sources and provides a programmable interrupt register which can be used to generate an interrupt under software control. The ***SoC-IP1002*** Interrupt Controller provides separate enable set and enable clear mechanisms to prevent dangerous read-modify-write operations within the critical interrupt system. Active high and active low interrupt request outputs are available to facilitate cascading of multiple interrupt controllers in order to support more than 32 interrupt sources.

IP Package

The ***SoC-IP1002*** Interrupt Controller package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

SoC Solutions LLC
3200 Peachtree Industrial Blvd.
Suite 301,
Duluth, Georgia, 30096
770-680-2500
www.socsolutions.com