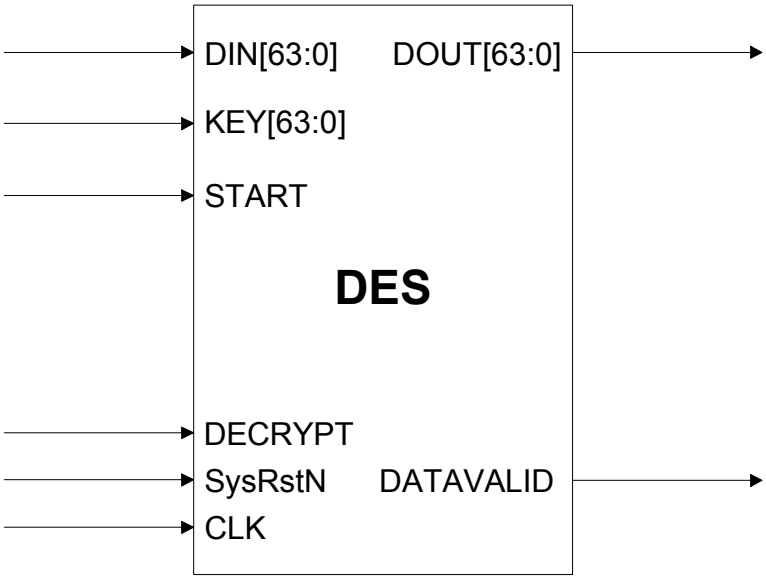
Features

- FIPS 46-3 Standard Compliant
- Encryption/Decryption performed in 16 cycles
- 56 bit security
- For use in FPGA or ASIC designs
- Verilog IP Core



Applications

- Secure video
- Electronic Funds Transfer
- Encrypted Storage Data
- Secure communications

General Description

The ***SoC-IP-2002*** core is a complete implementation of the Data Encryption Standard (DES) documented in the U.S. Government publication FIPS 46-3.

The ***SoC-IP2002*** DES core is a block cipher, working on 64 bits of data at a time. Key length is 56 bits. Encoding and decoding operations are performed in only 16 cycles.

The ***SoC-IP2002*** core can be used in wired, wireless secure data applications, and as a building block for Triple DES.

IP Package

The ***SoC-IP2002*** DES core package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and AMBA AHB/APB interfaces are also available.

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