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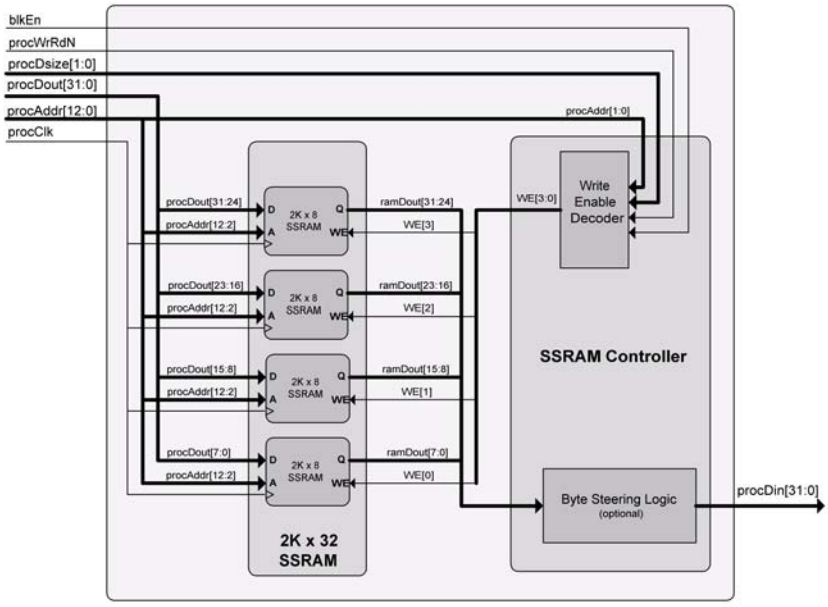
SoC-IP1006 SSRAM Controller

Features

- *Byte, 16 bit half-word, or 32 bit word access*
- *ARM7TDMI™ compatible*
- *Supports single cycle accesses*
- *Fully scalable*
- *Provides byte steering if necessary*



General Description

The ***SoC-IP1006*** Internal SSRAM Controller provides a method of communicating with an integrated Synchronous Static Random Access Memory (SSRAM). The SSRAM array comes in byte, half-word (double byte), and word (four bytes) widths and various depths. The default configuration is two kilowords where each word is 32 bits wide (2K x 32). The memory interface allows word, half-word, or byte wide addressing.

If needed, the ***SoC-IP1006*** provides byte steering logic to organize the output of the SSRAM onto the system data bus, although this option is not necessary for ARM7TDMI™ based systems such as the ***PiP-EC Pre-Integrated IP™.***

IP Package

The ***SoC-IP1006*** SSRAM Controller package includes fully tested and verified Verilog source and TCL simulation scripts. Comprehensive Verilog testbench and microprocessor Bus Functional Model are also available.

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