



USBLC6-2

ASD
(Application Specific Devices)

VERY LOW CAPACITANCE ESD PROTECTION

MAIN APPLICATIONS

- USB2.0 ports at 480Mbps (high speed) and USB OTG ports
- Backwards Compatible with USB1.1 Low and full speed
- Ethernet port: 10/100Mb/s
- SIM card protection
- Video line protection
- Portable and mobile electronics

DESCRIPTION

The **USBLC6-2P6** and **USBLC6-2SC6** are two monolithic Application Specific Devices dedicated to ESD protection of high speed interfaces such as USB2.0, Ethernet links and Video lines.

The very low line capacitance secures a high level of signal integrity without compromising in protection sensitive chips against the most stringent characterized ESD strikes.

FEATURES

- 2 data lines protection
- Protects V_{BUS}
- Very low capacitance: 3.5pF max
- Very low leakage current: 1 μ A max
- SOT-666 and SOT23-6L packages
- RoHS compliant

BENEFITS

- Very low capacitance between lines to GND for optimized data integrity and speed
- Ultra low PCB space consuming: 2.9mm² max for SOT-666 package and 9mm² max for SOT23-6L package
- Enhanced ESD protection: IEC61000-4-2 level 4 compliance guaranteed at device level, hence greater immunity at system level
- ESD protection of V_{BUS} . Allows ESD current flowing to Ground when ESD event occurs on data line
- High reliability offered by monolithic integration
- Very low leakage current for longer operation of battery powered devices
- Fast response time
- Constant D+/D- signal balance
 - Best capacitance matching tolerance I/O to GND of 0.04pF
 - Compliance with USB2.0 requirement (<1pF)

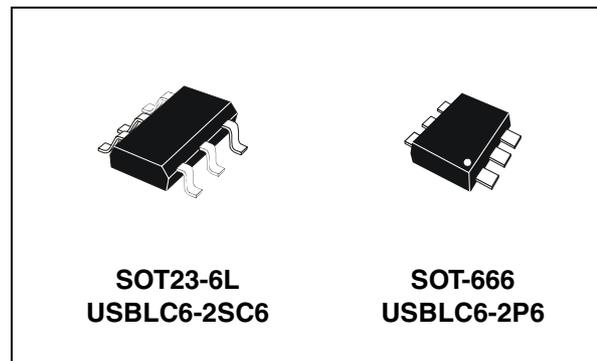
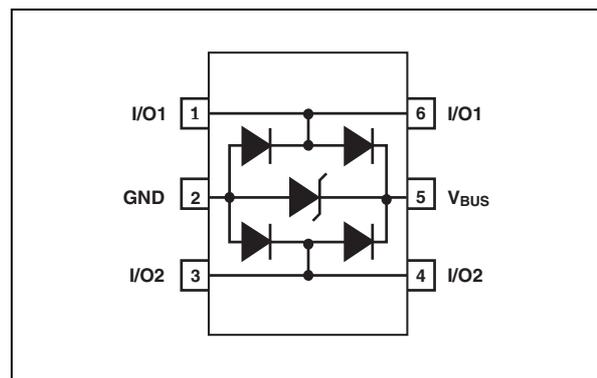


Table 1: Order Codes

Part Number	Marking
USBLC6-2SC6	UL26
USBLC6-2P6	F

Figure 1: Functional Diagram



COMPLIES WITH THE FOLLOWING STANDARDS:

- IEC61000-4-2 level 4:
 - 15kV (air discharge)
 - 8kV (contact discharge)

USBLC6-2

Table 2: Absolute Ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	At device level: IEC61000-4-2 air discharge IEC61000-4-2 contact discharge MIL STD883C-Method 3015-6	15 15 25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		125	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 3: Electrical Characteristics ($T_{amb} = 25^\circ\text{C}$)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{RM}	Reverse stand-off voltage				5	V
I_{RM}	Leakage current	$V_{RM} = 5V$			1	μA
V_{BR}	Breakdown voltage between V_{BUS} and GND	$I_F = 1\text{mA}$	6			V
V_F	Forward voltage	$I_F = 10\text{mA}$			1.1	V
V_{CL}	Clamping voltage	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{s}$ Any I/O pin to GND			12	V
		$I_{PP} = 5\text{A}$, $t_p = 8/20\mu\text{s}$ Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	$V = 0V$ $F = 1\text{MHz}$ any I/O pin to GND		2.5	3.5	pF
$\Delta C_{i/o-GND}$				0.04		
$C_{i/o-i/o}$	Capacitance between I/O	$V = 0V$ $F = 1\text{MHz}$ between I/O, GND not connected		1.2	1.7	pF
$\Delta C_{i/o-i/o}$				0.04		

Figure 2: Capacitance versus line voltage (typical values)

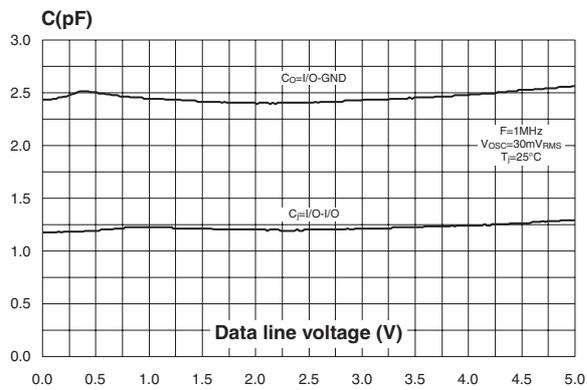


Figure 3: Line capacitance versus frequency (typical values)

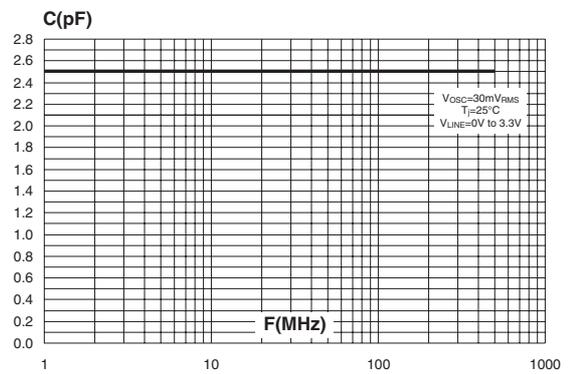


Figure 4: Relative variation of leakage current versus junction temperature (typical values)

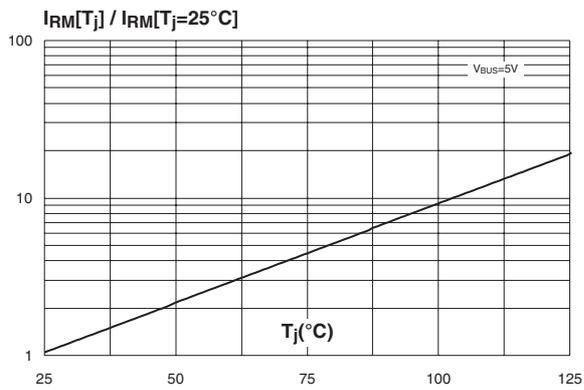
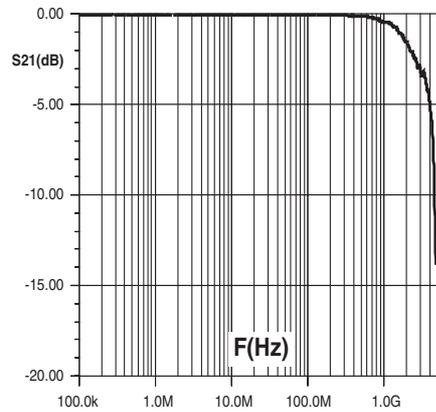


Figure 5: Frequency response



TECHNICAL INFORMATION

1. SURGE PROTECTION

The USBLC6-2 is particularly optimized to perform surge protection based on the rail to rail topology. The clamping voltage V_{CL} can be calculated as follow :

$$V_{CL+} = V_{BUS} + V_F \text{ for positive surge}$$

$$V_{CL-} = -V_F \text{ for negative surge}$$

with: $V_F = V_T + R_d \cdot I_p$
 (V_F forward drop voltage) / (V_T threshold voltage)

We assume that the value of the dynamic resistance of the clamping diode is typically:
 $R_d = 0.5\Omega$ and $V_T = 1.2V$.

For an IEC61000-4-2 surge Level 4 (Contact Discharge: $V_g=8kV$, $R_g=330\Omega$), $V_{BUS} = +5V$, and if in first approximation, we assume that : $I_p = V_g / R_g = 24A$.

So, we find:

$$V_{CL+} = +17V$$

$$V_{CL-} = -12V$$

Note: the calculations do not take into account phenomena due to parasitic inductances.

2. SURGE PROTECTION APPLICATION EXAMPLE

If we consider that the connections from the pin V_{BUS} to V_{CC} and from GND to PCB GND are done by two tracks of 10mm long and 0.5mm large; we assume that the parasitic inductances L_w of these tracks are about 6nH. So when an IEC61000-4-2 surge occurs, due to the rise time of this spike ($tr=1ns$), the voltage V_{CL} has an extra value equal to $L_w \cdot di/dt$.

The di/dt is calculated as: $di/dt = I_p/tr = 24 A/ns$

The overvoltage due to the parasitic inductances is: $L_w \cdot di/dt = 6 \times 24 = 144V$

By taking into account the effect of these parasitic inductances due to unsuitable layout, the clamping voltage will be :

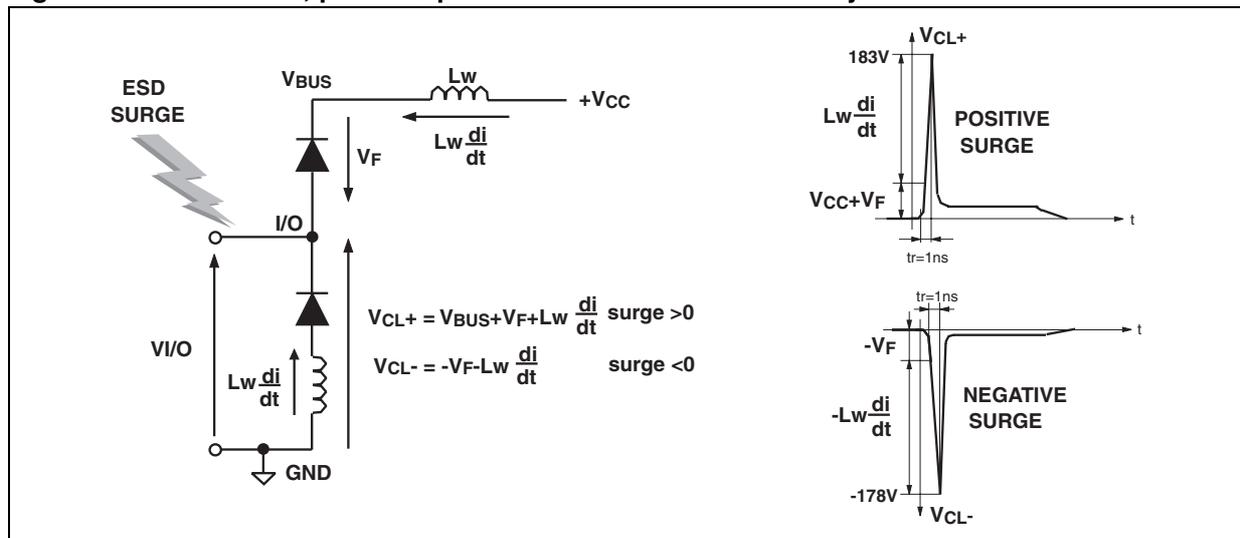
$$V_{CL+} = +17 + 144 = 161V$$

$$V_{CL-} = -12 - 144 = -156V$$

We can reduce as much as possible these phenomena with simple layout optimization.

It's the reason why some recommendations have to be followed (see paragraph "How to ensure a good ESD protection").

Figure 6: ESD behavior; parasitic phenomena due to unsuitable layout



3. HOW TO ENSURE A GOOD ESD PROTECTION

While the USBLC6-2 provides a high immunity to ESD surge, an efficient protection depends on the layout of the board. In the same way, with the rail to rail topology, the track from the V_{BUS} pin to the power supply $+V_{CC}$ and from the GND pin to GND must be as short as possible to avoid overvoltages due to parasitic phenomena (see figure 6).

It's often harder to connect the power supply near to the USBLC6-2 unlike the ground thanks to the ground plane that allows a short connection.

To ensure the same efficiency for positive surges when the connections can't be short enough, we recommend to put close to the USBLC6-2, between V_{BUS} and ground, a capacitance of 100nF to prevent from these kinds of overvoltage disturbances (see figure 7).

The add of this capacitance will allow a better protection by providing during surge a constant voltage.

The figures 8, 9 and 10 show the improvement of the ESD protection according to the recommendations described above.

Figure 7: ESD behavior: optimized layout and add of a capacitance of 100nF

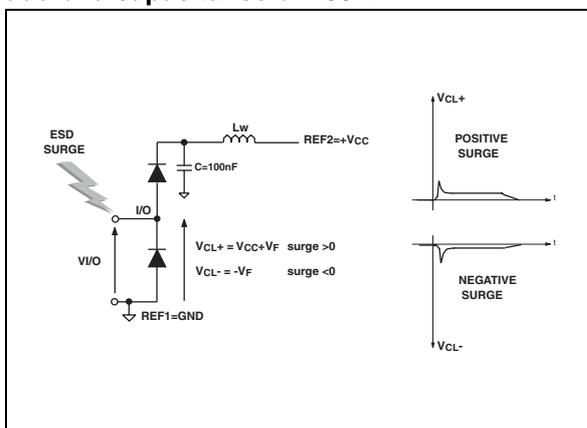


Figure 8: ESD behavior: measurements conditions (with coupling capacitance)

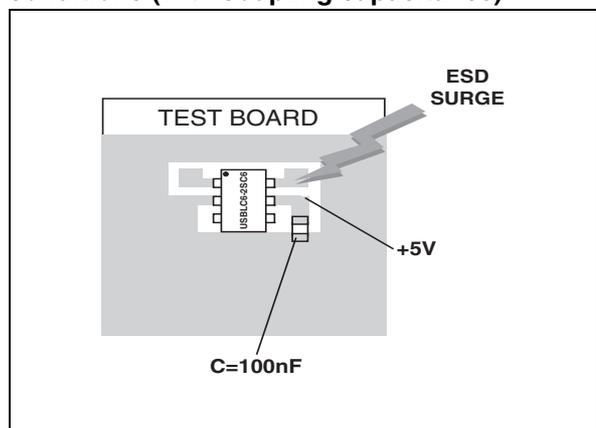


Figure 9: Remaining voltage after the USBLC6-2 during positive ESD surge

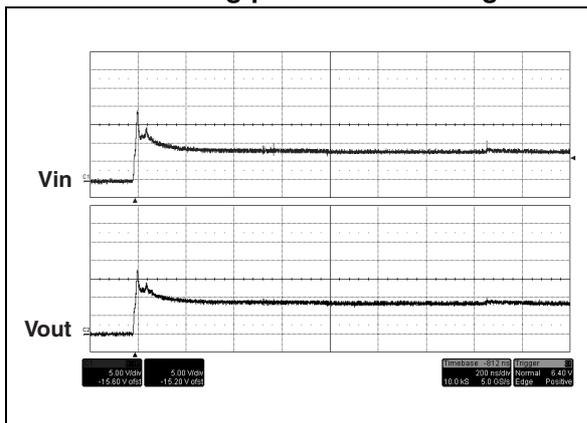
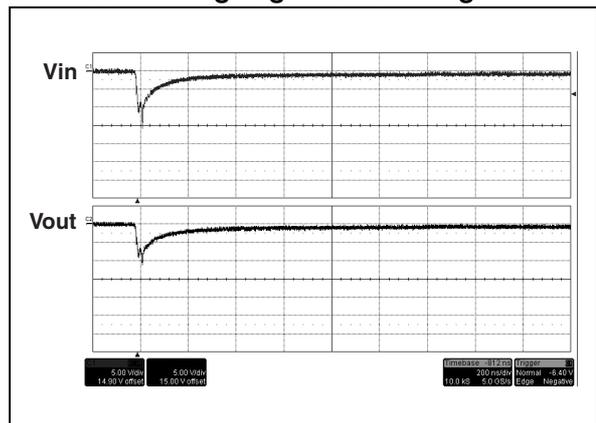


Figure 10: Remaining voltage after the USBLC6-2 during negative ESD surge



IMPORTANT:

A main precaution to take is to put the protection device closer to the disturbance source (generally the connector).

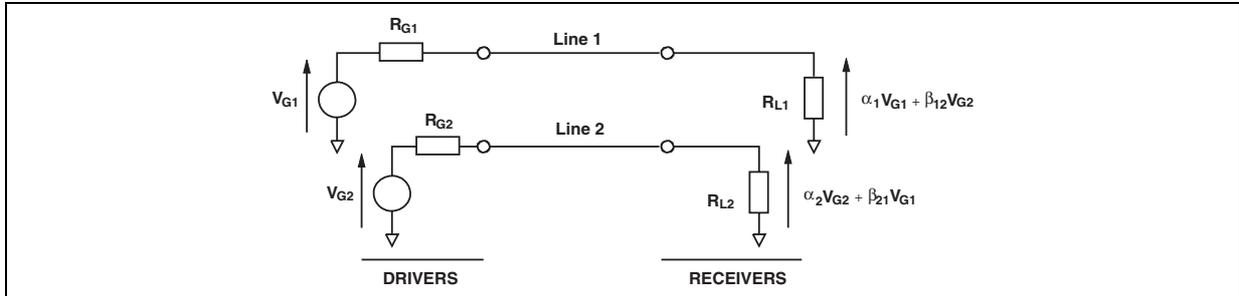
Note: The measurements have been done with the USBLC6-2 in open circuit.



4. CROSSTALK BEHAVIOR

4.1. Crosstalk phenomena

Figure 11: Crosstalk phenomena



The crosstalk phenomena are due to the coupling between 2 lines. The coupling factor (β_{12} or β_{21}) increases when the gap across lines decreases, particularly in silicon dice. In the example above the expected signal on load R_{L2} is $\alpha_2 V_{G2}$, in fact the real voltage at this point has got an extra value $\beta_{21} V_{G1}$. This part of the V_{G1} signal represents the effect of the crosstalk phenomenon of the line 1 on the line 2. This phenomenon has to be taken into account when the drivers impose fast digital data or high frequency analog signals in the disturbing line. The perturbed line will be more affected if it works with low voltage signal or high load impedance (few $k\Omega$).

Figure 12: Analog crosstalk measurements

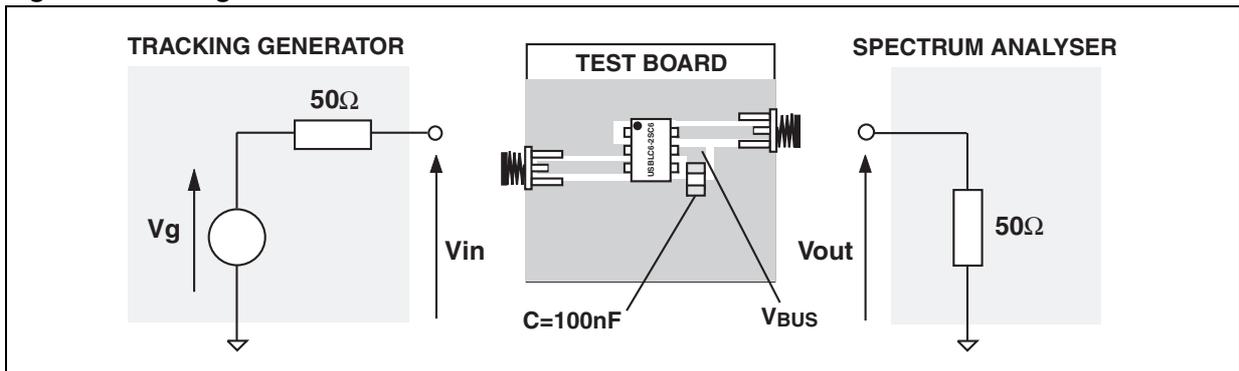
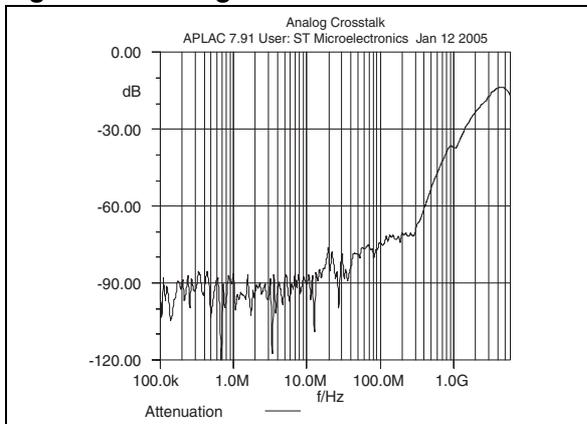


Figure 12 gives the measurement circuit for the analog application. In usual frequency range of analog signals (up to 240MHz) the effect on disturbed line is less than -55 dB (please see figure 13).

Figure 13: Analog crosstalk results



As the USBLC6-2 is designed to protect high speed data lines, it must ensure a good transmission of operating signals. The frequency response (figure 5) gives attenuation information and shows that the USBLC6-2 is well suitable for data line transmission up to 480 Mbit/s while it works as a filter for undesirable signals like GSM (900MHz) frequencies, for instance.

5. APPLICATION EXAMPLES

Figure 14: USB2.0 port application diagram using USBLC6-2

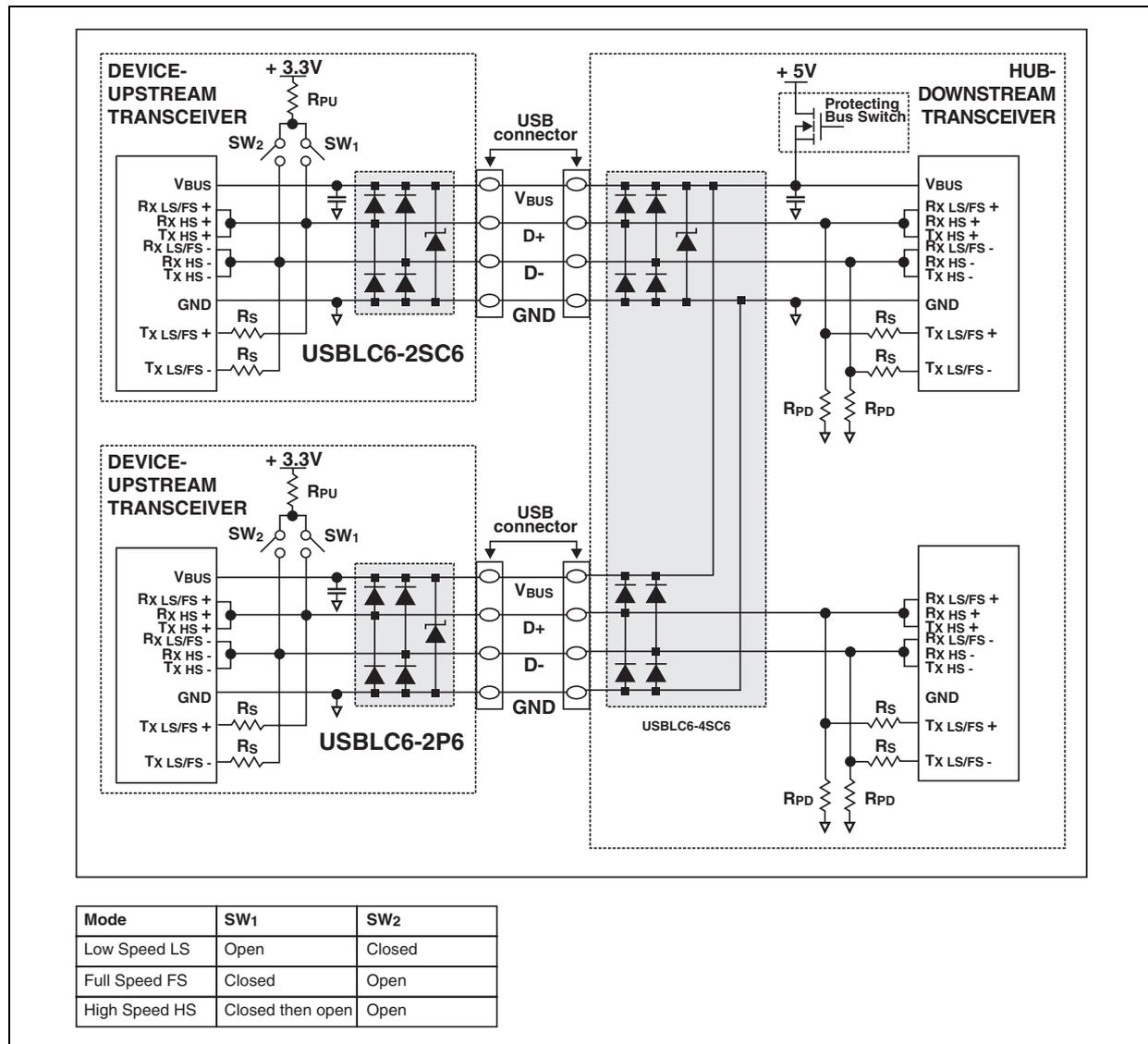
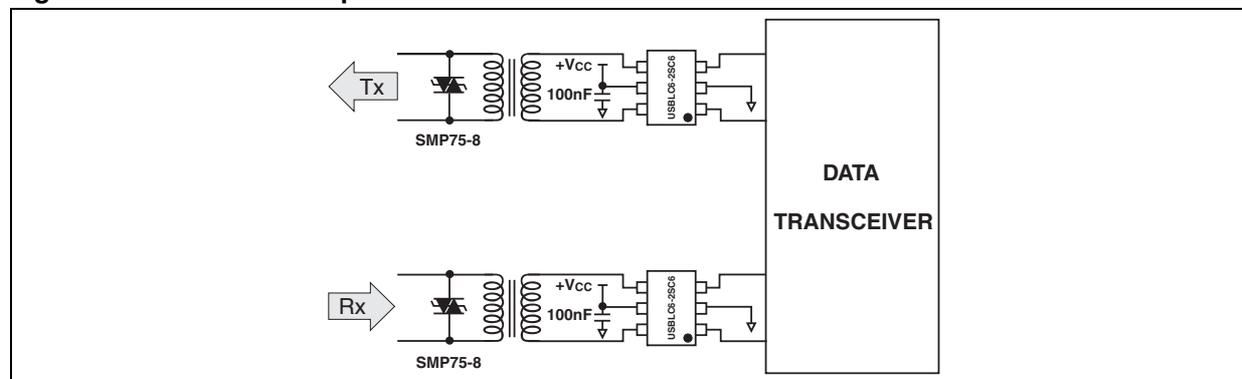


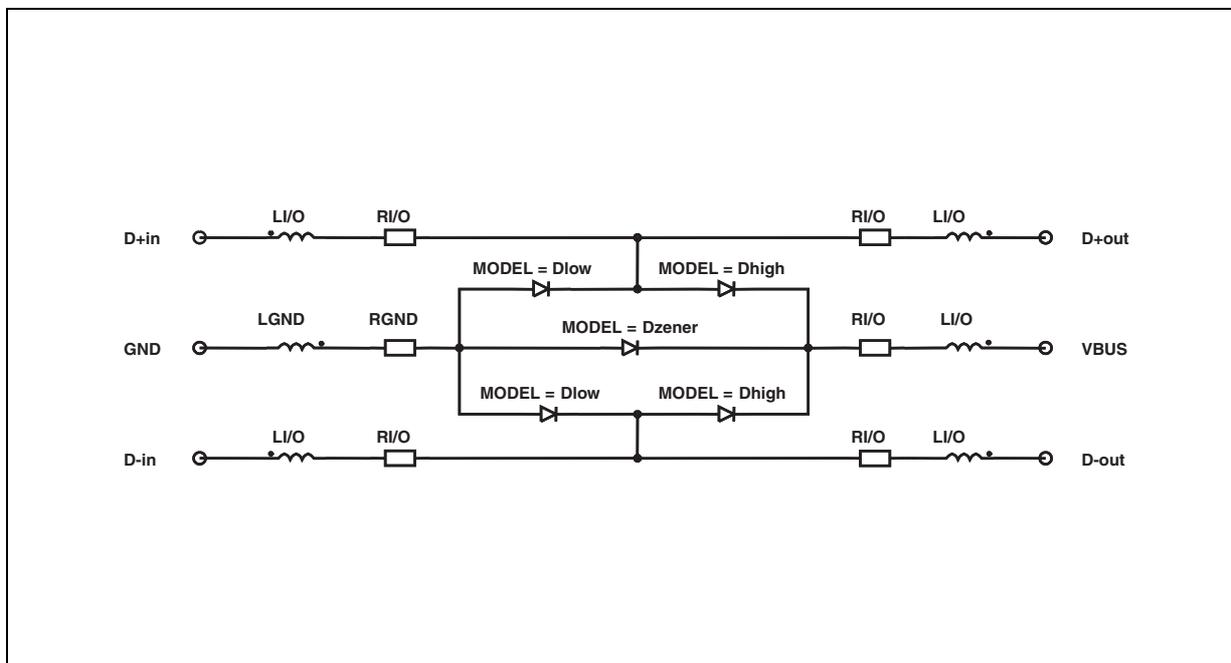
Figure 15: T1/E1/Ethernet protection



6. PSPICE MODEL

Figure 16 shows the PSPICE model of one USBLC6-2 cell. In this model, the diodes are defined by the PSPICE parameters given in figure 17.

Figure 16: PSPICE model



Note: This simulation model is available only for an ambient temperature of 27°C.

Figure 17: PSPICE parameters

	Dlow	Dhigh	Dzener	LI/O	750p
BV	50	50	7.3	RI/O	110m
CJO	0.9p	2.0p	40p	LGND	550p
IBV	1m	1m	1m	RGND	60m
M	0.3333	0.3333	0.3333		
RS	0.2	0.52	0.84		
VJ	0.6	0.6	0.6		
TT	0.1u	0.1u	0.1u		

Figure 18: USBLC6-2 PCB layout considerations

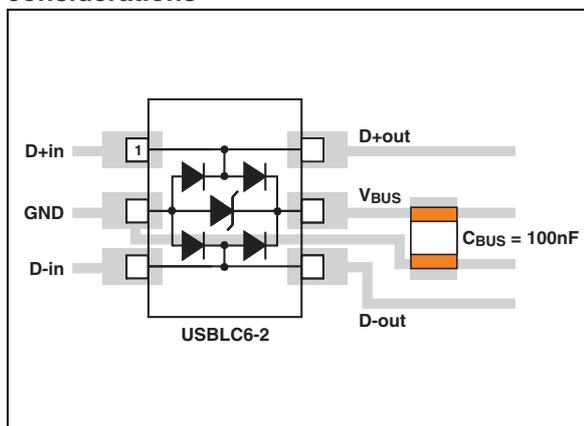


Figure 19: Ordering Information Scheme

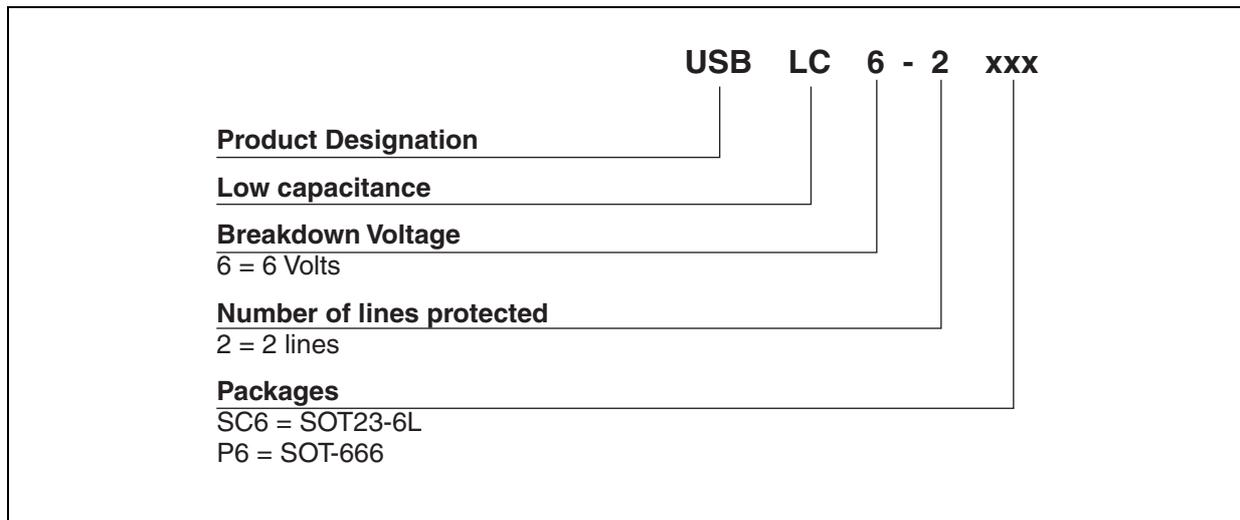


Figure 20: SOT-666 Package Mechanical Data

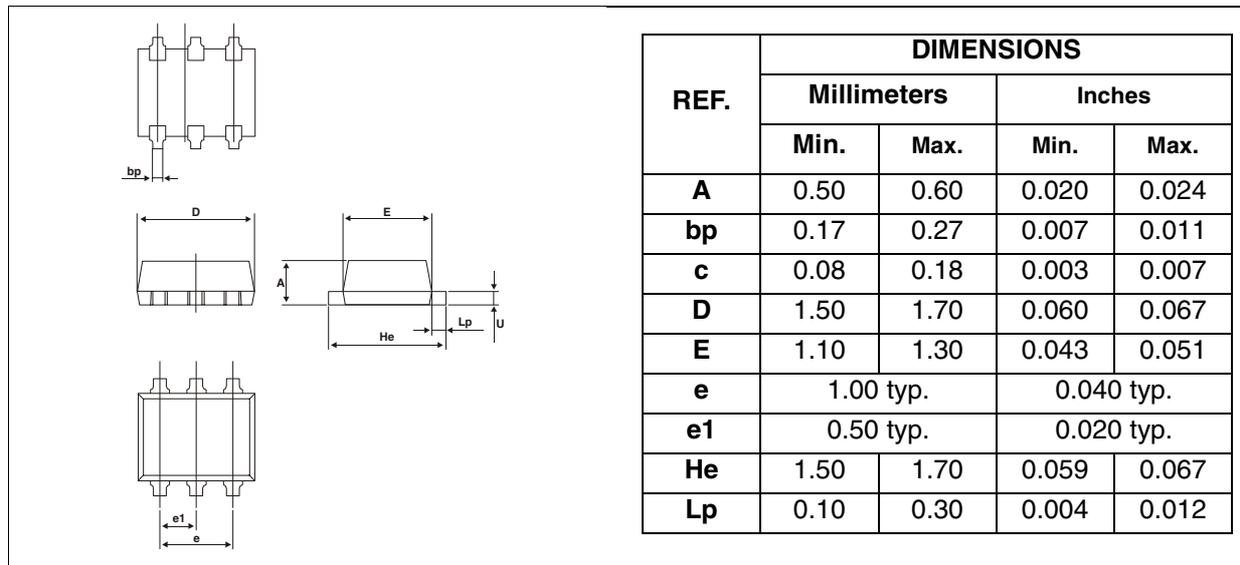


Figure 21: Foot Print Dimensions (in millimeters)

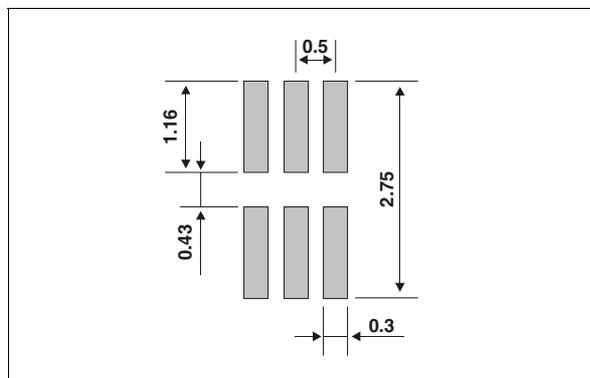


Figure 22: SOT23-6L Package Mechanical Data

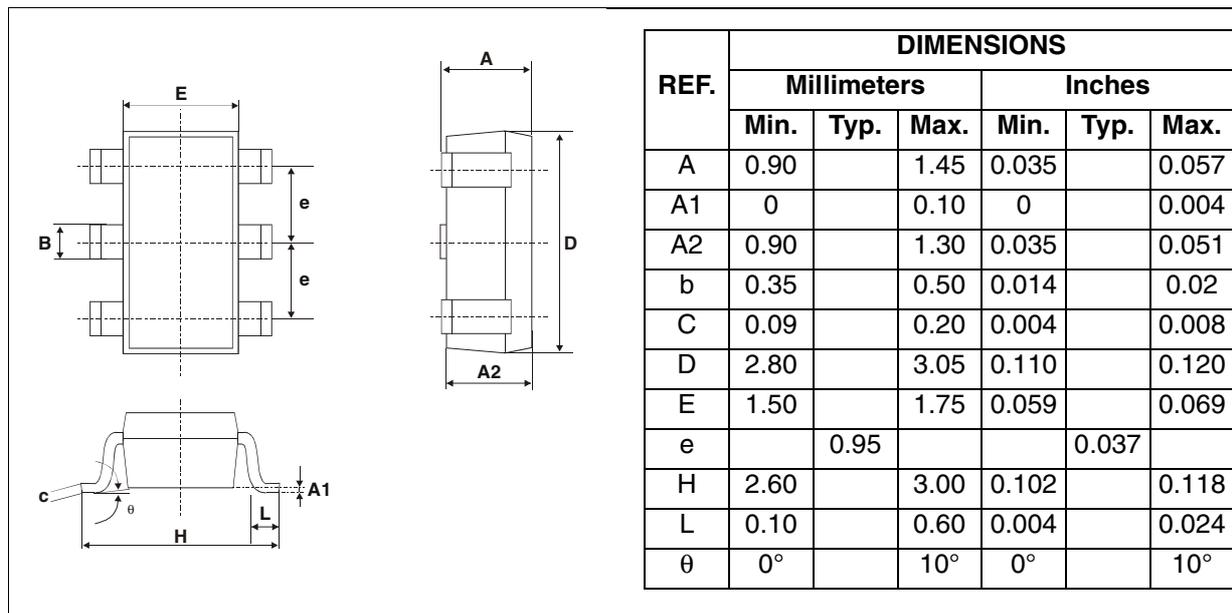


Figure 23: Foot Print Dimensions (in millimeters)

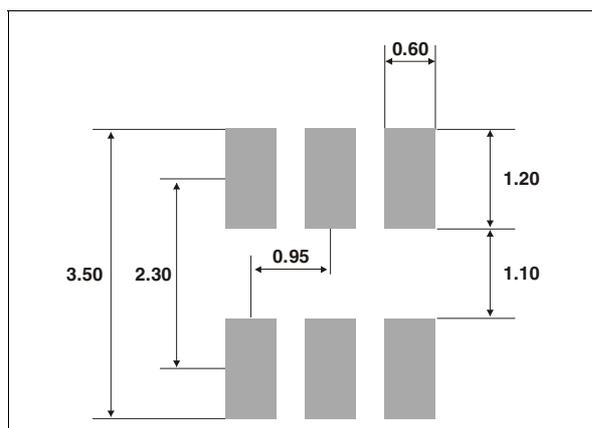


Table 4: Ordering Information

Ordering code	Marking	Package	Weight	Base qty	Delivery mode
USBLC6-2SC6	UL26	SOT23-6L	16.7 mg	3000	Tape & reel
USBLC6-2P6	F	SOT-666	2.9 mg	3000	Tape & reel

Table 5: Revision History

Date	Revision	Description of Changes
14-Mar-2005	1	First issue.
07-Jun-2005	2	Format change to figure 3; no content changed.

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