Intel® Embedded Flash Memory (J3 v. D)

32-, 64-, and 128-Mbit

Specification Update

February 2006

The 28F128J3D, 28F640J3D, 28F320J3D may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 311136, Revision: 002
8 Feb 2006

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Contents

Revision History 5

Preface 6

Summary Table of Changes 7

Errata 9

Revision History

Date	Version	Description
01/12/06	-001	Initial release: “Buffered Program Erratum” on page 9
02/08/06	-002	Summery table was corrected under status columns for Erratum number 1.

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata and specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
Intel StrataFlash® Memory (J3 v. D) datasheet	308551

Nomenclature

Errata are design defects or errors. These may cause the Intel StrataFlash® memory behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel StrataFlash® memory components. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document

Errata

28F128J3D (128-Mbit), 0.13 micron				
Number	**Stepping(s) Affected**	**Page**	**Status**	**Errata**
	A1			
1	X	9	Plan Fix	Buffered program erratum

28F640J3D (64-Mbit) 0.13 micron				
Number	**Stepping(s) Affected**	**Page**	**Status**	**Errata**
	A0			
1	X	9	Plan Fix	Buffered program erratum

28F320J3D (32-Mbit) 0.13 micron				
Number	**Stepping(s) Affected**	**Page**	**Status**	**Errata**
	A0			
1	X	9	Plan Fix	Buffered program erratum

Errata

1. Buffered Program Erratum

Problem: During buffered programming in byte mode, if the starting address is an odd address such as 0x01, 0x03, 0x05, and so on, and if the buffer size is 32 bytes, the 32nd byte in the array will wrap around to the address just before the starting address.

Implication: Data at address just before the starting address is overwritten, potentially causing invalid data reads from that array location.

Workaround: Set the maximum buffer size from 32 bytes to 31 bytes when starting at an odd address, e.g. 0x01, 0x03, etc., or start the buffered program at an even address, e.g. 0x00, 0x02, etc.

Status: A future stepping for this erratum is under evaluation.