CoreMemCtrl

DirectCore

Product Summary

Intended Use

- Intended for Use in a Processor Subsystem to Interface to External Flash or SRAM

Key Features

- Supplied in SysBASIC Core Bundle
- Two Independent Flash and SRAM AHB Ports for Separate Addressing
- Configurable External Memory Interface
- Interfaces to Synchronous or Asynchronous SRAM
- Supports Word, Halfword, and Byte Accesses to SRAM
- Supports Word Accesses to Flash
- Automatic Correct Connection to CoreAHB and CoreAHBLite in CoreConsole

Benefits

- Allows Easy Integration of External Memory Resources in a CoreMP7 or Cortex-M1 Subsystem
- Auto Stitch in CoreConsole for Rapid Development
- Compatible with Advanced Microcontroller Bus Architecture (AMBA), CoreMP7, and Cortex-M1

ARM Supported Families

- ProASIC®3 (M7A3P, M1A3P)
- ProASIC3E (M7A3PE, M1A3PE)
- Fusion (M7AFS, M1AFS)
- IGLOO™ (M1AGL)
- IGLOOe (M1AGLE)

Synthesis and Simulation Support

- Supported in the Actel Libero® Integrated Design Environment (IDE)

Verification and Compliance

- Compliant with AMBA

Contents

General Description

CoreMemCtrl is an AHB Slave component that supports access to external SRAM and flash memory resources. CoreMemCtrl uses two Slave slots on the Advanced High-Performance Bus (AHB). Typically, the flash Slave interface is connected to slot 0 and the SRAM Slave interface to slot 1. If Auto Stitching is used in CoreConsole, these connections will be made automatically.

CoreAHB and CoreAHBLite have a Remap input that can be used to swap slot 0 and slot 1 in the memory map seen by the processor. By toggling the Remap signal, either SRAM or flash can be made to appear at slot 0.

A top-level block diagram of CoreMemCtrl is shown in Figure 1, and the ports are listed in Table 1 on page 3.

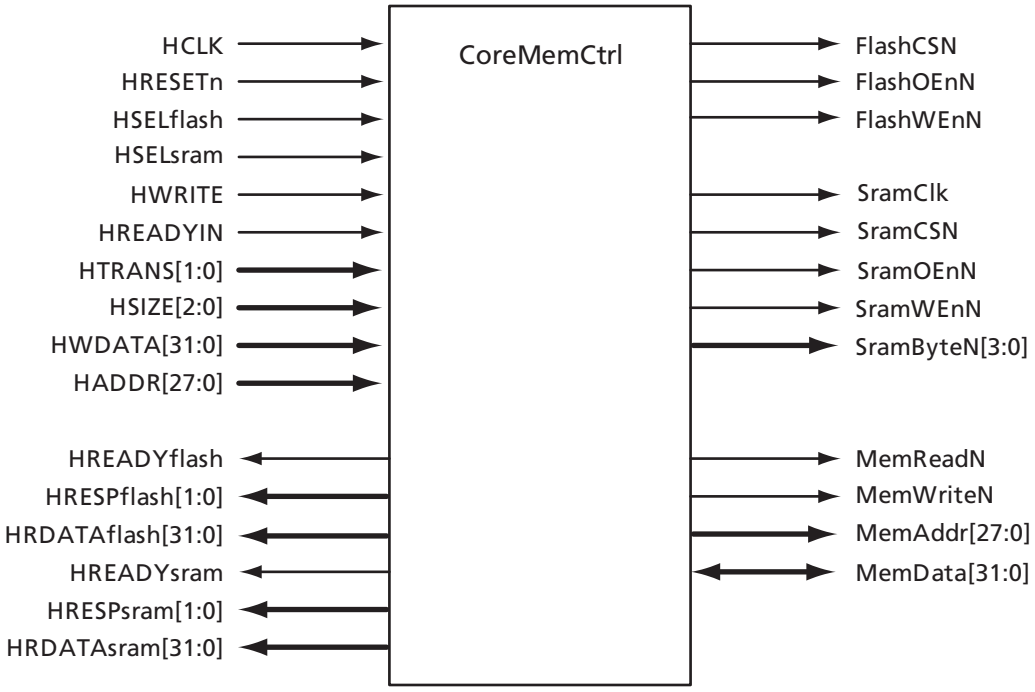

Figure 1 • **CoreMemCtrl Block Diagram**

Table 1 • **CoreMemCtrl Ports**

Port	Width	Direction	Description
HCLK	1	In	AHB clock
HRESETn	1	In	Active low AHB reset
HSELflash	1	In	AHB select signal for flash memory
HSELsram	1	In	AHB select signal for SRAM
HWRITE	1	In	AHB write signal
HREADYIN	1	In	AHB ready input from bus
HTRANS	2	In	AHB transfer type (idle, busy, sequential, non-sequential)
HSIZE	3	In	AHB size indication (word, halfword, byte)
HWDATA	32	In	AHB write data
HADDR	28	In	AHB address
HREADYflash	1	Out	AHB ready signal from flash
HRESPflash	2	Out	AHB response from flash
HRDATAflash	32	Out	AHB read data from flash
HREADYsram	1	Out	AHB ready signal from SRAM
HRESPsram	2	Out	AHB response from SRAM
HRDATAsram	32	Out	AHB read data from SRAM
FlashCSN	1	Out	Active low chip select for flash
FlashOEnN	1	Out	Active low output enable for flash
FlashWEnN	1	Out	Active low write enable for flash
SramClk	1	Out	Clock signal for synchronous SRAM (SSRAM). SramClk is the inverse of HCLK.
SramCSN	1	Out	Active low chip select for asynchronous or synchronous SRAM
SramOEnN	1	Out	Active low output enable for asynchronous or synchronous SRAM
SramWEnN	1	Out	Active low write enable for asynchronous or synchronous SRAM
SramByteN	4	Out	Active low byte enables for asynchronous or synchronous SRAM
MemReadN	1	Out	Active low memory read enable. This is asserted when either FlashOEnN or SramOEnN is asserted.
MemWriteN	1	Out	Active low memory write enable. This is asserted when either FlashWEnN or SramWEnN is asserted.
MemAddr	28	Out	Address bus output to flash and SRAM
MemData	32	Inout	Bidirectional data bus to/from flash and SRAM

Connecting CoreMemCtrl in CoreConsole

Table 2 lists the ports present on CoreMemCtrl and describes how to connect these in CoreConsole.

Table 2 • **CoreMemCtrl Connections**

Connection	CoreConsole Label	Description
Required Connections		
Flash AHB Slave Interface	AHBslave_flash	This interface groups together all of the signals used to connect the flash memory region to an AHB slot. Normally connected to Slave slot 0 (AHBmslave0) of the AHB bus.
SRAM AHB Slave Interface	AHBslave_sram	This interface groups together all of the signals used to connect the SRAM region to an AHB slot. Normally connected to Slave slot 1 (AHBmslave1) of the AHB bus.
External Memory Interface	ExternalMemoryInterface	This interface contains the signals that connect to the flash and SRAM devices and should be routed to the top level of your subsystem.
HCLK	HCLK	AHB system clock input Connect this to the HCLK output of the CoreMP7Bridge or Cortex-M1 core.
HRESETn	HRESETn	Active low AHB system reset Connect this to the HRESETn output of the CoreMP7Bridge or Cortex-M1 core.

External Memory Interface

The External Memory Interface of the Memory Controller should be routed to the subsystem top level to facilitate communication with flash and SRAM resources.

The Memory Controller is designed to accommodate a variety of flash and SRAM configurations. For this reason, the External Memory Interface is somewhat generic in nature to enable connection to a range of different memory devices and memory systems.

Memory devices typically have a number of inputs that are fixed at static levels dependent on the particular memory architecture in place. If the memory devices in your system have such static inputs, it is intended that these be handled in the top-level description for your FPGA device—that is, above the subsystem top level.

Table 3 lists and describes the signals make up the External Memory Interface. Active low control signals are suffixed with an *N*. All of the External Memory Interface signals are outputs from CoreMemCtrl, except for MemData, which is a bidirectional data bus.

CoreMemCtrl is designed to connect to synchronous SRAMs that exhibit either a pipelined or flow-through read behavior. The output data from the synchronous SRAM is assumed to be valid just after the SRAM clock edge that follows the edge on which the read address is clocked into the SRAM in Pipeline mode. In Flow-Through mode, an additional register is implemented in the FPGA to accomplish the same condition. CoreMemCtrl has been used with the GS88018 synchronous SRAM device from GSI Technology in Pipeline mode, with static values applied to some inputs of the device as follows: FTn = 1, LBOn = 1, E2 = 1, GWn = 1, ZZ = 0, ADSPn = 1, ADSCn = 0, ADVn = 1. CoreMemCtrl has also been used with the CY7C1363 synchronous Flow-Through SRAM device from Cypress, with static values applied to some inputs of the device as follows: MODE = 1, CE2 = 1, GWn = 1, ZZ = 0, ADSPn = 1, ADSCn = 0, and ADVn = 1.

Table 3 • **CoreMemCtrl External Memory Interface**

Signal	Width	Description
Flash Control Symbols		
FlashCSN	1	Flash chip select In some systems, the chip select pin of the flash might be fixed at an active level using, for example, a pull-down resistor, in which case this signal may be left unconnected.
FlashOEnN	1	Flash output enable
FlashWEnN	1	Flash write enable
SRAM Control Signals		
SramClk	1	Clock signal for use with synchronous SRAM. SramClk is the inverse of HCLK.
SramCSN	1	SRAM chip select In some systems, the chip select pin of the SRAM might be fixed at an active level using, for example, a pull-down resistor, in which case this signal may be left unconnected.
SramOEnN	1	SRAM output enable
SramWEnN	1	SRAM write enable
SramByteN	4	SRAM byte enables
Shared Memory Signals		
MemReadN	1	Combined flash/SRAM read enable This signal is asserted (LOW) when either FlashOEnN or SramOEnN is LOW, and is intended for use in a memory system that does not have separate connections to the flash and SRAM output enable pins.
MemWriteN	1	Combined flash/SRAM write enable This signal is asserted (LOW) when either FlashWEnN or SramWEnN is LOW, and is intended for use in a memory system that does not have separate connections to the flash and SRAM write enable pins.
MemAddr	28	Flash/SRAM address bus
MemData	32	Flash/SRAM bidirectional data bus

CoreMemCtrl Configurable Options

There are a number of configurable options that apply to CoreMemCtrl. These are detailed in Table 4. If a configuration different from the default is required, use the configuration dialog in CoreConsole to select appropriate values for the configurable options.

Table 4 • **CoreMemCtrl Configurable Options**

Configurable Option	Default Setting	Description
SRAM mode	Asynchronous	Selects either asynchronous or synchronous SRAM. Possible settings are "Asynchronous" and "Synchronous."
Synchronous SRAM mode	Pipeline	Only applicable when SRAM mode is set to "Synchronous." Selects either Pipeline or Flow-Through for the SRAM. Consult the SRAM's datasheet to determine which modes are supported on your device. Possible settings are "Pipeline" and "Flow Through."
Flash data bus width	32-bit	Selects the data bus width for the flash memory interface. Possible settings are "32-bit" and "16-bit."
Number of wait states for flash read	1	Selects the number of wait states inserted during a flash read access. Possible range is 0 to 3.
Number of wait states for flash write	1	Selects the number of wait states inserted during a flash write access. Possible range is 1 to 3.
Number of wait states for SRAM read	1	Only applicable when SRAM mode is set to "Asynchronous." Selects the number of wait states inserted during an SRAM read access. Possible range is 0 to 3.
Number of wait states for SRAM write	1	Only applicable when SRAM mode is set to "Asynchronous." Selects the number of wait states inserted during an SRAM write access. Possible range is 1 to 3.
Read and write enables shared for flash and SRAM	No	Only applicable when SRAM mode is set to "Synchronous." Set this to "Yes" if using shared read and write enables (MemReadN and MemWriteN) for flash and SRAM devices. When set to "Yes," a one-clock-cycle delay is inserted between a synchronous SRAM write and a flash read or write. Possible settings are "Yes" and "No."

Waveforms

The waveforms in the figures in this section show the timing of the CoreMemCtrl signals. For Figure 15 on page 14 to Figure 30 on page 21, one wait state is used in any flash or asynchronous SRAM transactions shown.

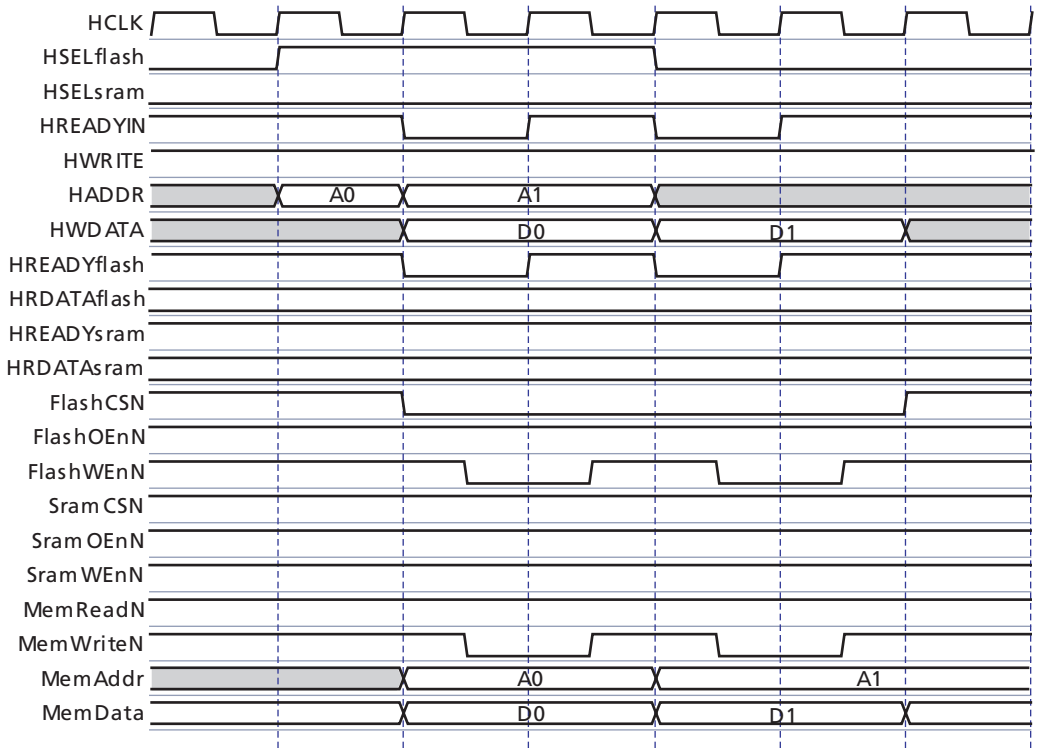

Figure 2 • **Flash Write with 0ne wait state**

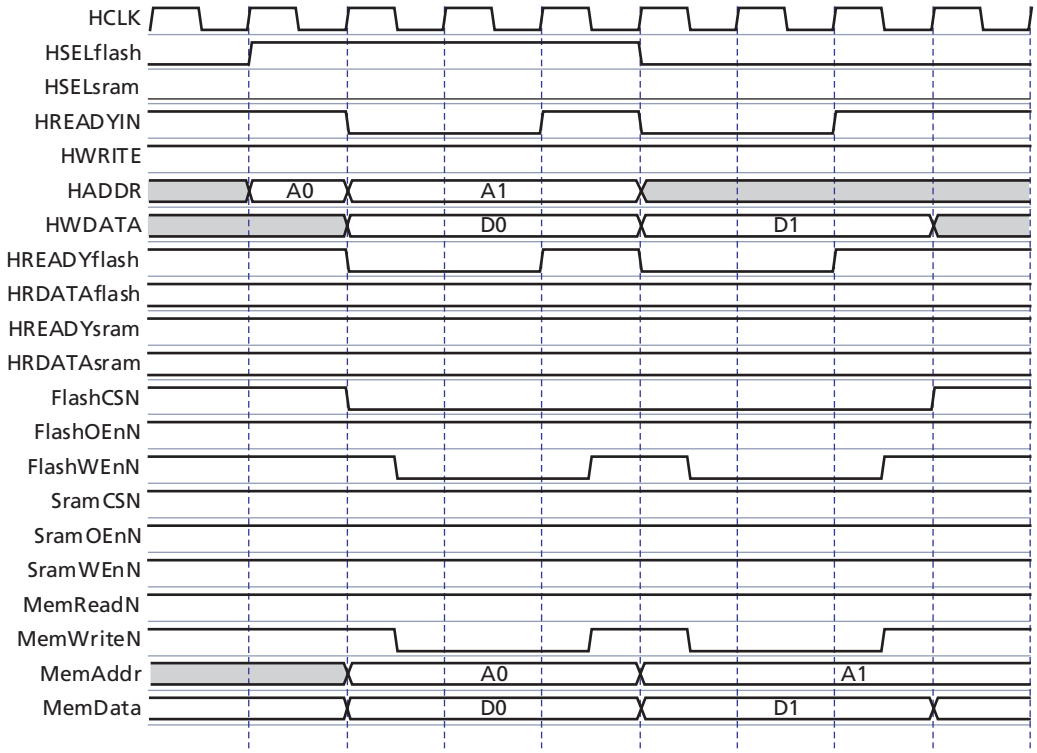

Figure 3 • **Flash Write with Two Wait States**

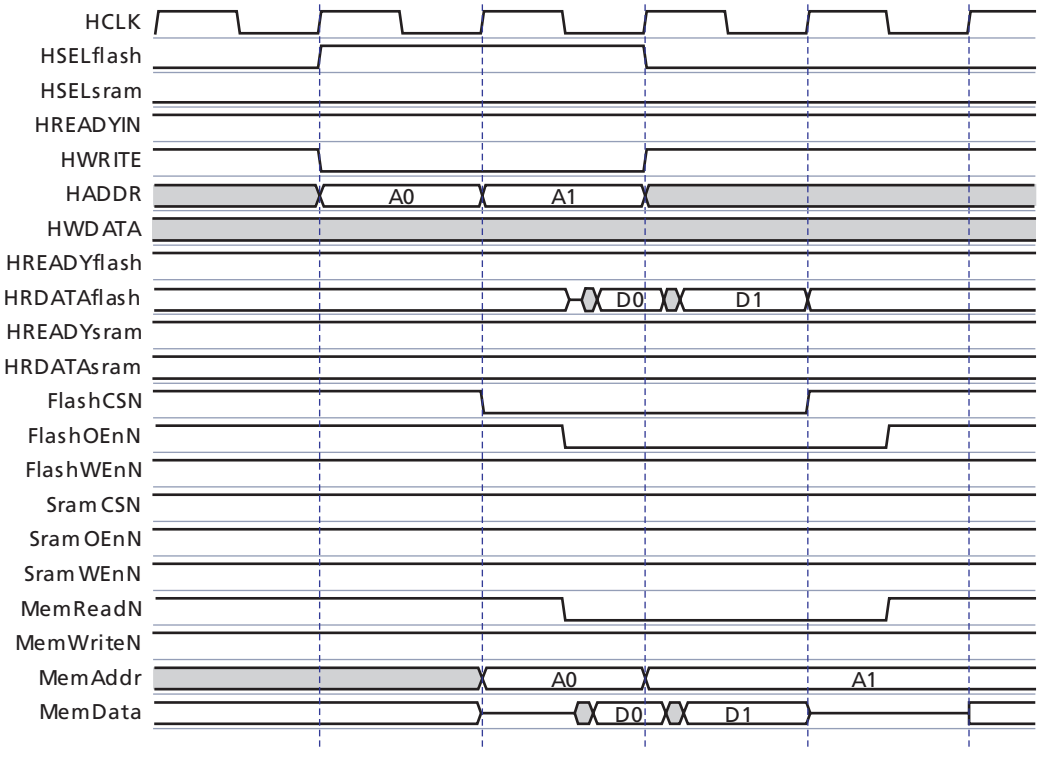

Figure 4 • **Flash Read with No Wait States**

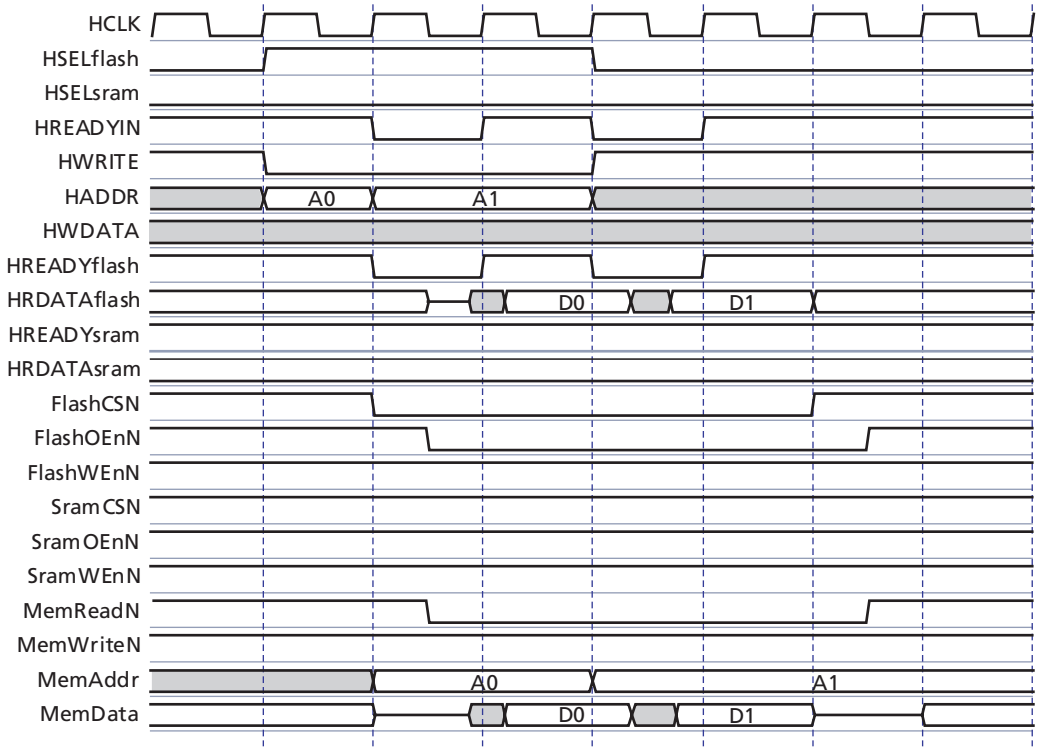

Figure 5 • **Flash Read with One Wait State**

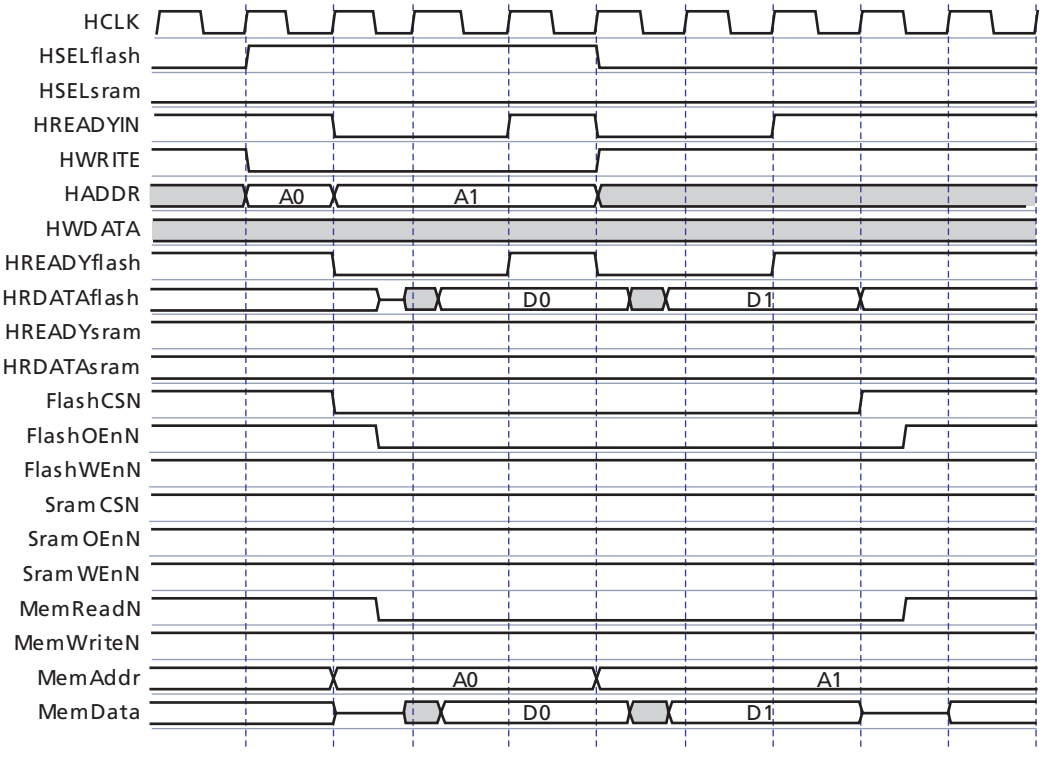

Figure 6 • **Flash Read with Two Wait States**

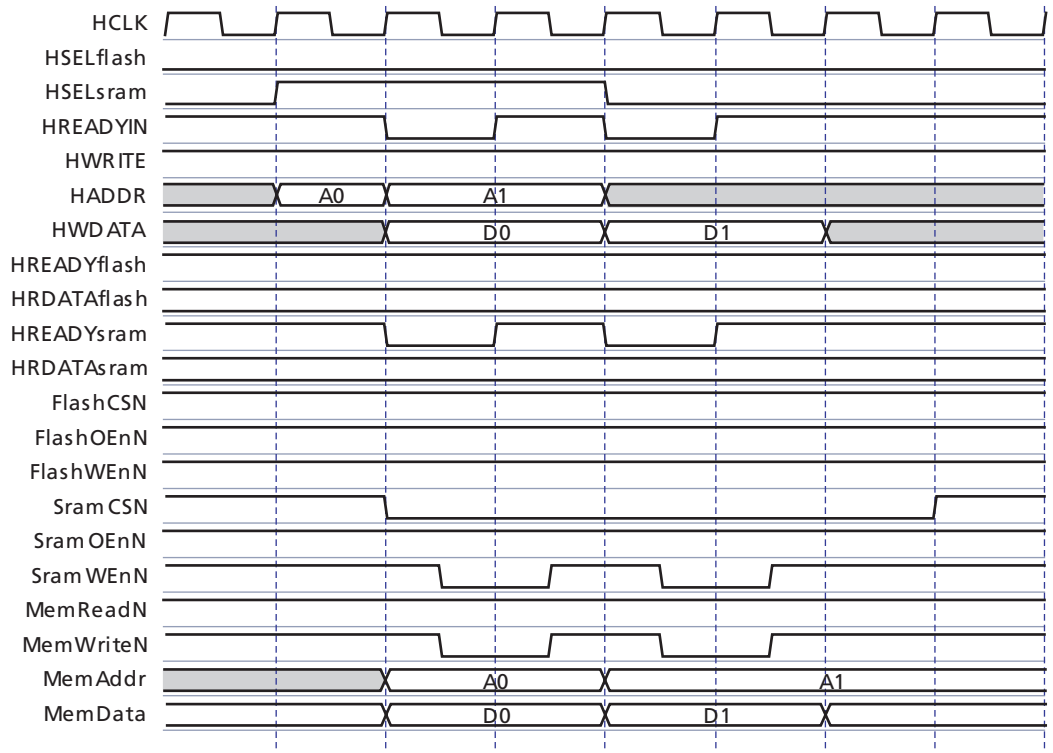

Figure 7 • **Asynchronous SRAM Write with One Wait State**

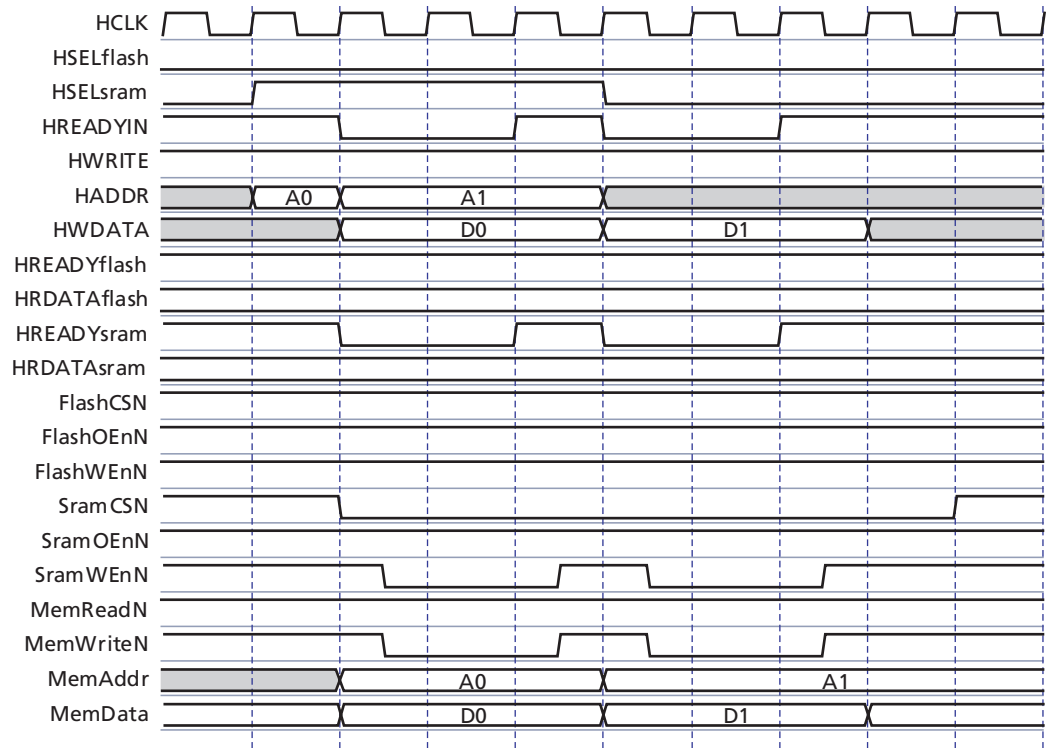

Figure 8 • **Asynchronous SRAM Write with Two Wait States**

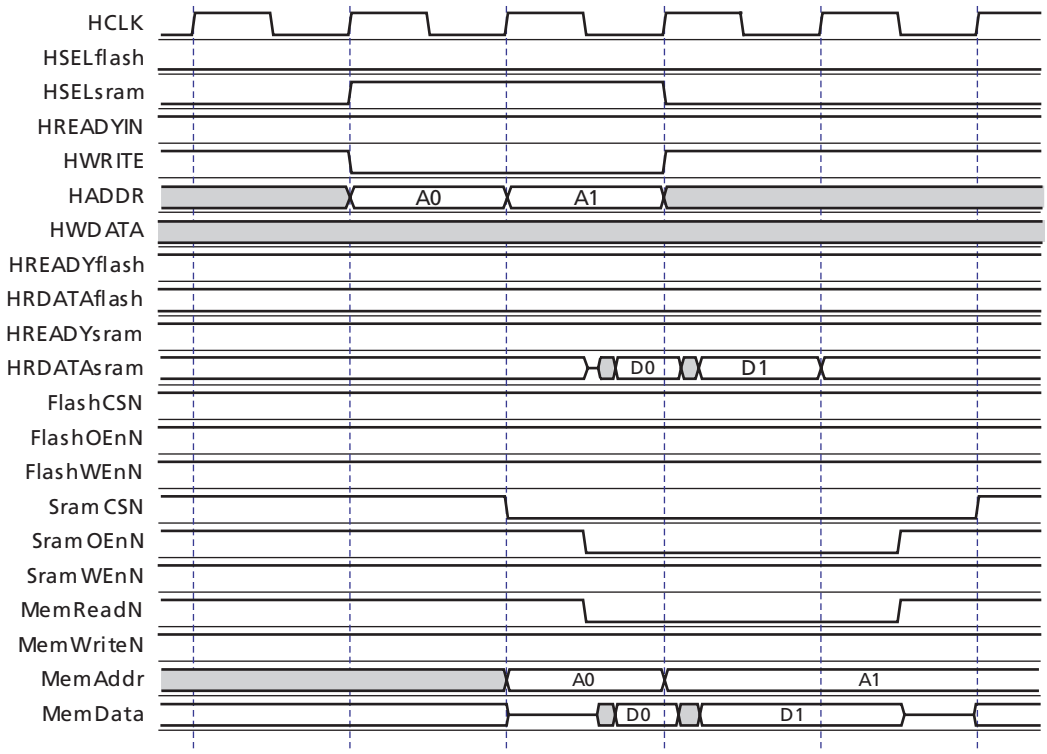

Figure 9 • **Asynchronous SRAM Read with No Wait States**

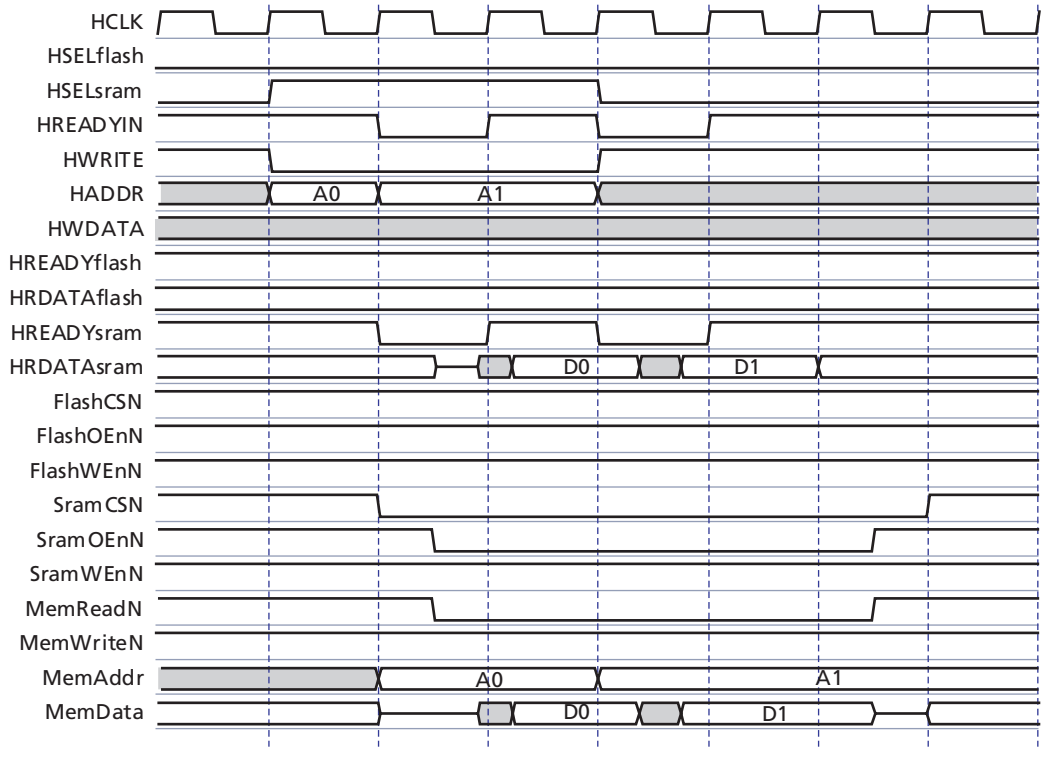

Figure 10 • **Asynchronous SRAM Read with One Wait State**

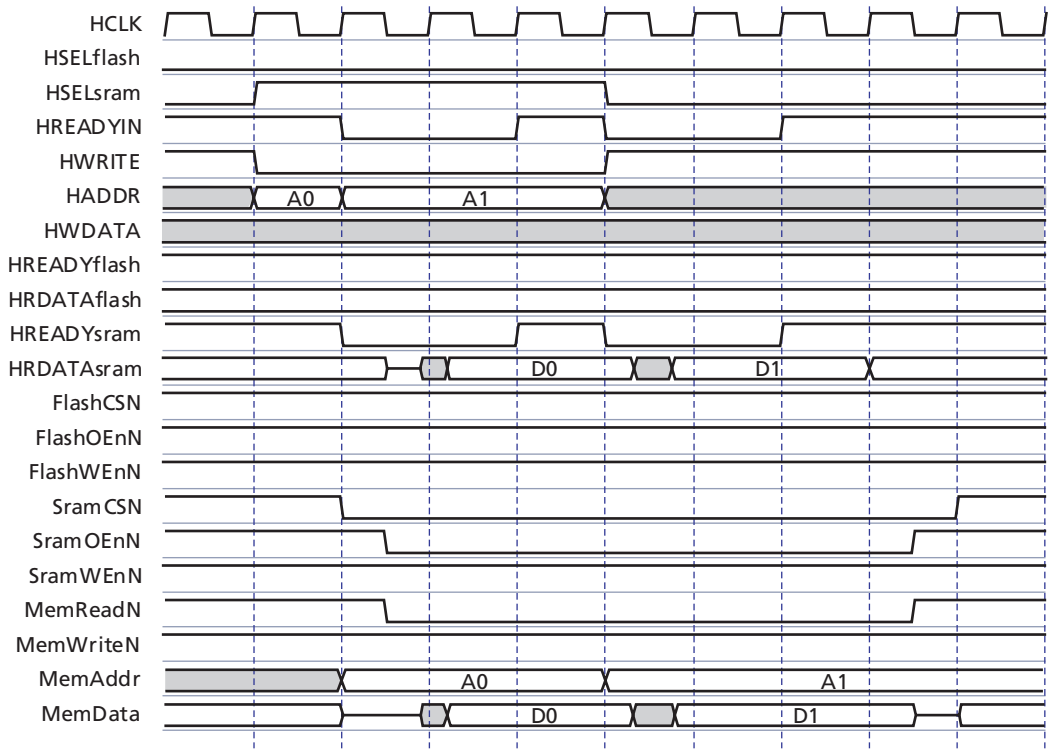

Figure 11 • **Asynchronous SRAM Read with Two Wait States**

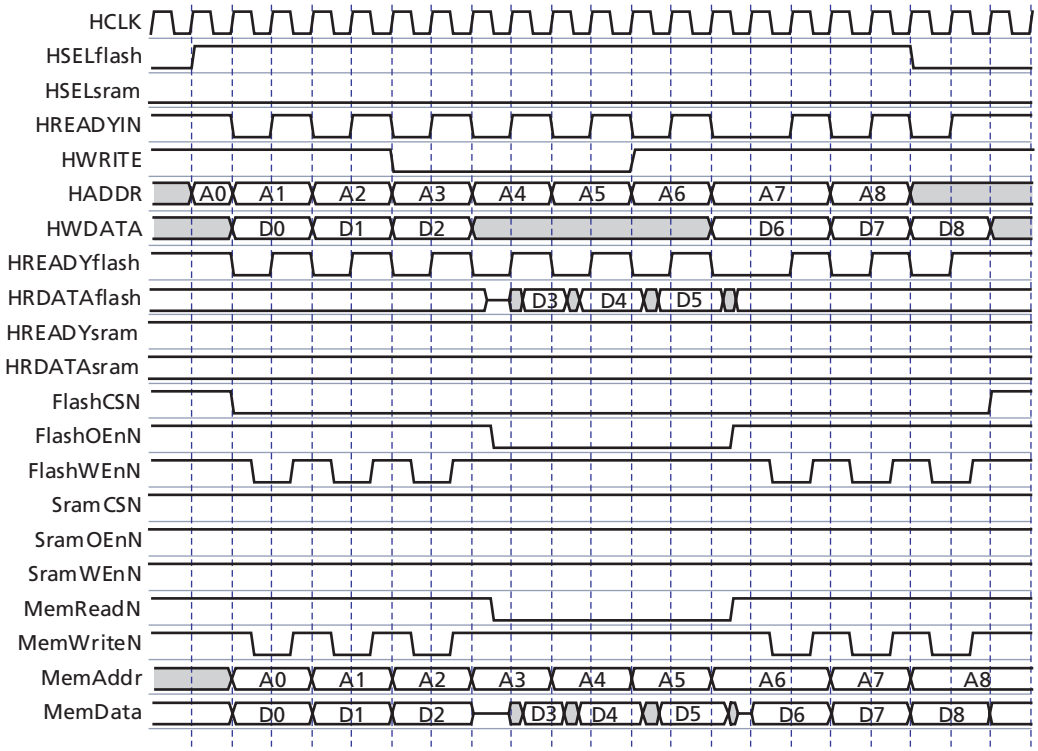

Figure 12 • **Multiple Flash Writes and Reads (one wait state)**

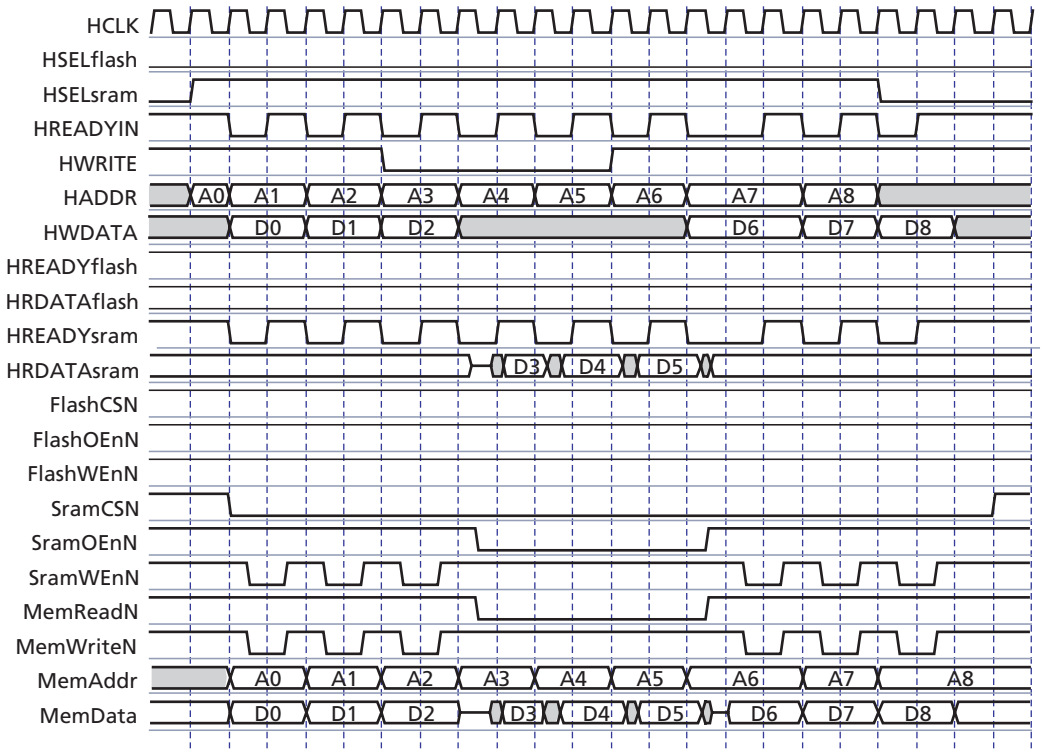

Figure 13 • **Multiple Asynchronous SRAM Writes and Reads (one wait state)**

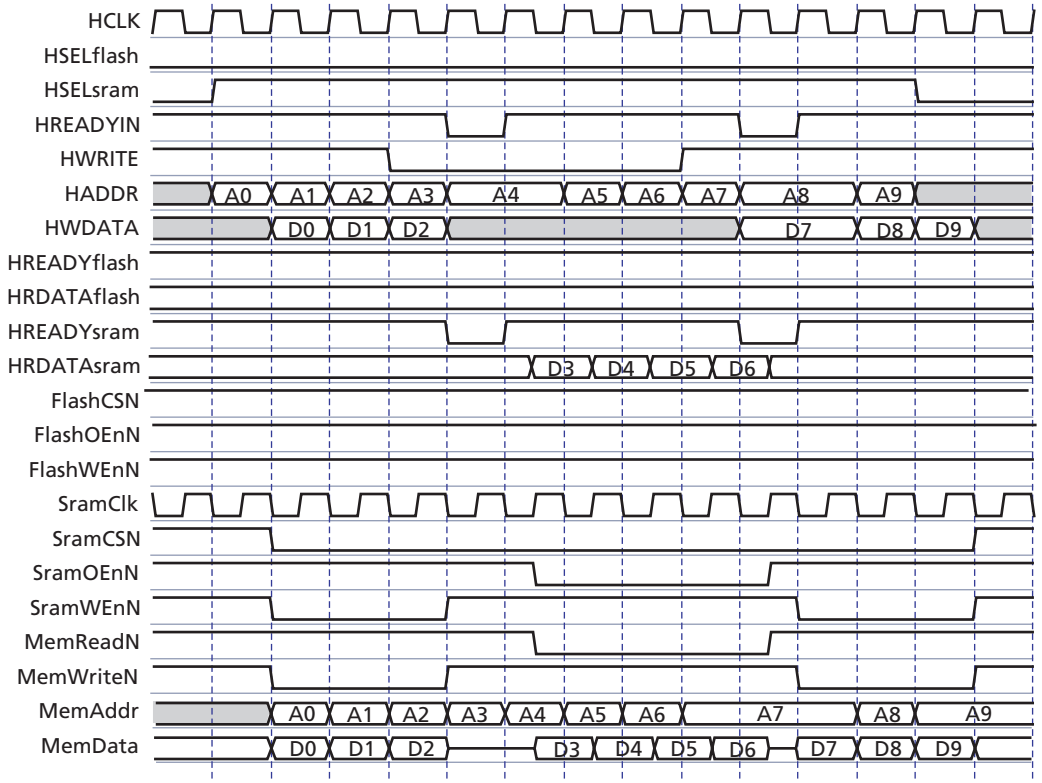

Figure 14 • **Multiple Synchronous SRAM Writes and Reads**

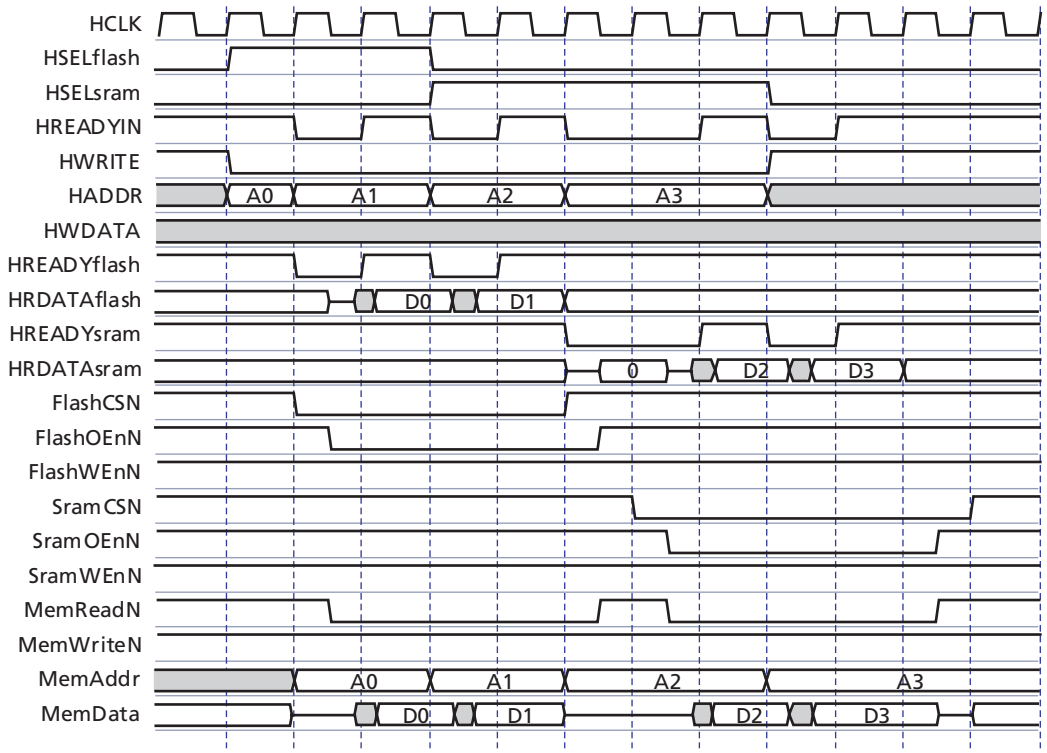

Figure 15 • **Flash Read Followed by Asynchronous SRAM Read**

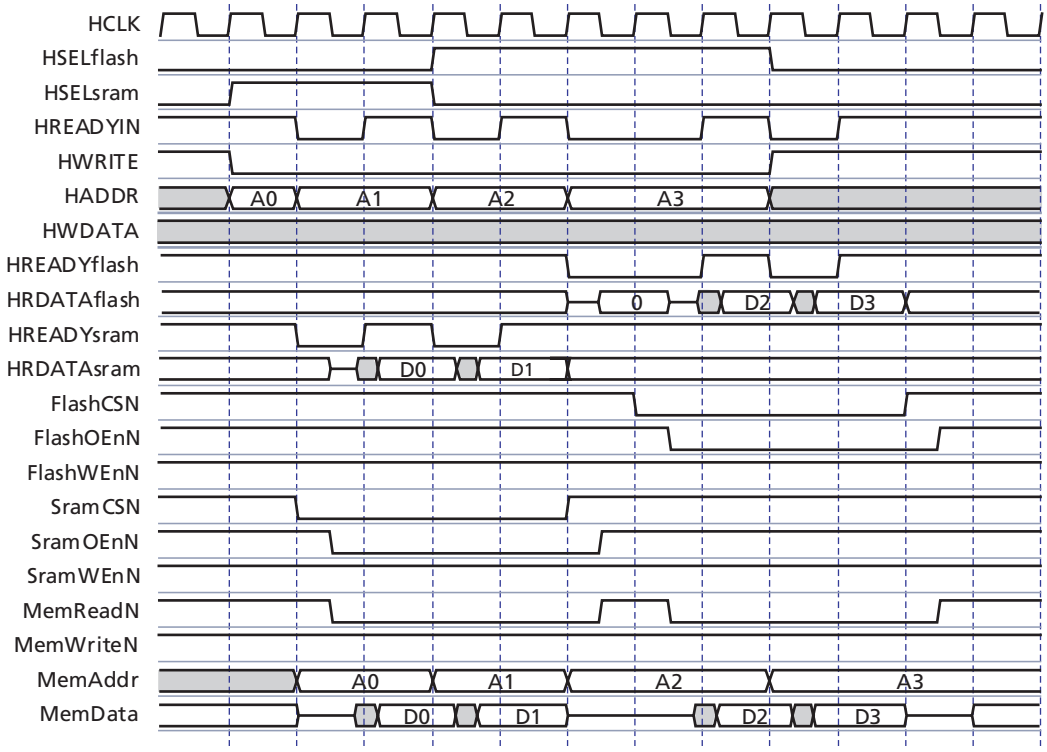

Figure 16 • **Asynchronous SRAM Read Followed by Flash Read**

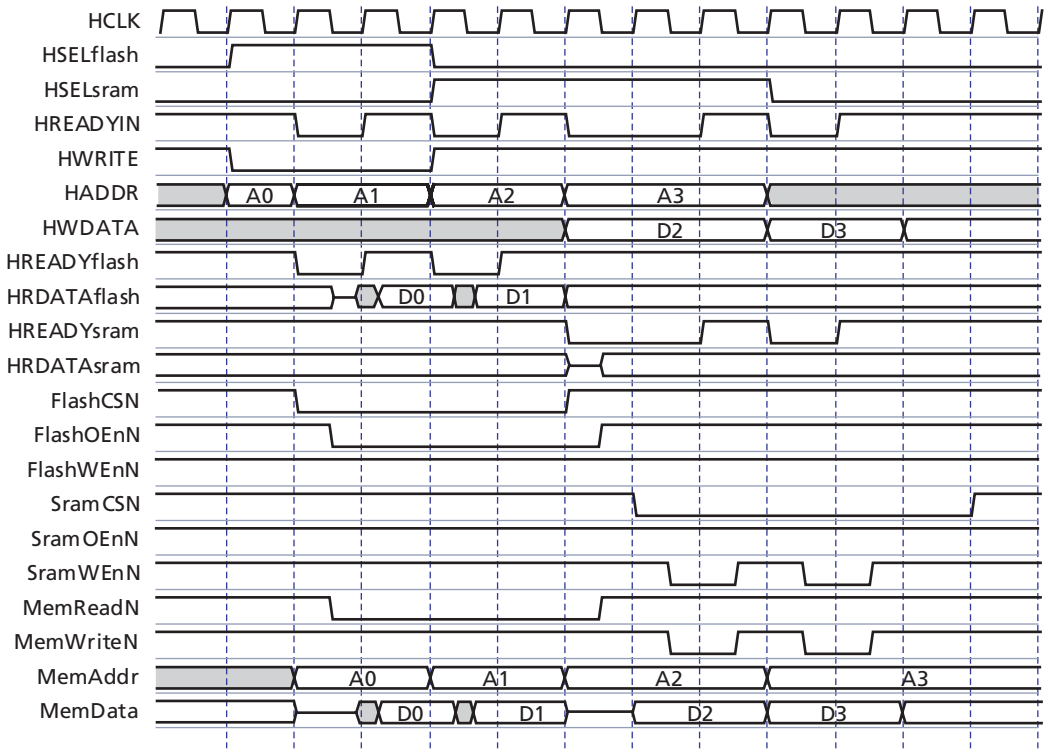

Figure 17 • **Flash Read Followed by Asynchronous SRAM Write**

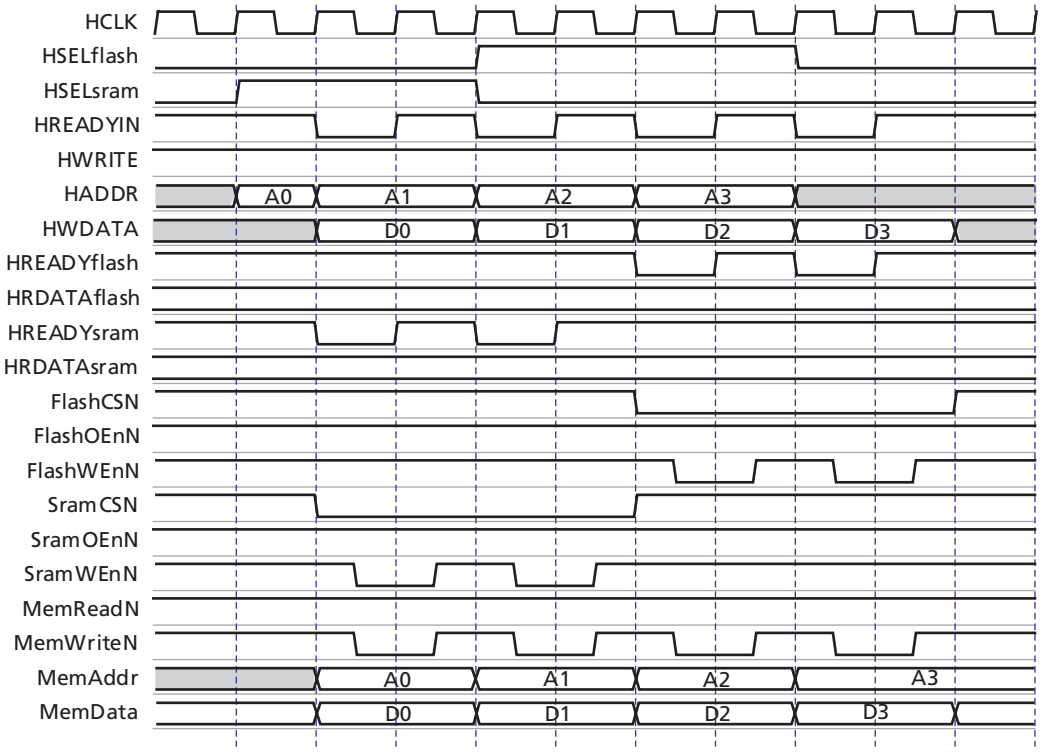

Figure 18 • **Asynchronous SRAM Write Followed by Flash Write**

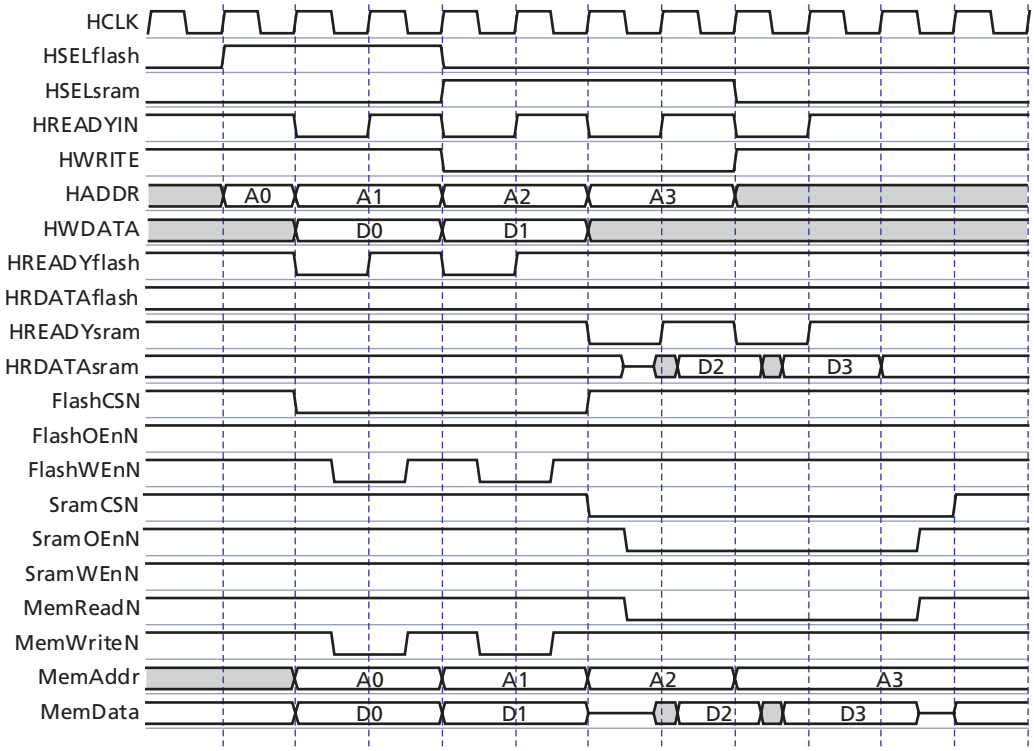

Figure 19 • **Flash Write Followed by Asynchronous SRAM Read**

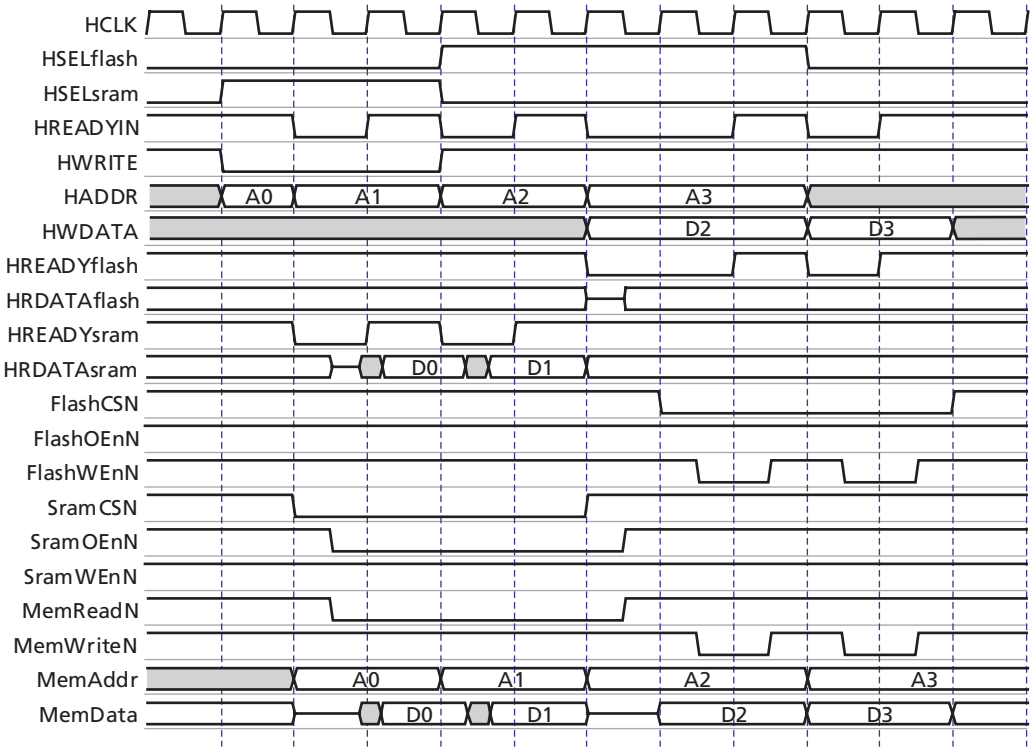

Figure 20 • **Asynchronous SRAM Read Followed by Flash Write**

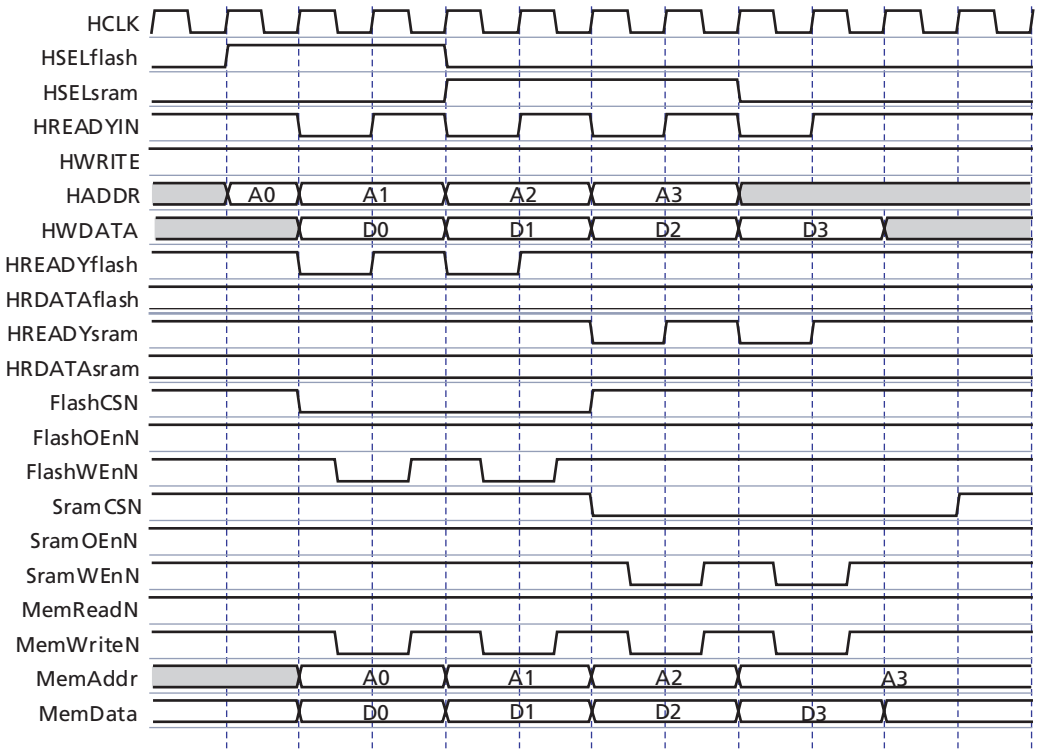

Figure 21 • **Flash Write Followed by Asynchronous SRAM Write**

Figure 22 • **Asynchronous SRAM Write Followed by Flash Read**

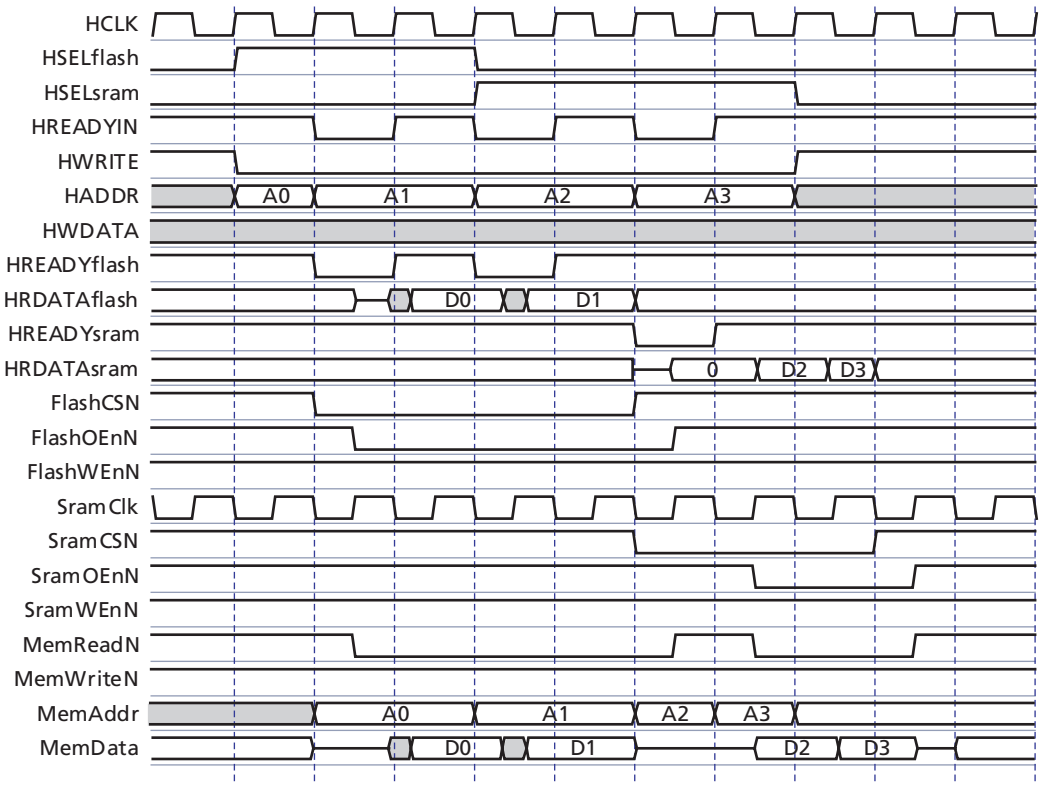

Figure 23 • **Flash Read Followed by Synchronous SRAM Read**

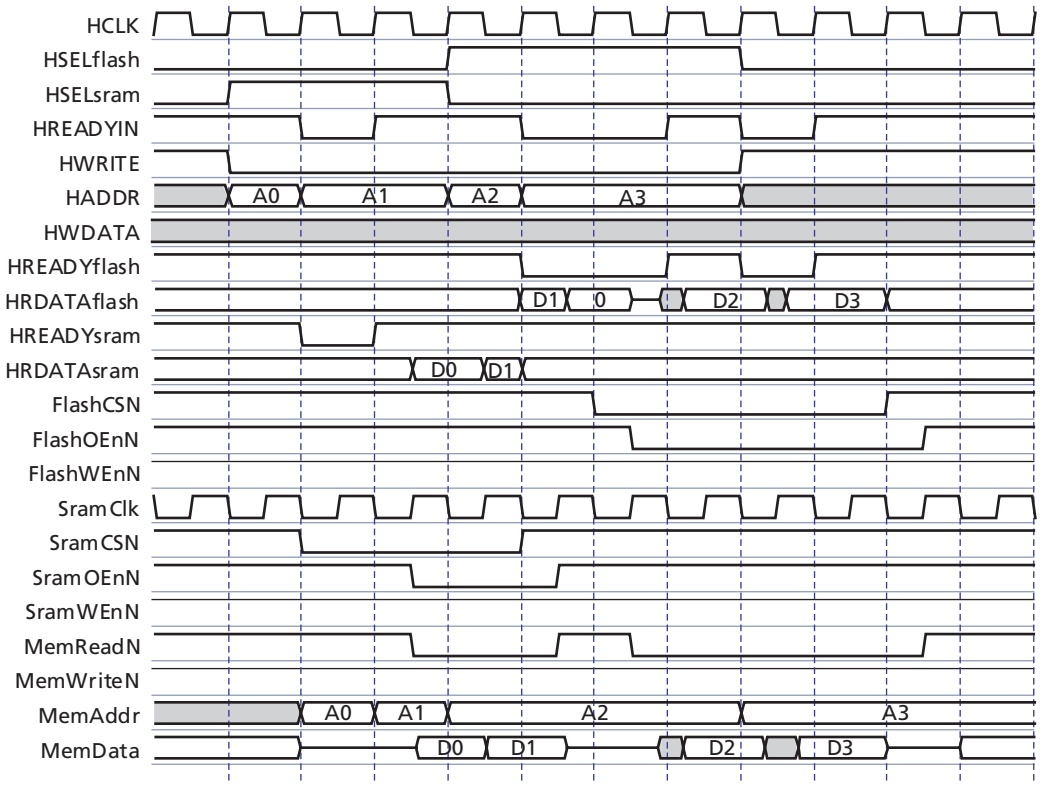

Figure 24 • **Synchronous SRAM Read Followed by Flash Read**

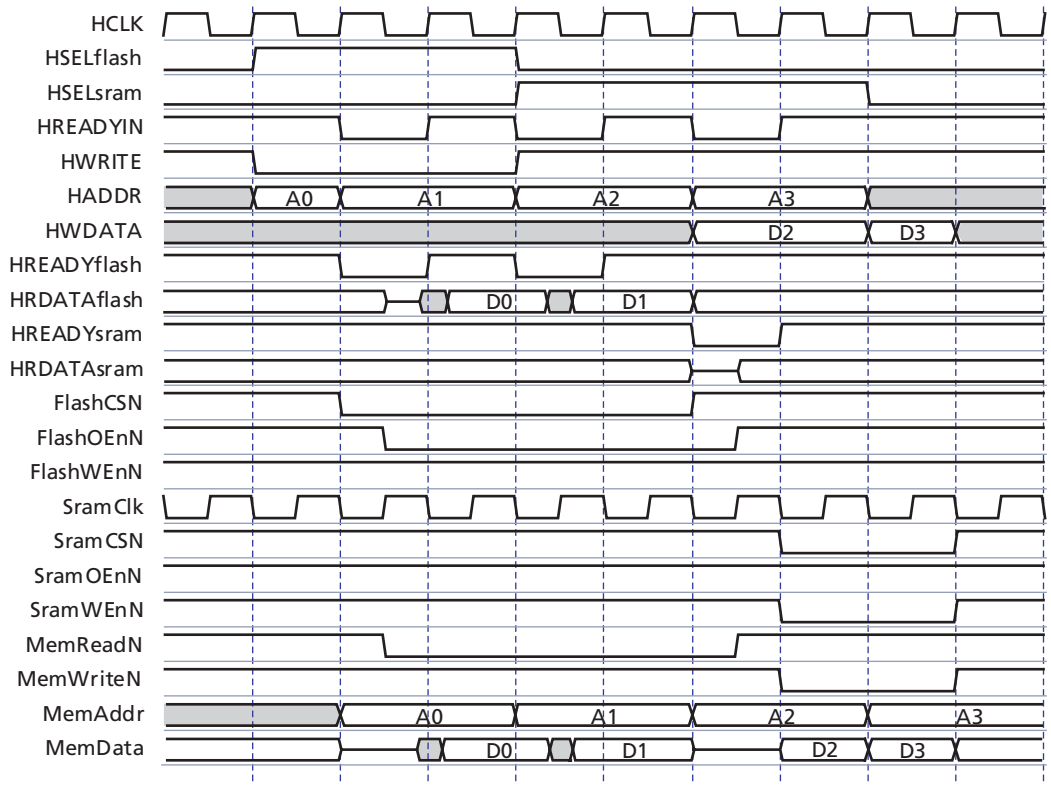

Figure 25 • **Flash Read Followed by Synchronous SRAM Write**

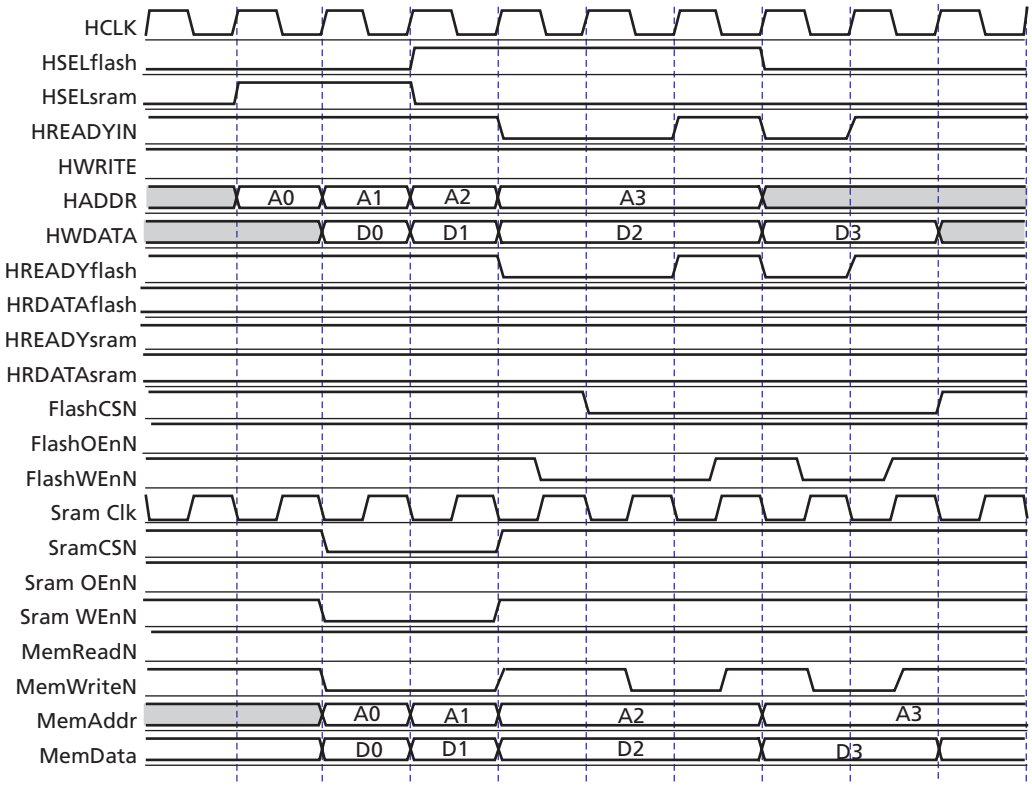

Figure 26 • **Synchronous SRAM Write Followed by Flash Write**

Figure 27 • **Flash Write Followed by Synchronous SRAM Read**

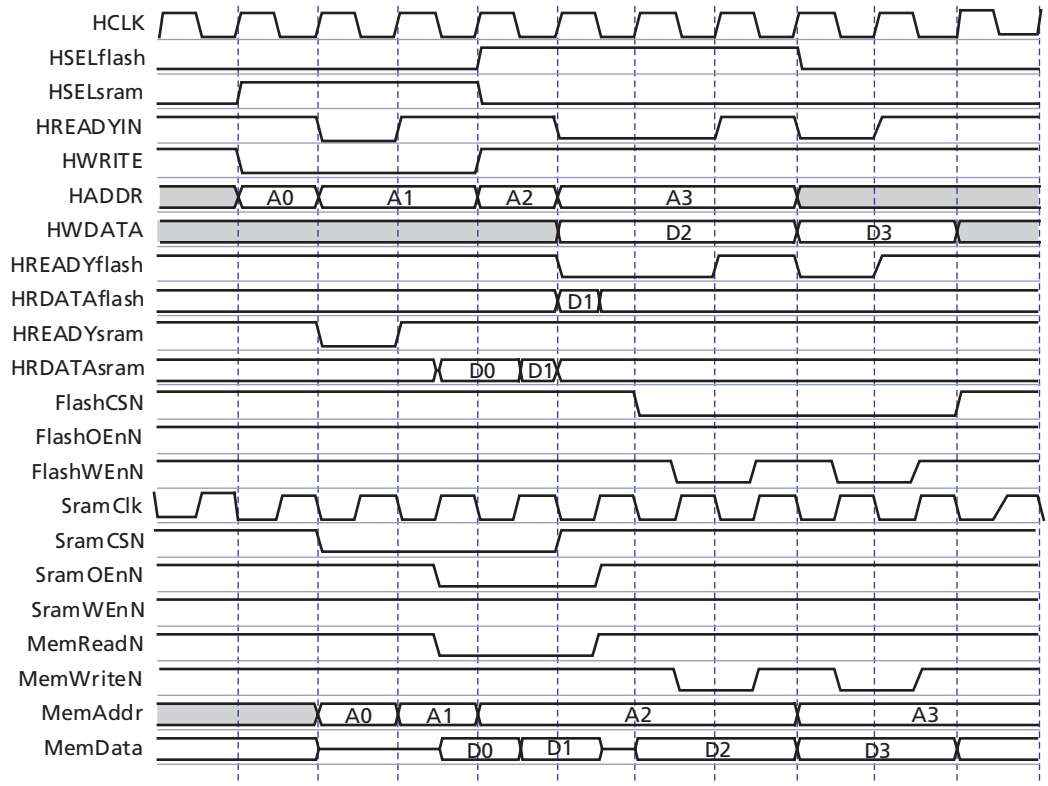

Figure 28 • **Synchronous SRAM Read Followed by Flash Write**

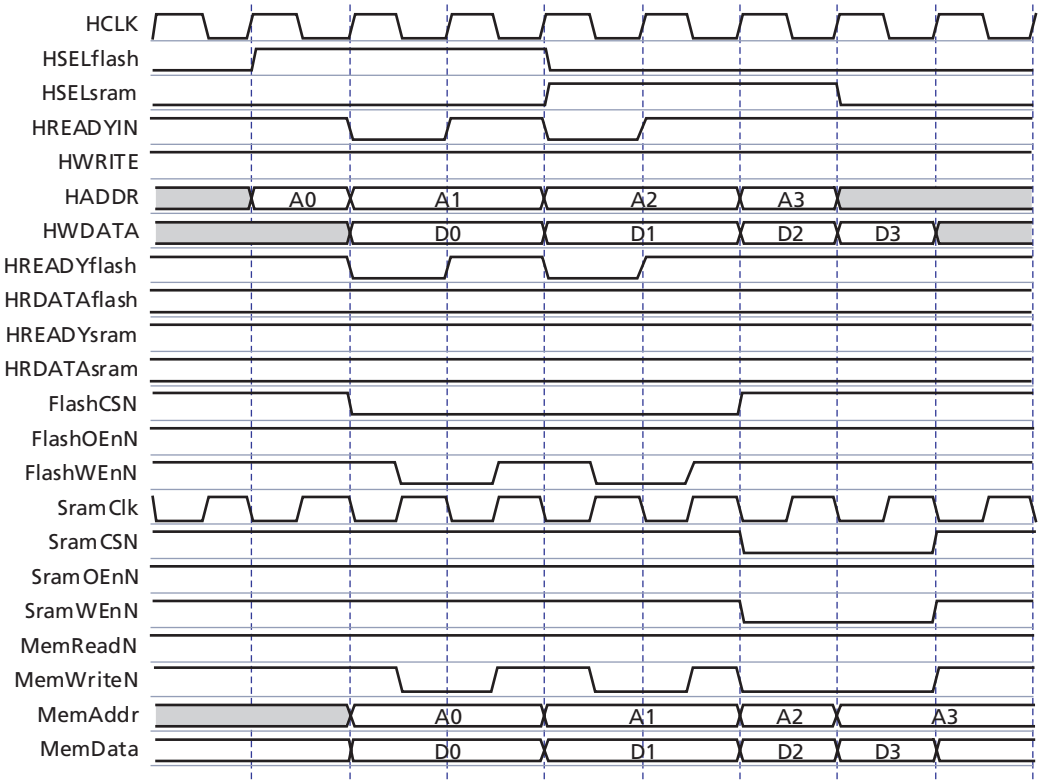

Figure 29 • **Flash Write Followed by Synchronous SRAM Write**

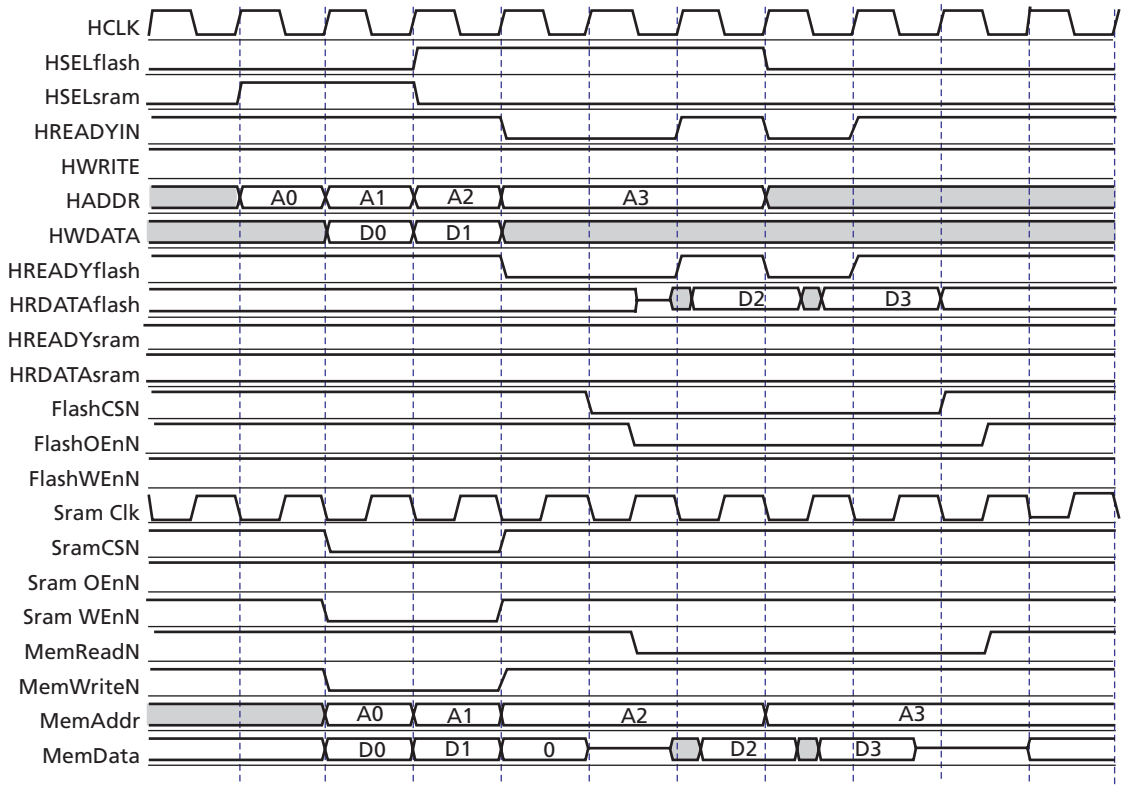

Figure 30 • **Synchronous SRAM Write Followed by Flash Read**

Resource Requirements

The utilization for CoreMemCtrl in a ProASIC3E device is 380 tiles.

Ordering Information

CoreMemCtrl is included in the SysBASIC core bundle supplied with the Actel CoreConsole IP Deployment Platform (IDP). The obfuscated RTL version of SysBASIC (SysBASIC-OC) is available for free with CoreConsole. The source RTL version of SysBASIC (SysBASIC-RM) can be ordered through your local Actel sales representative. CoreMemCtrl cannot be ordered separately from the SysBASIC core bundle.

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous Version	Changes in Current Version (v3.0)	Page
v2.0	The "Product Summary" section was updated to include Cortex-M1 and IGLOO/e information.	1
	Table 2 • CoreMemCtrl Connections was updated to include Cortex-M1 for HCLK and HRESETn.	4
Advanced v0.2	The "External Memory Interface" section was updated to include discussion of Pipeline and Flow-Through mode, and use of the **synchronous Flow-Through SRAM device from Cypress.**	5
	Table 4 • CoreMemCtrl Configurable Options was updated to include the Synchronous SRAM Mode configuration option.	6

Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advanced," and "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of an advanced or production datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Unmarked (production)

This datasheet version contains information that is considered to be final.

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