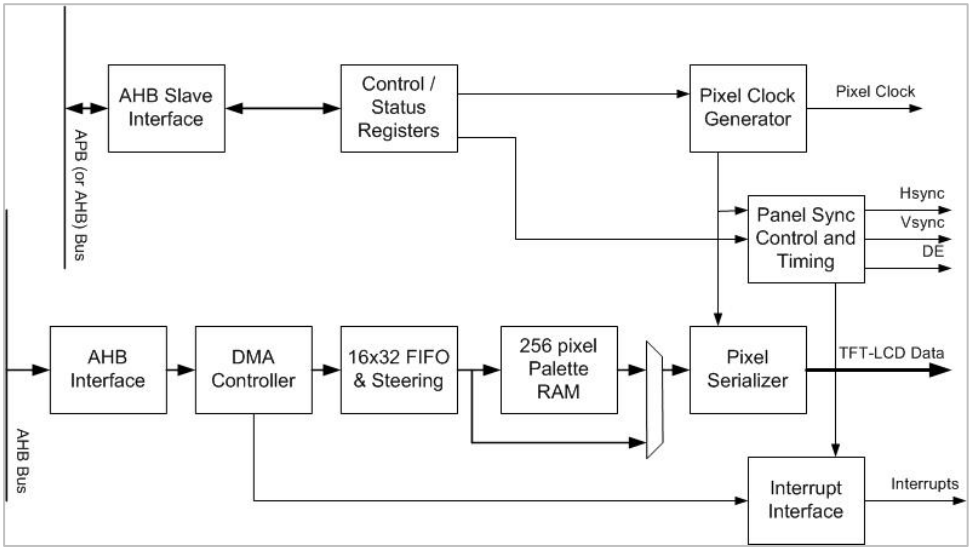
TFT LCD Controller
IPC-TFTLCD-AHB

Features

- 24 bit TFT LCD Controller
- 16x32 Pixel FIFO
- 256 Pixel Palette Mode
- True Color and 24 bit Color support
- Programmable Hsync and Vsync rates
- Supports up to 1024 x 768 resolution
- Pixel DMA controller
- Programmable Interrupt Interface
- Supports wide variety of system clock rates



General Description

The **IPC-TFTLCD** is a configurable TFT LCD Controller. The Core interfaces to an AHB or generic microprocessor bus and provides all the timing control and pixel serialization for controlling various TFT LCD Display Panels.

The **IPC-TFTLCD** controls both true color or 24bit color display mode using the 256 Pixel Palette Ram. Pixel clock generation, Sync Control and Display Enable controls are fully programmable and can be used with a wide range of system clock rates.

Display information is held in system memory and is accessed by the IPC-TFTLCD by the AHB DMA controller. In true color mode, 24bit pixels are accessed a 32bit word at a time. In 24bit color mode, 4 8bit pixels are accessed a 32bit word at a time and then serialized as 24bit palette mapped pixels.

The LCD data interface contains 8bit Red, 8bit Green, and 8bit Blue for a total of 24bits. The Interface will interface with 6bit RGB panels as well.

Interrupt sources timed to Hsync, Vsync and control signals are programmable and selectable to signal the processor to update display information.

IP Package

The **IPC-TFTLCD** package includes Verilog source and simulation test-benches. The **IPC-TFTLCD** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

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