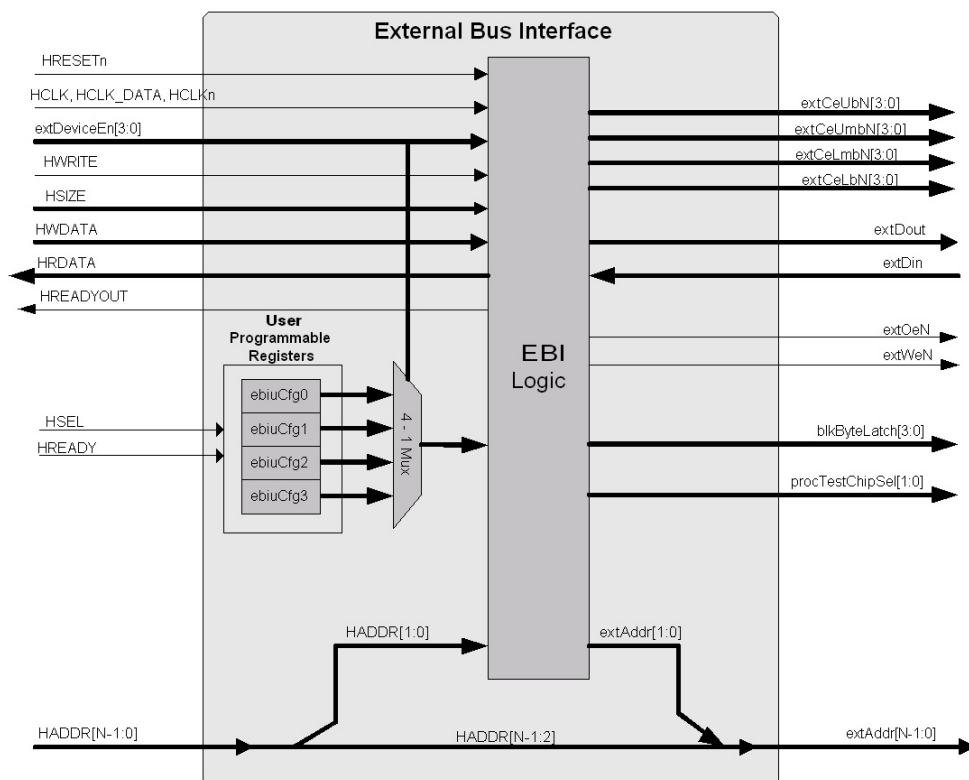SoC Solutions™

Features

- Configurable External Bus Interface

- Scalable number of external devices

- Programmable access times

- Independent 8, 16, or 32 bit data interface

- Byte, 16 bit half-word and 32 bit word accessible

- AMBA AHB compatible

- Single cycle external bus access selectable

- Single cycle processor bus access

General Description

The IPC-EBI External Bus Interface is a configurable module designed to interface an AMBA AHB bus to a generic External Bus. The external bus interface (EBI) allows the processor to transmit and receive data to and from external devices, one or more of which may be memory. External memory can be SRAM, Flash, etc. The user can configure (or program) the IPC-EBI to the proper number of read and write wait states and the memory size to allow proper communication. The IPC-EBI allows word, half-word, and byte width addressing to 32-bit, 16-bit, and 8-bit external devices.

The IPC-EBI interfaces the AHB bus to up to 4 external devices. The HDL source was designed to allow the user to easily scale the EBI to accomodate more than 4 devices. Each device has a configuration register. The 2 LSBs of the address bus are modified depending on the type of access specified by the processor and the capabilities of the device (as programmed into the configuration register). The EBI logic performs this and other tasks such as:

- breaks down device enables into upper, upper middle, lower middle, & lower bank chip enables

- steers data bytes or halfwords onto appropriate data bits

- sequences multi-byte or multi-halfword read and write operations

- puts the processor in a wait state until the access completes

IP Package

The **IPC-EBI** package includes fully tested and verified Verilog source and Verilog testbench. The **IPC-EBI** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.