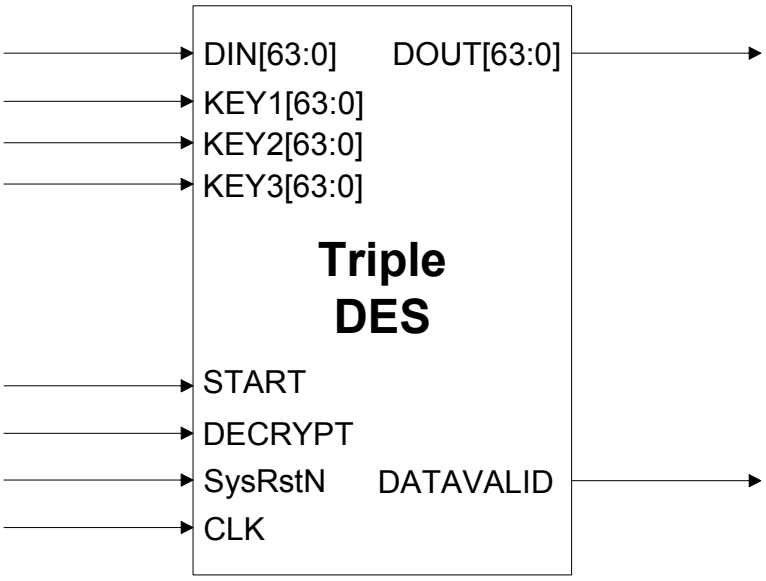
Triple Data Encryption Standard Core
IPC-TDES

Features

- FIPS 46-3 Standard Compliant
- Encryption/Decryption performed in 48 cycles (ECB mode)
- Up to 168 bits of security
- For use in FPGA or ASIC designs
- Verilog IP Core



Applications

- Secure video
- Electronic Funds Transfer
- Encrypted Storage Data
- Secure communications

Overview

The **IPC-TDES** core is a complete implementation of the Triple Data Encryption Standard (TDES) documented in the U.S. Government publication FIPS 46-3.

The **IPC-TDES** core is a block cipher, working on 64 bits of data at a time. It is built upon the **IPC-DES** core. Key length is 56 bits. Encoding and decoding operations are performed in only 48 cycles, in Electronic Codebook (ECB) mode. Other modes are available.

The **IPC-TDES** core can be used in wired, wireless secure data applications

IP Package

The **IPC-TDES** package includes fully tested and verified Verilog source. The **IPC-TDES** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

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