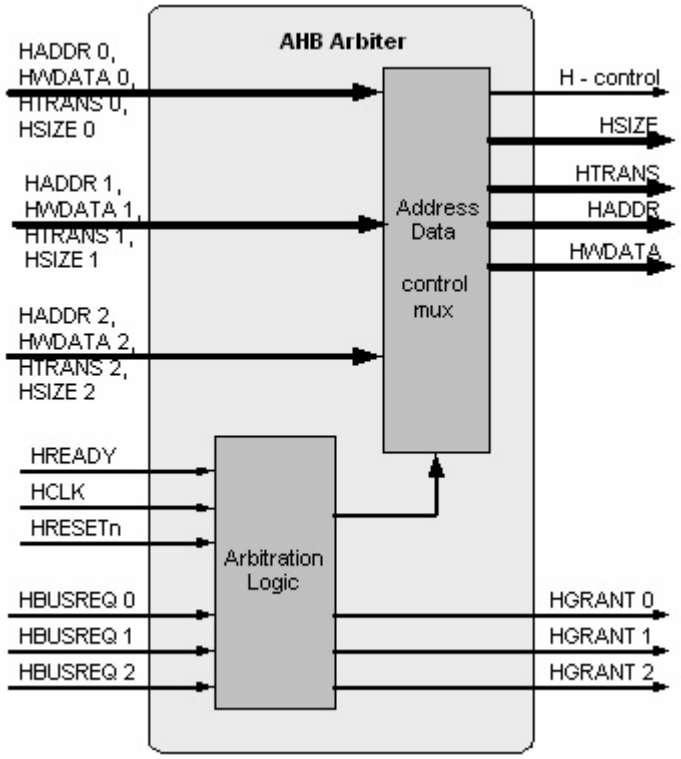
AMBA AHB Arbiter
IPC-AhbArbiter-AHB

Features

- Round robin priority
- Scalable (Up to 16 masters)
- AMBA AHB interface
- HWDATA, HADDR and AHB control steering
- HBUSREQ and HGRANT arbitration



General Description

The **IPC-AhbArbiter** is used in AMBA AHB multi-master systems to arbitrate the access to the AHB bus. The **IPC-AhbArbiter** is basically a "traffic controller" which allows the AHB bus to be shared between multiple bus masters such as processors, dma controllers, and peripheral core master interfaces.

The **IPC-AhbArbiter** uses a round robin priority scheme with Master0 having the default priority. This priority scheme assures that each master equally has it's turn at acquiring and completing an AHB bus transaction. Each inactive master is locked out (HLOCK) while the active master has access to the bus to prevent contention.

The **IPC-AhbArbiter** steers all the AHB HWDATA, HADDR, HTRANS, HWRITE, HSIZE and HBURST signaling from each master to the AHB system bus.

The **IPC-AhbArbiter** is delivered as a three master arbiter but can easily be configured to allow up to sixteen AHB bus masters.

IP Package

The **IPC-AhbArbiter** package includes fully tested and verified Verilog source. The **IPC-AhbArbiter** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

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