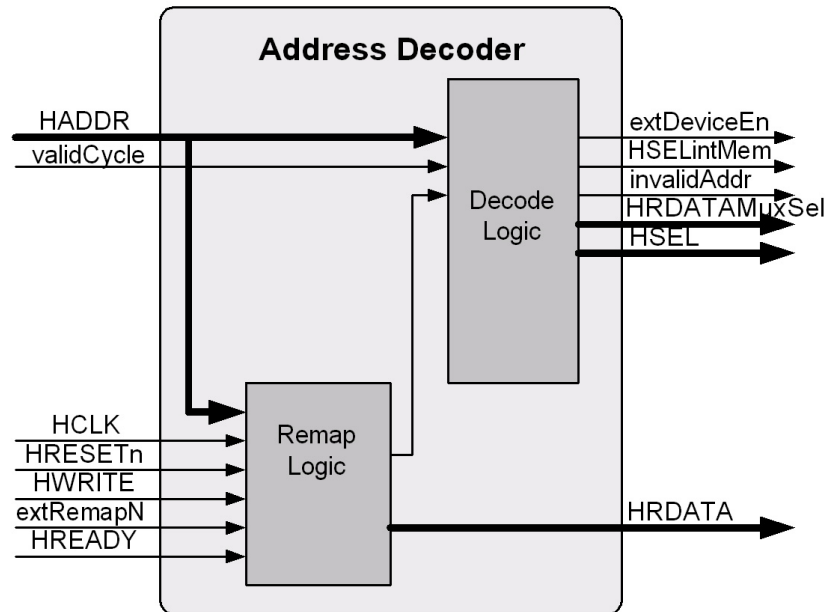## Features

- Scalable Address Decoder
- Hardware and software remap controls
- Invalid address detection
- AMBA AHB interface

Address Decoder

General Description

The **IPC-Adec** is a fully scalable Address Decoder with a built in remap function to support multiple memory maps. The **IPC-Adec** generates separate enable signals for external devices such as FLASH and SRAM, internal memory, and various internal blocks. Datamux select signals are also generated to control which data is muxed onto the AHB data bus. The Address Decoder also detects and reports invalid addresses from the address bus.

The built-in remap logic is controllable through hardware and software. Hardware remap controls allow developers to force a memory map with a jumper connection. This is useful during system development and debugging where an in-circuit debugging system is used to boot from volatile memory. Software remap control allows for the system to be remapped on the fly during normal operation.

The **IPC-Adec** has an AMBA AHB interface.

IP Package

The **IPC-Adec** package includes fully tested and verified Verilog source. The **IPC-Adec** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.