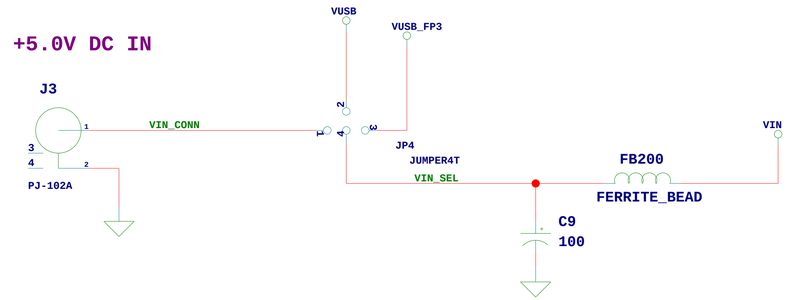
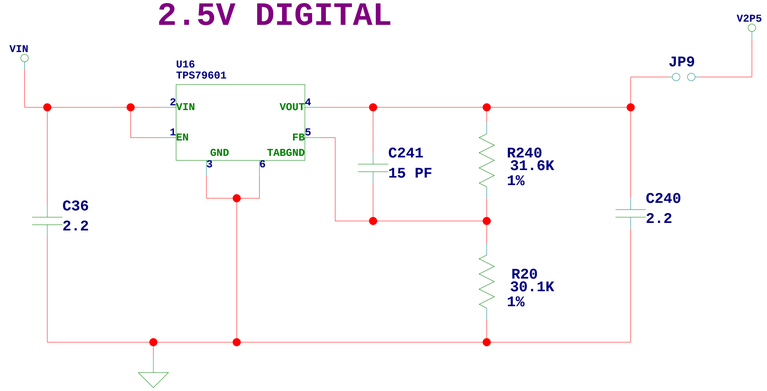
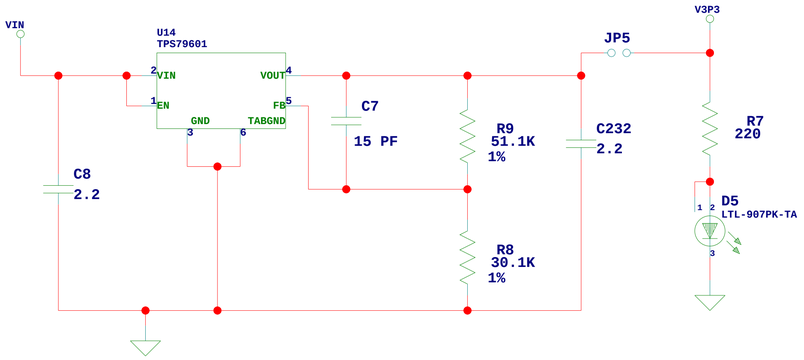
+5.0V DC IN



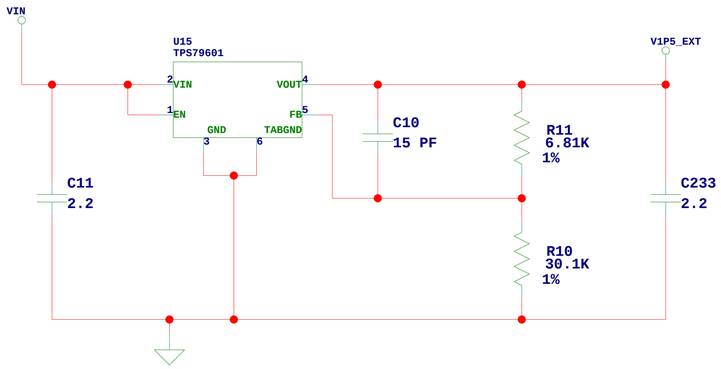
2.5V DIGITAL



3.3V DIGITAL & ANALOG



1.5V EXT



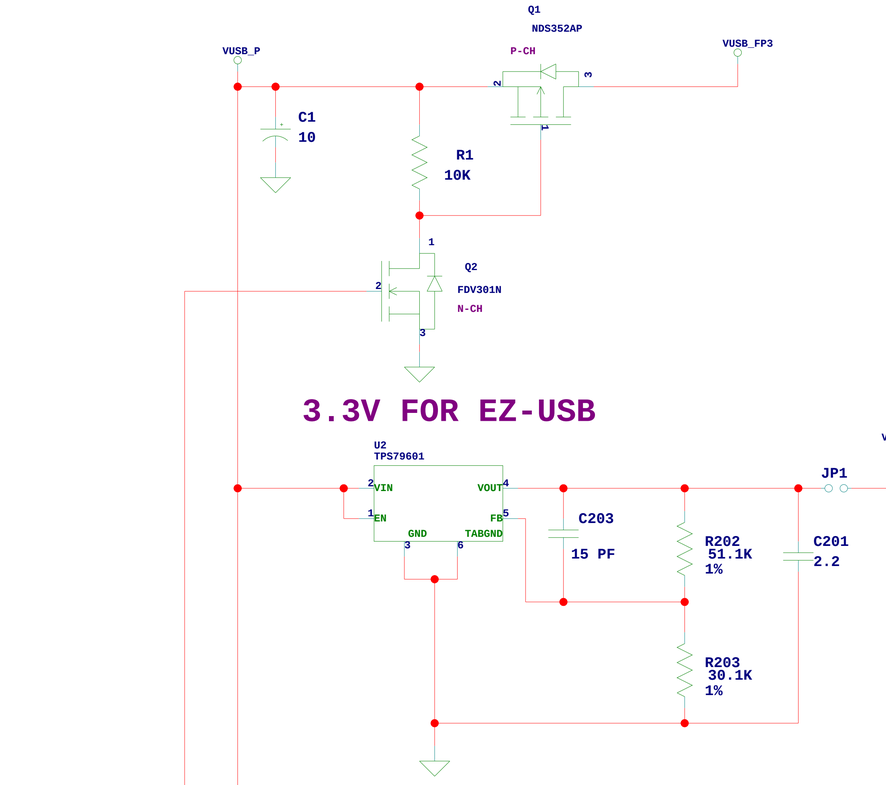
MOUNTING HOLES

MT1 MT2 MT3 MT4 MT5 MT6 MT7

GROUND TESTPOINTS

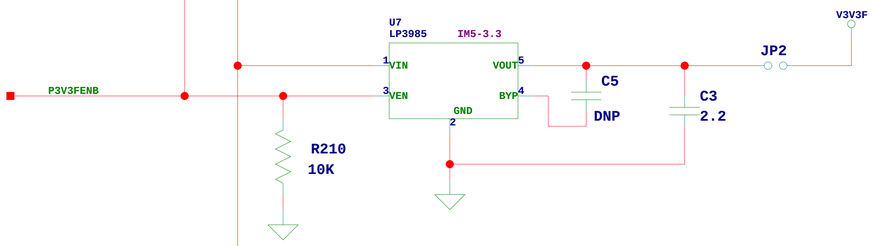
TPG2 TPG6 TPG5 TPG4 TPG1 TPG7 TPG3

DRAFTER: JIM AVANT	DATE	SoC Solutions
CHECKER	DATE	TITLE: POWER SUPPLIES
ENGINEER	DATE	SIZE: D — DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	
APPROVAL	DATE	DATE — SHEET: 1 OF 9

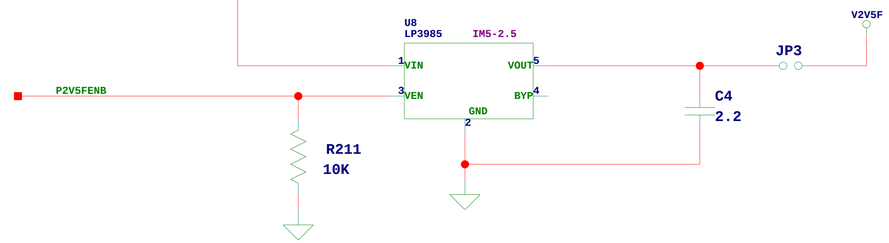


3.3V FOR EZ-USB

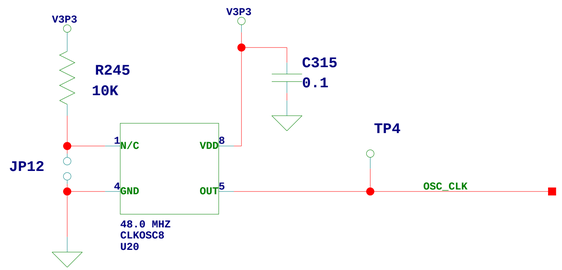
3.3V FOR APA FPGA



2.5V FOR APA FPGA

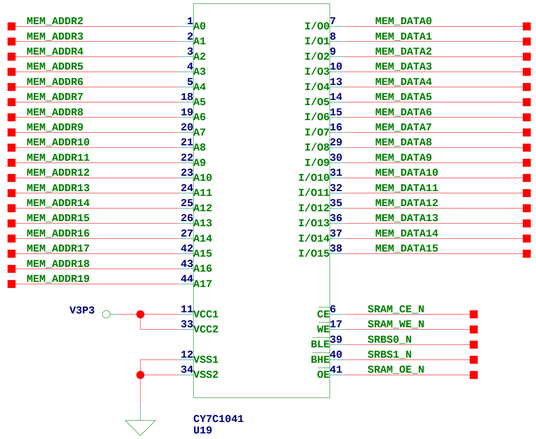


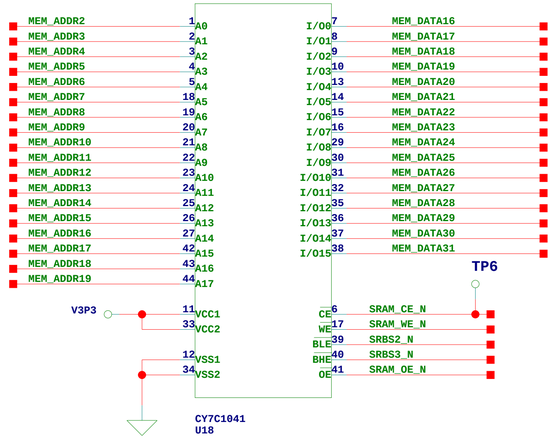
CLOCK OSCILLATOR



NOTE: FACTORY INSTALLED OSC. DOES NOT HAVE ENABLE INPUT.

DRAFTER: JIM AVANT	DATE	SoC Solutions
CHECKER	DATE	TITLE: PWR, CLOCK
ENGINEER	DATE	SIZE: D; DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	
APPROVAL	DATE	DATE; SHEET: 2 OF 9

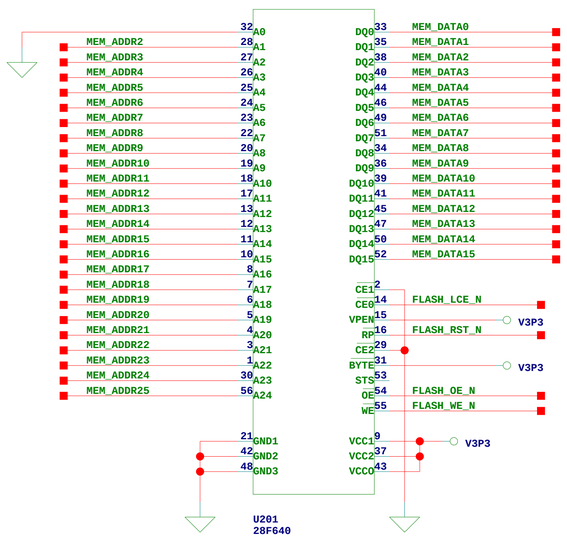


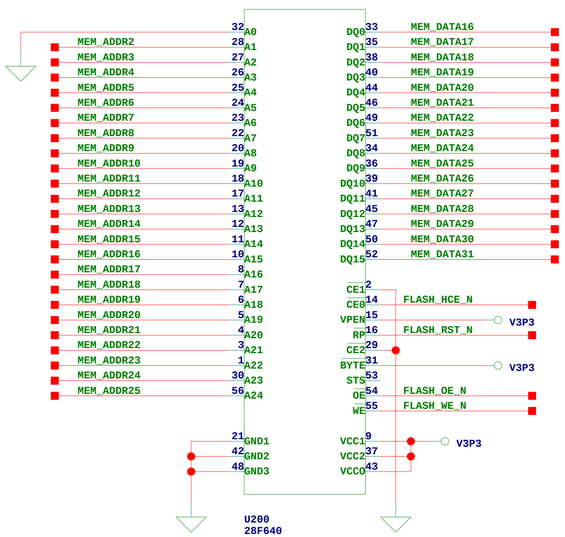


SRAM

1MB

256Kx32

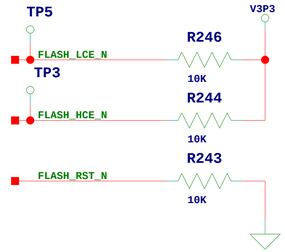


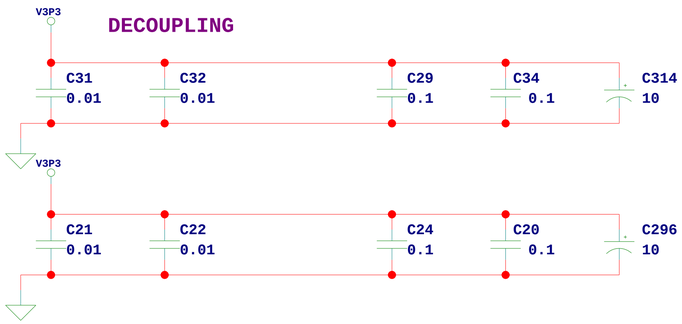


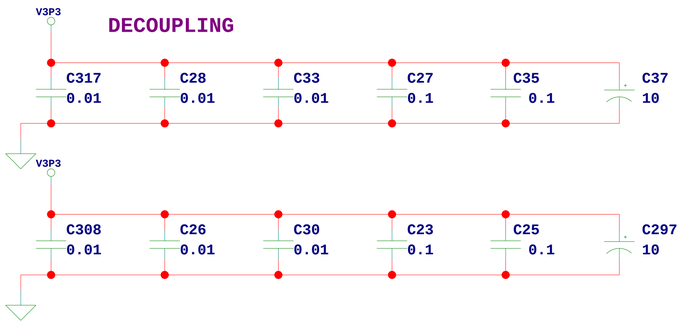
FLASH

16MB

4Mx32

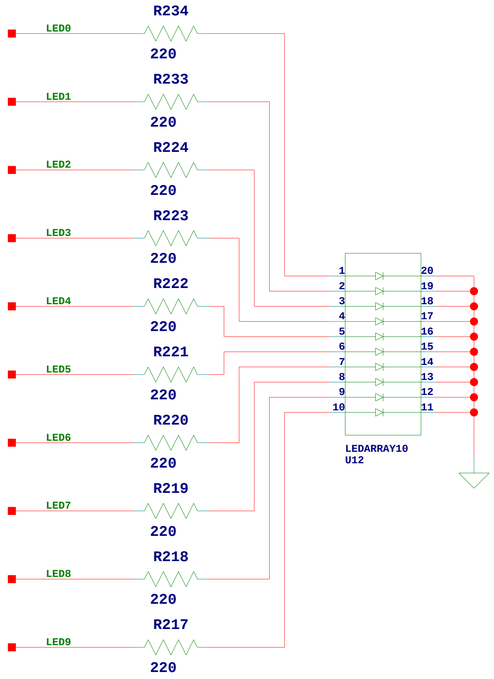




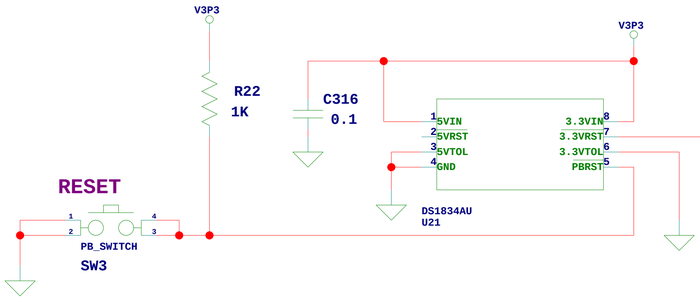


DRAFTER JIM AVANT	DATE	SoC Solutions
CHECKER	DATE	TITLE: SRAM & FLASH
ENGINEER	DATE	
APPROVAL	DATE	SIZE: D — DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	DATE — SHEET 3 OF 9

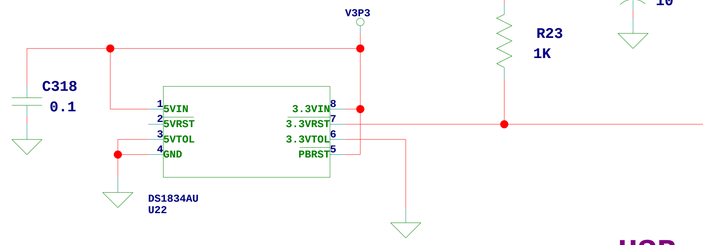
TEST LEDS



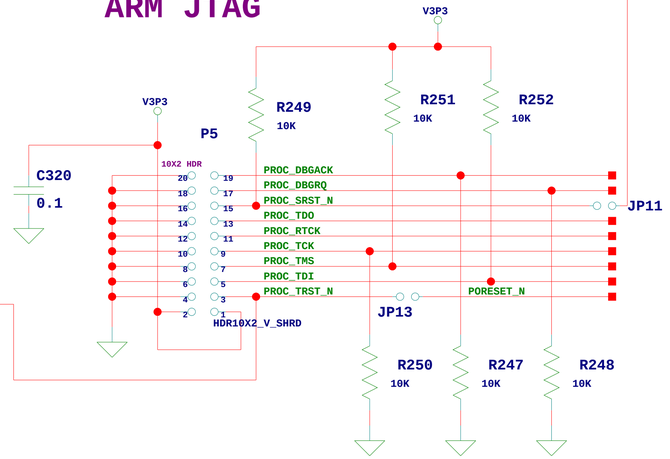
PUSH BUTTON SYSTEM RESET



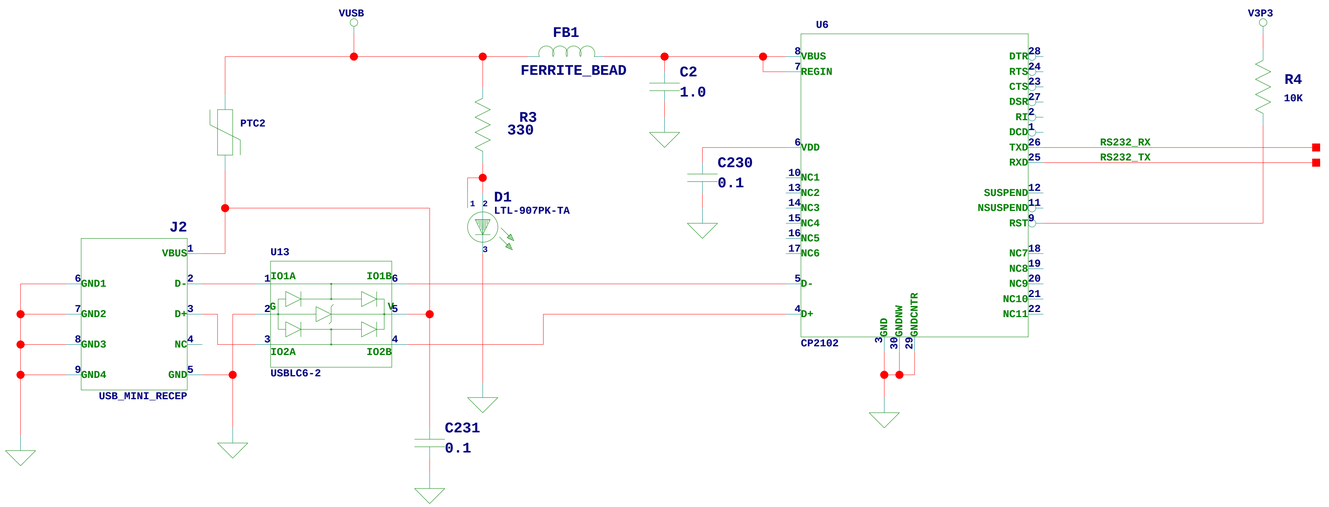
RESET FOR ARM nTRST



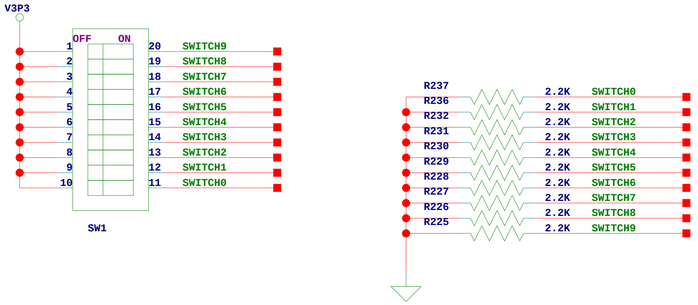
ARM JTAG



USB

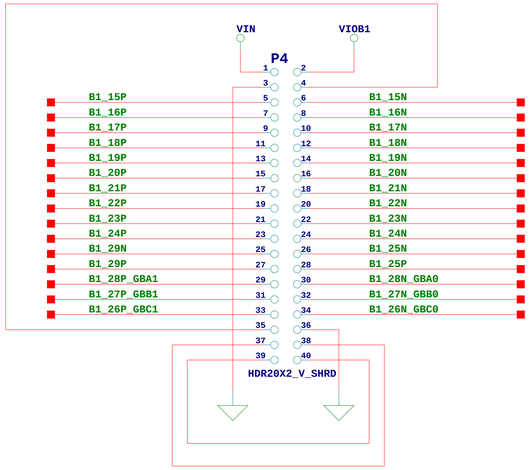


TEST SWITCHES

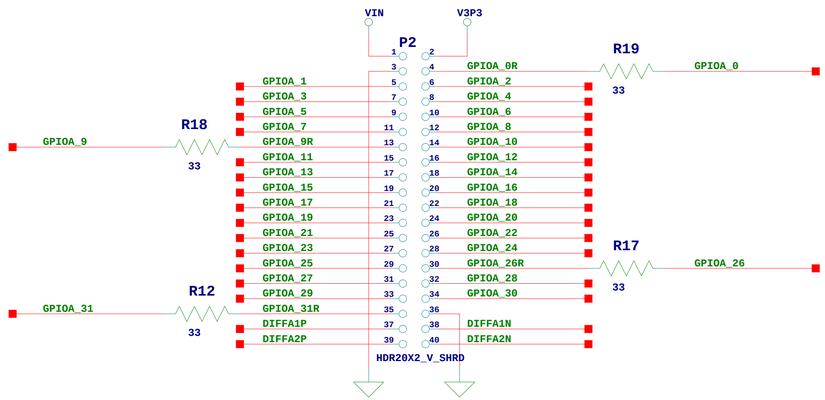


DRAFTER: JIM AVANT	DATE	SoC Solutions	
CHECKER	DATE	TITLE: RESET, TEST, USB	
ENGINEER	DATE		
APPROVAL	DATE	SIZE: D	DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	DATE	SHEET: 4 OF 9

2.5V DIGITAL HEADER

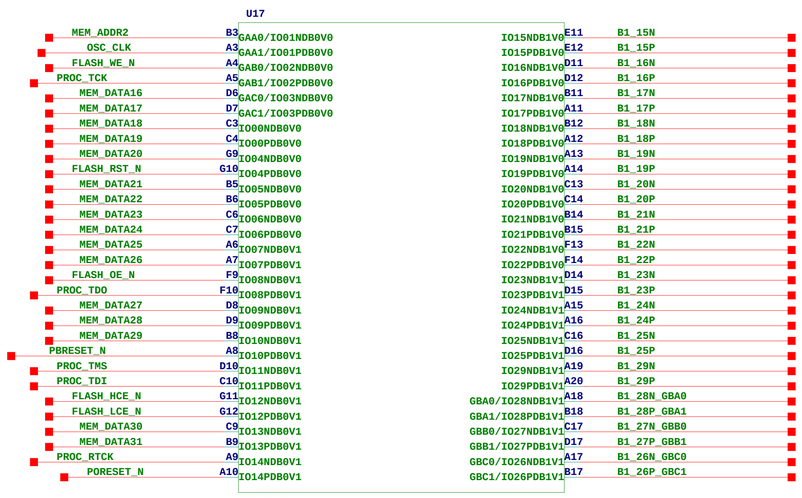


3.3V DIGITAL HEADER

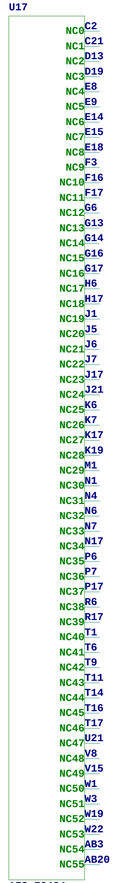


NOTE: PLACE RESISTORS NEAR FPGA.

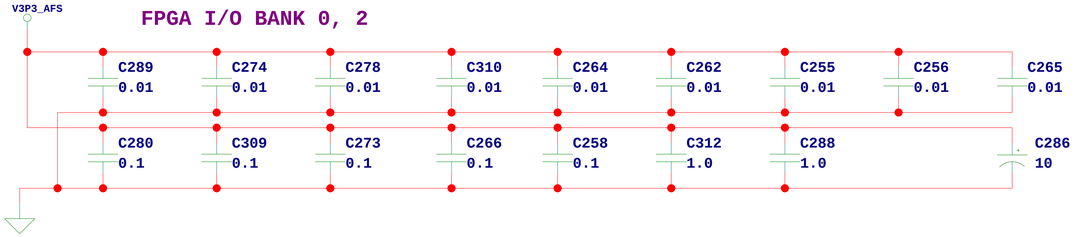
DRAFTER JIM AVANT	DATE	SoC Solutions	
CHECKER	DATE	TITLE	
ENGINEER	DATE	TEST CONN'S	
APPROVAL	DATE	SIZE D	DRAWING NUMBER SOC-M1AFS-S-002
APPROVAL	DATE	DATE	SHEET 5 OF 9



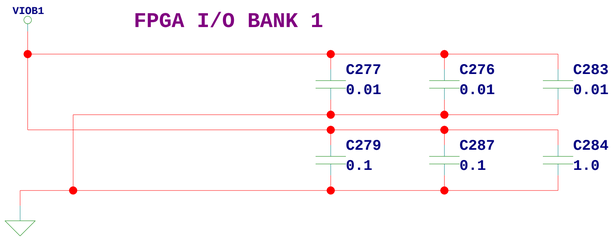
NC



FPGA I/O BANK 0, 2

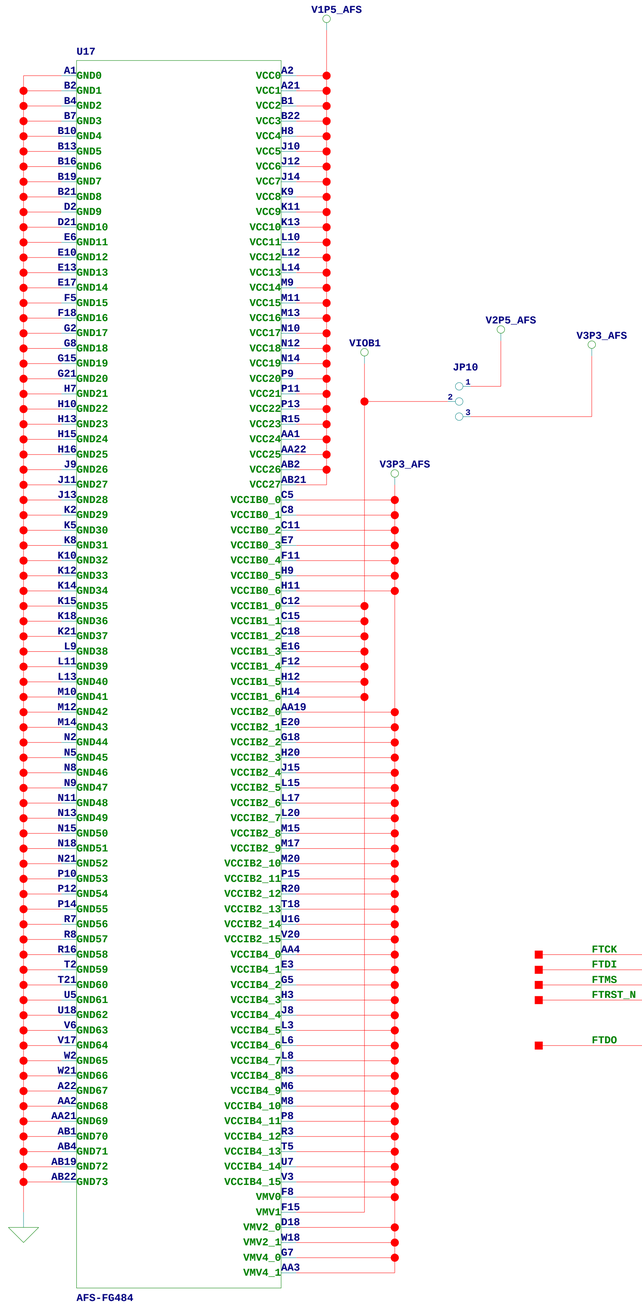


FPGA I/O BANK 1

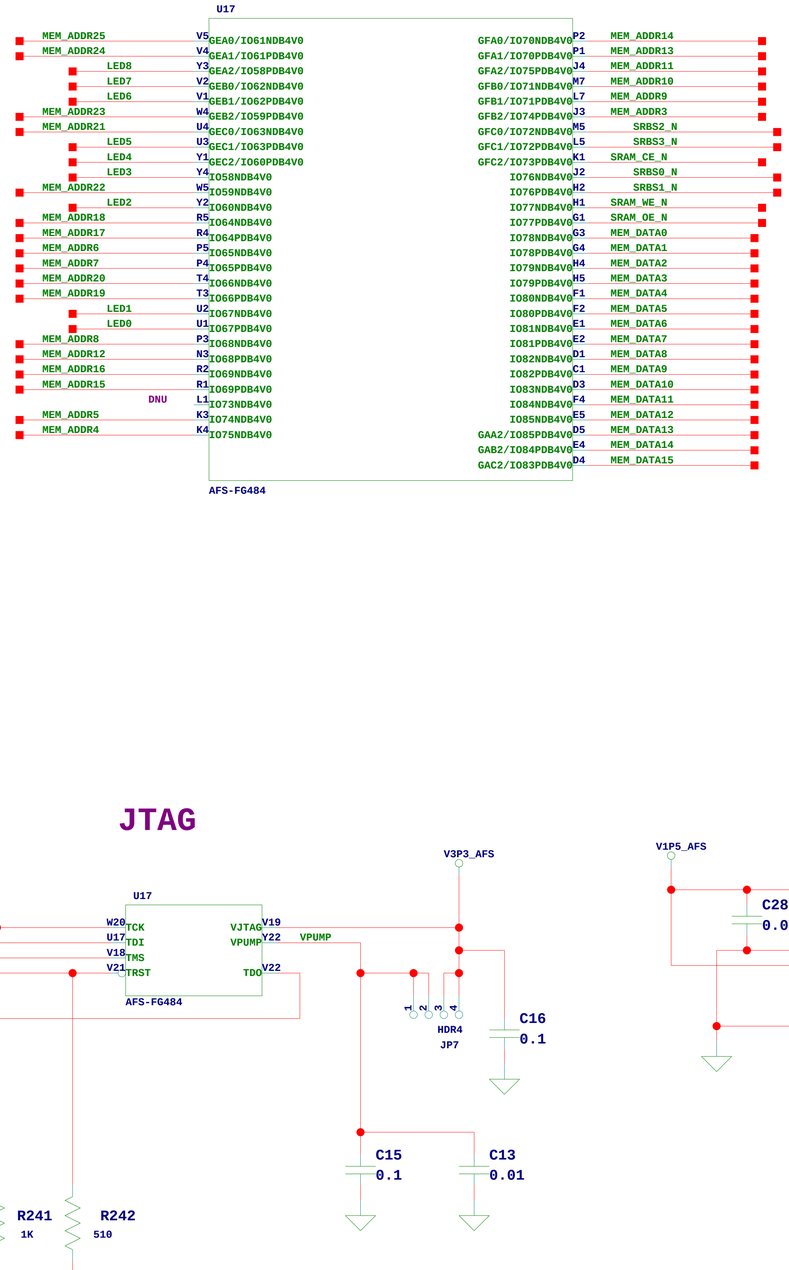


DRAFTER: JIM AVANT	DATE	SoC Solutions	
CHECKER	DATE		
ENGINEER	DATE	TITLE: FPGA	
APPROVAL	DATE	SIZE: D	DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	DATE	SHEET: 6 OF 9

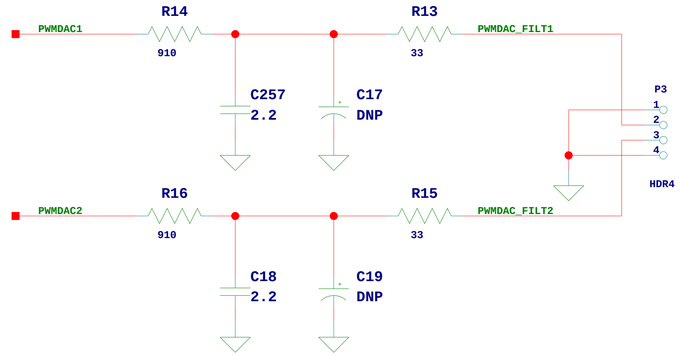
DIGITAL POWER & GND



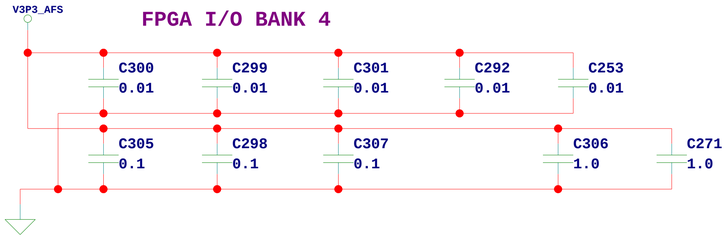
BANK 4



PWM DACS

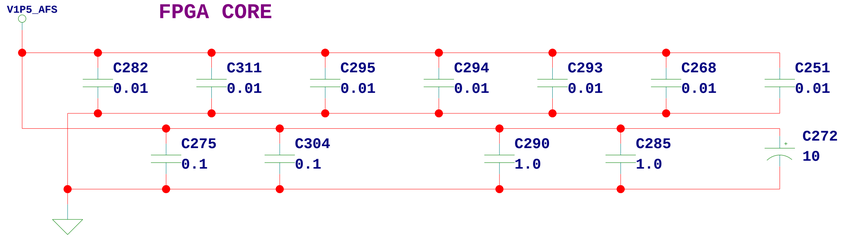


FPGA I/O BANK 4



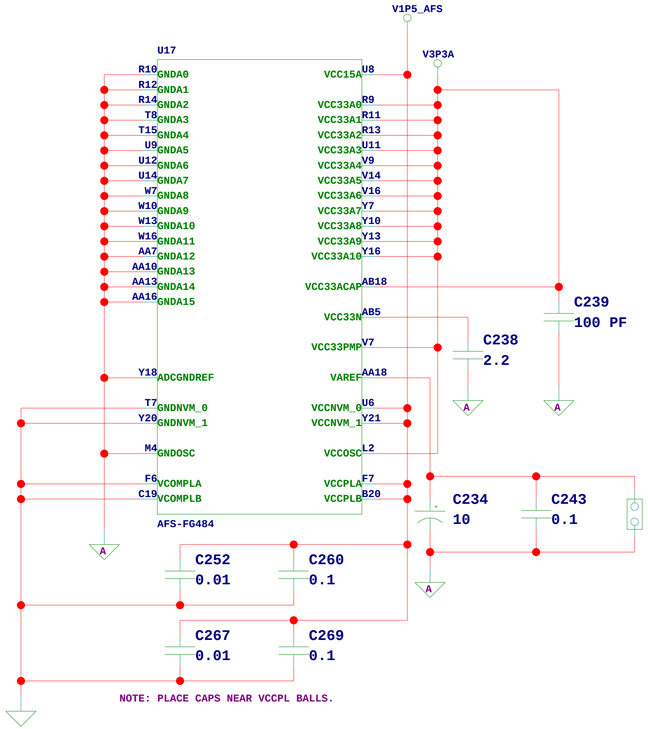
JTAG

FPGA CORE

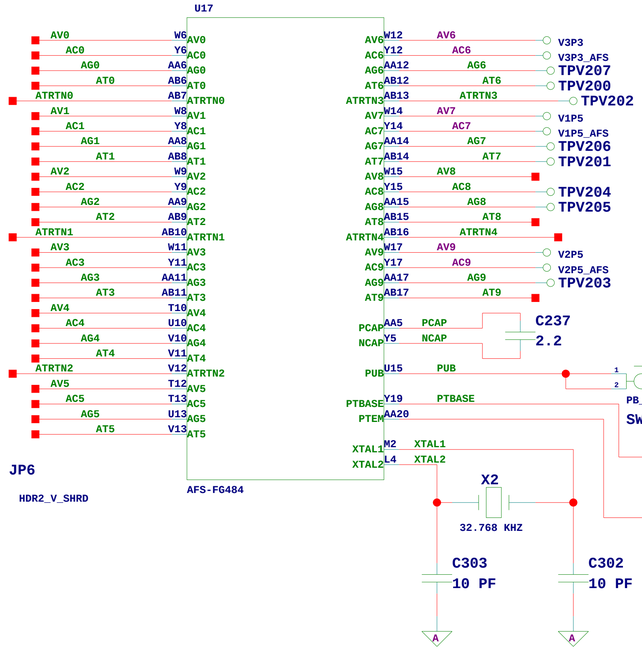


DRAFTER JIM AVANT	DATE	SoC Solutions
CHECKER	DATE	TITLE: FPGA
ENGINEER	DATE	
APPROVAL	DATE	SIZE: D — DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	DATE — SHEET 7 OF 9

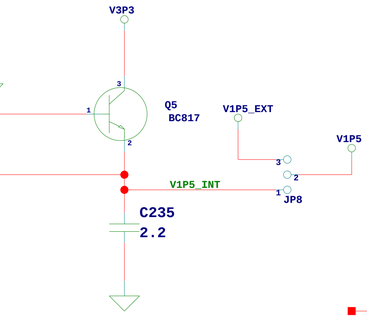
ANALOG POWER & GND



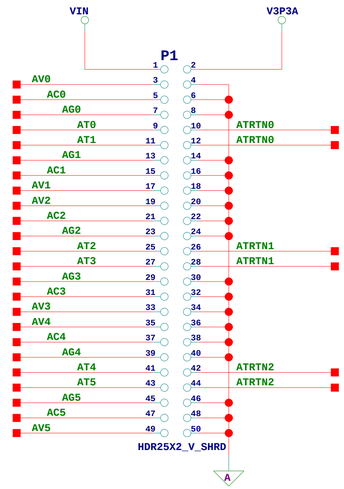
ANALOG

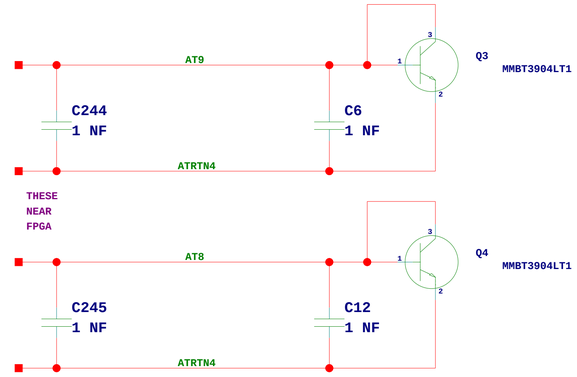


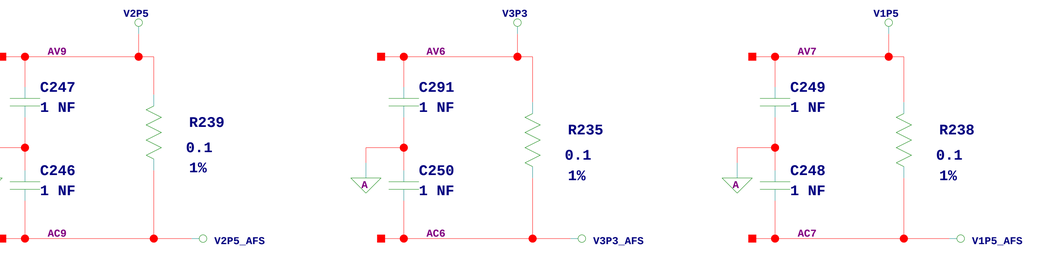
1.5V REG. PASS TRANSISTOR CIRCUIT



ANALOG HEADER

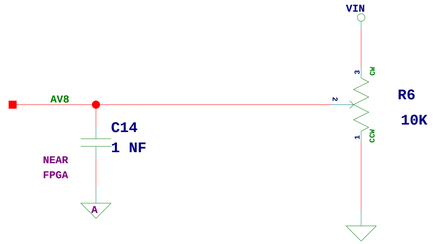






VOLTAGE & CURRENT SENSING

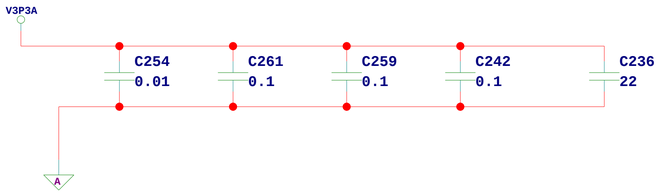
LAYOUT NOTES: PLACE CURRENT SENSE RESISTORS
NEAR VOLTAGE REGULATORS.
PLACE CAPS NEAR FPGA.



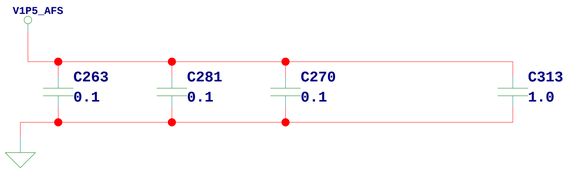
POTENTIOMETER

TEMPERATURE SENSORS

FPGA ANALOG 3.3V



FPGA ANALOG 1.5V



DRAFTER: JIM AVANT	DATE	SoC Solutions
CHECKER	DATE	TITLE: ANALOG
ENGINEER	DATE	
APPROVAL	DATE	SIZE: D — DRAWING NUMBER: SOC-M1AFS-S-002
APPROVAL	DATE	DATE — SHEET: 8 OF 9

USB 2.0

X1
24 MHZ
C212
12 PF
C213
12 PF
V3V3C
U4
TPS3820
RESET
GND
MR
VDD
WDI
VUSB_P
PTC1
TP1
TP2
R2
33
CP29
EZ_RST_N
EZ_SCL
EZ_SDA
CP30
J1
USB_MINI_RECEP
VBUS
GND1
GND2
GND3
GND4
D-
D+
NC
GND
U3
USBLC6-2
IO1A
IO1B
IO2A
IO2B
C202
0.1
U5
CY7C68013A-56
XTALIN
XTALOUT
RESET
WAKEUP
SCL
SDA
IFCLK
CLKOUT
DPLUS
DMINUS
RES
PA0/INT0#
PA1/INT1#
PA2/SLOE
PA3/WU2
PA4/FA0
PA5/FA1
PA6/PEND
PA7/SLCS#
FD0/PB0
FD1/PB1
FD2/PB2
FD3/PB3
FD4/PB4
FD5/PB5
FD6/PB6
FD7/PB7
FD8/PD0
FD9/PD1
FD10/PD2
FD11/PD3
FD12/PD4
FD13/PD5
FD14/PD6
FD15/PD7
RDY0/SLRD
RDY1/SLWR
FLAGA/CTL0
FLAGB/CTL1
FLAGC/CTL2
P3V3FENB
P2V5FENB
JTAGENB_N
TRSTENB_N
VPUMPENB
CP0
CP1
CP2
CP3
CP4
CP5
CP6
CP7
CP15
CP24
CP25
VCC
AGND
R215
10K
R214
10K
V3P3
V2V5F
V3V3F
U9
APA150-TQ100
R216
100
1%
R204
33
D2
LED_RG_TH
PASS/FAIL
FP3_LED1
FP3_LED0
FP3_LED2
R205
33
D3
LED_TH
ACTIVITY
FP3_LED3
R206
33
D4
LED_TH
ON
FP3_LED4
R212
2.2K
R213
2.2K
R207
DNP
R208
DNP
R209
DNP
BREV2
BREV0
BREV1
FTDO
VPUMP_GOOD
VJTAG_GOOD
GLMX2/IO
NPECL2
PPECL2
VPP
VPN
TCK
TDI
TMS
TDO
TRST
RCK
U11
U10
NC7WV125K8X
FTRST_N
FTCK
FTMS
FTDI
R5
33
R200
2.2K
R201
2.2K
U1
CAT24C64
SCL
SDA
A0
A1
A2
WP
VCC
VSS
C200
C204
C211
C205
C206
C208
C209
C210
C207
1.0
C215
C229
C222
C216
C225
C228
C224
C214
C226
C221
C217
C227
C220
C218
C219
C223

DRAFTER	JIM AVANT
CHECKER	
ENGINEER	
APPROVAL	
APPROVAL	
DATE	

SoC Solutions

TITLE: FLASHPRO3

SIZE: D

DRAWING NUMBER: SOC-M1AFS-S-002

DATE

SHEET 7 OF 7