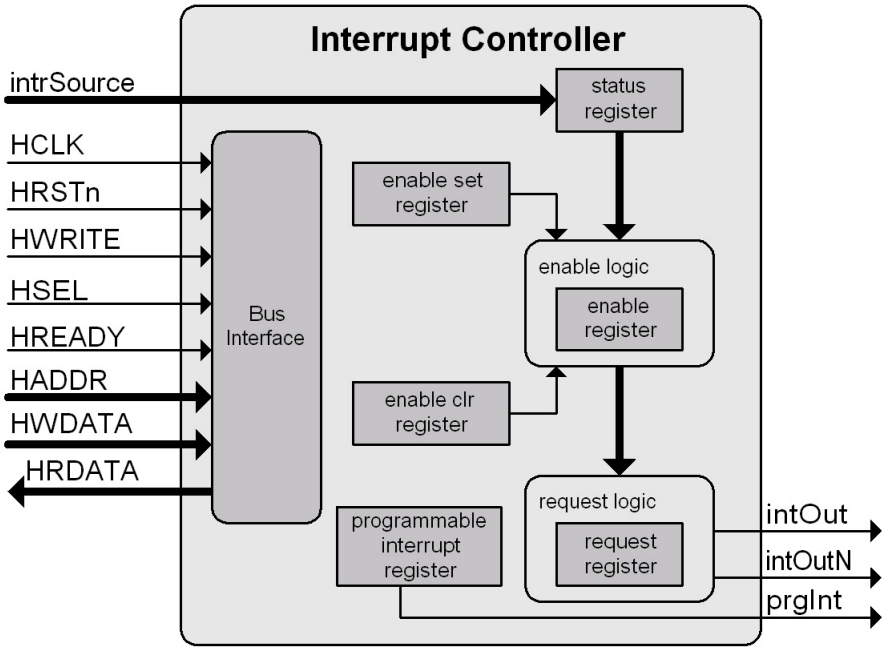
Interrupt Controller
IPC-IntrCtrl-AHB

Features

- Programmable Interrupt Controller
- Scalable (from 1 to 32 interrupts)
- Optional programmable interrupt
- AMBA AHB interface
- Easily cascaded to support more interrupts
- Separate interrupt enable set and clear mechanisms



General Description

The **IPC-IntrCtrl** is a programmable interrupt controller designed to interface to an AMBA AHB bus. The interrupt function is necessary for any embedded microprocessor based SOC that is running a Real Time Operating System (RTOS).

The **IPC-IntrCtrl** Interrupt Controller is fully scalable to support 1 to 32 interrupt sources and provides a programmable interrupt register which can be used to generate an interrupt under software control. The **IPC-IntrCtrl** Interrupt Controller provides separate enable set and enable clear mechanisms to prevent dangerous read-modify-write operations within the critical interrupt system. Active high and active low interrupt request outputs are available to facilitate cascading of multiple interrupt controllers in order to support more than 32 interrupt sources.

IP Package

The **IPC-IntrCtrl** package includes fully tested and verified Verilog source and Verilog testbench. The **IPC-IntrCtrl** can also be delivered as an FPGA Netlist for Xilinx, Altera and Actel FPGAs.

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