Fusion Technology

WP0029 White Paper

June 2015

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Introduction

Microsemi has developed Microsemi Fusion®, the revolutionary technology designed to usher in the era of the Programmable System Chip (PSC). The Microsemi Fusion technology combines analog capability, Flash memory, and FPGA fabric in a monolithic PSC. For the first time, customers will be able to receive a programmable logic solution incorporating analog and Flash memory components.

The Race to the Programmable System Chip

End applications continue to demand increased flexibility, configurability, and performance, along with reduced power demands, board space, and cost. Following increasing pressure for horizontal integration of analog, memory, logic, and soft microcontroller (MCU) implementations in a single chip, analog, microcontroller, and ASIC suppliers are all moving to add configurability to their product lines. In this race to PSC solutions, analog suppliers are adding processors to their solutions. By adding blocks of configurable logic to their products, microcontroller suppliers can service the application space with fewer products and with more functionality. This helps to reduce their product catalogs and overall development costs. ASIC suppliers continue to add new blocks to increase functionality: analog, SRAM, and now Flash memory (Figure 1).

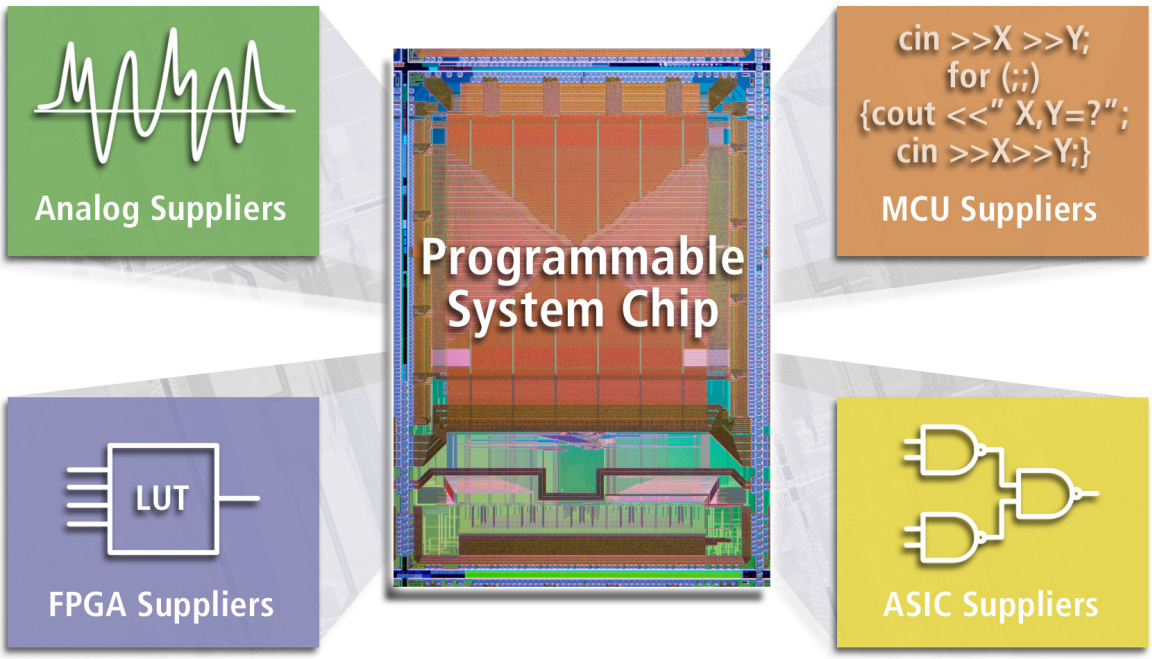

Figure 1: The Race to a Programmable System Chip Solution

As the race to develop PSC solutions heats up, FPGA suppliers have a leg up on the competition because programmable logic has proved the most difficult of these technologies to master. While a large number of FPGA suppliers have entered the market over the years, only a handful of suppliers still compete today due to several barriers to entry that continue to keep the number small. One barrier is a need for hardware that includes the development of efficient, flexible, and high-performance programmable fabric. On the software side, there is very large tool overhead to support design development, verification, validation, and programming.

FPGA suppliers have already overcome these various barriers and actively compete in the market. Integrating analog or Flash memory technologies is an easier and proven path, having already been integrated into both ASIC and MCU technologies. Therefore, FPGA suppliers are better positioned to offer fully integrated solutions: programmable logic, analog, and Flash memory.

Real-World Systems Require Multiple Silicon Technologies

Microsemi Fusion technology presents new capabilities for system development by allowing designers to use the same silicon for a variety of applications and/or quickly adapt to rapidly changing standards. Figure 2 shows a typical real-world application and many of the technologies used in the solution.

As shown in Figure 2, the main processor is supported by both volatile (SRAM/DRAM data memory) and nonvolatile (Flash) memory. Compared with ROMs and PROMs, the programmability and price points of Flash have made it the preferred code storage solution. Also illustrated in Figure 2, the system FPGA/ASIC resides next to the processor to offload the processor and add the customer's Intellectual Property (IP) to the board. Processing is moving from the analog domain to the digital. More systems now must communicate with analog signals, increasing the demand for integrated analog. The real world is analog, and higher levels of integration take digital solutions closer to the analog interface.

Many boards have a host of common housekeeping issues, including power and clock management. Controlling system power has become an important aspect of today's applications, as many components now run from multiple power supplies with specific sequencing requirements. Additionally, these supplies must be monitored for fluctuations that can put volatile resources in undetermined states.

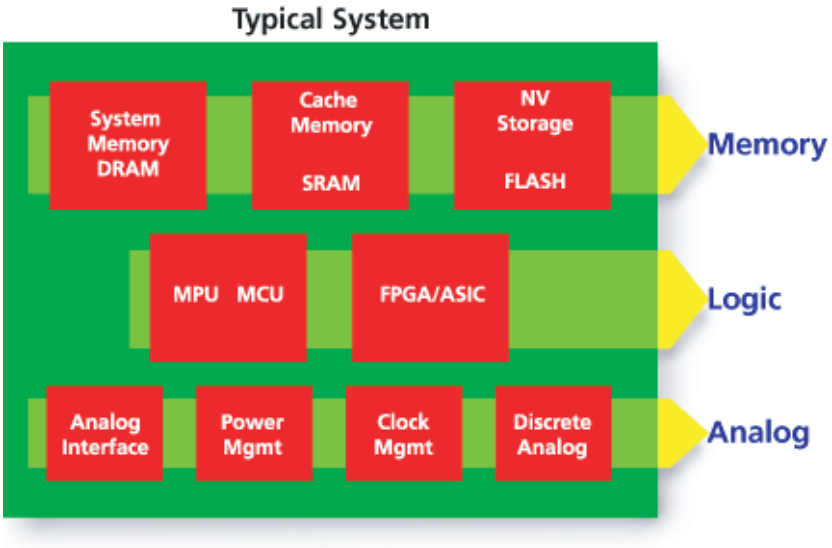

Figure 2: Typical Application

Embedded-Flash Process Supports Programmable System Chip

Of the FPGA technologies in the market today, the Microsemi Flash process is best suited for implementing a PSC. By combining both Flash and high-speed CMOS processes in a single chip, these devices offer the best of both worlds. The high-performance CMOS is used for building RAM resources. These high-performance structures support device operation up to 350 MHz. Additionally, the Microsemi advanced 0.13 µm Flash process incorporates high-voltage transistors and a high-isolation, triple-well process. Both of these are suited for the Flash-based programmable logic and nonvolatile memory structures.

High-voltage transistors support the integration of analog technology in several ways. They aid in noise immunity so that the analog portions of the chip can be better isolated from the digital portions, increasing analog accuracy. Because they support high voltages, Microsemi Flash FPGAs can be connected directly to high-voltage input signals, eliminating the need for external resistor divider networks, reducing component count, and increasing accuracy. By supporting higher internal voltages, the Microsemi advanced Flash process enables high dynamic range on analog circuitry, increasing precision and signal/noise ratio. Microsemi Flash FPGAs also drive high-voltage outputs, eliminating the need for external level shifters and drivers.

The unique triple-well process enables the integration of high-performance analog features with increased noise immunity and better isolation. By increasing the efficiency of analog design, the triple-well process also enables a smaller overall design size, reducing die size and cost.

Microsemi Fusion Integration

Microsemi Fusion technology represents a revolutionary new approach to PSC development and is the first to integrate mixed-signal capabilities with Flash memory and FPGA fabric in a monolithic PSC. Figure 3 on page 6 is illustrative of the type of functionality that can be integrated into a typical device based on this technology. The unprecedented level of integration offered by the Microsemi Fusion technology will enable system designers to remove multiple devices from their systems by integrating the functionality into a Fusion-enabled PSC, greatly simplifying board and system design. An Microsemi Fusion-based device can also offload peripheral tasks from the main processor, reducing microprocessor performance and development requirements. Further, the combination of reduced component count and the live at power-up, single-chip attributes of this technology will enable significant power savings.

As Figure 3 on page 6 illustrates, the Microsemi Fusion technology is also the world's only single-chip configurable processor solution, enabling the ultimate soft-processor implementation platform. A microcontroller core (ARM7® or 8051) can be implemented in logic gates with the on-chip Flash to support code and data space implemented in on-chip RAM. The ability to add peripherals directly to the processor bus further enables single-chip, custom SoC development.

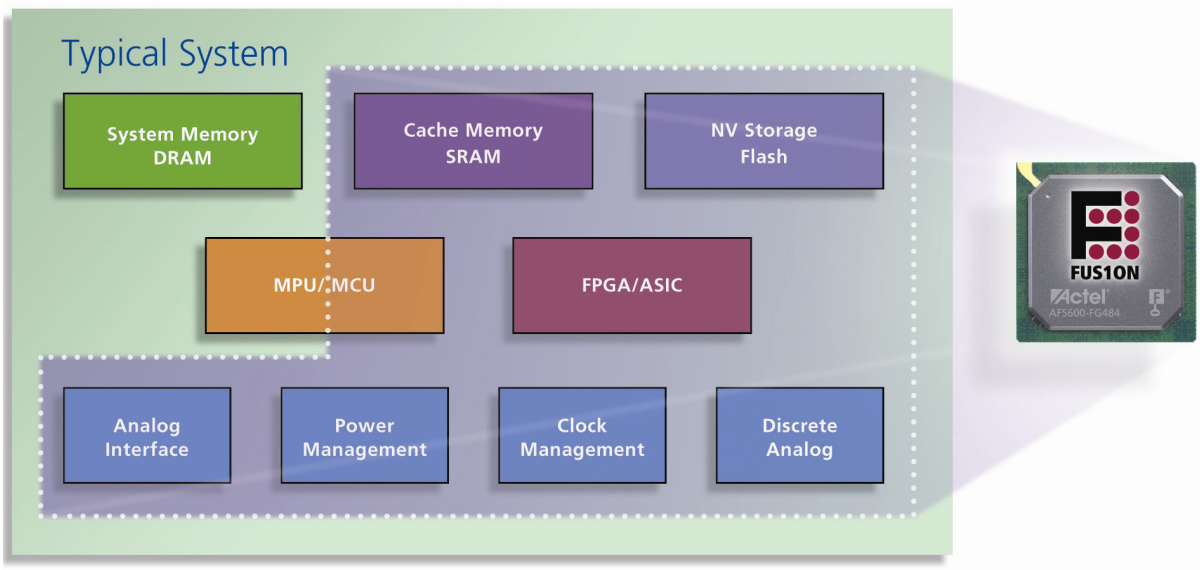

Figure 3: Microsemi Fusion Concept

Microsemi Fusion Technology Stack

To manage this unprecedented level of integration, Microsemi developed the Fusion technology stack (Figure 4 on page 7). This layered model offers a flexible design environment, enabling design at very high and very low levels of abstraction. Fusion Smart peripherals include hard analog IP and hard and/or soft digital IP. Peripherals will communicate across the FPGA fabric via a layer of soft gates – the Fusion Smart backbone. Much more than a common bus interface, this Fusion Smart backbone integrates a micro-sequencer within the FPGA fabric and will configure the individual peripherals and support low-level processing of peripheral data. Fusion applets are application building blocks that can control and/or respond to peripherals and/or other system signals. Applets can be rapidly combined to create large applications. The technology is scalable across devices, families, design types, and user expertise, and supports a well-defined interface for external IP and tool integration.

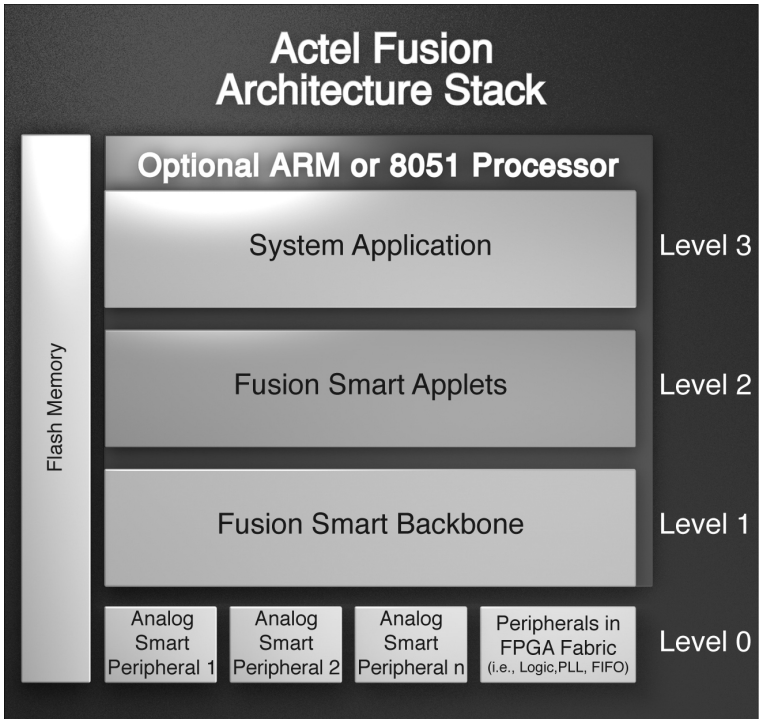

Figure 4: Microsemi Fusion Technology Stack

At the lowest level, Level 0, are Fusion Smart peripherals. These are configurable functional blocks that can be hardwired structures, such as a phase-locked loop (PLL) or analog input channel, or can be implemented in soft gates as a UART or two-wire serial interface. The Smart peripherals are configurable and support a standard interface to facilitate communication and implementation.

Connecting and controlling access to the peripherals is the Fusion Smart backbone, Level 1. The backbone is a soft-gate structure and is scalable to any number of peripherals. The backbone is a bus and much more; it manages peripheral configuration to ensure proper operation. Leveraging the common peripheral interface and a low-level state machine, the backbone efficiently offloads peripheral management from the system design. The backbone can set and clear flags based upon peripheral behavior and define performance criteria. The flexibility of the stack enables a designer to configure the silicon, directly bypassing the backbone if that level of control is desired.

One step up from the backbone is the Fusion applet, Level 2. The applet is an application building block that implements a specific function in FPGA gates. It can react to stimuli and board-level events coming through the backbone, or from other sources, and responds to these stimuli by accessing and manipulating peripherals via the backbone or initiating some other action. An applet controls or responds to the peripheral(s). Applets can be easily imported or exported from the design environment. The applet structure is open and well defined, enabling users to import applets from Microsemi, system developers, third parties, and user groups.

The system application, Level 3, is the larger user application that utilizes one or more applets. Designing at the highest level of abstraction supported by the Microsemi Fusion Technology stack, an entire FPGA system design can be created without any HDL coding. Implemented in FPGA gates, the application can be easily created by importing and configuring multiple applets.

An optional MCU enables a combination of software and HDL-based design methodologies. The MCU can be on-chip or off-chip as system requirements dictate. System portioning is very flexible, allowing the MCU to reside above the applets or to absorb applets, or applets and backbone, if desired.

The Microsemi Fusion technology stack enables a very flexible design environment. Users can engage in design across a continuum of abstraction from very low to very high.

Figure 5 illustrates a physical view of the Microsemi Fusion technology.

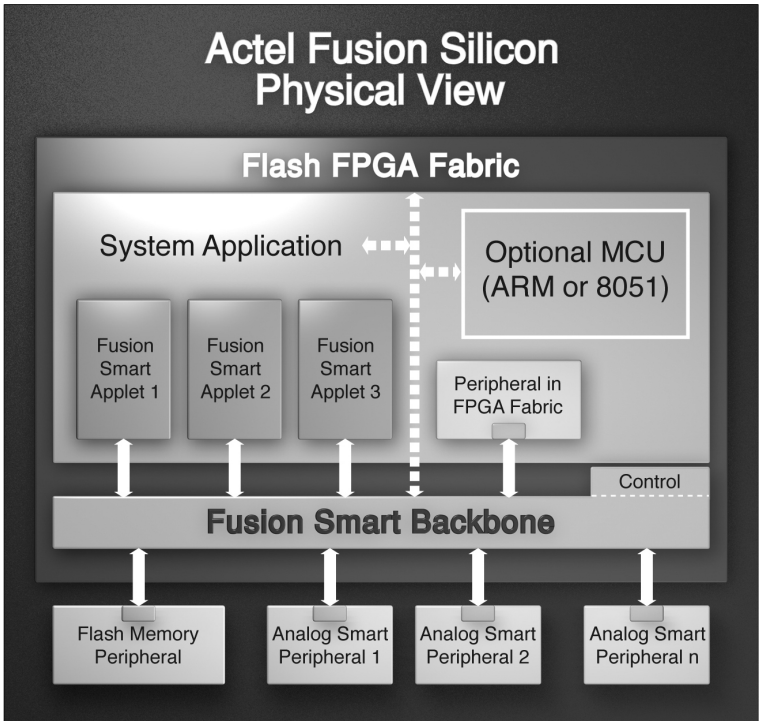

Figure 5: Microsemi Fusion Technology Physical View

Microsemi Fusion Tools

The increased level of integration afforded by PSC solutions adds new complexity and requirements to the development tools. Some of the key required tool features at this level are as follows:

- High level of design productivity
- New methods for rapid application generation
- Hardware/software co-verification
- Bus-based communication
- Device/system modeling and design partitioning
- Innovative debugging capability

To support this new groundbreaking technology, Microsemi is developing a series of major tool innovations to help maximize designer productivity. Implemented as extensions to the popular Microsemi Libero® Integrated Design Environment (IDE), these new tools will allow designers to easily instantiate and configure peripherals within a design, establish links between peripherals, create or import building blocks or reference designs, and perform hardware/software verification. This tool suite will also add a comprehensive hardware/software debug capability as well as a suite of utilities to simplify development of embedded soft ARM® and 8051 processor-based solutions.

System Modeling and Partitioning

The vibrant Microsemi Fusion ecosystem, which is supported by Microsemi and many third-party tool suppliers, offers the flexibility for users to approach system modeling from both hardware and/or software design. Design engineers and architects will have the freedom to partition their application on FPGA logic gates in software executed by either an 8051 or ARM processor or through a judicious combination of both.

Hardware Design Creation

Focusing on ease of use, Microsemi plans to adopt an integrated approach for design generation, foregoing macro generators and application wrappers. Configuration tools offer designers the capability to select Fusion peripherals, and configure and instantiate them into the Fusion backbone. Users can select from a variety of analog services such as temperature, voltage monitoring, and Flash memory services (save, restore, load, etc.) to include them in their application without creating a single line of RTL code. Fusion application generators and applet configuration utilities from external vendors are planned for the Microsemi Fusion tool's framework. These design creation tools will be tightly integrated and delivered through the Libero IDE. This enables users to design their applications from prepackaged application generators and configuration tools, with an unprecedented level of ease, cutting down design iteration time.

Hardware Synthesis and Simulation

The RTL created by users or application generators will seamlessly pass through logic and physical synthesis. Due to the added complexity and unprecedented integration of Microsemi Fusion technology, simulation will play a critical role in design verification. The Microsemi tool solution provides a full suite of simulation models, providing simulation support for all on-chip resources.

Silicon Debug

The unprecedented integration offered by the Microsemi Fusion technology poses significant challenges for design verification through debugging methods. Microsemi solves this issue by offering tools that address debugging needs at multiple levels of application abstraction. Users can embed a logic analyzer into the desired blocks within the application, enabling a real-time probe. It will also be possible to embed these analyzers in the Fusion backbone and monitor the activity of the Fusion peripherals in real time.

Microsemi will also offer additional invasive debug capability, enabling users to interactively access and modify information related to Fusion peripherals, register files, embedded SRAM, and Flash memory.

Software Design and Development Tools

Microsemi supports tools required to create code for MCU units such as the 8051 and ARM7. The tools from Microsemi and other vendors help users build applications in C that are efficient and optimized for MCU targets for Microsemi Fusion devices. A full range of protocol stacks in different application domains enable users to build applications quickly and easily. Users can debug their program code with the help of software debuggers and can also perform instruction set simulation in a co-simulation environment (Figure 6).

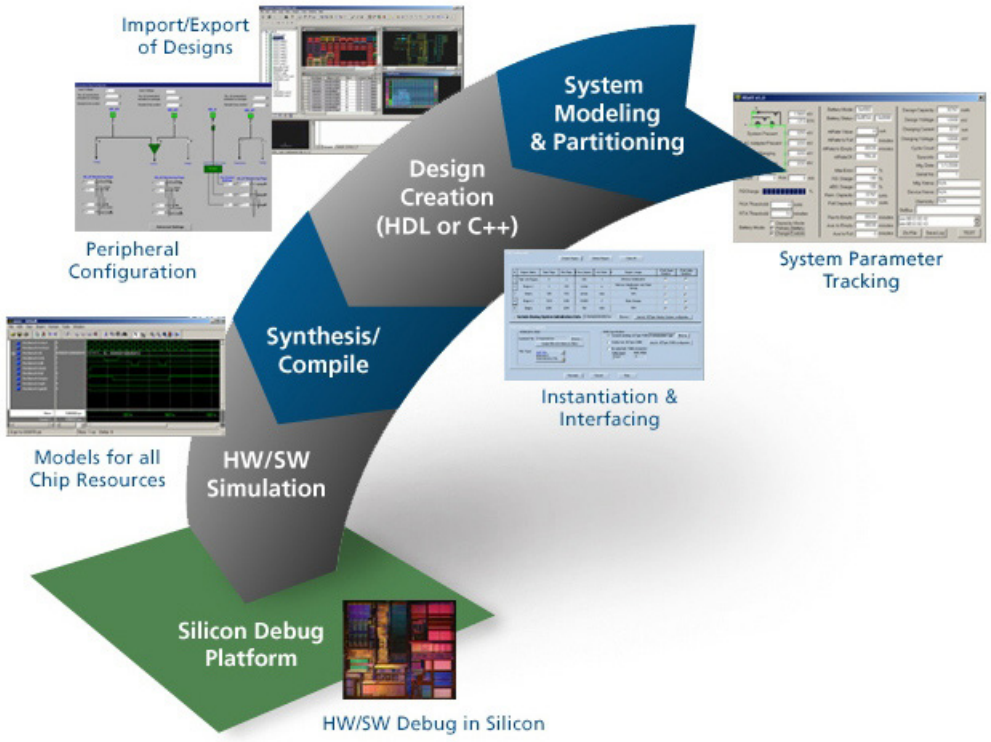

Figure 6: Innovative Microsemi Fusion Tools Solve Complexity

Microsemi Fusion-Enabled Ecosystem

Microsemi Fusion designers will be able to capitalize on a robust support ecosystem populated by many different communities. Microsemi Fusion technology and design development environment enable design at a very high level of abstraction in which users can easily import and export applets. These modular and well-defined applets facilitate IP reuse and sharing. Customers can develop applets to support their own application space. These can be easily mixed, matched, and shared internally. Microsemi third-party tool suppliers, applications solution providers, and design service houses can also create applet generators suited to particular vertical market applications or use models, and then distribute these as part of their solutions, enabling rapid design development. Further, combined with the vibrant ARM ecosystem, Microsemi Fusion designers will have multiple solution providers with whom to work.

Summary

Companies in many technology areas are pursuing the development of a PSC. Due to the barriers inherent in developing efficient, easy-to-use, cost-effective programmable logic, FPGA suppliers are better positioned to develop a PSC solution. Leveraging expertise gained in developing its successful line of Flash FPGAs, Microsemi is in a unique position to integrate analog, Flash, logic, FPGA fabric, and soft MCU into a monolithic PSC. The Microsemi Fusion technology stack provides a flexible and structured means of utilizing this unprecedented level of integration, facilitating IP reuse and rapid design development. Microsemi Fusion tools provide an easy-to-use graphical interface to simplify development. The Microsemi Fusion technology opens exciting new markets for Microsemi by offering functionality and benefits that can be utilized by system applications.

List of Changes

The following table shows important changes made in this document for each revision.

Date	Changes	Page
Revision 2 (June 2015)	Non-technical Updates.	NA
Revision 1 (April 2006)	Initial Release.	NA

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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