SmartTime Tutorial Libero SoC for ProASIC3

NOTE: PDF files are intended to be viewed on the printed page; links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



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The following tutorials explore common SmartTime features with example designs:

- <u>32-Bit Shift Register with Clock Enable</u>
- Design Using Both Clock Edges
- <u>16-Bit Binary Counter</u>
- False Path Constraints
- <u>Cross Clock Domain Analysis</u>

Many actions described in the tutorials can be performed from the menus or in the SmartTime Toolbar. The table below lists all the SmartTime Toolbar actions.

Table 1 · SmartTime Toolbar

lcon	Description
8	Commits the changes
4	Prints the contents of the constraints editor
	Copies data to the clipboard
Ē	Pastes data from the clipboard
	Modifies the selected object from the constraints editor
×	Deletes the selected object from the constraints editor
2	Undoes previous changes
<u>c</u>	Redoes previous changes
\leq	Opens the maximum delay analysis view
\leq	Opens the minimum delay analysis view
(b)	Opens the manage clock domains manager
×	Opens the path set manager
2	Recalculates all
37	Opens the constraints editor
ار	Opens the add clock constraint dialog box
Ťr.	Opens the add generated clock constraint dialog box
* **	Opens the set input delay clock constraint dialog box
*∞	Opens the set output delay clock constraint dialog box



lcon	Description
20.	Opens the set false path constraint dialog box
×	Opens the set maximum delay constraint dialog box
2	Opens the set minimum delay constraint dialog box
N.	Opens the set multicycle constraint dialog box
5 <u>.</u>	Opens the set clock source latency dialog box
1	Opens the set constraint to disable timing arcs dialog box
™	Opens the set clock-to-clock uncertainty constraint dialog box
~~	Checks timing constraints
<u>B</u>	Opens the constraint wizard



32-Bit Shift Register

Set Up Your Libero Project for 32-Bit Shift Register with Clock Enable

This tutorial section describes how to enter a clock constraint for the 32-bit shift register shown in the figure below. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

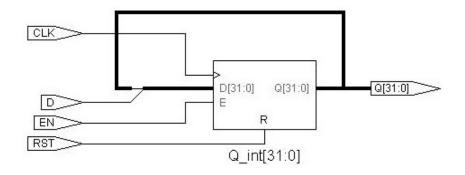


Figure 1 · 32-Bit Shift Registers

Use the links below to go directly to a topic:

- Add a Clock Constraint 32 Bit Example
- Run Place and Route
- <u>Maximum Delay Analysis with Timing Analyzer- 32-Bit Example</u>
- Minimum Delay Analysis with Timing Analyzer 32-Bit Example
- Changing Constraints and Observing Results 32-Bit Example

To set up your project:

- 1. Invoke Libero SoC. From the Project menu, choose New Project.
- 2. Enter Shift32 for your new project name and browse to a folder for your project location. Enter the following values for the project settings (as shown in the figure below):



New Project								
Project								
Enable Block C	Creation							
Name:					1			
Location:	D:					Browse		
Prefered HDL type		g 🔘 VHDL			Je.			
Description:		, ()				÷		
Edit Tool Prof	iles					*		
Device								
Family:	ProASIC3	•						
Die:	A3P060	•						
Package:	100 VQFP	•						
Speed:	-2	•						
Core Voltage (V):	1.5	•						
Operating Condition	ons:							
		Range	9	Best	Typical	Worst	-	
Junction Te	mperature (C)	COM	•	0	25	70		
Core Voltag	ge (V)	СОМ	•	1.575	1.500	1.425	~	
Design Templates								
			Core	•			Version	
						a		
						Show only lat	est version	
				Ш		Show only lat	test version	•

Figure 2 · 32 Bit Shift Register Project Settings

- Family: ProAsic3
- Die: A3P060
- Package: 100 VQFP
- Speed: -2
- Die Voltage: 1.5 V
- All other fields: Use default values
- 3. Click **OK** to continue.
- 4. From the View menu, display the following windows (View > Windows > <window name>):
- Design Flow
- Design Hierarchy
- Files
- Log



- Search Results
- HDL Source Files
- 5. From the **File** menu, choose **Import > HDL Source File**s and import the Verilog file **shift_reg32.v** for the 32-bit Shift Register.

After you import the file, confirm that the imported file appears in the Files window, as shown in the figure below.

Files			
🗀 compone	nt		
D 🗀 constraint			
🖻 🗀 designer			
🔺 🗀 hdl			
🖹 shift_re	eg32.v		
👂 🗀 simulatio			
🗀 smartgen			
🗀 stimulus			
Image: Synthesis			
👂 🗀 tooldata			

Figure 3 · HDL File shift_reg32.v in the Libero SoC File Window

Confirm that the shift_reg32 design appears in the Design Hierarchy window, as shown in the figure below.



esign Hierarchy	
Show: Components 💌	
4 🇰 work	
shift_reg32 (shift_reg32.v)	
< III	4

Figure 4 · shift_reg32 in the Design Hierarchy Window

- 6. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
- 7. Double-click **Compile** in the Design Flow window to run Compile with default settings. A green check mark appears next to Compile when it completes successfully (as shown in the figure below).



Project File Edit View Design Tools H	elp					
□ 🚰 🗖 🗠 🗠 🗢 🙆 📑						
esign Flow	ð×	StartPage 🗗 🗙	Reports 5	×		
shift_reg32 Tool Tool Simulate Simulate Simulate Simulate Simulate Simulate Simulate Create Constraints Simulate Simulate Configure Flash*Freeze Design Hie Desig Stimulus Hie Ca	÷ talog	shift_re Synthesize Synplif shir run_op Compile shift_re shift_re shift_re	2 2322pinrpt 2322pinrpt 4 1000 1000 1000 1000 1000 1000 1000	The The The The The The The The The The	I O Errors ▲ 0 Warning ● 1 Info 'set_compile_info' command succeeded. 'set_compile_info' command succeeded.	
						8
E Messages & Errors A Warning info The 'set_compile_info' command suc The 'set_compile_info' command suc O INFO: No User PDC file(s) was sp The 'compile' command succeeded. The Execute Scribt command succeeded.	ceeded ceeded ceeded ceeded ceeded ceeded ceeded ceeded ceeded ceeded ceeded					A III A

Figure 5 · Synthesis and Compile Complete - 32-Bit Shift Register with Clock Enable

Add a Clock Constraint - 32 Bit Example

To add a clock constraint to your design:

1. In the **Design Flow** window double-click **Create/Edit Timing Constraints** to open the Constraints Editor (as shown in the figure below). Designer opens before the Constraints Editor appears; minimize Designer and continue in the **Constraints Editor**.

SmartTime [shift_reg32 *] - [Cor	straints Editor]	
😳 File Edit View Actions To	ols Window Help	_ & ×
0 🖨 🖬 🖥 🕁 X 🗅 🗅	😹 🐵 末 32 😏 施 施 施 施 施 為 為 急 烈 白 超 塑 🦈 🕒	
Constraints	Synta x Clock Name Clock Source Peri od Frequen cy Dutycyc le (%) First Edg e (ns) Offs (ns) (MHz) (ms) (ms) (ms) (ms) (ms)	File Comments
Generated Clo Input Delay Output Delay Exceptions ≡ Max Delay Multicycle False Path Advanced Clock Source Lat Disable Timing ↓	Click here to add a constraint	
Ready	Temp: COM Volt	: COM Speed: -2

Figure 6 · SmartTime Constraints Editor



2. From the **Actions** menu, choose **Constraints > Clock** to open the Create Clock Constraint Editor, as shown in the figure below.

Create Clock Co	onstraint	x
Clock	CLK	
Clock		
T(zero)		
	Period: ns or Frequency:	MHz
 Offset: 0.000 	ns 50.0000 %	
Comment:		
Help	OK Canc	el

- Figure 7 · Create Clock Constraint Dialog Box
- 3. Set the **Frequency** to **150 MHz** (as shown in the figure below) and leave all other values at the default setting. Click **OK** to continue.

Create Clock Co	onstraint		The second		X
Clock Clock T(zero)	CLK	– Period: 6.667		or Frequency: 150	MHz
Comment:		Duty cycle:			
Help				ОК	Cancel

Figure 8 · Add a 150 MHz Clock Constraint

The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).



Constraints Editor												
□ Constraints □ Requirements □ Clock		Synta x	Clock Name	Clock Source	Peri od (ns)	Frequen cy (MHz)	Dutycyc le (%)	First Edg e	Offs et (ns)	Waveform	File	Comments
Generated Clock		Click he	ere to add a con	straint					2010 - 1813) 7	5. 7.		
Input Delay	1	٣	CLK	CLK	6.667	150.000	50.000	rising	0.000	0 3.33333	GUI	
Exceptions Max Delay Min Delay Multicycle False Path Advanced Clock Source Laten. Disable Timing Clock Uncertainty												

Figure 9 · 150 MHz Clock Constraint in the Constraint Editor

- 5. From the $\ensuremath{\textit{File}}$ menu, choose $\ensuremath{\textit{Commit}}$ to save the constraints.
- $6. \quad \mbox{From the SmartTime File menu, choose Exit to continue.}$

Run Place and Route

You must run Place and Route from Designer. To do so:

1. View Designer, as shown in the figure below.



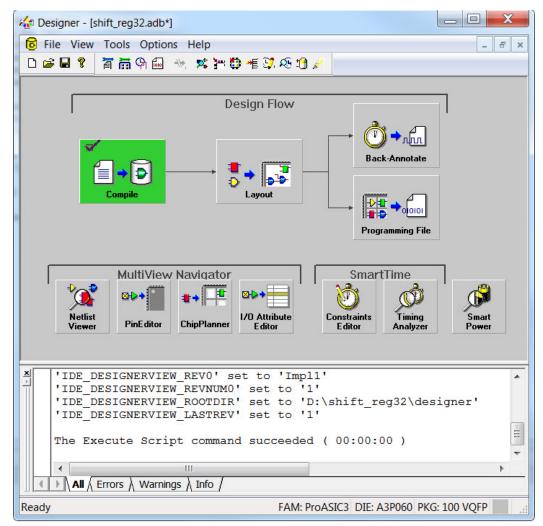


Figure 10 · Compile Complete, Ready for Layout

- 2. Click Layout.
- 3. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings (as shown in the figure below). Click **OK** to continue.



Maximum Delay Analysis with Timing Analyzer- 32-Bit Example

Layout Options	X
✓ Timing-driven	
Power-driven	
Run place	
Place incrementally	
Lock existing placement (Fix)	
Run route	
Route incrementally	
🔲 Use Multiple Passes	
Configure	
Advanced	
Help OK	Cancel

Figure 11 · Layout Options Dialog Box

The Layout button turns green to indicate that Layout has completed successfully.

Maximum Delay Analysis with Timing Analyzer- 32-Bit Example

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays the:

- Maximum operating frequency for the design
- External setup and hold requirements
- Maximum and minimum clock-to-out times. In this example, the maximum clock frequency for CLK is 250 MHz.



I SmartTime [shift_reg32] - [Maximum	Delay Analysi	s View]									x
Arile Edit View Action	s Tools	Window He	lp									e x
6 6 6 6 7 × 9	2 🛛 🔁	≲ 🐵 🌫	2 37 8	in 🐜 🗛 🌠	***	l 📴 🕼 🙀	🗤 💃					
MAX	Data source Using Enh Clock Deta	Period (ns)	Mir Vo Te ed ay Analysis Frequency (MHz)	n Operating Co Itage: mperature: eed Grade: Required Period (ns)	(MHz)	External Setup (ns)	COLOR DISAS STATE	and street state	to Out (ns)			
User Sets	CLK	4.000	250.000	6.667	149.993	4.135	-0.160	6.241	2.296			
Illi Select a set of paths to see here its slack distribution. Stack distribution (ns)	I/O Details Name Input to Ou	Min Dela	ay (ns) Max N/A	Delay (ns)								
Ready									Temp: (COM Volt: (COM Speed: ·	•2 at

Figure 12 · Maximum Delay Analysis - Summary

- 2. Click the + sign next to CLK to expand the display and show the Register to Register, Input to Register and Register to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.

a File Edit View Action a line interview inte		ools Window He		₩a ta ¥a ≫a	221	N Cr 12	ን 🚛 🛷	9				-	5
MAX	From						то *						
이 없 Summary -		Source Pin	Sink	Pin Dela (ns)		Arrival (ns)	Required (ns)	Setup (ns)	Apply Fi Minimum Period (ns)	skew (ns)	Store Filter	Reset Filte	er
Register to Register	1	Q_int[9]/U1:CLK	Q_int[10]/U1	:D 2.33	6 3.915	3.782	7.697	0.428	2.752	-0.012			
External Setup	2	Q_int[2]/U1:CLK	Q_int[3]/U1:E	2.09	5 4.120	3.569	7.689	0.428	2.547	0.024	-		
Clock to Output	3	Q_int[8]/U1:CLK	Q_int[9]/U1:E	2.06	8 4.164	3.521	7.685	0.428	2.503	0.007			
Register to Asynch	4	Q_int[4]/U1:CLK	Q_int[5]/U1:0	2.07	5 4.174	3.525	7.699	0.428	2.493	-0.010			
External Recove	5	Q_int[26]/U1:CLK	Q_int[27]/U1	D 2.06	6 4.183	3.510	7.693	0.428	2.484	-0.010			
Asynchronous to R	6	Q_int[1]/U1:CLK	Q_int[2]/U1:E	2.05	4 4.210	3.503	7.713	0.428	2.457				
□ In to Pin	7	Q_int[16]/U1:CLK	Q_int[17]/U1			3.429	7.703	0.428	2.393				
Input to Output	8	Q_int[3]/U1:CLK	Q_int[4]/U1:0		3 4.286	3.403	7.689	0.428	2.381	0.000			
Ser Sets	9	Q_int[10]/U1:CLK	Q_int[11]/U1			3.394	7.725	0.428	2.336				
	10	Q intf51/U1·CLK	Q intf61/U11) 189	7 4 342	3 357	7 699	0 428	2 325	0.000			
		Details for path From: Q_int[9]/U1 To: Q_int[10]/U1:[
		Pin Nar	ne	Туре	Ne	t Name	Cell	Name	Op Del	ay (ns)	Total (ns)	Fanout Edg	je
100		data required time			1						7.697		
50-		data arrival time							-		3.782		
50-		slack									3.915		
		Data arrival time (algulation									I	
slack distribution (ns)		CLK	aculation							0.000	0.000		-

Figure 13 · SmartTime Register to Register Delay

4. Double-click a path row to open the **Expanded Path Window**. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below).



Maximum Delay Analysis with Timing Analyzer- 32-Bit Example

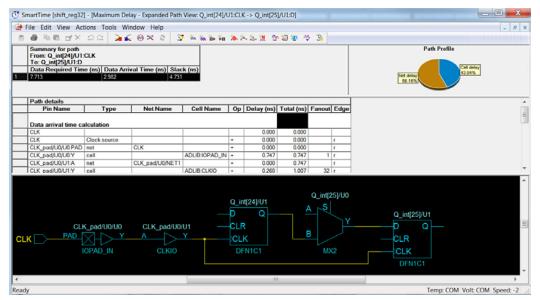


Figure 14 · Register-to-Register Expanded Path View

5. Select **External Setup** to display the Input to Register timing. Select **Path 24**. The Input Arrival time from the EN pin to Q_int[29]/UI:D is 3.162 ns, as shown in the figure below.

File Edit View Actio				n 34a 13+	¥a 10.	AB)	n 197 22	1 in 13	3							ð.
G	From	m •						1	ro •							
MAX												Apply I	Filter	Store Filte	r Reset Filter	1
B Summary B Datasheet CLK		Source Pin	Sink	2277	(ns)	Slack (ns)	(ns)	Required (ns)	(ns)	External Setup (n:						
 Register to Regis 	21	EN	Q_int[3]/U1		3.442	1000	3.442		0.402	2.39						
External Setup	22	EN	Q_int[26]/U		3.293	-	3.293		0.402	2.25						
Clock to Output	23	EN	Q_int[28]/U		3.211		3211		0.402	2.15						
Register to Asynchror	24	EN	Q_int[29]/U Q_int[9]/U1		3 086		3.162		0.402	2.11						
External Recove	26	EN	Q_int[8]/U1		2.939	-	2,939	-	0.402	1.88						
Asynchronous to Reg	27	EN			2.892	-	2.892		0.402	1.84						
S Pin to Pin	~~	120	Q_int[31]/U	0	0.074	-	0.002		0.102	1.01	2					
R User Sets		Details for path From: EN To: Q_int[29]/U1:D														
	_	Pin Nar	10	1	уре	Ne	t Name	Cell	Name	Op D	elay (ns)	Total (ns)	Fanout	Edge		
	-															
	_	data required time		-		-		_				N/C				
		data arrival time						_		• · ·		3.162				
	-	slack				-		1				N/C	1	-		
	_	Data arrival time o	alculation								1.000					
		EN									0.000	0.000		1		
	-	EN_pad/U0/U0:PAD	6	net		EN		10101		•	0.000	0.000		1		
		EN_pad/U0/U0:Y		cell		C 11			OPAD_IN		0.747	0.747		r		
• III •	-	EN_pad/U0/U1:YIN EN_pad/U0/U1:Y		net cell		EN_pa	d/U0/NET	ADUB!	0.01.10	•	0.000	0.747		r		

Figure 15 · SmartTime - Input to Register Path Analysis

6. Select **Clock to Output** to display the register to output timing. Select Path 14. The maximum clock to output time from CLK to Q[27] is 5.790 ns, as shown in the figure below.



	File Edit View Action												
(3	5 8 6 7 ×.	<u>0 0</u>	≥≤∞≍∂	😏 🕅 💏	8+ ¥0 🔉	~ & ;	M Gr ¥	3 💯 🦈	Э,				
		From	n *				То	*					_
6	MAX												
	P . 0									Apply Filter	Store Fil	ter Re	set
	୍ଡିରା Summary ୁକ୍ତି Datasheet କଙ୍କ ୧୦୦୦ CLK		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Clock Out (to ns)			
	Register to Regi:	9		Q[16]	4.358		5.822	20 0001 0		822			
	External Setup	10		Q[8]	4.364		5.817			817			
	Clock to Output	11		Q[24]	4.356		5.814			814			
	Register to Asynch	12		Q[25]	4.335		5.809			809			
	External Recove	13		Q[13]	4.314		5.800			800			
	Asynchronous to R	14 15		Q[27] Q[2]	4.336		5.790 5.788			790 788			
	😑 🏹 Pin to Pin	16		Q[2] Q[29]	4.314		5.763			763			
	Input to Output	17		Q[14]	4.255		5.741			741			
	S User Sets	18		Q[4]	4.291		5.741			741			
		19		Q[20]	4.280		5.739			739			
		20		Q[5]	4.263		5.723	3	5.	723			
•	4 11	21		Q[15]	4.252		5.720			720			
		22		Q[6]	4.259		5.719			719			
		23	Q_int[11]/U1:CLK	Q[11]	4.226		5.712		5.	712			
			Details for path From: Q_int[27]/U1:C To: Q[27]	LK									
2			Pin Name	Туре	Net Na	ne	Cel	Name	Ор	Delay (ns)		Fanout	E
# of paths	This set has no slack for any of its paths.		CLK	Clock source					+	0.000	0.000		r.
jo #	for any or to paths.		CLK_pad/U0/U0:PAD	net	CLK				+	0.000	0.000		r.
1			CLK_pad/U0/U0:Y	cell			ADLIB:10	PAD_IN	+	0.747	0.747	1	r
			CLK_pad/U0/U1:A	net	CLK_pad/U0/	NET1			+	0.000	0.747		r
			CLK_pad/U0/U1:Y	cell			ADLIB:CL	.KIO	+	0.260	1.007	32	_
			Q_int[27]/U1:CLK	net	CLK_c		ADUD ST	NIOI	+	0.447	1.454		r
			Q_int[27]/U1:Q	cell	0.1.1.077		ADLIB:DF	NICI	+	0.550	2.004		1
	slack distribution (ns)		Q_pad[27]/U0/U1:D	net	Q_int_c[27]		ADUD 10		+	0.935	2.939		1
			Q_pad[27]/U0/U1:DOU	cell	1		ADLIB:10	TRI_OB_EB	+	0.492	3.431	1	1

Figure 17 · SmartTime Clock to Output Path Analysis

Minimum Delay Analysis with Timing Analyzer - 32-Bit Example

The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

To perform Minimum Delay Analysis:

1. From the SmartTime **Tools** menu, choose **Timing Analyzer > Minimum Delay Analysis**. The Minimum Delay Analysis window appears, as shown in the figure below.

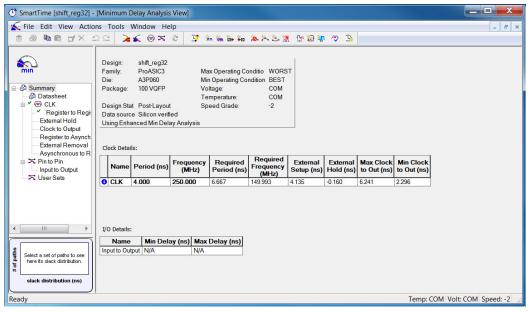


Figure 18 · SmartTime Minimum Delay Analysis View- Summary

2. Click the + next to CLK to expand the list and display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Reset path sets.



- 3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.
- 4. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.

File Edit View Actio	ons To	ools Window Help	l)									-	5
. 		≥≤ ∞ ≍ «		ä+ ¥a .⊗. :	× 25 %	N (r 12	👷 🛷	Э.					
\sim	From	*				То	*						
min													
								Annh	Filter	Store Fi	lter	Reset Filter	٦
Summary					01.1					- Store II		NGOCCT IIICO	-
- 🖓 Datasheet		Source Pin	Sink Pin		Slack (ns)	Arrival (ns)	Required (ns)	(ns)	SKew (ns)				
🖃 🖌 🐵 CLK	1	Q_int[5]/U1:CLK	Q_int[5]/U1:D	0.656	0.637	1.340		0.000	-0.019				
Register to Regi:	2	Q int[8]/U1:CLK	Q int[8]/U1:D	0.656	0.638	1.337	0.699	0.000	-0.018				
External Hold	3	Q_int[4]/U1:CLK	Q_int[4]/U1:D	0.656	0.638	1.335	0.697	0.000	-0.018				
Clock to Output	4	Q_int[3]/U1:CLK	Q_int[3]/U1:D	0.656	0.638	1.335	0.697	0.000	-0.018				
Register to Asynch External Removal	5	Q_int[1]/U1:CLK	Q_int[1]/U1:D	0.656	0.638	1.335	0.697	0.000	-0.018				
Asynchronous to R	6	Q_int[10]/U1:CLK	Q_int[10]/U1:D	0.656	0.638	1.340	0.702	0.000	-0.018				
Pin to Pin	7	Q_int[31]/U1:CLK	Q_int[31]/U1:D	0.656	0.638	1.334	0.696	0.000	-0.018				
Input to Output	8	Q_int[16]/U1:CLK	Q_int[16]/U1:D	0.667	0.647	1.353	0.706	0.000	-0.020				
S User Sets	9	Q_int[26]/U1:CLK	Q_int[26]/U1:D	0.666	0.649	1.342	0.693	0.000	-0.017				
	10	Q_int[9]/U1:CLK	Q_int[9]/U1:D	0.666	0.649	1.343	0.694	0.000	-0.017				
	11	Q_int[2]/U1:CLK	Q_int[2]/U1:D	0.676	0.655	1.368	0.713	0.000	-0.021				
	12	Q_int[19]/U1:CLK	Q_int[19]/U1:D	0.683	0.663	1.369	0.706	0.000	-0.020				
	1.3		I Q INTEL7//UTID	0.683	0 hh.3	1.369	0.706	0 000	-0.020				_
		Details for path From: Q int[5]/U1:0	1 K										
4 III		To: Q_int[5]/U1:D											
		Pin Name	Туре	Net Nan	ne	Cell Na	me Or	Dela	ay (ns)	Total (ns)	Fanout	Edge	
60													
50-													
40-		data arrival time								1.340			
30-		data required time					-			0.703			
		slack								0.637			
20-													
10		Data arrival time ca	lculation										
		CLK							0.000	0.000			
0.5 1 1.5		CLK	Clock source				+		0.000	0.000		r	
slack distribution (ns)		CLK pad/U0/U0:PAD	net	CLK		-	+		0.000	0.000		r	

Figure 19 · SmartTime Minimum Delay Analysis

Changing Constraints and Observing Results - 32-Bit Example

You can use SmartTime to adjust constraints and view the results in your design. To do so:

1. Open the SmartTime Constraints Editor. From the **Tools** menu, choose **Constraints Editor > Primary**. The Constraints Editor displays the clock constraint at 150 MHz that you entered earlier, as shown in the figure below.

Constraints — Requirements — * Clock	Synta x	Clock Name	Clock Source	Peri od (ns)	Frequen cy (MHz)	Dutycyc le (%)	First Edg e	Offs et (ns)	Waveform	File	Commer
Generated Clock	Click he	ere to add a con	straint					onto intera c			
Input Delay	1 🚩	CLK	CLK	6.667	150.000	50.000	rising	0.000	0 3.33333	GUI	
Max Delay Min Delay Multicycle False Path Advanced Clock Source Laten. Disable Timing Clock Uncertainty											

Figure 20 · Clock Constraint Set to 150 MHz



- 2. Double-click the first row to open the Edit Clock Constraint dialog box. Change the clock constraint from **150 MHz** to **600 MHz** and click **OK** to continue.
- 3. From the **View** menu, choose **Recalculate All** to recalculate the delays using your new clock constraint.
- 4. From the **Tools** menu, choose **Timing Analyzer > Maximum Delay Analysis View** to view the max delay analysis.
- 5. Expand the **CLK** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the negative slack (timing violations) are shown in red (as shown in the figure below).

File Edit View Actio	ons To	ools Window Hel	D													5
		≥≼ ⊚≍		w. w. v			N (br 12)	۰n m	Э							-
		× ••••	C 4 10	L JAA 1241+ 1		~~ ^	N 147-480	₩	-							_
\sim	From	*					Т	. *								
A	FIOII															
MAX																_
P. o.										Арр	ly Filter		Store Filter	Reset	Filter	1
해 Summary - 해 Datasheet - [×] ሙ CLK		Source Pin	Sink	Pin	Delay (ns)	Slack (ns)	Arrival I (ns)	Required (ns)	Setup (ns)	Minim Perio (ns	d S	kew ns)				
Register to Regi:	1	Q_int[9]/U1:CLK	Q_int[10]/U1	:D	2.242	-1.000	3.702	2.702	0.428			0.003				
External Setup		Q_int[2]/U1:CLK	Q_int[3]/U1:	D	2.209	-0.971	3.667	2.696	0.428	2	.638 (0.001				
Clock to Output	3	Q_int[4]/U1:CLK	Q_int[5]/U1:	D	2.159	-0.920	3.629	2.709	0.428	2	.587 (0.000				
Register to Asynch	4	Q_int[26]/U1:CLK	Q_int[27]/U1		1.985	-0.749	3.445	2.696	0.428			0.003				
External Recove Asynchronous to R	5	Q_int[1]/U1:CLK	Q_int[2]/U1:		1.968	-0.731	3.428	2.697	0.428			0.002				
- St. Pin to Pin	6	Q_int[30]/U1:CLK	Q_int[31]/U1		1.968	-0.729	3.412	2.683	0.428			0.000				
Input to Output	7	Q_int[24]/U1:CLK	Q_int[25]/U1		1.947	-0.708	3.410	2.702	0.428			0.000				
S User Sets		Q_int[8]/U1:CLK	Q_int[9]/U1:		1.917	-0.678	3.377	2.699	0.428			0.000				
Pi User Jers		Q_int[29]/U1:CLK	Q_int[30]/U1		1.911	-0.677	3.360	2.683	0.428			0.005				
	10	Q_intf101/U1·CLK	Q intf111/U1	D	1 889	-0.649	3 352	2 703	0 428		316 -0	001				Ļ
		Details for path From: Q_int[9]/U1: To: Q_int[10]/U1:D														
		Pin Nam	ie	Ту	ре	Ne	t Name	Cell	Name	Ор	Delay (ns)	Total (ns)	Fanout	Edge]
4 111		CLK										000	0.000			
		CLK		Clock sou	urce					+		000	0.000		r	
00		CLK_pad/U0/U0:PAD		net		CLK				+	0.	000	0.000		r	-
		CLK_pad/U0/U0:Y		cell					OPAD_IN	+		747	0.747	1	r	-
50 -		CLK_pad/U0/U1:A		net		CLK_pa	ad/U0/NET			+		000	0.747		r	-
0		CLK_pad/U0/U1:Y		cell				ADLIB:C	LKIO	+	0.:	260	1.007	32	r	
-1.5 -1 -0.5 0		Q_int[9]/U1:CLK		net		CLK_c				+		453	1.460		r	1
slack distribution (ns)		Q int[9]/U1:Q		cell				ADLIB:C	CALLO 1	+	0	550	2.010	3		11

Figure 21 · Maximum Delay Analysis After Setting Clock Constraint to 600 MHz

- 6. Close SmartTime. Click **No** when prompted to commit your unsaved edits.
- 7. Close Designer. Click Yes if asked to save changes to shift_reg32adb.



Design Using Both Clock Edges

This example analyzes SmartTime reports that include both rising and falling edges of a clock in the same design. The design (as shown in the figure below) consists of a 16-bit serial-in parallel-out (SIPO) shift register, a control block and a 16-bit output register. The control block enables the output register after 16 bits of data have been shifted in. The shift register and the control block are clocked on the rising edge of the clock. The output register is clocked on the falling edge of the clock.

You will import the EDIF netlist (shifter.edn) and enter a clock constraint of 100 MHz. After routing the design you will analyze the timing to determine the maximum operating frequency and export a timing report.

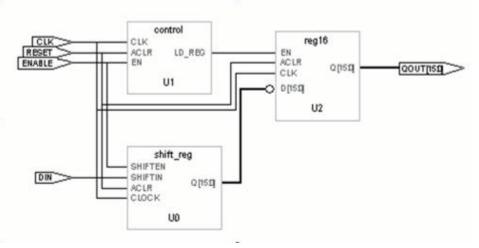


Figure 22 · Example Design that Uses Both Clock Edges

Set Up Your Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **Shifter** and set the project location according to your preferences. Enter the following values for your new project:
- Family: ProASIC3
- Die: A3P060
- Package: 100 VQFP
- Speed: -2
- Die Voltage: 1.5 V

Import the EDIF Netlist - Design Uses Both Clock Edges

You must import the shifter.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import the EDN file:

- 1. From the **File** menu, choose **Import > Others**.
- 2. Choose EDIF Netlists from the file type dropdown list in the Import Files dialog box.
- 3. Browse to the location of the shifter.edn file and select it. Click Open to import the file.
- 4. Verify that the file appears in your project, as shown in the figure below.



🕒 🝰 📊 🖾 🍋 🧇 🕻 Design Hierarchy	a x	StartPage	shifter.edn 🔯	Reports		
Show: Components work Shifter (shifter.edn) Components Design Hie Desig Log) Files	1 (edif al 2 (edif 3 (edif) 4 (kayw 5 (statu 6 (wr: 7 (statu 6 (wr: 7 (statu 9 (i) 10) 11) 12 (libru 13 (edi 14 (tec 15 (cei 16 (cei 16 (cei 16 (cei 17 (cei 16 (cei 17 (Version 2 0 0) Level 0) ordMap (keyword) is itten author "Synplic orogram "Synplic orogram "Synplic ifLevel 0) chnology (number 1) BUFF (cellTy property dont_to property dont_to (view prim (view (interface	Level 0)) # 22 16 12 44) ity, Inc.") Fy" (version "7. CDefinition)) >= GENERIC) puch (string "fa integer 1))	7.0, Build 060R"))	•
Search Results						8)
•					Die: A3P060 Pkg: 100 VQ	

Figure 23 · shifter.edn in the Design Hierarchy

Add a Clock Constraint - Design Uses Both Clock Edges

To add a clock constraint to your example design:

- 1. In the Design Flow window, right-click **Create/Edit Timing Constraint** and choose **Open Interactively**. Designer opens and runs Compile with the default settings. After Compile is complete the Compile button in Designer turns green and the SmartTime Constraints Editor opens.
- 2. Click the Clock Constraint tab and enter a constraint for the clock source (CLK) of 100 MHz at a 50% duty cycle.



Run Place and Route for a Design that Uses Both Clock Edges

Create Clock (Constraint					X
Clock	CLK	-				
T(zero)						
	 	Period: 10.000	ns	or Frequency:	100	MHz
 Offset 0.000 		Duty cycle:				
Comment:		5				
	<u>_</u>					
Help				ОК	Cance	el

Figure 24 · Add 100 MHz Clock Constraint

The new constraint appears in the Constraints Editor, as shown in the figure below.

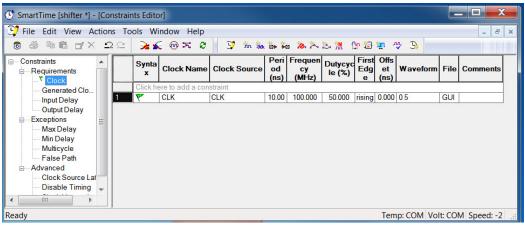


Figure 25 · 100 MHz Clock Constraint in the Design shifter

- 3. From the SmartTime File menu, choose Commit to save the constraints.
- 4. From the SmartTime File menu, choose Exit to proceed to Place and Route step.

Run Place and Route for a Design that Uses Both Clock Edges

To run Layout on the design 'shifter':

- 1. In Designer, click Layout.
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.



Maximum Delay Analysis with Timing Analyzer - Design Using Both Clock Edges

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

C SmartTime [shifter] - [Max	imum De	alay Analysis	View]						(II)		×
File Edit View Action		s Window ≽ 🖌 🎯 🤊	CONTRACTOR NO.	70x 30x 5+ +	a 🔉 🕹 🕹	M. Gr 10	m 19 J	8			5 ×
Summary A Datasheet CK CK Register to R Edemail Setup Clock to Outp Register to Asy Cotton Outp	Data so	Stat Post-Lay urce Silicon v nhanced Min E	P	Max Operating Min Operating Voltage: Temperature: Speed Grade:	Condition BE CO CO	ST M					- Hi
	Name	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Max Clock to Out (ns)			
	CLK	6.690	149.477	10.000	100.000	3.334	0.206	5.915	2.184		
Select a set of paths to see here its slack distribution slack distribution (na)	I/O Deta)elay (ns) M	lax Delay (ns)	1						-
Ready		1		-10-1				Temp: C	OM Volt: CON	A Speed: -	2

Figure 26 · Maximum Delay Analysis for Design shifter

The Summary in the Maximum Delay Analysis window indicates the maximum operating frequency for this design is 149.477 MHz.

- 2. Click the + sign next to CLK to expand the display and show the Register to Register, Input to Register and Register to Output path sets.
- 3. Select **Register to Register** to display the register-to-register paths. The window displays a list of register-to-register paths and detailed timing analysis for the selected path (as shown in the figure below). Note that all the slack values are positive, indicating that there are no setup time violations.
- 4. Click to select row 1 and study the timing analysis (resize the Maximum Delay Analysis window as required). The path is from the control block (U1) to the output register (U2). Note that SmartTime uses 5 ns in the data required calculation (as shown in the figure below). This is because the source flip flop uses the rising edge of the clock and the destination flip-flop used the falling edge of the clock.



🎽 File Edit View Acti			State of the state	n de de 40 .00	22		1. T	3					6 1
	Fro	n *					To *						
									A	ply Filter	Store	Filter Reset Filb	
୍ତମ Summary - ଶ୍ରୀ Datasheet ∋ [⊀] ଡ଼ CLK =		Source Pin	Sink	Pin Dela	y Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)			
 Register to R 	1	U1/count[2]:CLK	U2/Q[9]:E	2.60	1 1.655	4.142	5.797	0.454	6.690	0.230			
External Setup	2	U1/count[0]:CLK	U2/Q[6]:E	2.60	4 1.680	4.106	5.786	0.454	6.640	0.262			
Clock to Outp	3	U1/count[1]:CLK	U2/Q[6] E	2.6	7 1.688	4.098	5.786	0.454	6.624	0.241	l'		
Register to Asyr	4	U1/count[3]:CLK	U2/Q[6].E	2.60			5.786	0.454	6.592	0.241	1		
External Recov. *	5	U1/count[3]:CLK	U2/Q[9]:E	2.60			5.797	0.454	6.582	0.230			
1	6	U1/count[1]:CLK	U2/Q[9] E	2.4			5,797	0.454	6.324	0.230			
75	7	U1/count[2]:CLK	U2/Q[13]:E	2.4			5.797	0.454	6.310	0.230			
70-	8	U1/count[2] CLK	U2/Q[15].E	2.4			5.797	0.454	6.310	0.230			
65-	9	U1/count[2]:CLK	U2/Q[11]:E	2.4	1 1.845	3.952	5.797	0.454	6.310	0.230			
60- 55-		Details for path From: U1/count[2] To: U2/Q[9]:E	CLK										
50-		Pin Na	ne	Type	N	t Name	Cell	Name	Op De	lay (ns)	Total (ns)	Fanout Edge	
		U1/count[2]:Q		cell		A	ADLIB:0	DFN1C1	+	0.550	2.031	4 f	
45-		U1/G_1:B		net	U1/coi	int[2]			+	0.241	2272	f	
40- 35-		U1/G_1:Y		cell			ADLIB #	NOR2B	+	0.469	2.741	1 f	
35-		U1/un1_ld_reg:C		net	U1/un1	_ld_reg_0	1		•	0.249	2.990	f	
30-		U1/un1_ld_reg:Y		cell			ADLIB:	NOR3C	•	0.509	3.499	7 f	
25-		U2/Q[9]:E		net	Id_reg	sig			•	0.643	4.142	f	
20-		data arrival time									4.142		
				0	- 22								
15-		Data required tim	e calculation							-			
10-		CLK		Clock Constrain			1			5.000	5.000		
5		CLK		Clock source					*	0.000	5.000	t	
0		CLK_pad/U0/U0:PAI	2	net	CLK				+	0.000	5.000	f	
0 5 10		CLK_pad/U0/U0:Y		cell			ADLIB:	OPAD_IN	+	0.514	5.514	1 f	
slack distribution (ns)	1	CLK pad/U0/U1:A		net	CLK p	ad/UD/NET	1		+	0.000	5514	f	

Figure 27 · Slack Calculation in Maximum Delay Analysis View

Cross Probing with SmartTime - Design Using Both Clock Edges

You can use SmartTime to cross probe in Designer and analyze your design.

To cross probe with SmartTime:

1. Double-click the first row in the Maximum Delay Analysis view to open the **Expanded Path** window (as shown in the figure below). The window shows the required data and arrival time calculation and a schematic of the path.

Click and drag in the schematic to view the selected area.



		< 🐵 × २ 🕓	7 In 10 0+ +0		e we want has		Э	
Summary for path From: U1/count[2]:CLK To: U2/Q19/E Data Required Time (ns) 5797 4142							Path Profile Net delay 53.6/%	
Path details								
Pin Name	Туре	Net Name	Cell Name	Op	Delay (ns)	Total (ns)	Fanout Edg	ge
CLK_pad/U0/U0:Y	cell		ADLIB:IOPAD_IN	+	0.747	0.747	1 1	
CLK_pad/U0/U1:A	net	CLK_pad/U0/NET1		+	0.000	0.747	r	
CLK_pad/U0/U1:Y	cell		ADLIB:CLKIO	+	0.260	1.007	36 r	
U1/count[2]:CLK	net	CLK_c		+	0.474	1.481	r	
U1/count[2]:Q	cell		ADLIB:DFN1C1	+	0.550	2.031	4 f	
U1/G_1:B	net	U1/count[2]	с. С. С. С	+	0.241	2.272	f	
U1/G_1:Y	cell		ADLIB:NOR2B	+	0.469	2.741	1 f	
U1/un1_Id_reg:C	net	U1/un1_Id_reg_0		+	0.249	2.990	f	
U1/un1 ld rea:Y	cell		ADLIB:NOR3C	+	0.509	3.499	7 f	
	K pad/U0/U0	CLK_pad/U0/U1	U1/cour D CLR	nt[2] Q	4	U1/G_1		
		CLKIO	DENT			NOR2B		

Figure 28 · Cross-Probing a Path in the SmartTime Expanded Path Window

- 2. In Designer, click ChipPlanner to open the tool.
- 3. In the SmartTime Expanded Path window select an object (such as a net), right-click it and choose **Cross-probe path**, as shown in the figure below.

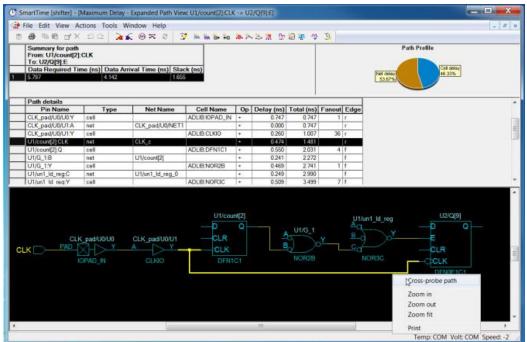


Figure 29 · Cross-probe path in SmartTime

View **ChipPlanner** and notice that the path you selected in SmartTime is highlighted in ChipPlanner, as shown in the figure below. See the <u>ChipPlanner online help</u> for more information on using the tool.



Generate a Timing Report - Design Uses Both Clock Edges

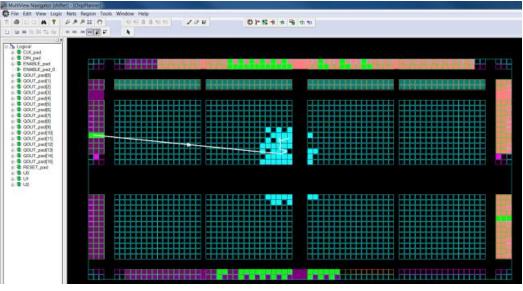


Figure 30 · Cross-Probe Path in ChipPlanner

4. Close ChipPlanner to continue.

Generate a Timing Report - Design Uses Both Clock Edges

Timing reports can be generated from SmartTime. Timing reports enable you to quickly determine if there are any timing problems. The timing report lists the following information:

- Design information including device, speed grade and operating conditions.
- Design performance summary (maximum frequency, external setup and hold, minimum and maximum clock-to-out)
- Clock domain details.
- Inter clock domain details.
- Pin to pin timing

The timing report can be printed and saved.

To generate a Timing Report:

1. In SmartTime from the **Tools** menu, choose **Reports > Report Paths** to open the Timing Report Options Dialog box, as shown in the figure below.



Option Categories	Paths	
 Select a category: General Paths Sets Clock Domains 	Display of paths	
	Limit the number of reported paths per section to:	1
	Limit the number of expanded paths per section to:	1
	Limit the number of parallel paths in expanded path to:	1
		Restore Defaults
Help	OK	Cancel

Figure 31 · Timing Report Options Dialog Box

2. Click the **Paths** category. Limit the number of reported paths to **1**, and click **OK**. The timing report opens in a new window, as shown in the figure below.



Generate a Timing Report - Design Uses Both Clock Edges

File Actions Help		
Timing Report Max Delay Ana	alysis	
SmartTime Version v11.2		0
	crosemi Libero Software Release v11.2 (Version	11 2 0 191
Copyright (c) 1989-2013	rosemi pipero portware nerease vira (version	11.2.0.10)
Date: Tue Nov 05 14:40:58 2	2013	
Date: 146 Nov 05 14.40.50 1		
Design: shifter		
Family: ProASIC3		
Die: A3P060		
Package: 100 VQFP		
Temperature: COM		
Voltage: COM		
Speed Grade: -2		
Design State: Post-Layout		
Data source: Silicon verifi	ed	
Min Operating Condition: BE		
Max Operating Condition: WC		
Using Enhanced Min Delay Ar		
Scenario for Timing Analysi		
SUMMARY		
	CLR	
SUMMARY		
SUMMARY Clock Domain: Period (ns):	CLK	
SUMMARY Clock Domain: Period (ns): Frequency (MHz):	CLK 6.690 149.477	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns):	CLK 6.690 149.477 10.000	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz):	CLK 6.690 149.477 10.000 100.000	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns):	CLK 6.690 149.477 10.000 100.000	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns):	CLK 6.690 149.477 10.000 100.000 3.334	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns): Max Clock-To-Out (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915 Input to Output	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns): Max Clock-To-Out (ns): Min Delay (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915 Input to Output N/A	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Setup (ns): Min Clock-To-Out (ns): Max Clock-To-Out (ns): Min Delay (ns): Max Delay (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915 Input to Output N/A	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Setup (ns): Min Clock-To-Out (ns): Min Delay (ns): Max Delay (ns):	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915 Input to Output N/A	
SUMMARY Clock Domain: Period (ns): Frequency (MHz): Required Period (ns): Required Frequency (MHz): External Setup (ns): External Hold (ns): Min Clock-To-Out (ns): Max Clock-To-Out (ns): Min Delay (ns): Max Delay (ns): END SUMMARY	CLK 6.690 149.477 10.000 100.000 3.334 0.206 2.184 5.915 Input to Output N/A	

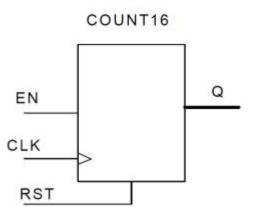
Figure 32 · Timing Report for shifter

The timing report contains the following sections:

- Header
- Summary
- Clock domain details for CLK and expanded path information
- External setup information
- Clock to output delay information
- 3. Save the timing report as shifter_timing.rpt and close the report window.
- 4. Close SmartTime and Designer.

16-Bit Binary Counter Example

This example describes how to enter a clock constraint, input delay and output delay constraints for the 16bit counter pictured in the figure below. You will import an SDC file with a clock constraint of 200 MHz and add input delay constraints of 8 ns and an output delay constraint of 5 ns using SmartTime . After routing the design you will analyze the timing and set multi-cycle path constraints to determine the maximum operating frequency.





Set Up Your 16-Bit Binary Counter Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **Counter16** and set the project location according to your preferences. Enter the following values for your new project:
- Family: ProASIC3
- Die: A3P060
- Package: 100 VQFP
- Speed: -2
- Die Voltage: 1.5 V

Import the 16-Bit Binary Counter Example Design Source File

You must import the count16.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import the EDN file:

- 1. From the **File** menu, choose **Import > Others**.
- 2. Choose EDIF Netlists from the file type dropdown list in the Import Files dialog box.
- 3. Browse to the location of the counter16.edn file and select it. Click Open to import the file.
- 4. Verify that the file appears in your project, as shown in the figure below.



Libero - D:\Cpounter16\Cpounter16.prjx*		
Project File Edit View Design Tools Help		
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4 🇰 work	4 (keywordMap (keywordLevel 0))	
COUNT16 (COUNT16.edn)	5 (status	
	6 (written	
	7 (timeStamp 2005 4 22 7 31 38)	
	8 (author "Synplicity, Inc.")	
	<pre>9 (program "Synplify" (version "7.7.0, Build 060R"))</pre>	
	12 (library PA3	
	13 (edifLevel 0)	
	14 (technology (numberDefinition))	
	15 (cell XOR2 (cellType GENERIC)	
	<pre>16 (property dont_touch (string "false"))</pre>	
	17 (property area (integer 1))	
	18 (view prim (viewType NETLIST) 19 (interface	
•	20 (port Y (direction OUTPUT)	
	21 (property max fanout (integer 2000))	-
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А		
	Fam: ProASIC3 Die: A3P060	Pkg: 100 VQFP Verilog

Figure 34 · COUNT16 (COUNT16.edn) in the Design Hierarchy Window

Import a Timing Constraint File

The SDC file contains a Timing Constraint of 5.714 ns for the CLK of the COUNT16 design.

To import the Timing Constraint:

- 1. From the File menu, choose Import > Timing Constraint (SDC) Files.
- 2. Navigate to the folder that contains the file COUNT16.sdc. Click to select it and click Open.
- 3. A pop-up dialog appears to ask if you want to organize the constraint files for your current root (COUNT16). Click **Yes** to continue.
- 4. In the Libero SoC Files window, check that the COUNT16.sdc file appears in the constraint directory and that COUNT16.edn appears in the synthesis directory, as shown in the figure below.



🕑 Libero - D:\Cpounter16\Cpounter16.prjx*					. 🗆	X
Project File Edit View Design Tools Help						
🗋 🚔 🚍 😂 🗇 🗿 📝						
Files & ×	StartPage 🗵	COUNT16.edn	COUNT16.sdc			
Component		Design Paramete				
4 🔁 constraint	2	Dobryn raramoto				
COUNT16.sdc	3 # Clocks					
🗀 coreconsole	5 create cloc	k -period 5.714	-waveform { 0.	.000 2.857	} {CI	LK }
designer	6		(- ·			
🗀 hdl 💳	7					
Image: Simulation						
🗀 smartgen						
🗀 stimulus						
synthesis						
COUNT16.edn						
Design Hierarchy Design Flow Log Files						
Search Results						đΧ
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a						
•						
		_				
		f	Fam: ProASIC3 Die: /	A3P060 Pkg: 1	0 VQFP	Verilog

Figure 35 · COUNT16.edn and COUNT16.sdc in the Libero SoC File Window

- In the Design Flow window, right-click Create/Edit Timing Constraint and choose Open Interactively. Designer opens and runs Compile with the default settings. After Compile is complete the Compile button in Designer turns green and the SmartTime Constraints Editor opens.
- 6. Expand **Requirements** and click **Clock**. Notice the CLK Constraint of 5.714 ns. The File column lists the SDC file you have imported as the source of the Constraint, as shown in the figure below.

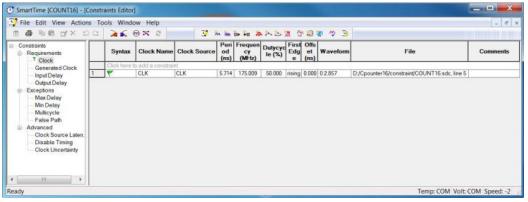


Figure 36 · SmartTime Constraint Editor with SDC Clock Constraint

Add an Input Delay Constraint

Input Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA so that the external setup requirements to the FPGA can be met. If external setup requirements are not met, the design may not work on the board.

To add an input delay constraint for the EN and RST ports:

1. From the **Actions** menu, choose **Constraint > Input Delay**. The Set Input Delay Constraint dialog box opens, as shown in the figure below.



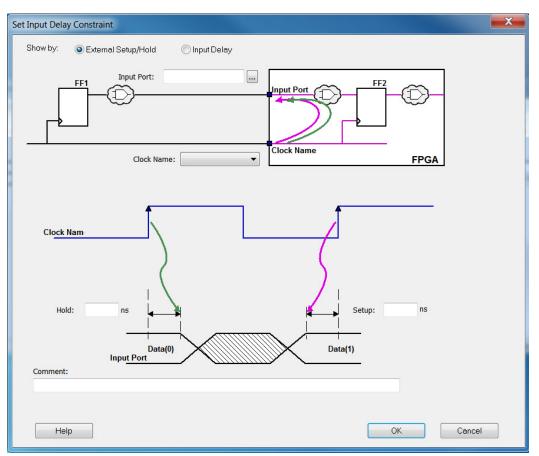
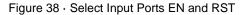


Figure 37 · Set Input Delay Constraint Dialog Box

- 2. Click Show by: External/Setup Hold.
- 3. Select the Input port for the input delay constraint. Click the **Browse** button to open the Select Ports for Input Delay dialog box.
- 4. Select the ports **EN** and **RST** and click **Add** to move the pins to Assigned Pins list (as shown in the figure below). Click **OK** to continue.



Select Ports for Inpu	t Delay			X
Specify pins	by explicit list) by keyword and w	ildcard	
Available Pins:			Assigned Pins:	
CLK		Add >	EN RST	
		Add All >		
		< Remove		
		< Remove All		
				6
Filter available pi	ns:			
Pin Type:	Input Ports	•		
*		Filter		
Help			ОК	Cancel



- 5. Enter the following values in the **Set Input Delay Constraint** dialog box (as shown in the figure below):
- Clock Port: Select CLK from the drop down menu.
- Hold: 1 ns
- Setup: 0.5 ns



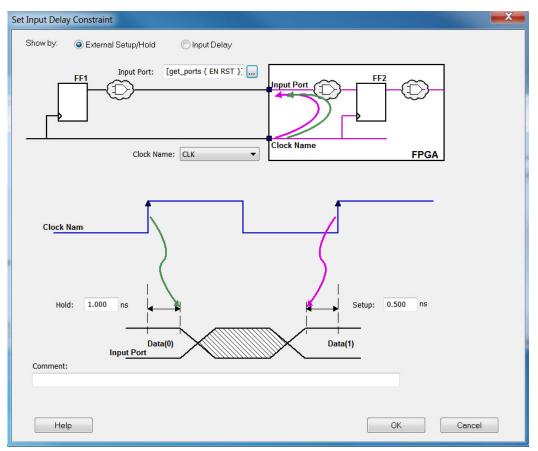


Figure 39 · Select Input Ports and Add a Delay Constraint

6. Click **OK** to continue.

Your new Input Delay constraints are visible in the SmartTime Constraints Editor, as shown in the figure below. Notice that the editor displays the external setup/hold requirement.

SmartTime [COUNT16]										
File Edit View Actions Tools Window Help										
◎ ● ● ● ○ ↓ 2 2 えん ◎ オ ◇ ↓ ◆ ● ★ ◇ ★ ◇ ★ ◇ ★ ◇ ★ ◇ ◆ ◇ ◆ ●										
Constraints Editor										
Constraints	Synta x	Input ports	Clock	Setup (ns)	Hold (ns)	Max Delay (ns)	Min Delay (ns)	Clock Edge	File	Comments
Generated Clock		ere to add a constraint [get_ports { EN RST }]	CLK	0.500	1.000			rising	GUI	
Output Delay Exceptions Max Delay Min Delay Min Delay Multicycle False Path Advanced Clock Source Laten. Disable Timing Clock Uncertainty										
Ready							Tom	p: COM Vol	- COM	Canada 2

Figure 40 · Input Delay in the SmartTime Constraints Editor



Add an Output Delay Constraint

Output Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA for the output ports of the design. If external output delay requirements are not met, the design may not work on the board.

To add an output delay constraint:

- 1. From the **Actions** menu, choose **Constraint > Output Delay**. The Set Output Delay Constraint dialog box opens, as shown in the figure below.
- 2. Click Show by: Output Delay.

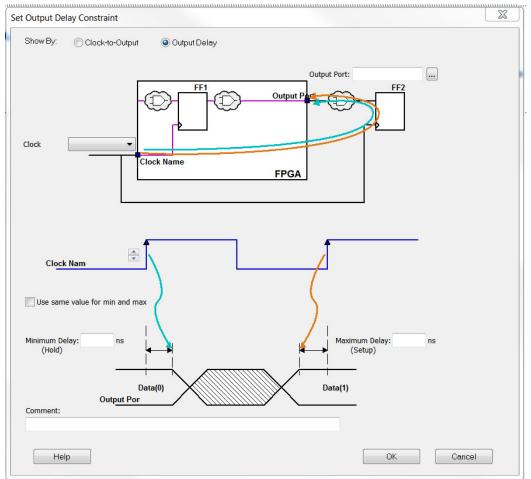


Figure 41 · Set Output Delay Dialog Box

 Click the Browse button to select the ports for the Output Delay Constraint. The Select Ports for Output Delay dialog box appears, as shown in the figure below. Click Add All to add all ports to the Assigned Pins list. Click OK to continue. NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. **View the online help included with software to enable all linked content.**



Specify pins 💿 by explicit list	by keyword and w	ildcard	
Available Pins:		Assigned Pins:	
	Add >	Q	
		Q(0)	
		Q(1)	
	Add All >	Q(10) Q(11)	=
		Q(11) Q(12)	
	< Remove	Q(12)	
		Q(14)	
		Q(15)	
	< Remove All	Q(2)	
		Q(3)	-
		Q(4)	1
Filter available pins:			
Pin Type: Output Ports	-		
*	Filter		

Figure 42 · Select Output Ports and Add Output Delay Constraints

- 4. Enter the following values in the Set Output Delay Constraint dialog box (as shown in the figure above):
- Clock Port: Select CLK from the drop down menu
- Enable Use same value for min and max
- Maximum Delay (Setup): 1.25 ns
- 5. Click **OK** to continue. The Output Delay constraint appears in the SmartTime Constraints Editor, as shown in the figure below.

SmartTime [COUNT16 *]						-		-	-			
File Edit View Actions Tools	Windov	v Help										
5 6 6 6 7× 20	≥ ≤	⊛≍ ¢	😏 🕅 💑	ő+ ¥a 🖄	入る法	🔓 😡 🕯	n 🖓 i	9				
😲 Constraints Editor												- • ×
Constraints Requirements Clock	Synta x	Output ports	Clock	Clk To Out Max (ns)	Clk To Out Min (ns)	Max Delay (ns)	Min Delay (ns)	Clock Edge	File	Comments		
Generated Clock		ere to add a con]	
1 Input Delay	٣	[all_outputs]	CLK			1.250	1.250	rising	GUI			
Courteut Delay Exceptions Max Delay Max Delay Min Delay Multicycle False Path Advanced Clock Source Laten. Disable Timing Clock Uncertainty												
eady										Temp:	COM Volt:	COM Speed: -2





- 6. From the **File** menu, choose **Commit** to save your changes.
- 7. From File menu, choose Exit to close SmartTime.

Place and Route the 16-Bit Binary Counter Design

To run Layout on the design 'Counter16':

- 1. In Designer, click Layout
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.

Using Filters and Creating Analysis Sets - 16-Bit Binary Counter Example

Filters can be used and saved to display analysis sets in the Maximum Delay Analysis window and the Minimum Delay Analysis window.

To create a filter:

- 1. When Layout is complete, click **Timing Analyzer** in Designer to open the SmartTime Timing Analyzer.
- 2. Select the **Register to Register path** in the Maximum Delay Analysis View. Enter the following in the Filter fields (as shown in the figure below) then click **Apply Filter**:

From: Q[0]:CLK

To: *:D

ile Edit View Acti				• ¥o 🎗		31 De 3	a 🗴 🦘	3								-
À	From	n Q[0]:CLK	11						ro ":D				Apply Filter	Store F	ilter	Reset Filt
Summary Datasheet × CLK	F	Source Pin	Sink Pin	Delay (ns)	Slack (ns)	Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)			Abbil Linds	540101		THE SECTION
 Register to Register External Setup 	<u> </u>	Q[0].CLK	Q[11]:D	5.25			6.729	0.428	5.696	0.009						
× Clock to Output	2	O[0]:CLK	Q[10]:D	5.25			6.727	0.428	5.692	0.011						
Register to Asynch	4	Q[0]:CLK	Q[6]:D	5.12			6.736	0.428	5.551	0.002						
 External Recov. 	4	Q[0]:CLK Q[0]:CLK	Q[9]:D Q[8]:D	4.93			6.755	0.402	5.346 5.318	0.009						
Asynchronous to R	6	Q[0]:CLK	Q[7]:D	4.60			6.741	0.402	5.032	-0.007						
S Pin to Pin	7	Q101:CLK	Q[5]:D	4.54			6.767	0.402	4.947	-0.003						
Input to Output	8	QIDICLK	Q[4]:D	4.48			6.767	0.402	4.884	-0.003						
X User Sets	9	Q[0]:CLK	Q[15]:D	4.40			6,753	0.402	4.816	0.011						
	10	Q[0]:CLK	Q[14]:D	4.164			6.755	0.402	4.575	0.009						
	11	Q[0]:CLK	Q[13]:D	4.000	1.304	5.458	6.762	0.402	4.410	0.002						
	12	Q[0]:CLK	Q[12]:D	4.00		5.453	6.762	0.402	4.405	0.002						
		Details for path From: Q[0]:CLK To: Q[11]:D														
		Pin Name	Туре				Net Nar	ne		(ell Name	Op	Delay (ns)		Fanout	Edge
		CLK	(Ale ale							_			0.000	0.000		
		CLK	Clock source		м					_		+	0.000	0.000		r
		CLK_pad/U0/U0:PAD		C	.К							+	0.000	0.000		r
		CLK_pad/U0/U0.Y	cell							ADI	IB:IOPAD_IN		0.747	0.747	1	
		CLK_pad/U0/U1:A	net	C	.K_pad/U	JU/NET1						•	0.000	0.747		r
		CLK_pad/U0/U1:Y Q[0]:CLK	cell	-	Kc					ADI	IB:CLKIO	•	0.260	1.007	16	r
			net													

Figure 44 · Applying a Filter in the Maximum Delay Analysis View

 Click Store Filter to save the filter. Enter Q0_filter in the Store Filter as Analysis Set dialog box. The set will be visible in the Maximum Delay Analysis View under Register to Register, as shown in the figure below.



File Edit View Actio								-				-	8
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	From	*				1	Fo *						
MAX ତ୍ରୀ Summary									Apply Filte	r S	Store Filter	Reset Filte	— Ì
⊖ [©] Datasheet ⊖ [×] [™] CLK		Source Pin	Sink	Pin Dela		Arrival (ns)	Required (ns)	Setup (ns)	Minimum Period (ns)	Skew (ns)			
Register to Regi: ✓ Q0 filter	1	Q[0]:CLK	Q[11]:D	5.2			6.729	0.428	5.696	0.009	ĺ		
Q[1] filter	2	Q[0]:CLK	Q[10]:D	5.2		6.705	6.727	0.428	5.692	0.011			
Q[2]_filter	3	Q[0]:CLK	Q[6]:D	5.1		6.573	6.736	0.428	5.551	0.002			
Q[4] filter	4	Q[0]:CLK	Q[9]:D	4.9		6.387	6.755	0.402	5.346	0.009			
× External Setup	5	Q[0]:CLK	Q[8]:D	4.9		6.361	6.757	0.402	5.318	0.007	_		
Clock to Output	6	Q[0]:CLK	Q[7]:D	4.6		6.059	6.741	0.428	5.032	-0.003			
Register to Asynch	7	Q[0]:CLK	Q[5]:D	4.5		6.000	6.767	0.402	4.947	-0.003	_		
External Recov	8	Q[0]:CLK	Q[4]:D	4.4		5.937	6.767	0.402	4.884	-0.003	-		
Asynchronous to R		Q[0]:CLK	Q[15]:D	4.4		5.855	6.753	0.402	4.816	0.011			
Pin to Pin	10	Q[0]:CLK	Q[14]:D	4.1	64 1.139	5.616	6.755	0.402	4.575	0.009			
Input to Output		Details for path From: Q[0]:CLK To: Q[11]:D		-							-		(
		Pin Nan	ne	Туре			Net	Name			Cell Name	e Op	De
■ III													
		data required time									1		
		data arrival time										-	
		slack											-
-5 Slack distribution (ns)													

Figure 45 · Store Filter as Analysis Set

- 4. Click the **Reset Filter** button.
- 5. Repeat the steps above using the following filter values to create the sets listed in the table below.

From	То	Name
Q[1]:CLK	*:D	Q1_filter
Q[2]:CLK	*:D	Q2_filter
Q[3]:CLK	*:D	Q3_filter
Q[4]:CLK	*:D	Q4_filter

The path sets appear under Register to Register in the Maximum Delay Analysis View, as shown in the figure above.

6. Close SmartTime, Designer, and Libero SoC.

False Path Constraints

This section describes how to enter false path constraints in SmartTime. You will import an EDIF netlist from the design shown below. After routing the design you will analyze the timing and set false path constraints and observe the maximum operating frequency in the SmartTime Timing Analysis window.

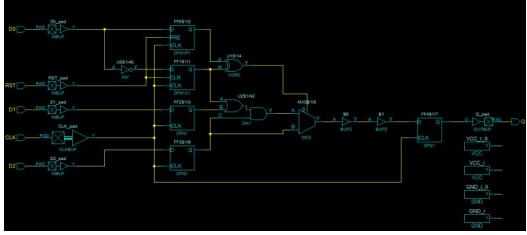


Figure 46 · Example Design with False Paths

Set Up Your False Path Example Design Project

- 1. Open Libero and create a new project (from the **Project** menu, choose **New Project**).
- 2. Name the project **FALSE_PATHS** and set the project location according to your preferences. Enter the following values for your new project:
- Family: ProASIC3
- Die: A3P060
- Package: 100 VQFP
- Speed: STD
- Die Voltage: 1.5 V

Import the FALSE_PATH File and Add A Constraint

You must import the FALSE_PATH design file into your design for this tutorial. Download the design files from the Microsemi website.

To import and constrain the design:

- 1. From the File menu, choose Import > HDL Source Files.
- 2. Browse to the location of the **FALSE_PATHS** design file (Verilog or VHDL) file and select it. Click **Open** to import the file.
- 3. Verify that the file appears in your project, as shown in the figure below.



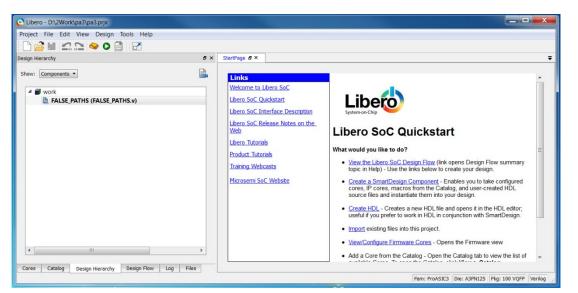


Figure 47 · FALSE_PATHS Design in Design Hierarchy

- 4. In the Design Flow window double-click **Compile** to Compile with default settings. A green check mark appears next to Compile to indicate that it has completed successfully.
- Click to access the Design Flow window in Libero SoC. Right-click Create/Edit Timing Constraints and choose Open Interactively. Designer opens along with the SmartTime Constraint Editor. Minimize Designer.
- 6. In the SmartTime Constraints Editor, enter a constraint for the clock source (**CLK**) of **100 MHz** (50% duty cycle), as shown in the figure below.

SmartTime [FALSE_PATHS *]											
File Edit View Actions Too	ls Window	Help									
8 8 8 8 7 × 20	: 🔉 🖌	⊛≍ <i>2</i>	10 AN IN 10	+0	8×3	11 fr	10 i n	'nŋ	Э		
Constraints Editor											
Constraints Requirements Clock	Synta x	Clock Name	Clock Source		Frequen cy (MHz)	Dutycyc le (%)	First Edg e	Offs et (ns)	Waveform	File	Comments
Generated Clock	Click he	ere to add a con	straint								
Input Delay	1 7	CLK	CLK	10.00	100.000	50.000	rising	0.000	05	GUI	
Output Delay Exceptions Max Delay Min Delay Multicycle False Path Advanced Clock Source Laten. Disable Timing Clock Uncertainty											
Ready							1	Temp:	COM Volt:	MOC	Speed: -2

Figure 48 · Clock Constraint of 100 MHz in FALSE_PATHS

8. Commit your changes and close SmartTime.

Place and Route Your FALSE_PATH Design

To run Layout on FALSE_PATH:

- 1. In Designer, click Layout .
- 2. Click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. The Layout button in Designer turns green when Layout has completed successfully.



Timing Analysis - Maximum Clock Frequency

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

To perform Maximum Delay Analysis:

1. Click the **Timing Analyzer** button in Designer to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). The Maximum Delay Analysis View displays a summary of design performance and indicates that the design will operate at 188.679 MHz.

SmartTime [FALSE_PATHS]	- [Maxir	num Delay Ar	nalysis View]									x
À File Edit View Actior	ns Tools	Window	Help								-	e ×
6 8 6 8 7 × 5	2 🗠	🌬 🖌 🐵 🎙	र २ 🖸	n 🦗 🌬	6 🔉 🕆 🖄	🕅 🔓 🖾	🏧 🧄 J	9				
MAX Summary S Datasheet V @ CLK Register to Regi Ctock to Output Register to Asynch External Recover Asynchronous to R X Pin to Pin Input to Output	Data so Using E Clock De	ProASIC A3P060 e: 100 VQF Stat Post-Lay surce Silicon v inhanced Min E	3 P rout erified		Conditio WO Condition BES CO CO STE Required Frequency	T 1 1	External Hold (ns)					
User Sets	CLK	5.300	(MI12) 188.679	10.000	(MHz) 100.000	1.380	0.247	7.678	2.327			
Select a set of paths to see here its slack distribution.	I/O Deta Nar Input to		ielay (ns) M. N/	ax Delay (ns) A	2			1	,			
Ready									Temp:	COM Volt: CO	OM Speed: S	TD

Figure 49 · Maximum Delay Analysis Summary

- 2. Click the + sign next to CLK to expand the display and show the Register to Register path sets.
- 3. Select **Register to Register** to display the register-to-register paths. Notice that the slack values are positive.
- 4. Click to select the first row in the path list. The path is from the clock pin flip flop FF1 to the D input of flip flop FF4. Note that the path goes through the A input of multiplexer MX0.

The <u>design schematic</u> shows that the S input of MX0 will always be logic 1; consequently, all the paths through the A input of MX0 and the S input of MX0 are false paths. You must set a false path on these paths in order to determine the true maximum operating frequency.

5. To set the path from FF1\$111:CLK to FF4\$117:D as false, select the row containing this path in the Register to Register path set, right-click and choose **Add False Path Constraint** (as shown in the figure below). The Set False Path Constraint dialog box appears.



SmartTime [FALSE_PATHS] - [Maximum Delay Analysis View] à File Edit View Actions Tools Window Help @ B @ d X 20 ≥£ @× 0 J m m & + + * * * * * * * * * * * * * * * 10 From To 6 Store Filter Reset Filter Apply Filter 8 mary Delay (ns) Slack Required Setur Skew Datasheet Arrival Source Pin Sink Pin ind CLK (ns) (ns) (ns) (ns) (ns) Register to R FE1\$101CLK 3.849 11.049 0.402 0.004 2 800 External Setup Сору 0.00 2\$113 CLK 11.049 0.403 Clock to Outp. FF3\$1I6-CLK Print 3 567 11.023 0.428 2 5 4 4 0.000 Register to Asy 11.049 0.402 2.422 0.004 FF0\$112-CLK 3.471 External Recov Add False Path Constraint Add Max Delay Constraint Add Min Delay Constraint Details for p From: FF1\$1 Add Multicycle Path Constraint To: FF4\$117 Expand selected paths Pin Nan Cell Name Op Delay (ns) Total (ns) Fanout E Cross-probe selected paths dack distribu Temp: COM Volt: COM Speed: -2 Create a new false path constraint

Figure 50 · Right-Click and Choose Add False Path Constraint

- 6. Click the Browse button in the Set False Path Constraint dialog box.
- 7. In the **Select Through Pins for False Path Constraint** window, select MX0\$115:A from the list of Available Pins, then click **Add**. Click **OK** to close the dialog box.
- 8. Click OK to close the Set False Path Constraint dialog box.
- 9. From the View menu, choose Recalculate All to recalculate the delays.
- 10. The next longest delay, from: FF1\$111:CLK to: FF4\$117:D is also a false path. Repeat the steps above to set a false path constraint from FF1\$111:CLK to: FF4\$117:D through MX0\$115:S, using the values as shown in the table below.

From	То	Through
FF1\$1I1:CLK	FF4\$1I7:D	MX0\$1I5:A
FF1\$1I1:CLK	FF4\$117:D	MX0\$1I5:S
FF2\$113:CLK	FF4\$117:D	MX0\$1I5:A
FF3\$116:CLK	FF4\$117:D	MX0\$1I5:A
FF0\$1I2:CLK	FF4\$1I7:D	MX0\$1I5:S

11. Open the Constraint Editor and click **False Paths > Exceptions**. The False Path constraints are listed as shown in the figure below.



	straints	Synta	From	Through	То	File	Comm
	Requirements	Click be	ere to add a constrai				
	Generated Clock		FF1\$111:CLK	[get_pins { MX0\$115:A }]	FF4\$117:D	GUI	
	-Input Delay 2	- è	FF3\$116:CLK	[get_pins { MX0\$115:A }]	FF4\$117:D	GUI	
	-Output Delay 3	- *	FF0\$1l2:CLK	[get_pins { U1\$114:A }]	FF4\$117:D	GUI	
-E	xceptions 4	1	FF2\$113:CLK	[get_pins { MX0\$1I5:A }]	FF4\$117:D	GUI	
	Max Delay 5	٣	FF1\$111:CLK	[get_pins { MX0\$115:S }]	FF4\$117:D	GUI	
	Disable Timing						
	– Disable Timing – Clock Uncertainty						

Figure 51 · False Path Constraints in the SmartTime Constraint Editor

12. Recalculate the delays and view the summary in the **Maximum Delay Analysis View**. Note that SmartTime now reports the maximum operating frequency as 232.396 MHz, as shown in the figure below.

≽ Maximum Delay Analysis V	/iew										3
Al Summary Al Datasheet ✓ ✓	Data so Using E	Stat Post-Lay urce Silicon v nhanced Min E	3 P rout erified			8т И И					
	Clock De	tails:									
	Name	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)		Max Clock to Out (ns)			H
	CLK	4.303	232.396	10.000	100.000	1.380	0.247	7.678	2.327		
Select a set of paths to see here its slack distribution.	I/O Deta Nan Input to (elay (ns) M	ax Delay (ns j A)						
slack distribution (ns)											-
											T

Figure 52 · Maximum Delay Analysis View - Summary

13. Select the **Register to Register** set for CLK. Observe that only one path is visible from F3:CLK to F4:D. This is the only path that propagates a signal (as shown in the figure below).



Timing Analysis - Maximum Clock Frequency

≽ Maximum Delay Analysis View												• ×
MAX	From	•				То	•	Appl	ly Filter	Store Fil	ter Reset	
해 Summary 이 Datasheet 이 CLK		Source Pin	Sink F	··· ("	s) (ns)	(ns)	(ns)	Setup (ns)	Minimum Period (ns)	¹ Skew (ns)		Filter
External Setup Clock to Output Register to Asynchrono	1 F	F3\$116:CLK	FF4\$117:D	3.	764 5.69	7 5.719	11.416	0.539	4.30	0.000	I	
External Recovery Asvnchronous to Reais	F	Details for path rom: FF3\$116:CLK to: FF4\$1170		_								<u> </u>
		Pin Name		Туре		et Name	Cell	Name	Op De	elay (ns)	Total (ns) f	anout
0.8-		ata required time									11.416	
atte		ata arrival time lack			-		-		-9		5.719 5.697	
stited 0.6	H)ata arrival time ca	lculation								0.007	
0.2		LK								0.000	0.000	
		LK		Clock source					+	0.000	0.000	
4 5 6 7		LK_pad/U0/U0:PAD		net	CLK		40110		+	0.000	0.000	
slack distribution (ns)							1000			1 001	1 001	•

Figure 53 · Maximum Delay Analysis View - Register to Register

- Close SmartTime and Designer. 14.
- 15. Close Libero SoC.

Cross Clock Domain Analysis

SmartTime performs inter-clock domain timing checks for designs that contain functional paths that cross two clock domains (the register launching the data and the register capturing the data are clocked by two different clock sources). Accurate specification of both clocks is required to allow a valid inter-clock domain timing check.

SmartTime analyzes each inter-clock domain by determining a common period equal to the least common multiple of the two clock periods.

For setup check, the tightest launch-capture time period is considered to ensure that the data arrives before the capture edge (as shown in the figure below). The hold check verifies that a setup relationship is not overwritten by a following data launch.

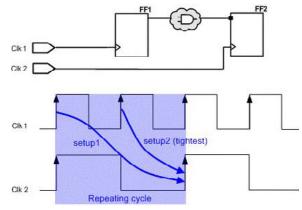


Figure 54 · Tightest Launch - Capture Relation for Setup Check in SmartTime In this tutorial you will:

- 1. Create a new Libero project.
- 2. Import an EDIF netlist for the design shown in the figure below.
- 3. Enter timing constraints for the two clock domains.
- 4. Use SmartTime to analyze the inter-clock domain timing.

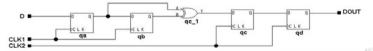


Figure 55 · Inter-Clock Domain Example Design Diagram

Set Up Your Cross Clock Domain Analysis Example Design Project

- 1. Open Libero and create a new project (from the Project menu, choose New Project).
- 2. Name the project **multi_clocks** and set the project location according to your preferences. Enter the following values for your new project:
- Family: ProASIC3
- Die: A3P060
- Package: 100 VQFP
- Speed: STD
- Die Voltage: 1.5 V

Leave all other fields at their default values.



Import EDN File and Run Compile for Cross Clock Domain Analysis Example

Project								
Enable Block Crea	tion							
Name:	multi_cloc	ks						
Location:	C:\Actelpr	'j				Browse		
Prefered HDL type:	Verilog	VHDL						
Description:						¢		
A Edit Tool Profiles								
Device	tion: C:\Actelprj Browse ered HDL type: Verilog VHDL cription: Edit Tool Profiles ce Hly: ProASIC3 A3P060 A3P060 Ce ed: -2 Voltage (V): 1.5							
Family:								
Die:	A3P060	-						
Package:	100 VQFP	•						
Speed:	-2	•						
Core Voltage (V):	1.5	•						
Operating Conditions:								
		Range	ŝ.	Best	Typical	Worst	<u>^</u>	
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Core Voltage (V) Creators		_				-	
Core Voltage (Design Templates and	V) Creators		_	1.575			Version	
Core Voltage (Design Templates and	V) Creators		•	1.575				

Figure 56 · multi_clocks Project Settings

Import EDN File and Run Compile for Cross Clock Domain Analysis Example

You must import the multi_clocks.edn file into your design for this tutorial. Download the design files from the Microsemi website.

To import and constrain the EDN file:

- 1. From the File menu, choose Import > Others.
- 2. Choose EDIF Netlists from the file type dropdown list in the Import Files dialog box.
- 3. Browse to the location of the **multi_clocks.edn** file and select it. Click **Open** to import the file.
- 4. Verify that the file appears in your project, as shown in the figure below.



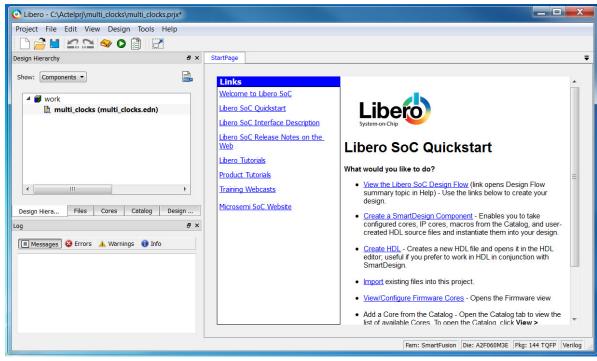


Figure 57 · multi_clocks Design in the Design Hierarchy Window

5. Double-click **Compile** in the Design Hierarchy window to run Compile with default settings. A green check mark appears next to Compile when it has run successfully, as shown in the figure below.

NOTE: Links and cross-references in this PDF file may point to external files and generate an error when clicked. View the online help included with software to enable all linked content.



Enter Timing Constraints for the Cross Clock Domain Analysis Example

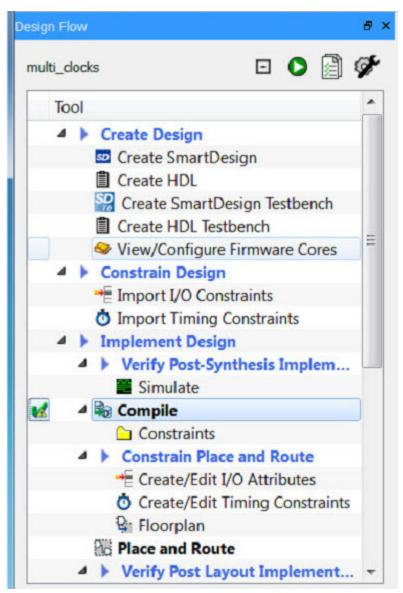


Figure 58 · Design Flow Window - Compile Successful

Enter Timing Constraints for the Cross Clock Domain Analysis Example

To add a clock constraint to your example design:

- 1. In the Design Flow window, right-click **Create/Edit Timing Constraint** and choose **Open Interactively**. Designer opens and then the SmartTime Constraints Editor opens.
- 2. Minimize Designer.
- 3. Use the **Constraints Editor** to enter the following constraints:
- CLK1: 250 MHz
- CLK2: 100 MHz
- 4. Verify that your new constraints are listed in the Constraints Editor, as shown in the figure below.



	Constraints	*		Synta x	Clock Name	Clock Source	Period (ns)	Frequency (MHz)	Dutycycle (%)	First Edge	Offset (ns)	Waveform	File	Comment
Generated Clo.	-	1	Cick he	re to add a con CLK1	cloant CLK1	4.000	250.000	50.000	rising	0.000	02	GUI		
	- Generated Clo Input Delay		2	-		CLK2	10.000	100.000	50.000	rising		05	GUI	-
	Max Delay Min Delay													
4														

Figure 59 · Clock Constraints in the SmartTime Constraints Editor

- 5. Click Commit to save your constraints.
- 6. From the **Tools** menu, choose **Options**. Click the checkbox to enable Inter-Clock domain analysis, as shown in the figure below.

Option Categories	General		
Select a category: General Analysis View Advanced	Operating Conditions Perform maximum delay analysis based on Perform minimum delay analysis based on Clock Domains Clock Domains Include Inter-clock domains in calculations Enable recovery and removal checks.		case case vase lysis. ore Defaults
Help		ОК	Cancel

Figure 60 · Inter-Clock Domain Analysis Enabled in the SmartTime Options Dialog Box

Place and Route Your Cross Clock Domain Analysis Example

To run Layout on multi_clocks:

- 1. View Designer and click Layout.
- Click the checkbox to enable Timing-Driven layout in Layout Options and leave the other values at the default settings, as shown in the figure below. Click OK to continue. The Layout button in Designer turns green when Layout has completed successfully.



Layout Options	J
✓ Timing-driven	
Power-driven	
Run place	
Place incrementally	
Lock existing placement (Fix)	
Run route	
Route incrementally	
Configure	
Advanced	
Help OK Cancel	

Figure 61 · Layout Options - multi_clocks

Analyze Inter-Clock Domain Timing

Inter-clock domain timing enables you to analyze timing for designs that contain functional paths that cross two clock domains.

To analyze inter-clock domain timing:

- 1. Click the **Timing Analyzer** button in Designer. SmartTime opens and displays the Maximum Delay Analysis View.
- 2. Click + to expand the CLK2 paths in the Maximum Delay Analysis View. Click to select the **CLK1 to CLK2** path and observe the inter-clock domain path timing (as shown in the figure below).



File Edit View Actions T	Fools Window Help						2	0
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MAX								
B *					Apply Fi	Iter Store Filter	Reset Filte	Hr.
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 Register to Regist. 	1 qa:CLK qc:D		5 -0.211 3.230	3.019 0.428				
External Setup	2 qb:CLK qc.D) 1.41	8 0.146 2.873	3.019 0.428				
Clock to Output								
Register to Asynchronic	Details for path						1	_
External Recovery	From: ga:CLK							
Asynchronous to Regis	To: qc:D	1000	100			20		
	Pin Name	Type	Net Name	Cell Name	Op Delay (ns)	Total (ns) Fanou	t Edge	
Register to Regist	slack			8		-0.211		
- External Setup +								
111	Data arrival time calcula	tion						
	CLK1			(d)	0.000	0.000		
2	CLK1	Clock source			+ 0.000	0.000	1	
-	CLK1_pad/U0/U0/PAD	net	CLK1	S	+ 0.000	0.000	r	
	CLK1_pad/U0/U0.Y	cell		ADLIB:IOPAD_IN			l r	
	CLK1_pad/U0/U1 A	net	CLK1_pad/U0/NET1		+ 0.000	0.747	r	
8-	CLK1_pad/U0/U1:Y	cell		ADLIB:CLKIO	+ 0.260		1 5	
	qa:CLK	net	CLK1_c		+ 0.448	1,455	t	
.5-	Q:GD	cell	4	ADUB:DFN1	* 0.550	2.005 2	2 1	
	qc_1.8	net	qa		+ 0.249	2.254	1	
4-	qc_1.Y	cell		ADLIB:XOR2	+ 0.737	2.991	f	
	gc:D	net	qc_1		+ 0.239	3.230	f	
12-	data arrival time					3.230		
				<u>0.</u>				
0	Data required time calco	lation						
-0.4 -0.2 0 0.2 stack distribution (ns)	CLK2	Clock Constraint		1	2.000	2.000		
	1 Journ	Mark	(add)		0.000	2,000		

Figure 62 · Maximum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design

The Paths list shows the detailed timing analysis. The longest reported path is from qa:clk to qc:d, as shown in the figure below. This path has a negative slack of 0.211 ns. The clock edges used in the calculation are shown in the timing diagram below.

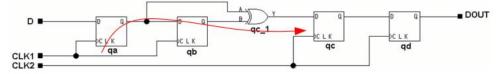


Figure 63 · Longest Reported Inter-Clock Domain Path - multi_clocks Example Design

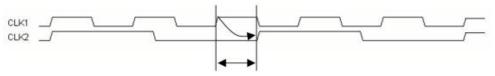


Figure 64 · Clock Edges Used in Inter-Clock Domain Max Delay Calculation - multi_clocks Example Design

- 3. From the **Tools** menu, choose **Timing Analyzer > Minimum Delay Analysis**.
- 4. Expand the CLK2 paths in the Minimum Delay Analysis View. Click to select the **CLK1 to CLK2** path and observe the inter-clock domain path timing, as shown in the figure below.



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B Summary B Datasheet		Source Pin	Sink Pin	Delay (ns)	Slack (ns)	A	rrival (ns)	Required (ns)	Hold (ns)	1	-
e * @ QLK1	1 1	qb:CLK	qc D	0.5	94 0.582	10000	1.276	0.694	0.00		
Register to Regi:	2		qcD	0.7			1.384	0.694			
External Hold	-	de contra de la co		1	57.4 (S.19)	-	1000		d		
Clock to Output Register to Asynch External Removal		Details for path From. gb:CLK								1	-
Asynchronous to R		To: qc:D									
≓ @ CLK2		Pin Name	Type	Net Name	Cell Name	Op	Delay (ns)	Total (ns) F	anout Edge	<u>s</u>	
 Register to Register to Register and Hold 											
Clock to Output		data arrival time				-		1.276			
Register to Asynch		data required time				÷		0.694	1		
- External Removal		alack				1.		0.582			
Asynchronous to R CLK1 to CLK2		Data arrival time cal	rrival time calculation								
B 🌫 Pin to Pin		CLK1				-	0.000	0.000		-	
Input to Output		CLK1	Clock source			+	0.000	0.000	1	-	
I User Sets		CLK1 pad/U0/U0 PAD	net	CUK1		+	0.000	0.000	1		
		CLK1_pad/U0/U0.Y	cell		ADUB KOPAD IN	+	0.319	0.319	11	-	
		CLK1_pad/U0/U1:A	net	CLK1 pad/U0/NET1		+	0.000	0.319	1		
		CLK1 pad/U0/U1/Y	cell		ADLIB CLK0	+	0.123	0.442	2 1	-	
		qb:CLK	net	CLK1_c		+	0.240	0.682	e		
		ab Q	cell		ADLIB DFN1		0.206	0.888	11		
		gc_1:A	net	qb	Company and the second	+	0.114	1.002	t		
		gc_1.Y	cell	100	ADLIB XOR2	+	0.158	1.160	1.6		
		qc0	net	gc_1	and the second se	+	0.116	1276	1		
		data attival time		1.00		1.1		1.276	1		
		D-1								-	
		Data required time of CLK2	Clock Constraint	1		-	0.000	0.000		-	
	-	CLK2	Clock source			+	0.000	0.000	1	-	
		CLK2_pad/U0/U0.PAD		CLK2	-		0.000	0.000	1	-	
		CLK2_pad/U0/U0 Y	cell	44-46	ADUB KOPAD IN		0.319	0.319	1,	-	
		CLK2_pad/U0/U1:A	net	CLK2 pad/U0/NET1	THE REAL PROPERTY OF THE	+	0.000	0.319		-	
05 05 07		CLK2_pad/U0/U1:Y	cell	cone_product i	ADUB/CLKID	+	0.123	0.442	2 1	-	

Figure 65 · Minimum Delay Inter-Clock Domain Timing Analysis - multi_clocks Example Design The Paths list shows the detailed timing analysis. The shortest reported path is from qb:clk to qc:d, as

shown in the figure below. This path has a positive slack of 0.582 ns. The clock edges used in the calculation are shown in the timing diagram below.

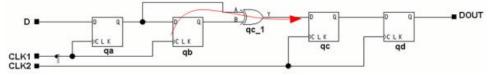


Figure 66 · Shortest Reported Inter-Clock Domain Path - multi_clocks Example Design

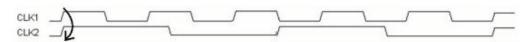


Figure 67 · Clock Edges Used in Inter-Clock Domain Min Delay Calculation - multi_clocks Example Design



Product Support

The Microsemi SoC Products Group backs its products with various support services including a Customer Technical Support Center and Non-Technical Customer Service. This appendix contains information about contacting the SoC Products Group and using these support services.

Contacting the Customer Technical Support Center

Microsemi staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Technical Support

Microsemi customers can receive technical support on Microsemi SoC products by calling Technical Support Hotline anytime Monday through Friday. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.800.262.1060

Phone (International): +1 650.318.4460

Email: soc_tech@microsemi.com

ITAR Technical Support

Microsemi customers can receive ITAR technical support on Microsemi SoC products by calling ITAR Technical Support Hotline: Monday through Friday, from 9 AM to 6 PM Pacific Time. Customers also have the option to interactively submit and track cases online at My Cases or submit questions through email anytime during the week.

Web: www.actel.com/mycases

Phone (North America): 1.888.988.ITAR

Phone (International): +1 650.318.4900

Email: soc_tech_itar@microsemi.com

Non-Technical Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

Microsemi's customer service representatives are available Monday through Friday, from 8 AM to 5 PM Pacific Time, to answer non-technical questions.

Phone: +1 650.318.2470



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