

TOTAL IONIZING DOSE TEST REPORT

No. 05T-RTSX72SU-D1HLH4

Sept 21, 2005

J.J. Wang

(650) 318-4576

jih-jong.wang@actel.com

I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Extrapolated data to 10-year mission passed 90 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 10 days room temperature annealing: average $I_{CCA} = 201.4$ mA; average $I_{CCI} = 123.2$ mA.
3. Input Threshold (V_{THL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in <http://www.actel.com> and <http://www.klabs.org/>) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to the automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements. However, since the tolerance is usually determined by the most degraded parameter, which is often either I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μ m CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	D1HLH4*
Quantity Tested	5
Serial Number	73230, 73117, 73144, 73164, 73176
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min ($\pm 5\%$)
Total Dose	100 krad(Si) ($\pm 5\%$)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

* This report applies to both D1HLH1 and D1HLH4, which are processed as the same wafer lot throughout the processes. Lot number difference was due to End-of-Line split at wafer fab.

B. Test Method

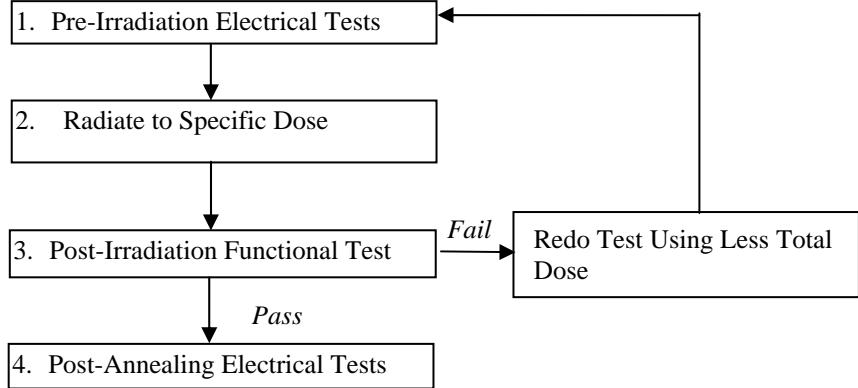


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. The DUTs are annealed for approximately 10 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNR/Y00, ENCNRH/Y00H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC} -plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
73230	100 krad	252	175	227	114
73117	100 krad	271	215	215	121
73144	100 krad	297	184	257	132
73164	100 krad	245	189	208	121
73176	100 krad	302	244	243	128

A semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 73144, the tolerance is extracted as 90 krad for a 10 year mission.



Figure 2 DUT 73230 in-flux I_{CCA} and I_{CCI} ; blue line is I_{CCA} , and red line I_{CCI} .

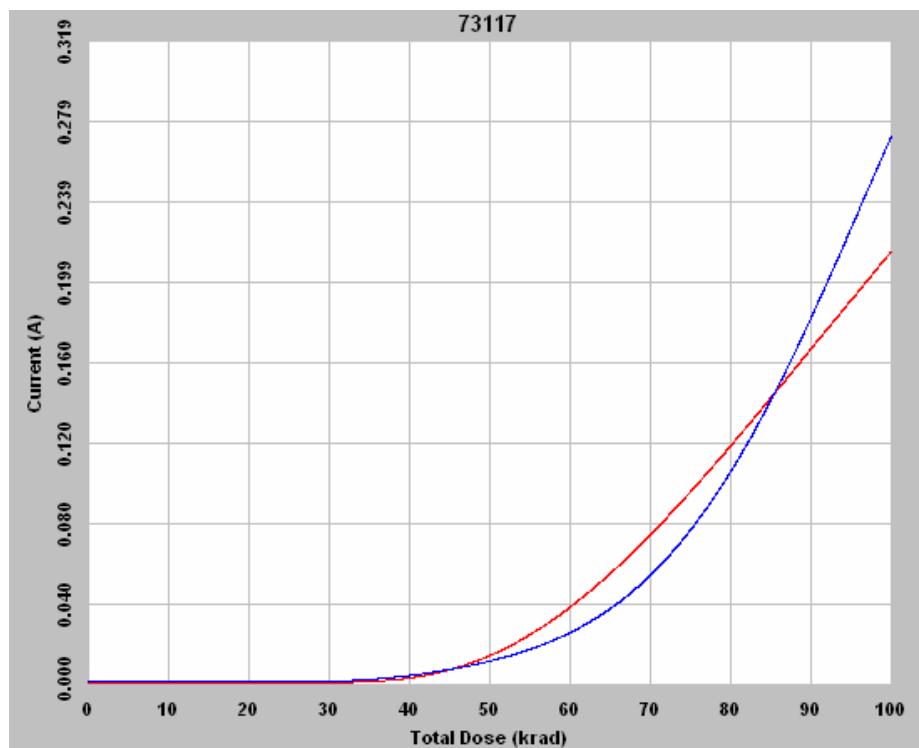


Figure 3 DUT 73117 in-flux I_{CCA} and I_{CCI} ; blue line is I_{CCA} , and red line I_{CCI} .

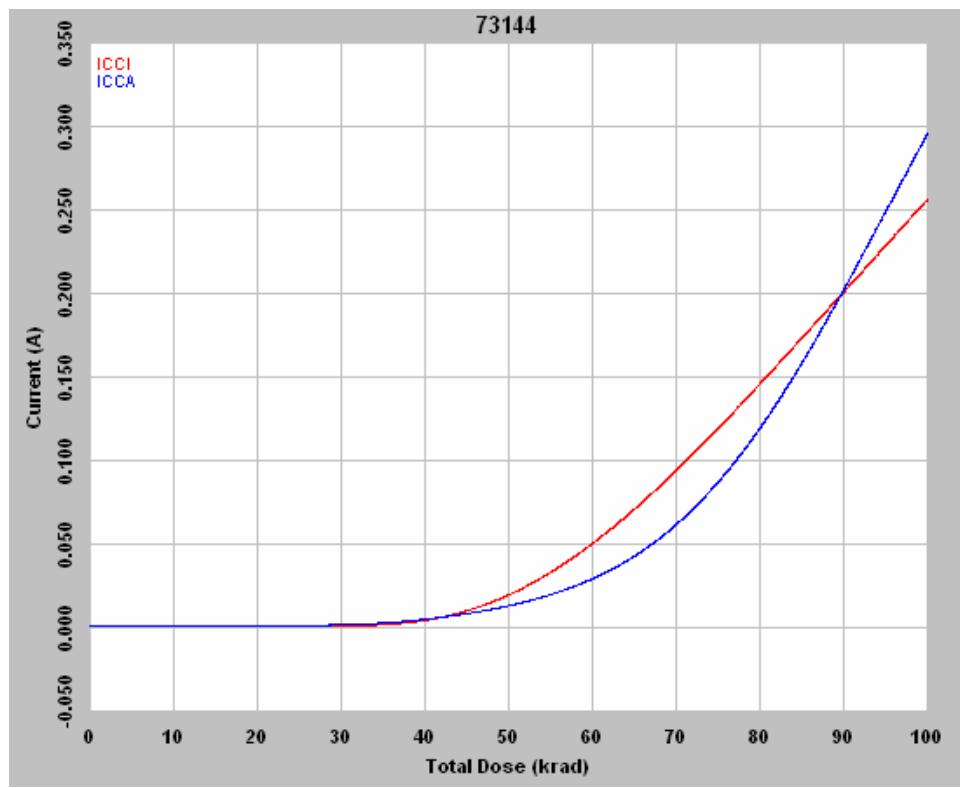


Figure 4 DUT 73144 in-flux I_{CCA} and I_{CCI} ; blue line is I_{CCA} , and red line I_{CCI} .

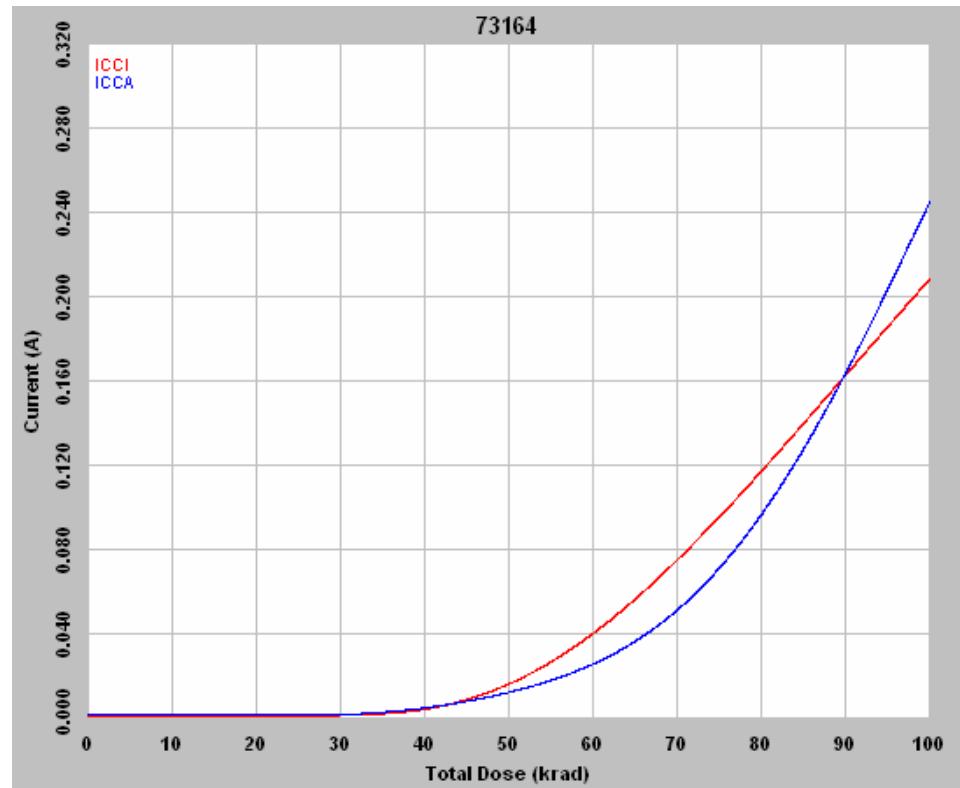


Figure 5 DUT 73164 in-flux I_{CCA} and I_{CCI} ; blue line is I_{CCA} , and red line I_{CCI} .

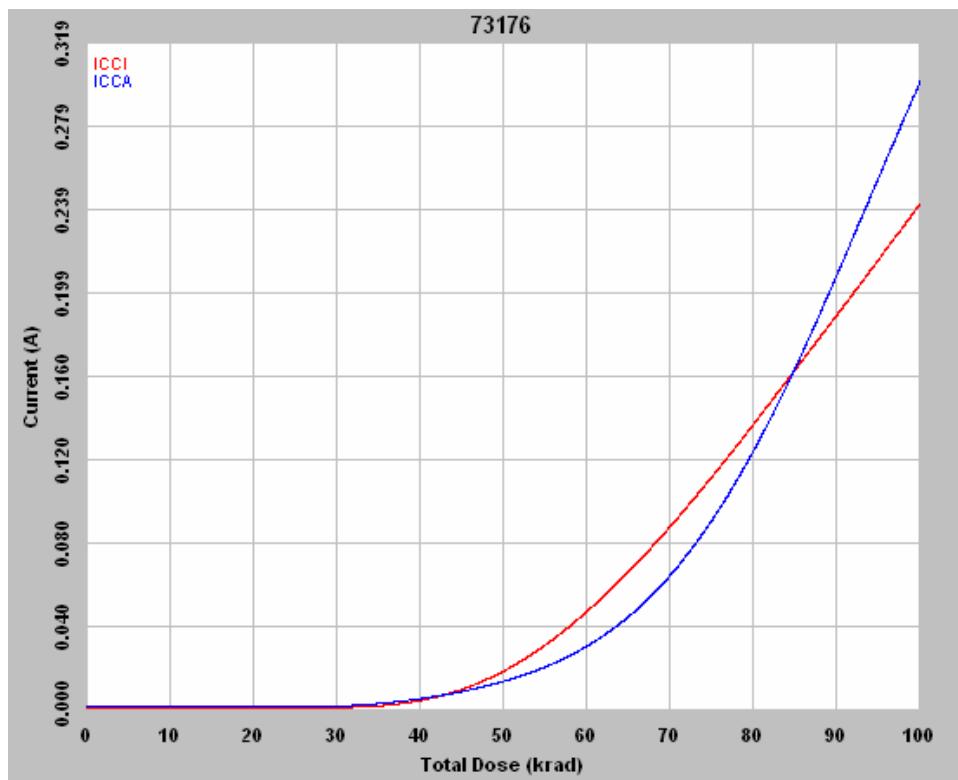


Figure 6 DUT 73176 in-flux I_{CCA} and I_{CCI} ; blue line is I_{CCA} , and red line I_{CCI} .

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA/QA0				DAH/QA0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)						
73230	100 krad	1.38	1.40	1.47	1.43	1.38	1.45	1.43	1.45
73117	100 krad	1.38	1.40	1.47	1.47	1.37	1.46	1.42	1.47
73144	100 krad	1.38	1.44	1.47	1.54	1.38	1.47	1.43	1.48
73164	100 krad	1.38	1.42	1.47	1.47	1.38	1.45	1.43	1.47
73176	100 krad	1.37	1.43	1.46	1.46	1.37	1.46	1.42	1.47

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTR/YO0				ENCNTRH/YO0H			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)						
73230	100 krad	1.38	1.23	1.47	1.43	1.38	1.38	1.48	1.45
73117	100 krad	1.38	1.39	1.48	1.42	1.38	1.36	1.46	1.43
73144	100 krad	1.37	1.41	1.46	1.45	1.37	1.39	1.46	1.44
73164	100 krad	1.38	1.42	1.47	1.45	1.38	1.41	1.47	1.46
73176	100 krad	1.37	1.42	1.45	1.48	1.36	1.43	1.45	1.49

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII0/IDIO0				IDII1/IDIO1			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V_{IL} (V)	V_{IH} (V)						
73230	100 krad	1.39	1.39	1.47	1.47	1.38	1.40	1.47	1.48
73117	100 krad	1.38	1.41	1.46	1.43	1.38	1.39	1.47	1.43
73144	100 krad	1.38	1.40	1.46	1.46	1.37	1.42	1.46	1.47
73164	100 krad	1.38	1.42	1.47	1.46	1.38	1.39	1.47	1.46
73176	100 krad	1.37	1.43	1.45	1.48	1.37	1.43	1.45	1.48

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2/IDIO2				IDII3/IDIO3			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V _{IL} (V)	V _{IH} (V)						
73230	100 krad	1.38	1.41	1.46	1.46	1.39	1.39	1.47	1.45
73117	100 krad	1.37	1.39	1.46	1.42	1.38	1.41	1.46	1.45
73144	100 krad	1.37	1.42	1.47	1.47	1.38	1.42	1.47	1.47
73164	100 krad	1.38	1.43	1.46	1.48	1.38	1.40	1.47	1.48
73176	100 krad	1.37	1.45	1.46	1.50	1.37	1.42	1.46	1.49

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4/IDIO4				IDII5/IDIO5			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V _{IL} (V)	V _{IH} (V)						
73230	100 krad	1.39	1.41	1.48	1.48	1.38	1.40	1.47	1.45
73117	100 krad	1.38	1.40	1.47	1.45	1.38	1.36	1.47	1.42
73144	100 krad	1.38	1.40	1.46	1.46	1.38	1.39	1.46	1.45
73164	100 krad	1.38	1.38	1.47	1.46	1.38	1.38	1.47	1.42
73176	100 krad	1.37	1.43	1.46	1.48	1.37	1.39	1.46	1.46

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6/IDIO6				IDII7/IDIO7			
DUT	Total Dose	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
		V _{IL} (V)	V _{IH} (V)						
73230	100 krad	1.37	1.38	1.43	1.44	1.38	1.38	1.47	1.45
73117	100 krad	1.38	1.35	1.43	1.40	1.38	1.39	1.46	1.41
73144	100 krad	1.37	1.38	1.45	1.42	1.37	1.41	1.46	1.45
73164	100 krad	1.38	1.36	1.44	1.42	1.38	1.41	1.46	1.47
73176	100 krad	1.36	1.39	1.43	1.44	1.37	1.43	1.46	1.47

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an								
73230	100 krad	0.009	0.009	0.106	0.110	0.176	0.183	0.448	0.462	0.922	0.952
73117	100 krad	0.010	0.009	0.116	0.110	0.188	0.184	0.550	0.466	0.952	0.962
73144	100 krad	0.009	0.009	0.109	0.109	0.182	0.182	0.464	0.459	0.951	0.944
73164	100 krad	0.009	0.009	0.110	0.109	0.183	0.182	0.458	0.461	0.943	0.952
73176	100 krad	0.009	0.009	0.119	0.106	0.176	0.178	0.445	0.450	0.989	0.926

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an								
73230	100 krad	4.98	4.98	4.85	4.85	4.64	4.62	4.04	3.99	2.68	2.47
73117	100 krad	4.98	4.98	4.84	4.85	4.63	4.63	4.04	4.01	2.66	2.52
73144	100 krad	4.98	4.98	4.85	4.85	4.64	4.63	4.02	4.00	2.68	2.55
73164	100 krad	4.98	4.98	4.85	4.85	4.62	4.62	4.02	3.99	2.67	2.48
73176	100 krad	4.98	4.98	4.85	4.85	4.45	4.62	4.00	4.00	2.63	2.50

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. DUT 73230 has the worst degradation of 7.98%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation	Post-Annealing	Degradation
73230	100 krad	1.109	1.198	7.98%
73117	100 krad	1.187	1.226	3.29%
73144	100 krad	1.143	1.181	3.29%
73164	100 krad	1.149	1.191	3.65%
73176	100 krad	1.154	1.190	3.10%

F. Transition Time

Figures 7 to 16 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

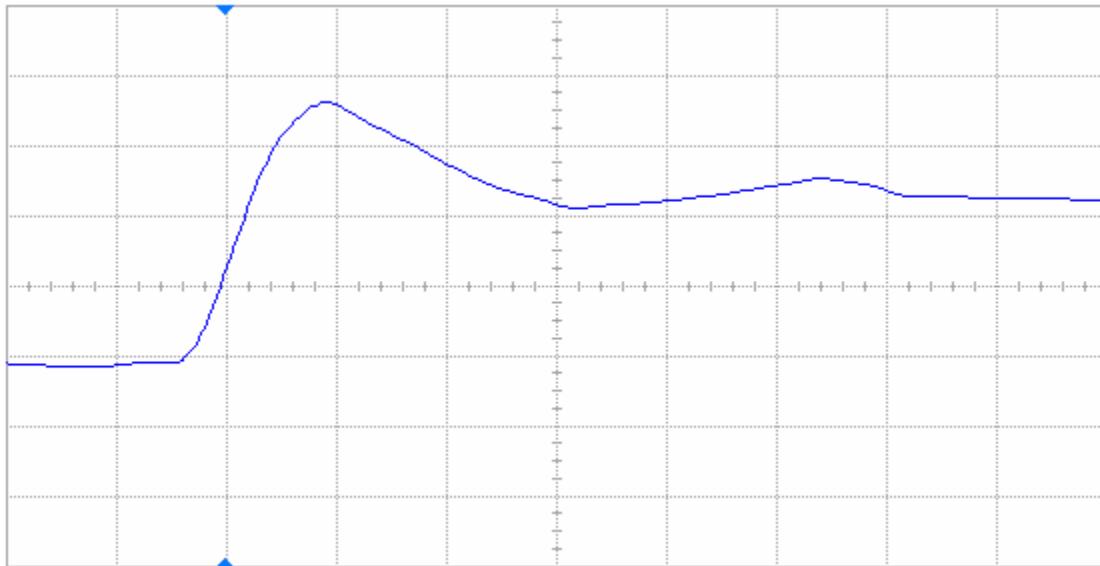


Figure 7(a) DUT 73230 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

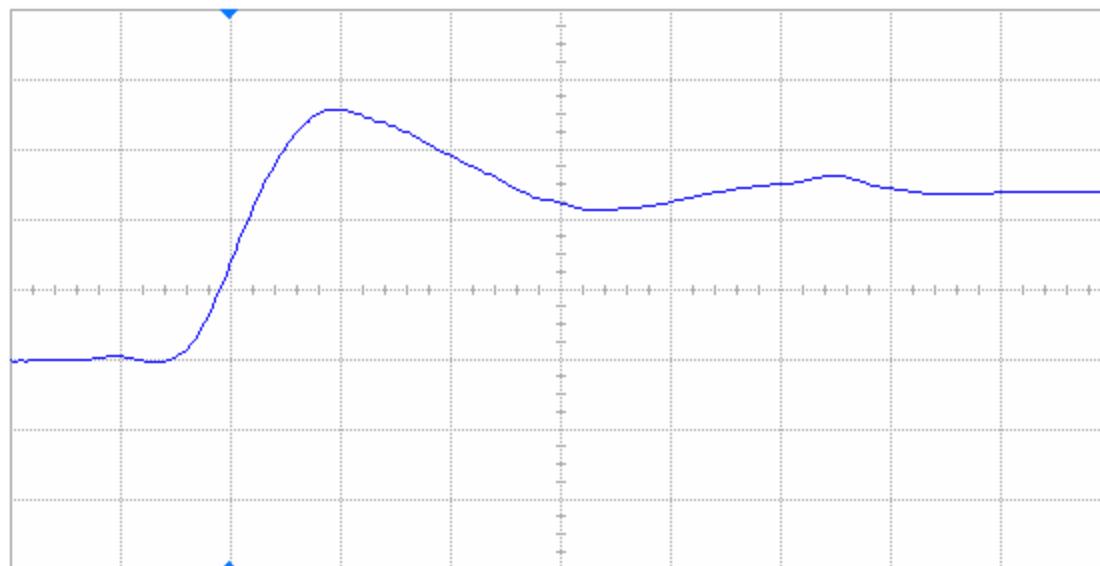


Figure 7(b) DUT 73230 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

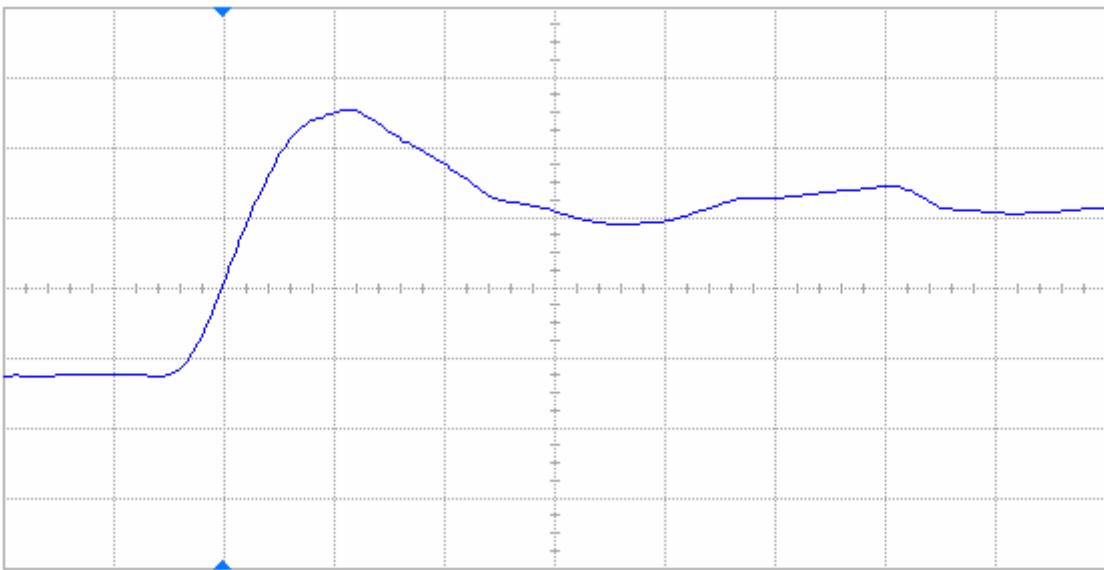


Figure 8(a) DUT 73117 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

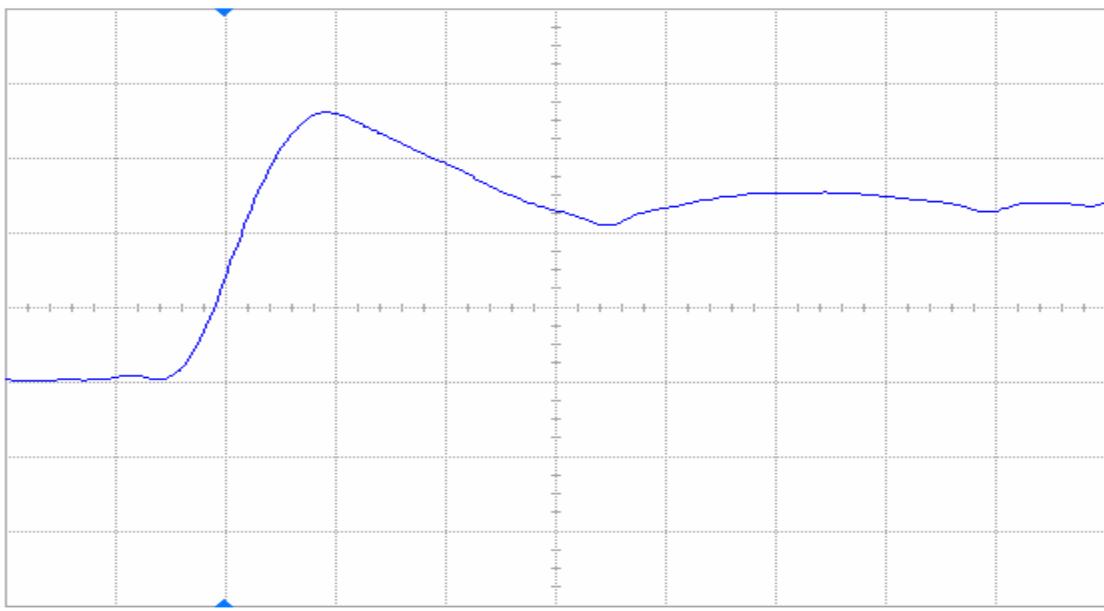


Figure 8(b) DUT 73117 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

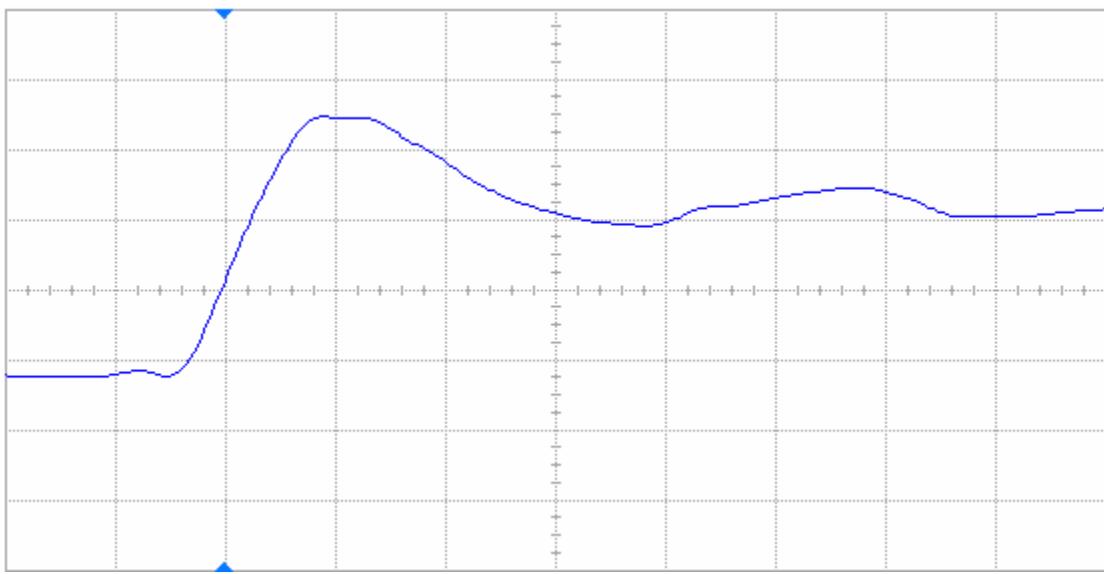


Figure 9(a) DUT 73144 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

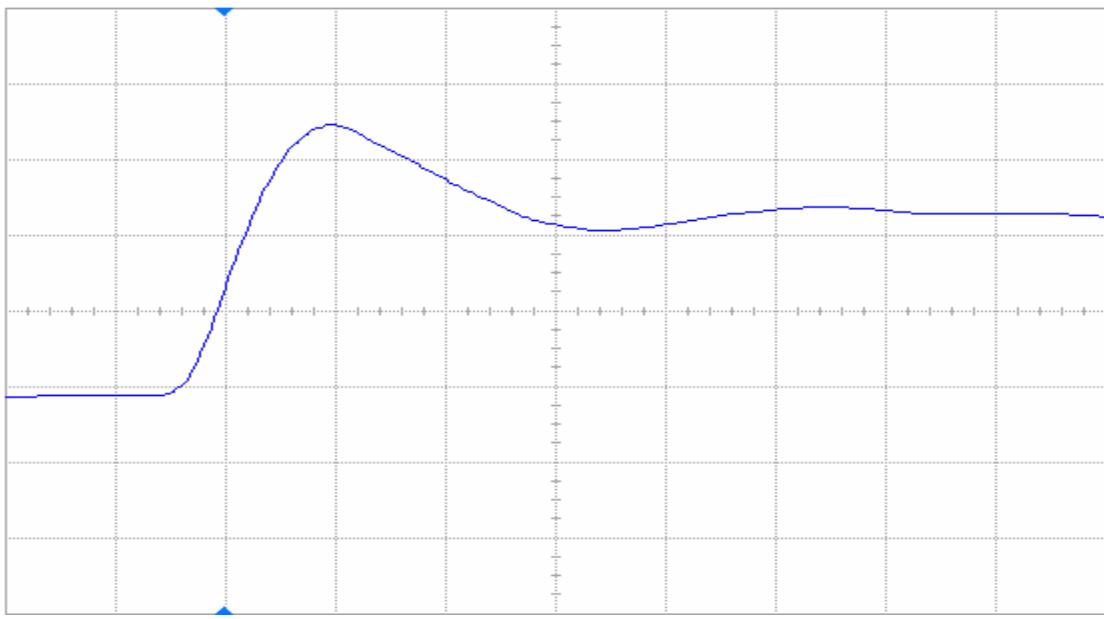


Figure 9(b) DUT 73144 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

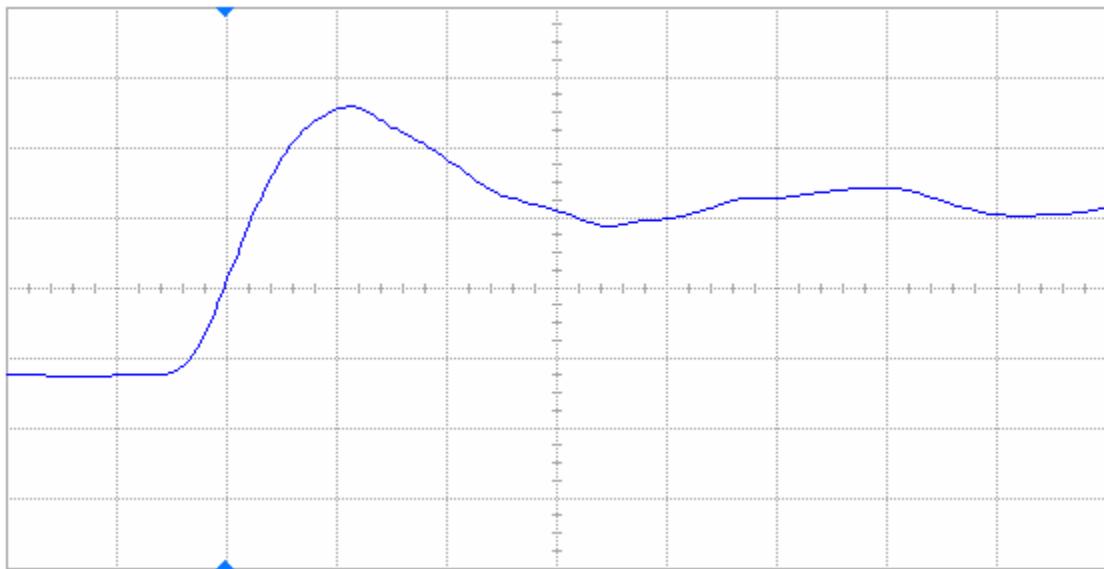


Figure 10(a) DUT 73164 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

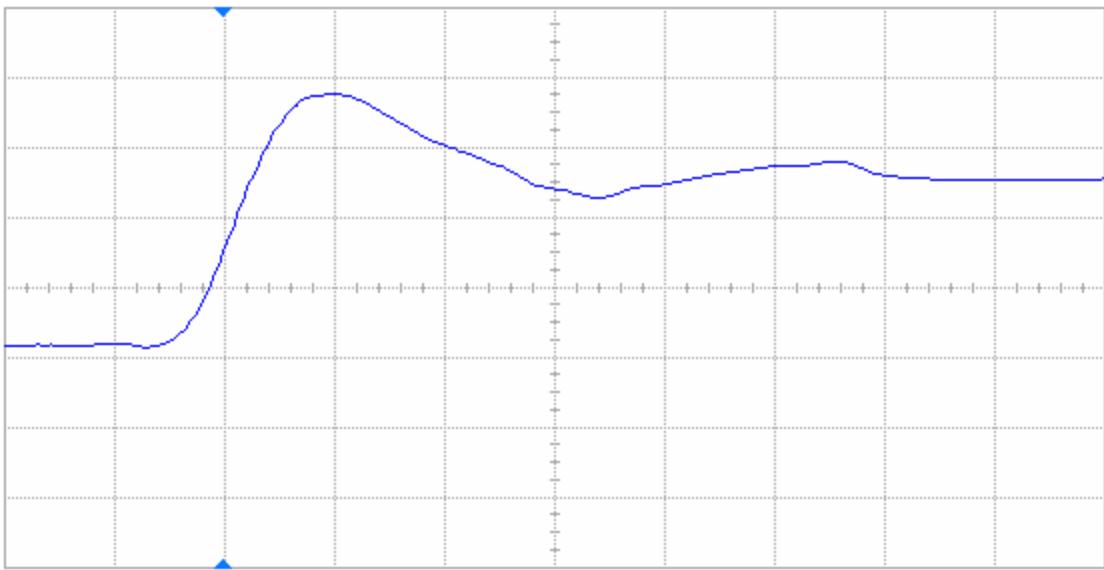


Figure 10(b) DUT 73164 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

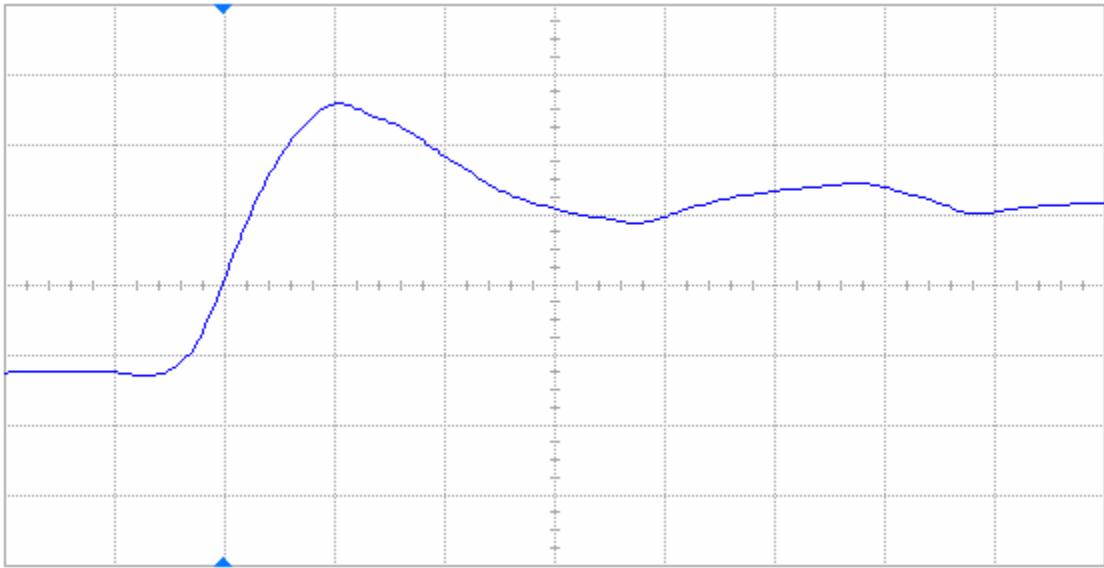


Figure 11(a) DUT 73176 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

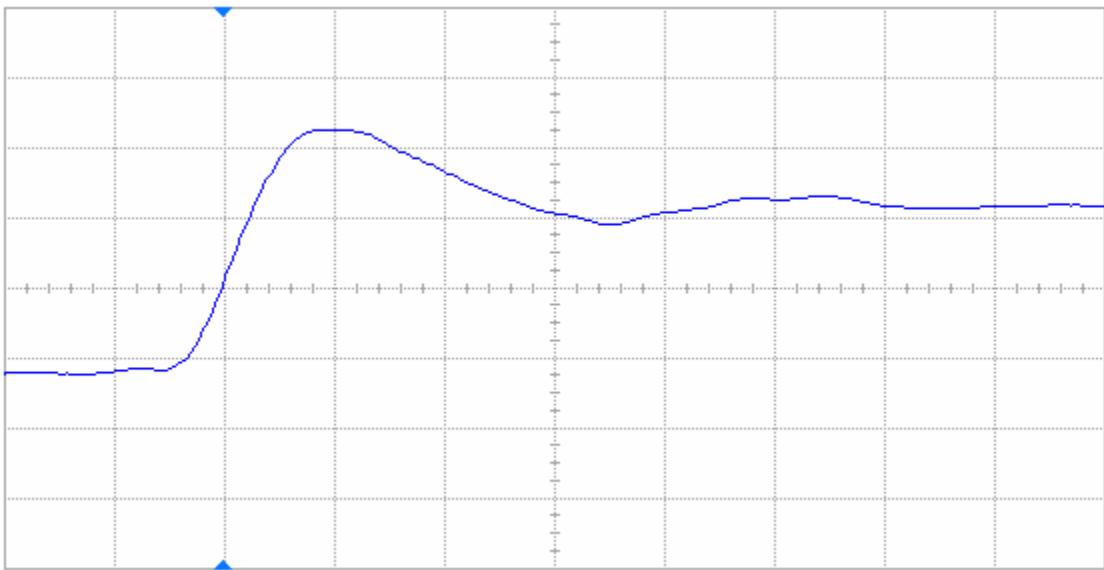


Figure 11(b) DUT 73176 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

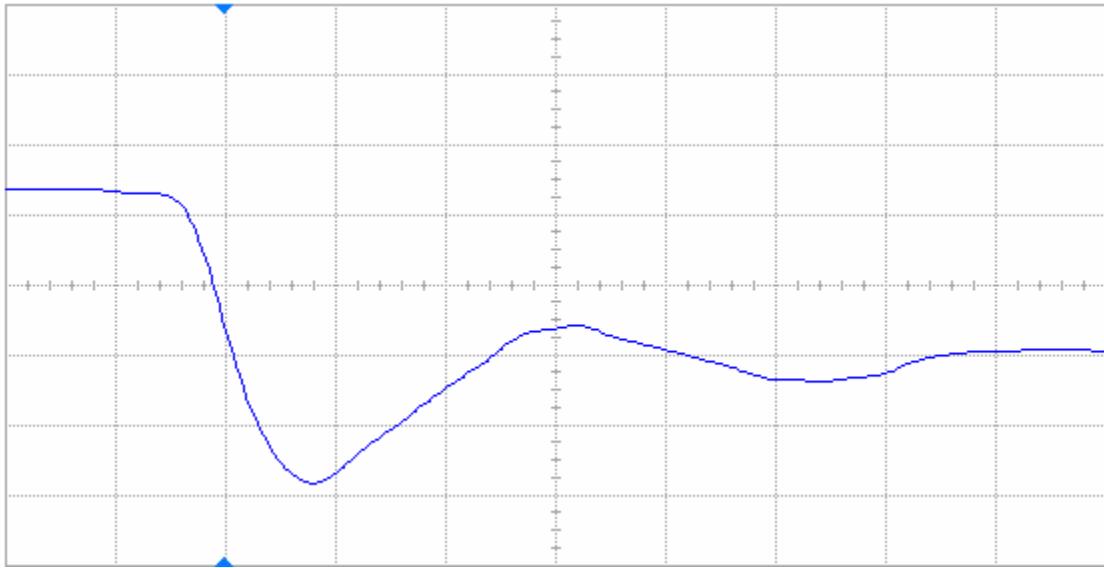


Figure 12(a) DUT 73230 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

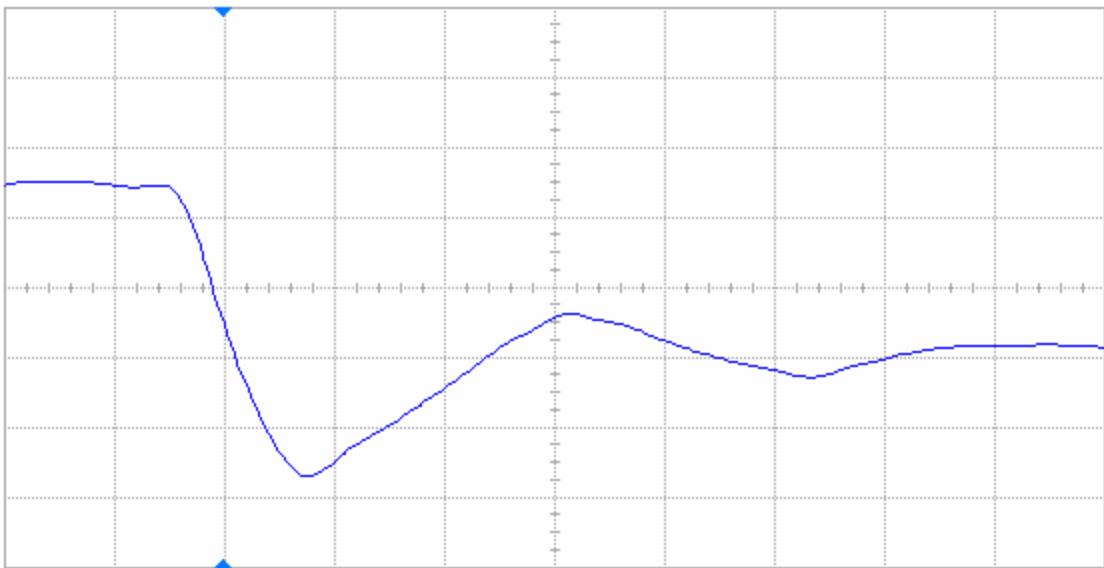


Figure 12(b) DUT 73230 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

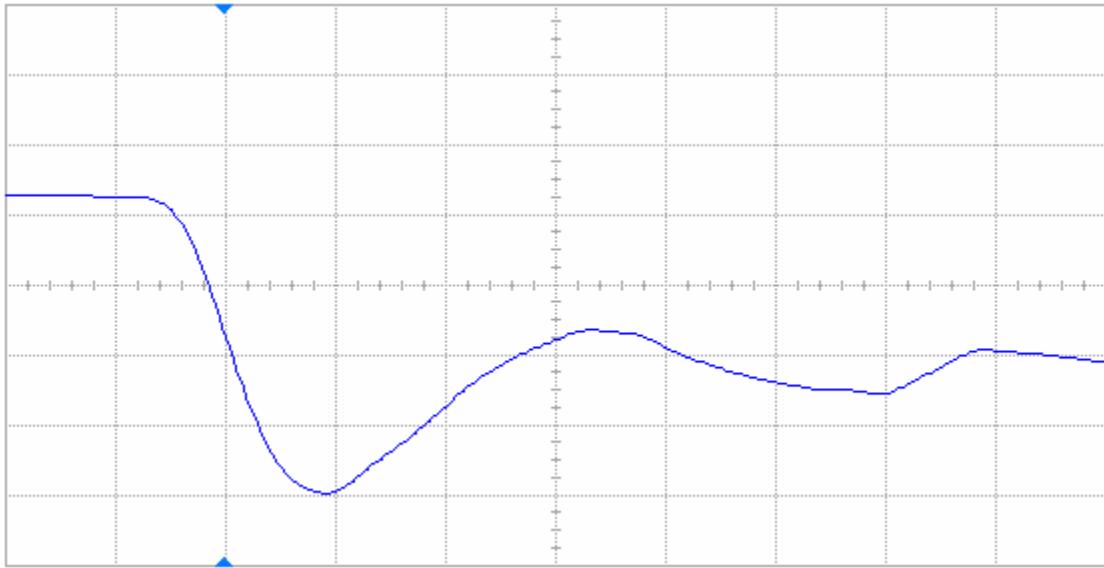


Figure 13(a) DUT 73117 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

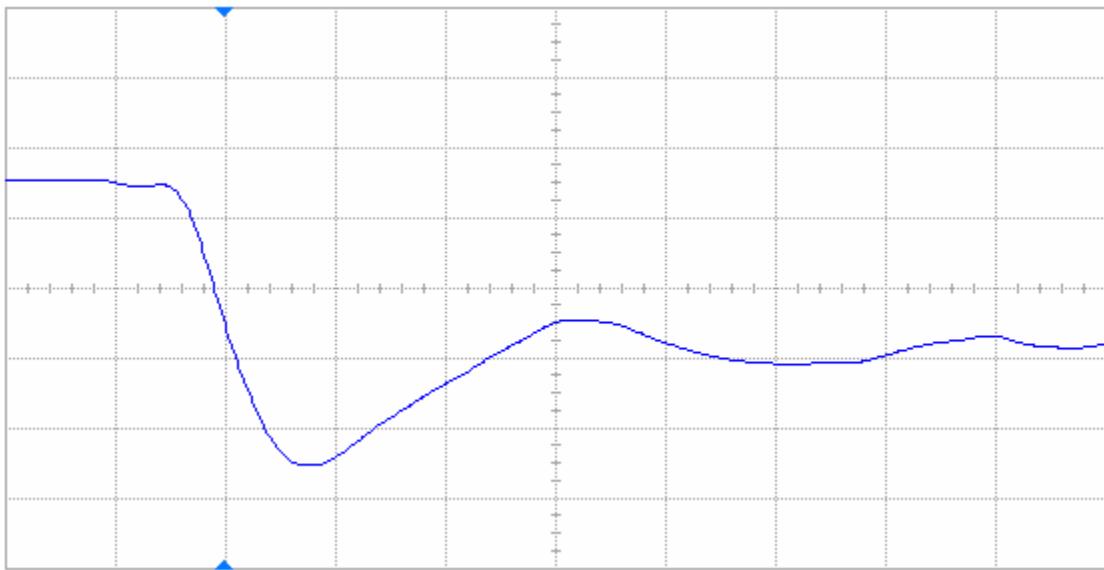


Figure 13(b) DUT 73117 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

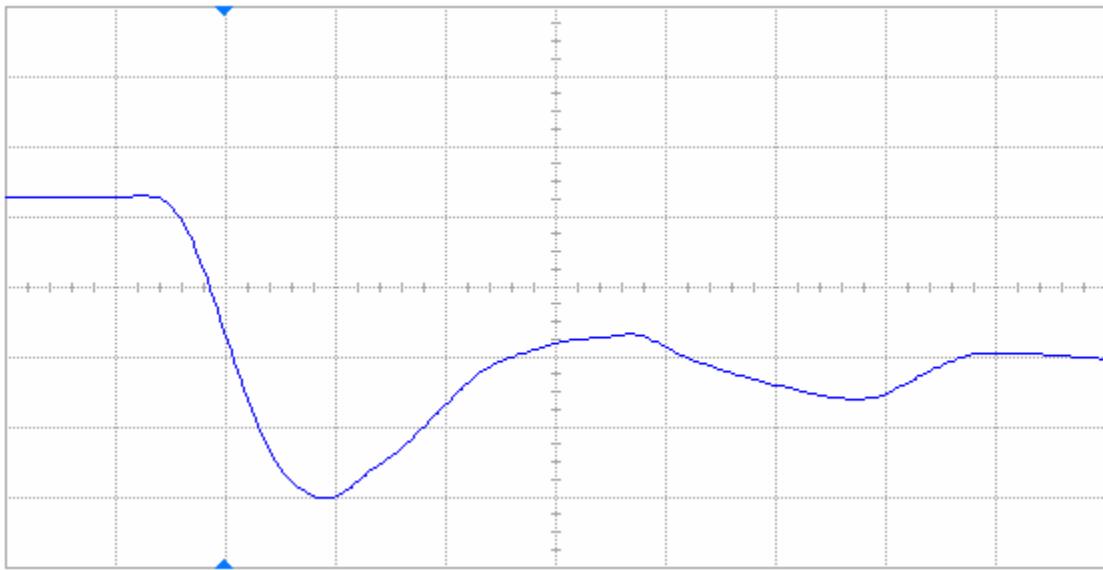


Figure 14(a) DUT 73144 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

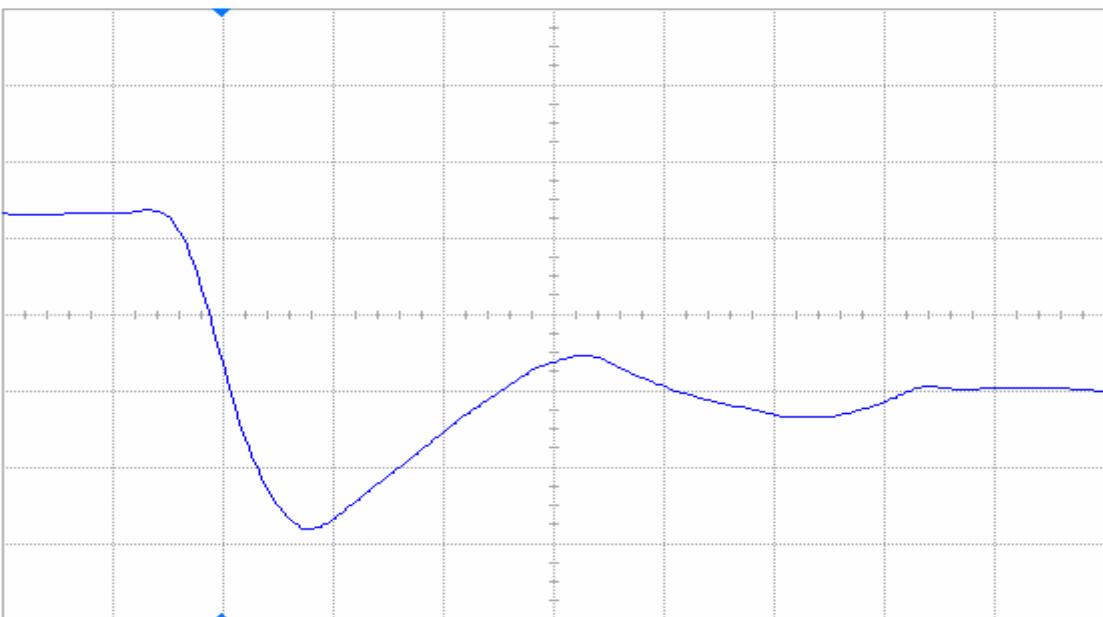


Figure 14(b) DUT 73144 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

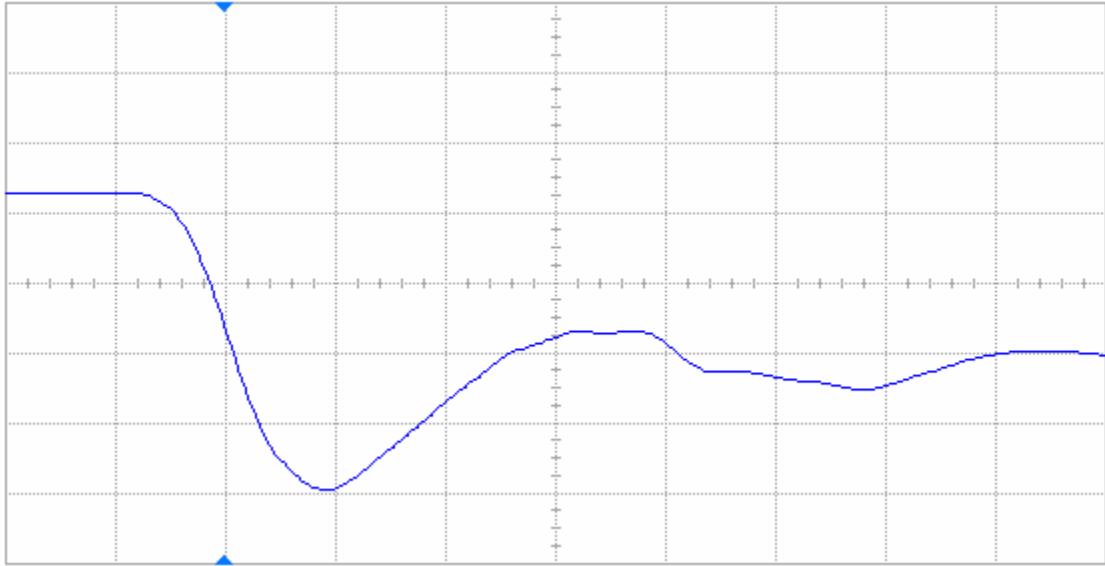


Figure 15(a) DUT 73164 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

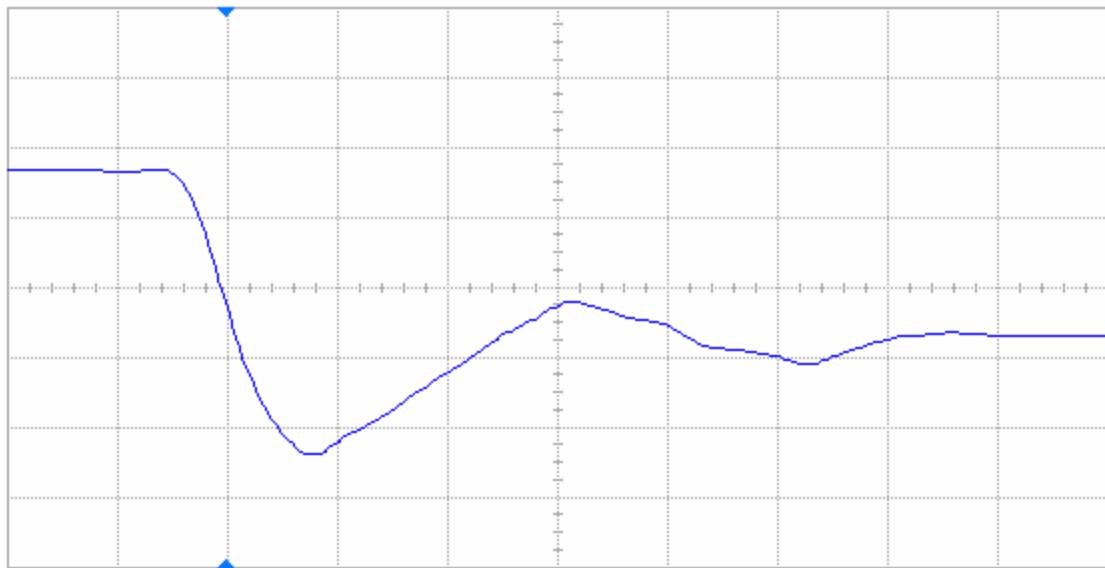


Figure 15(b) DUT 73164 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

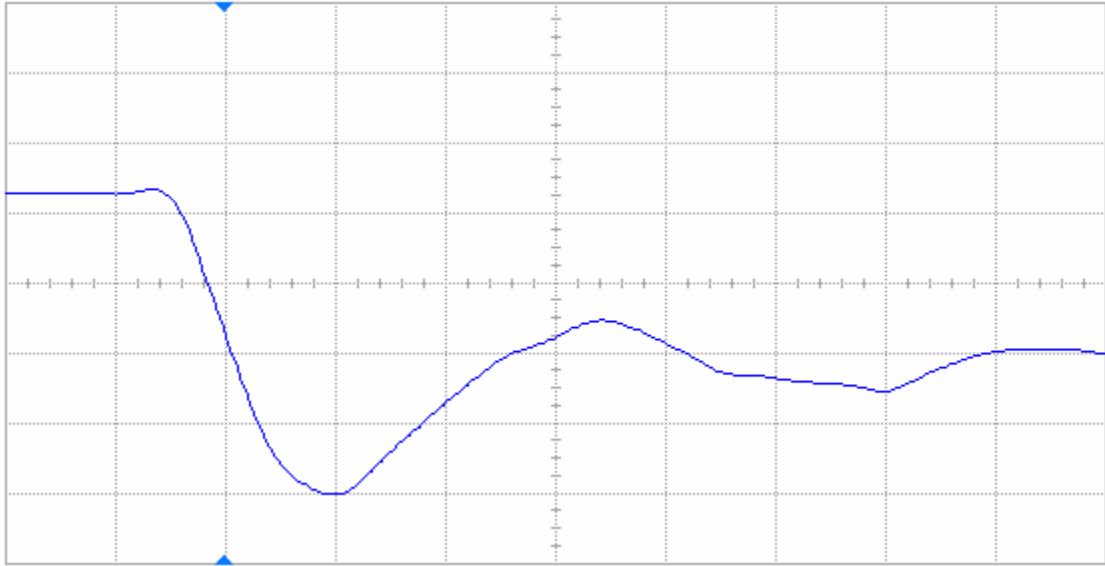


Figure 16(a) DUT 73176 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

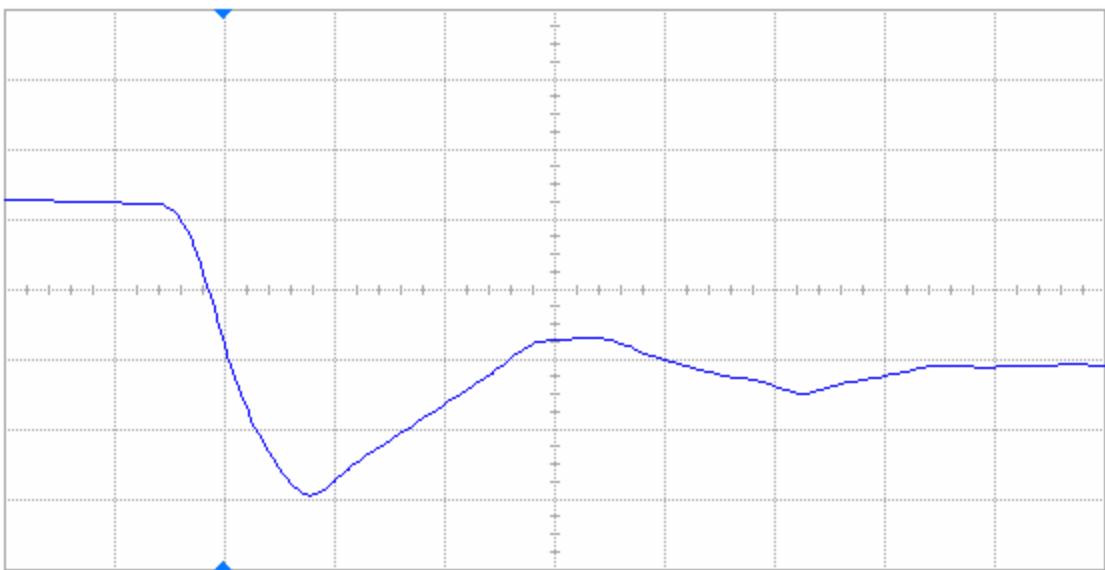
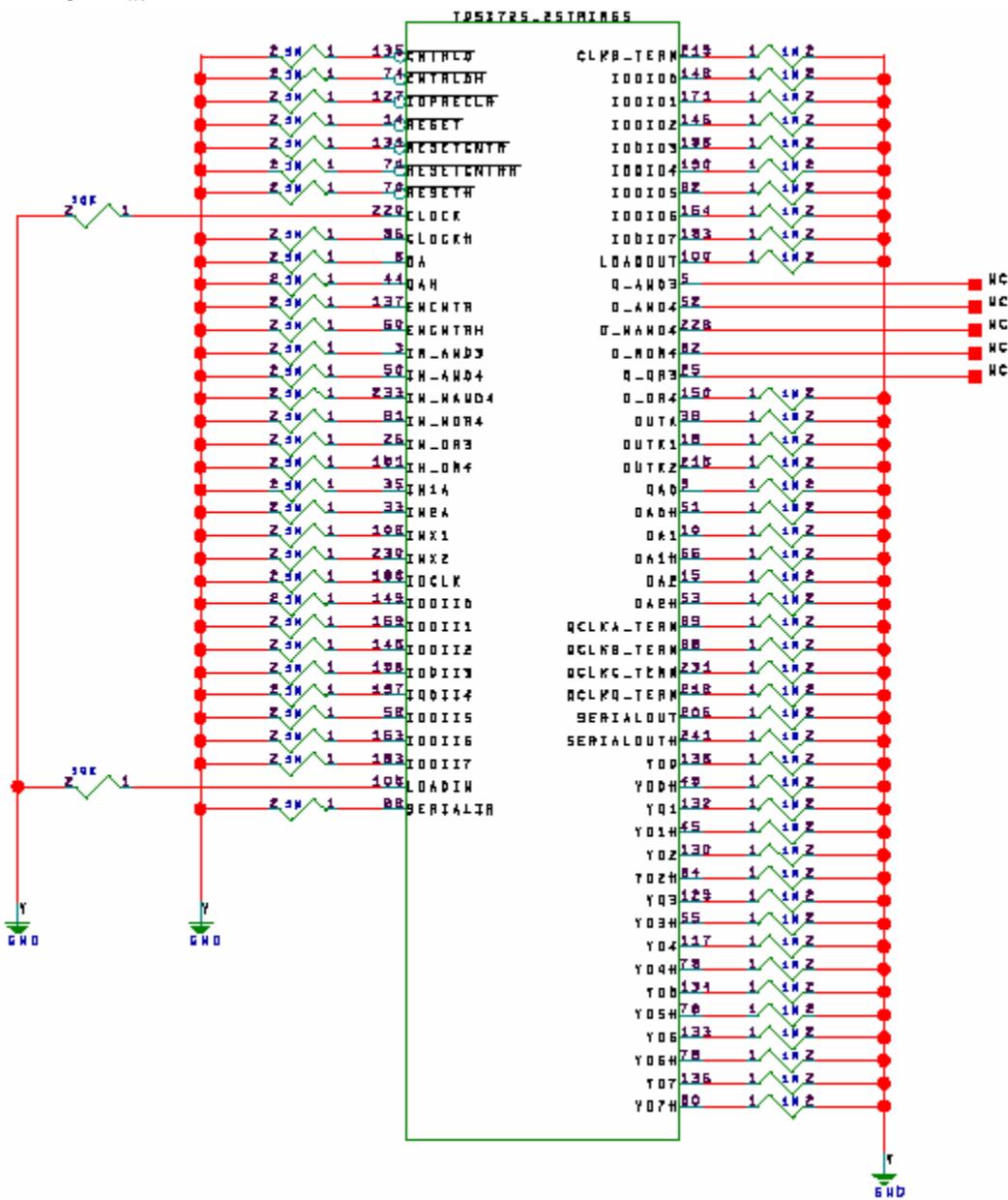
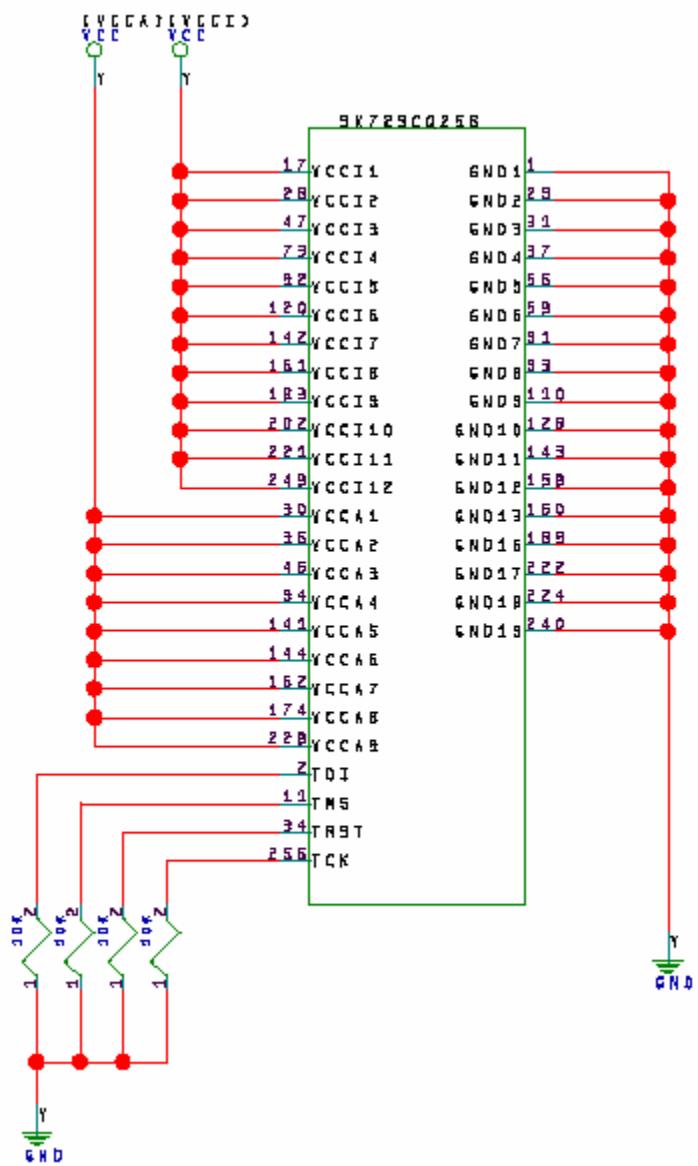


Figure 16(b) DUT 73176 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

Appendix A DUT Bias





APPENDIX B DUT DESIGN SCHEMATICS

