TOTAL IONIZING DOSE TEST REPORT

No. 02T-RT54SX32S-T25JS001-Rev 1
February 24, 2002

J.J. Wang
(408) 522-4576
jih-jong.wang@actel.com

Igor Kleyner
(301) 286-5683
igor.kleyner@gsfc.nasa.gov

I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	> 100 krad(Si), full limit TBD
2. $I_{DDSTDBY}$ (static I_{CC})	Reached 25 mA spec at ~80 krad(Si), ~50 mA at 100 krad(Si)
3. Input Threshold (V_T)	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 100 krad(Si)
6. Transition Time	Passed 100 krad(Si)
7. Power-up Transient	Passed 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT Information and Irradiation Conditions

Part Number	RT54SX32S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 µm CMOS
DUT Design	TDSX32CQFP256_4Strings
Die Lot Number	T25JS001
Quantity Tested	6
Serial Number	LAN6401, LAN6402, LAN6403, LAN6404, LAN6405, LAN6406
Radiation Facility	NASA/Goddard
Radiation Source	Co-60
Dose Rate	1 krad(Si)/hr (±10%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	5.0 V/2.5 V
IO Configuration	5V CMOS

B. Test Method

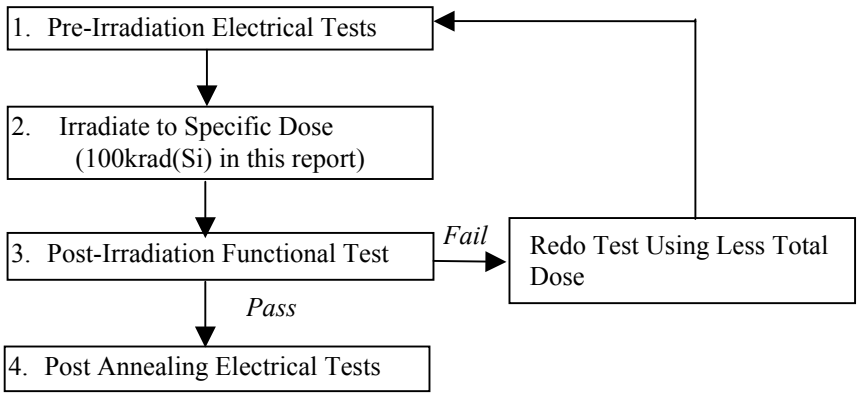


Fig 1 Parametric test flow chart.

There are two types of radiation test regularly performed by Actel. For "functional test", the DUT is irradiated to the total dose level at which the gross functional failure occurs. This total dose level is determined as the tolerance for functional failure (the first data row in the summary table). The task of testing AC/DC parameters is called "parametric test." It follows the military standard test method 1019.5. Fig 1 shows the testing flow. In a previous product (RT54SX32S) manufactured by the same 0.25 µm CMOS process, the time dependent effect (TDE) was evaluated by comparing the results between a high dose rate (1 krad(Si)/min) and a low dose rate (1 krad(Si)/hr) exposure. No adverse TDE was observed. Consequently, the accelerate aging or rebound test is omitted in this report.

C. Electrical Parameter Measurements

1) Type 1 Functional Test

All the parameters are measured in-flux. The parameters usually include I_{CC}, output voltage of combinatorial circuits and sequential circuits, and the propagation delay of a buffer string.

2) Type 2 Parametric Test

A high utilization design (in this report, TDSX32CQ256_4Strings) to address radiation reliabilities is used. Appendix A illustrates all the schematics in the design.

Table 2 lists the electrical parameters measured in the parametric test. The functionality is measured pre and post-irradiation, and also in-flux monitored on the output pin (O_AND3 or O_AND4) of the two global combinatorial buffer-strings. The I_{CC} is measured in-flux, statically on the power supply (I_{CC}). The sampling rate is every 5 or 10 minutes. The input logic threshold (V_T) and output drives (V_{OH}/V_{OL}) are measured pre and post-irradiation on a combinatorial net, input pin DA to output pin QA0. The propagation delay is measured pre and post-irradiation and also in-flux on one of the global combinatorial buffer string with 500 buffers, input pin LOADIN to output pin O_AND4. The transient time is measured pre and post-irradiation on the same design. The global combinatorial buffer strings are controlled by clocked D flip-flops during the propagation delay and transient measurements. Power up transient test measures the I_{CCA} when the V_{CCA} is ramping with V_{CCI} powered (5.0 V in this case).

During irradiation, the unused input is grounded with a 10,000 Ω resistor.

Table 2. Logic Design for Parametric Test

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC}	DUT power supply
3. Input Threshold (V_T)	Input buffer (pin DA to QA0)
4. Output Drives (V_{OH}/V_{OL})	Output buffer (pin QA0)
5. Propagation Delays	String of 500 buffers (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)
7. Power-up Transient	DUT power supply

III. Test Results

A. Type-1 Functional Test

This type test was not performed.

B. Type-2 Parametric Test

1) Functionality

Fig 2, 3, and 4 show the in-flux output of the functionality test circuit for every DUT. In each case, the degradation after 100 krad(Si) irradiation is negligible. The pre and post-irradiation functional tests also show no detectable radiation degradation on each DUT.

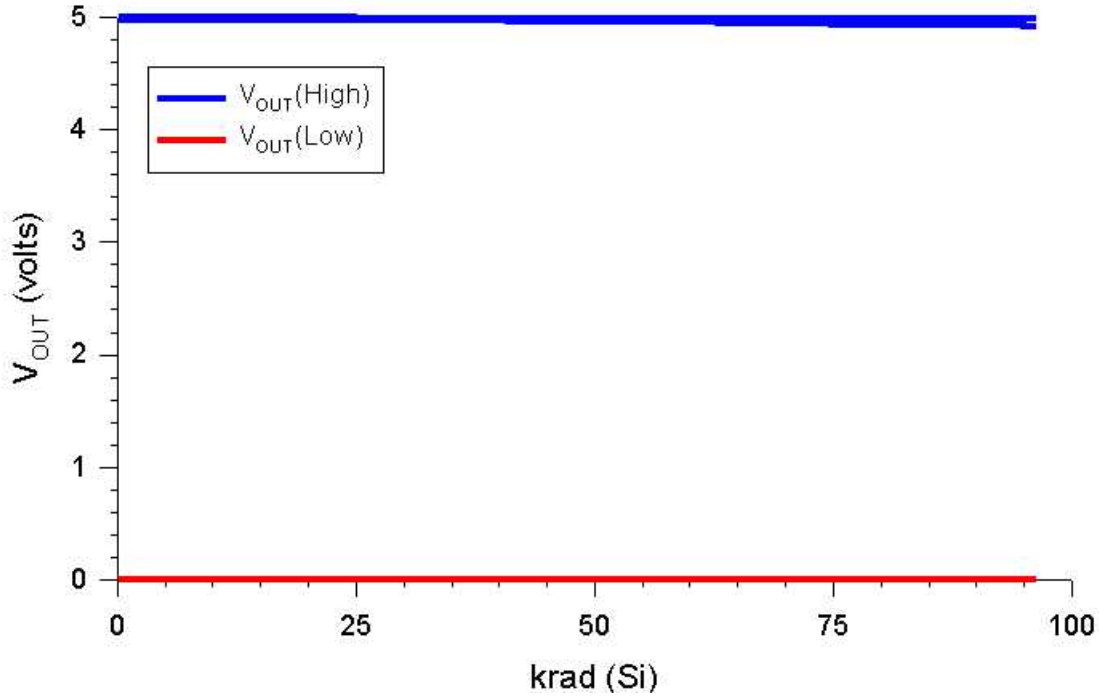


Fig 2 In-flux V_{OUT} of the functionality test circuit in LAN6401 and LAN6402

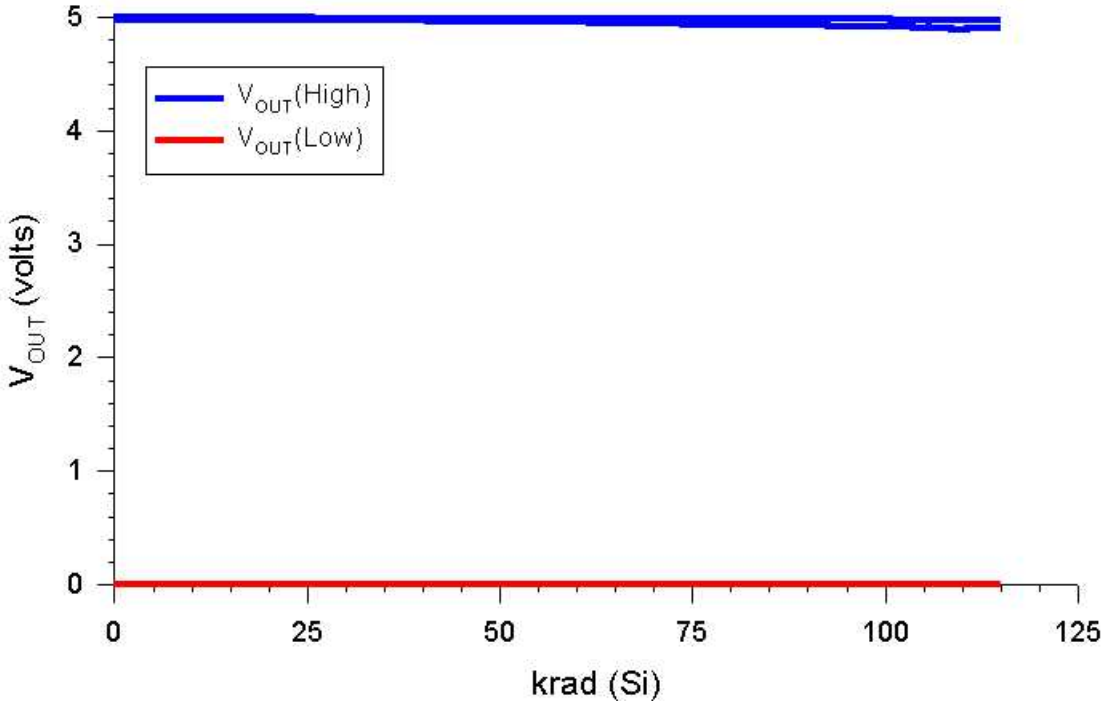


Fig 3 In-flux V_{OUT} of the functionality test circuit in LAN6403 and LAN6404

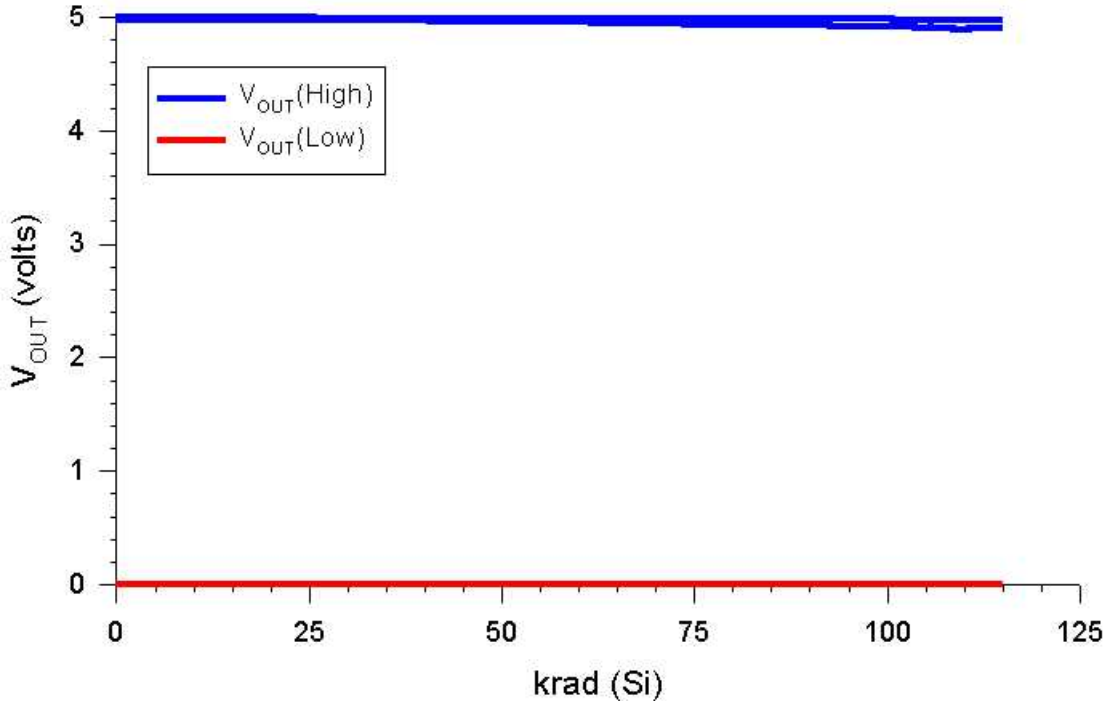


Fig 4 In-flux V_{OUT} of the functionality test circuit in LAN6405 and LAN6406

2) In-Flux I_{CC}

Fig 5, 6 and 7 show the in-flux I_{CC}. In this design, only I_{CCA} shall be monitored because I_{CCI} is mainly from the test board. However, the radiation induced I_{CCI} is minute comparing to that of the I_{CCA}. Monitoring I_{CCA} should be sufficient. In Fig 5, the transient peak in I_{CCA} curves for LAN6401 or LAN6402 is due to a testing error. An unused clock input was accidentally left floating, causing CMOS transition current in input buffering circuit. These peaks should be ignored.

Table 3 lists, for each DUT, the total dose level at which I_{CCA} reaches the spec limit of 25 mA.

Table 3 Total Dose level at which I_{CCA} = 25 mA

DUT	Total Dose @ I_{CCA} = 25 mA
LAN6401	87 krad(Si)
LAN6402	87 krad(Si)
LAN6403	84 krad(Si)
LAN6404	90 krad(Si)
LAN6405	82 krad(Si)
LAN6406	83 krad(Si)

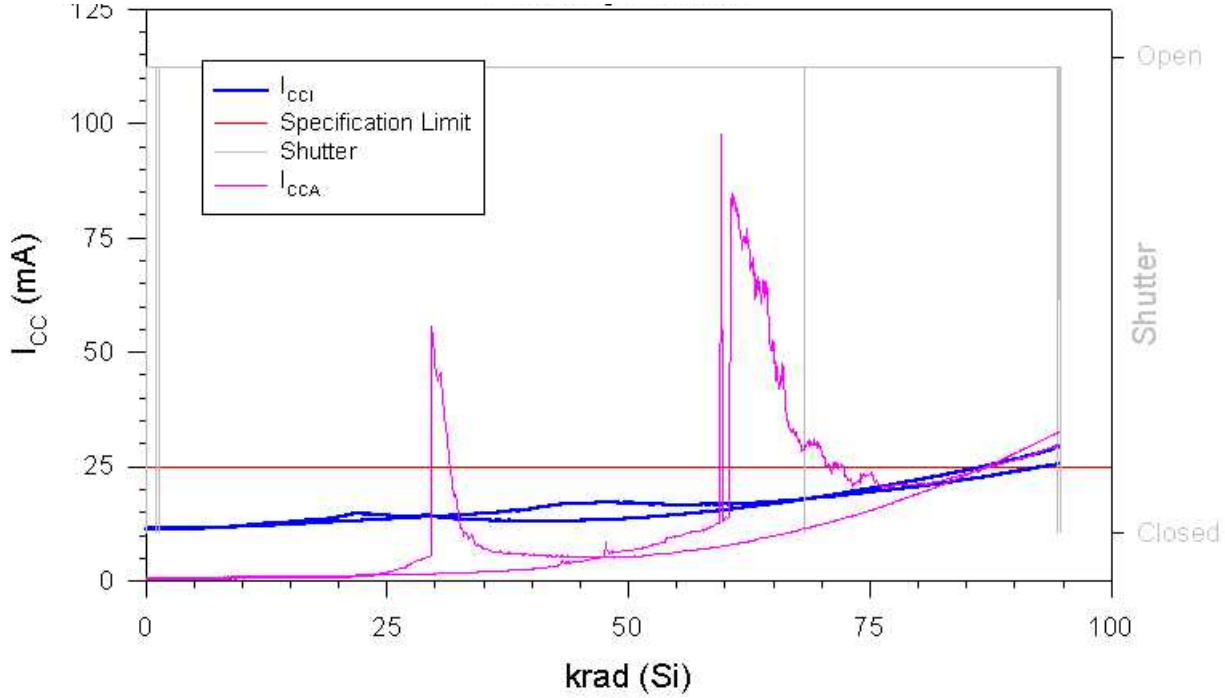


Fig 5 In-flux I_{CC} of LAN6401 and LAN6402

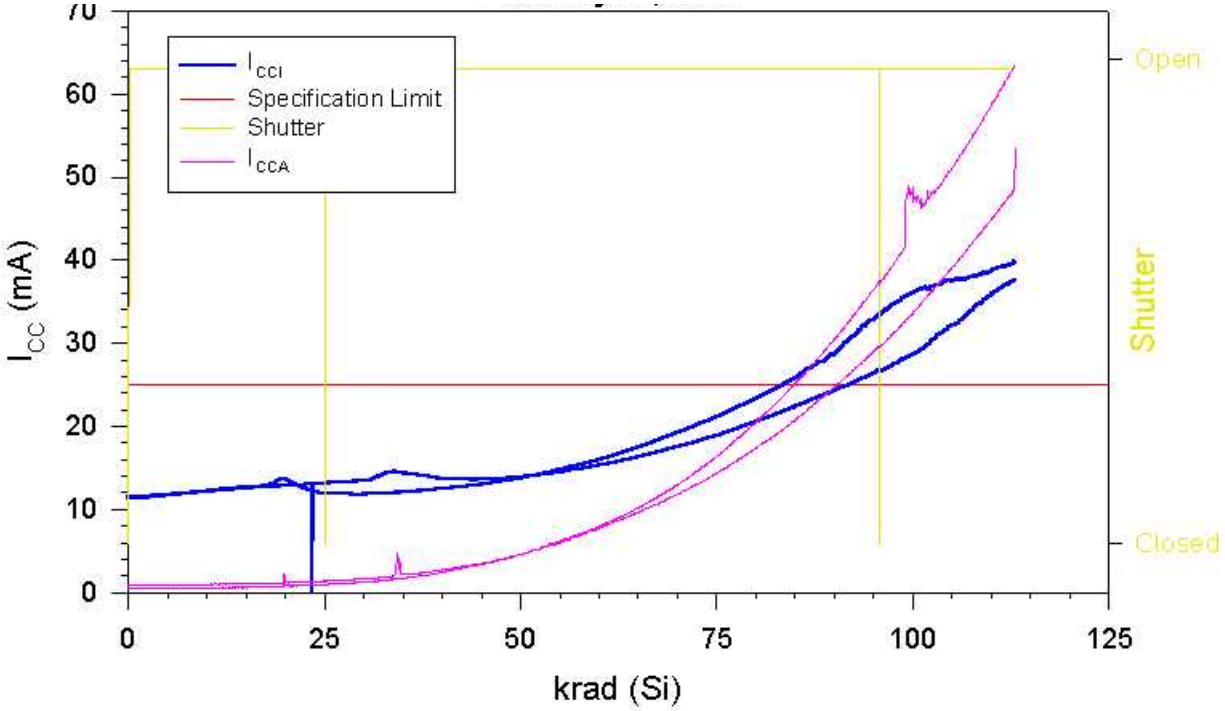


Fig 6 In-flux I_{CC} of LAN6403 and LAN6404

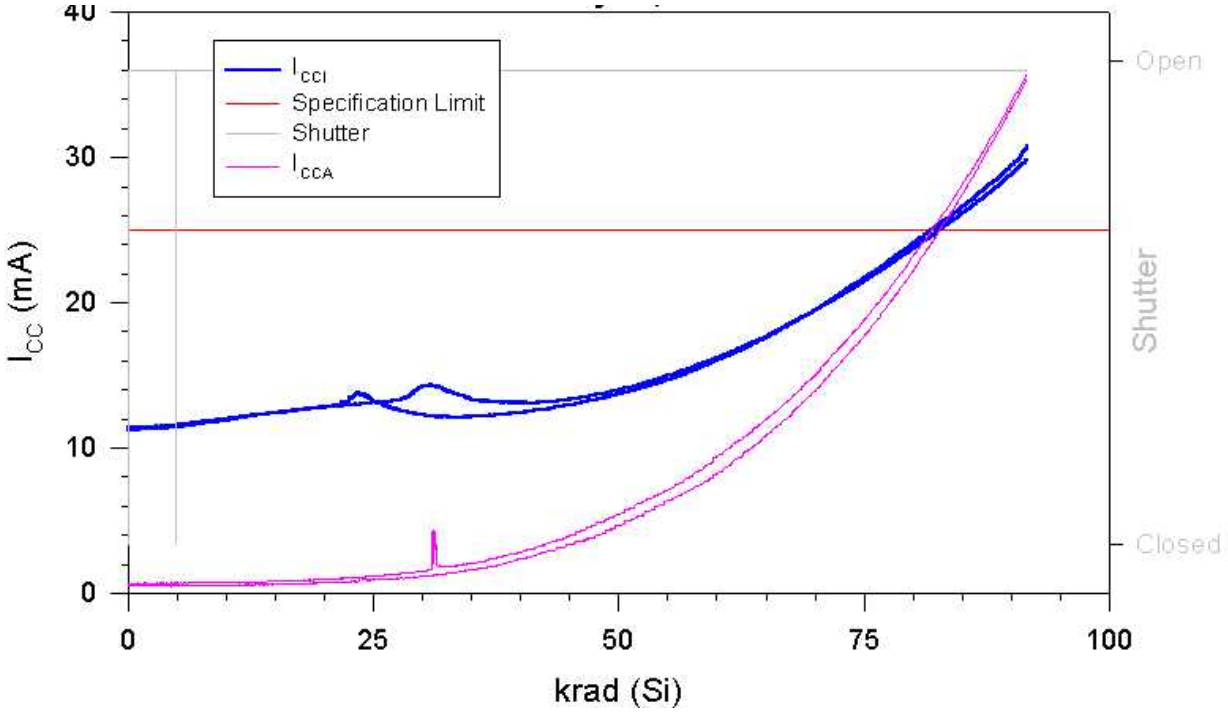


Fig 7 In-flux I_{CC} of LAN6405 and LAN6406

3) Input Logic Threshold

Table 4 lists the pre and post-irradiation input logic threshold of each DUT. The radiation effect is negligible.

Table 4 Pre and Post-Irradiation Input Logic Threshold (V_{IL}/V_{IH})

	Pre-Irradiation	Post-Irradiation
LAN6401	2.8 V	2.8 V
LAN6402	2.8 V	2.8 V
LAN6403	2.8 V	2.8 V
LAN6404	2.8 V	2.8 V
LAN6405	2.8 V	2.8 V
LAN6406	2.8 V	2.8 V

4) Output Characteristics

Fig 8 and 9 shows the pre and post-irradiation V_{OH} characteristics for every DUT. In every case, the degradation after 100 krad(Si) irradiation is negligible. The pre and post-irradiation of V_{OL} of every DUT were also measured with negligible radiation effects.

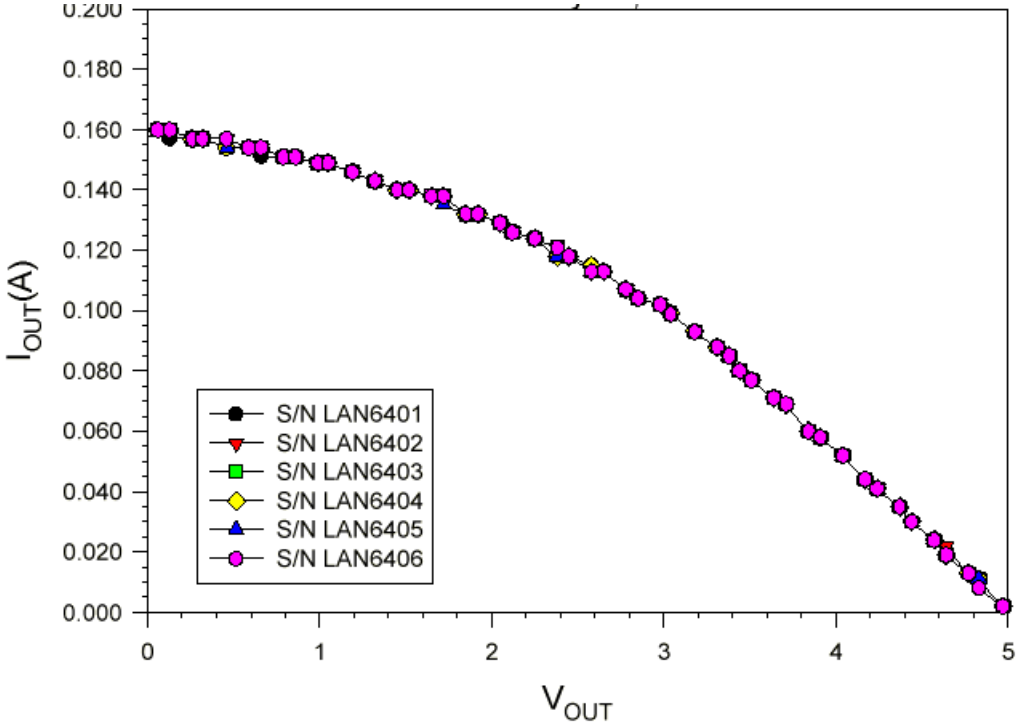


Fig 8 Pre-irradiation V_{OH} characteristic curves for every DUT

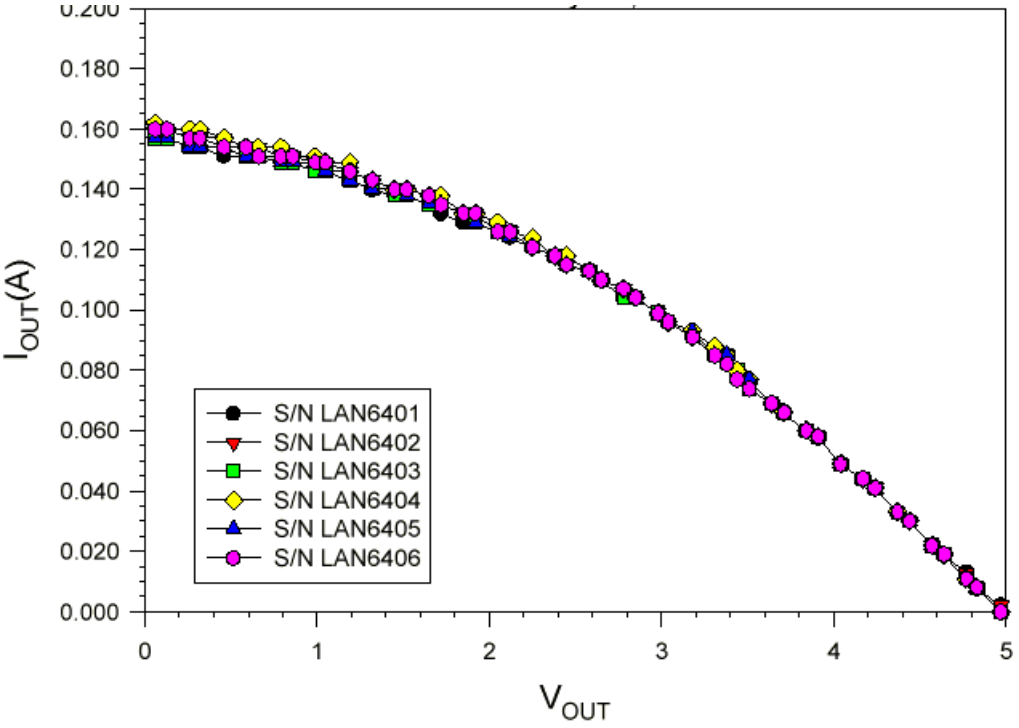


Fig 9 Post-irradiation V_{OH} characteristic curves for every DUT

5) Propagation Delays

Table 5 lists the pre and post-irradiation propagation delays and radiation-induced degradations in percentages. Note that LAN6403 and LAN6404 were irradiated to 115 krad(Si). In each case, the degradation is within the typical 10% guard-band margin. Fig 10, 11 and 12 shows the in-flux propagation delay curve of LAN6401, LAN6403 and LAN6405 respectively.

Table 5 Propagation delays (ns)

DUT	Rising Output			Falling Output		
	Pre-Irrad	Post-Irrad	Degradation	Pre-Irrad	Post-Irrad	Degradation
LAN6401	379	396	4.48%	324	340	4.94%
LAN6402	372	393	5.64%	320	333	4.06%
LAN6403	370	395	6.76%	327	338	3.36%
LAN6404	367	386	5.18%	314	330	5.10%
LAN6405	377	392	3.98%	332	340	2.41%
LAN6406	381	402	5.51%	318	333	4.72%

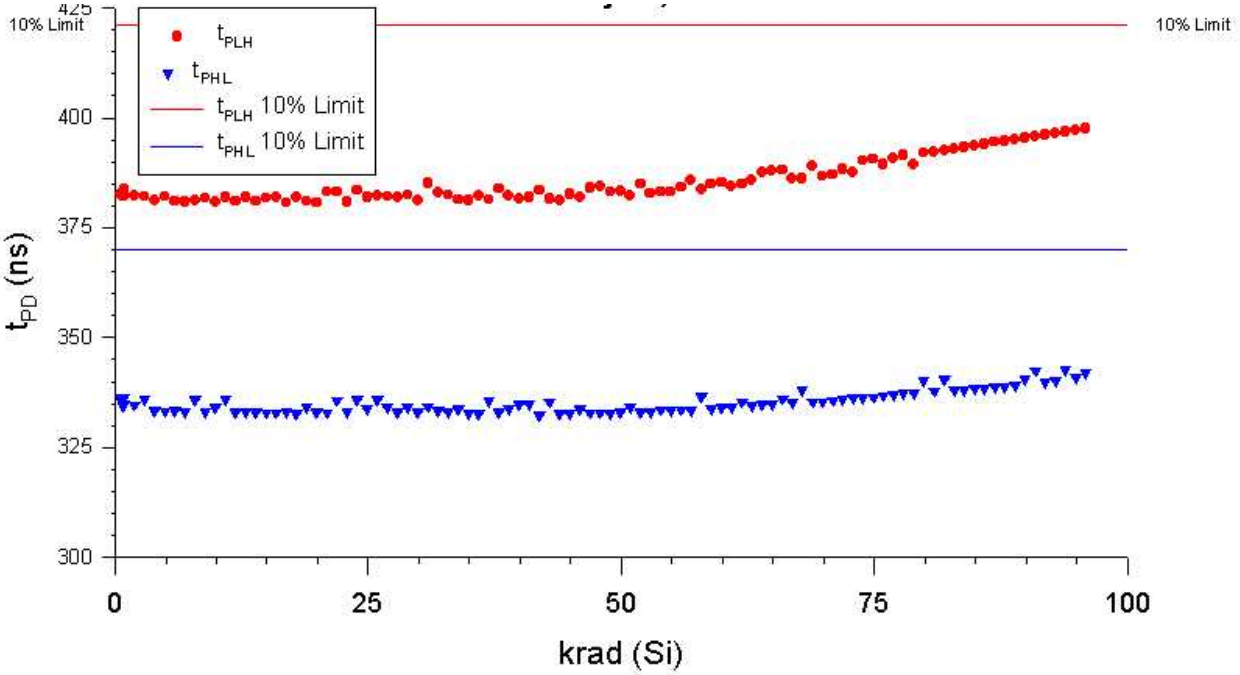


Fig 10 In-flux propagation delay of LAN6401

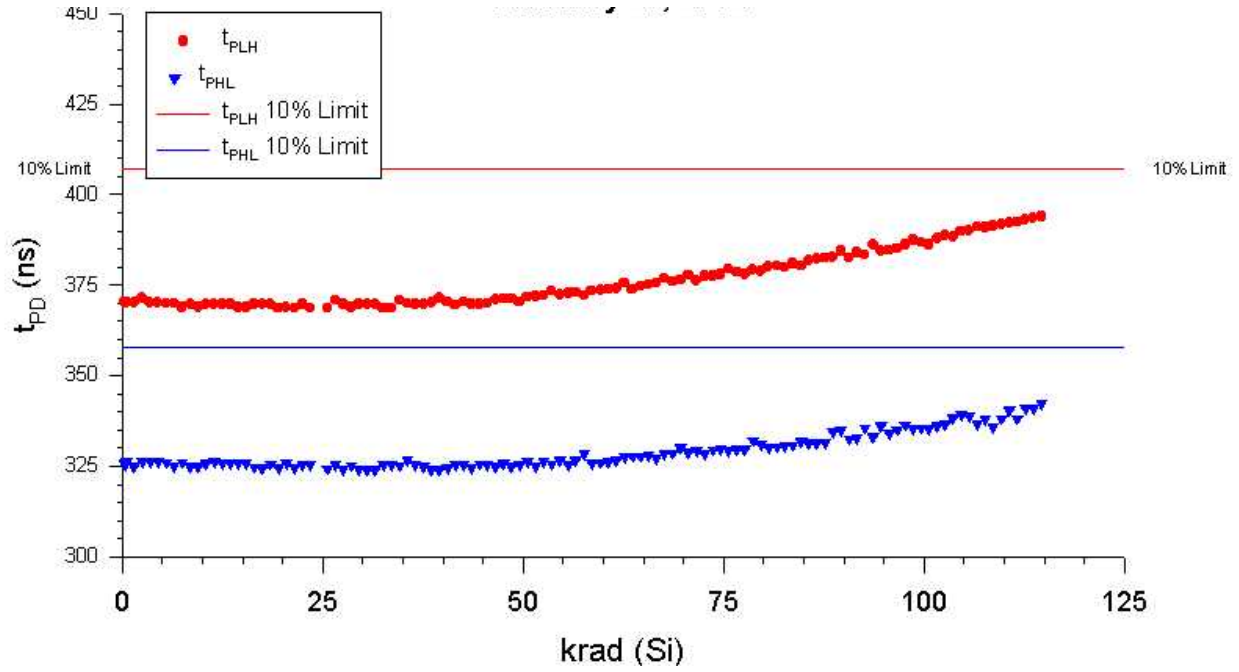


Fig 11 In-flux propagation delay of LAN6403

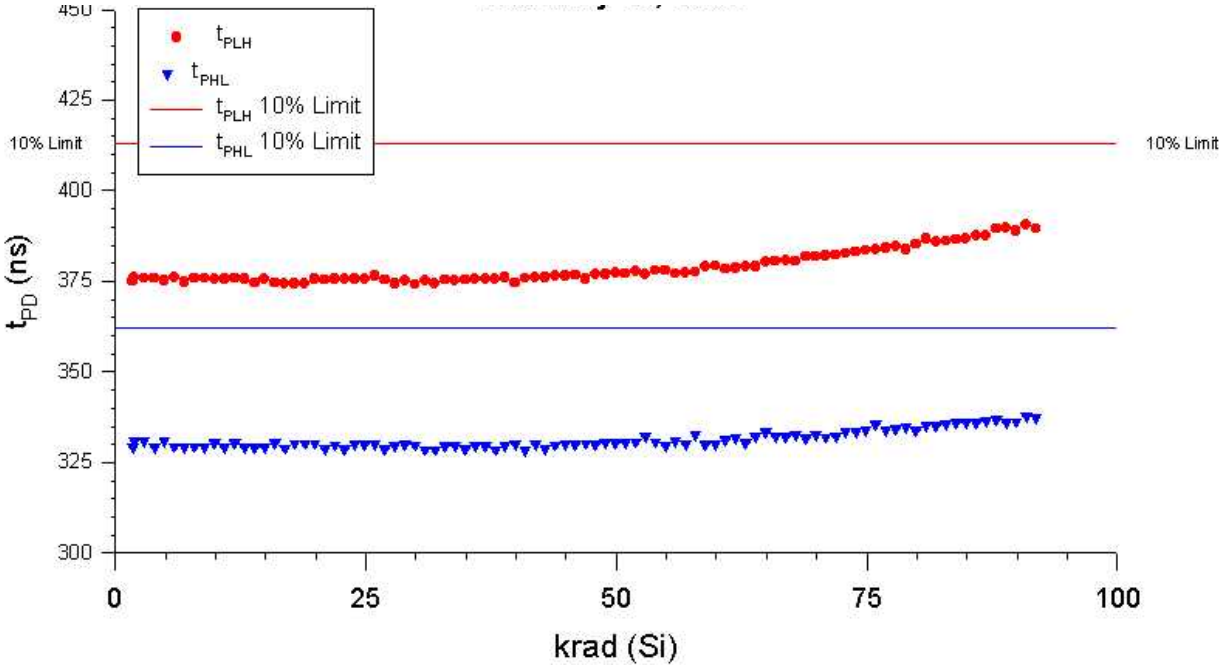


Fig 12 In-flux propagation delay of LAN6405

6) Transition Time

The pre and post-irradiation rising and falling time of every DUT were measured. Fig 13 shows a typical rising edge. In every DUT, the post-irradiation rising edge is approximately the same as that of the pre-irradiation. No visible radiation effect can be detected. Fig 14 shows a typical falling edge. Again, there is no detectable radiation effect on it either.

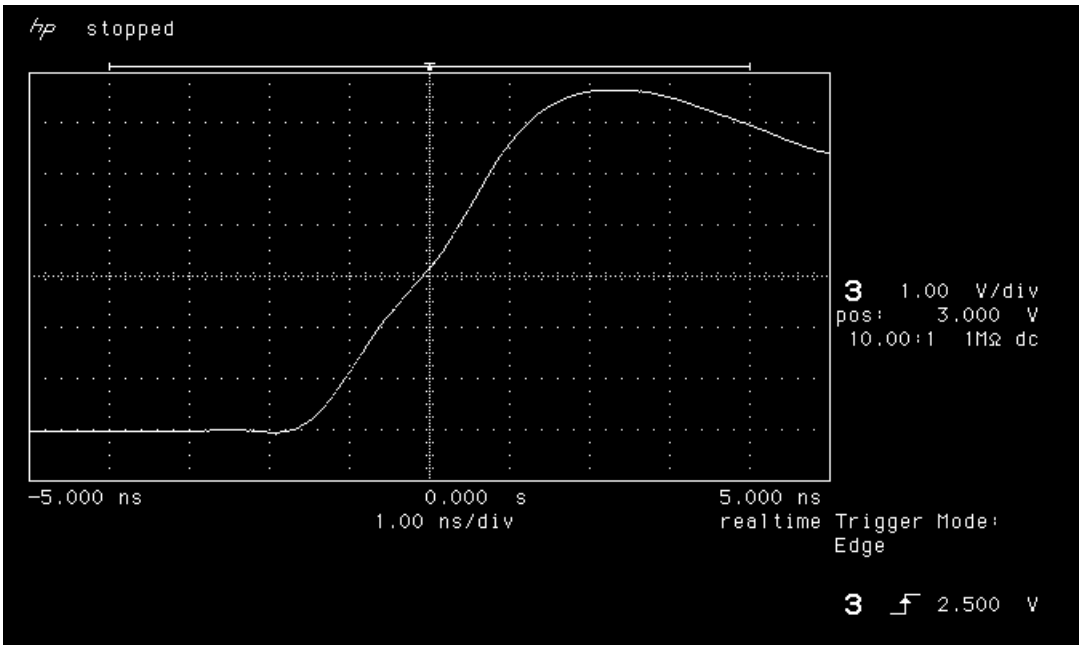


Fig 13 A typical rising edge in one of the DUT

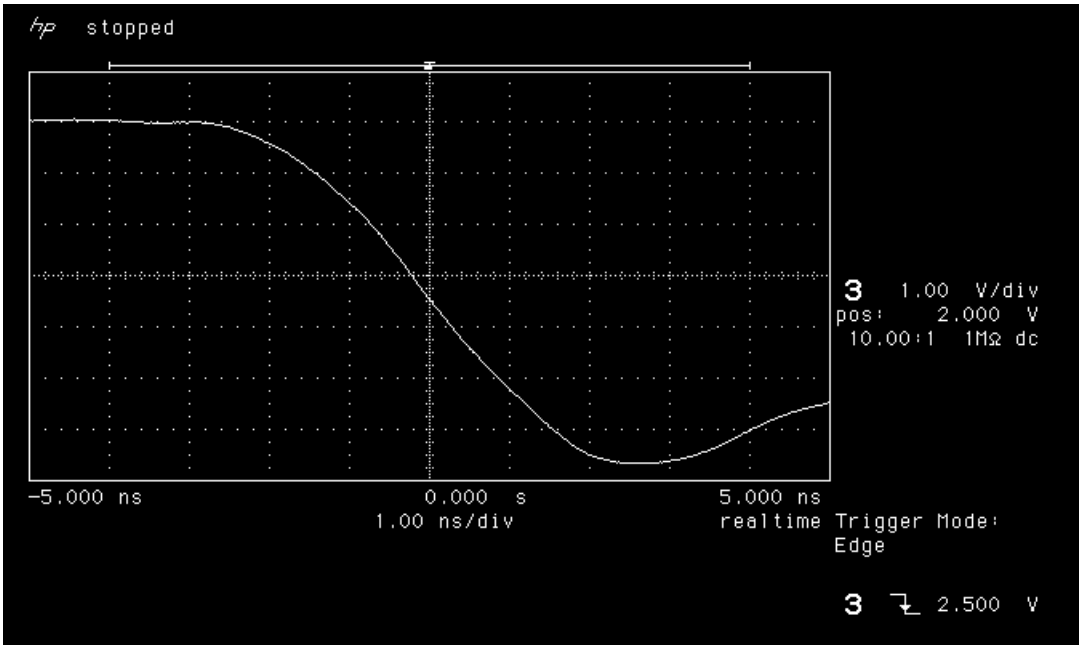


Fig 14 A typical falling edge in one of the DUT

7) Power-Up Transient

Fig 15a and b shows the typical power-up transient pre and post-irradiation respectively. The ramping curve is V_{CCA} with 1 V per division. The other curve is I_{CCA} with 100 mA per division. No significant transient can be observed either pre or post-irradiation in any DUT.

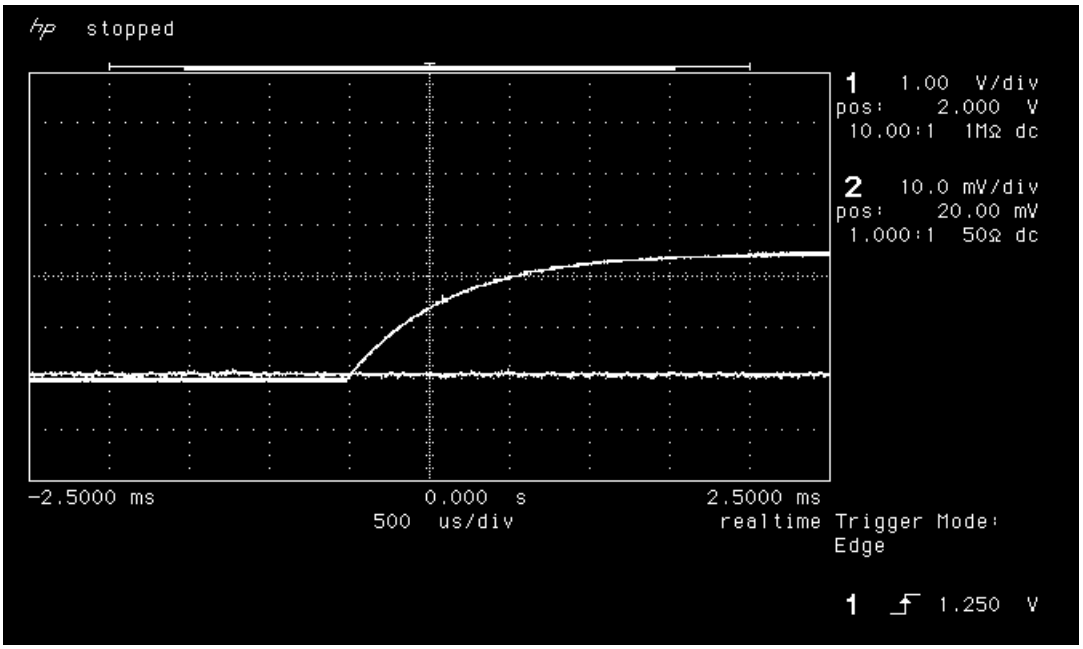


Fig 15a A typical pre-irradiation power up transient in one of the DUT

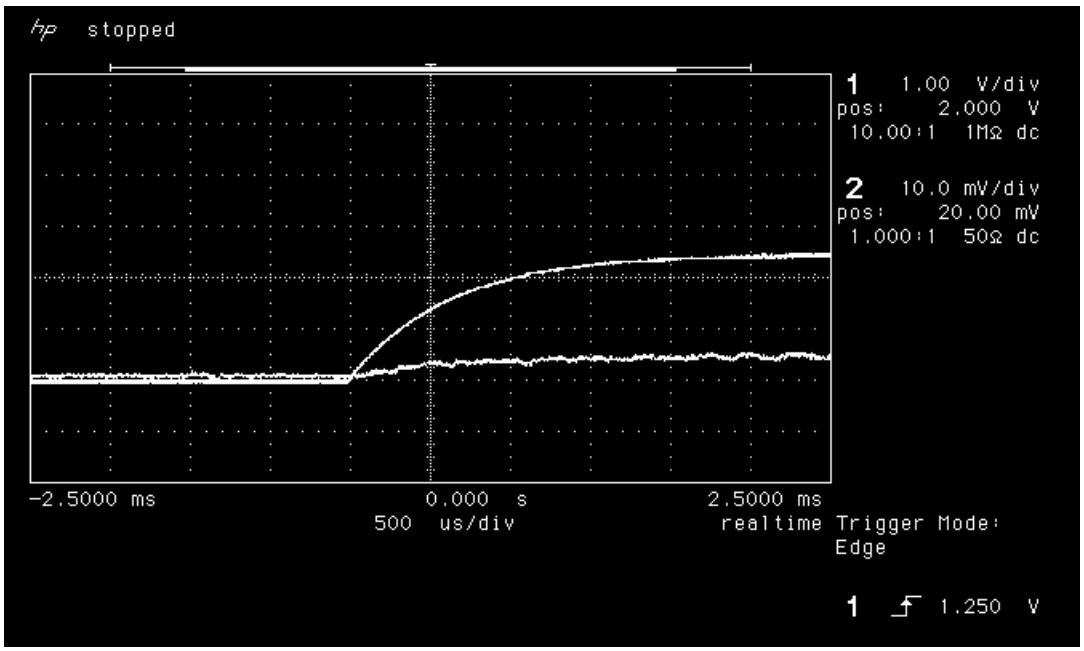
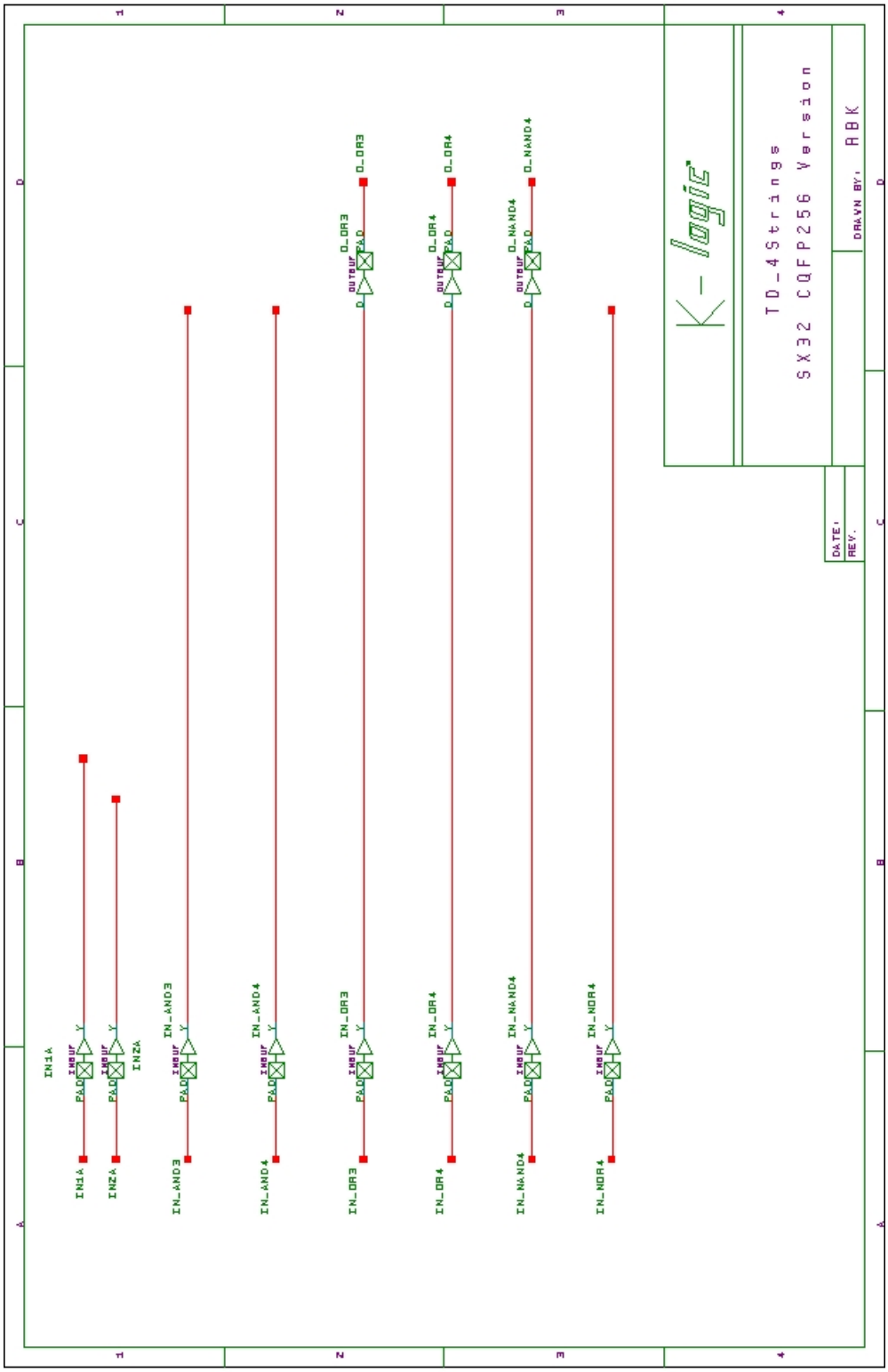
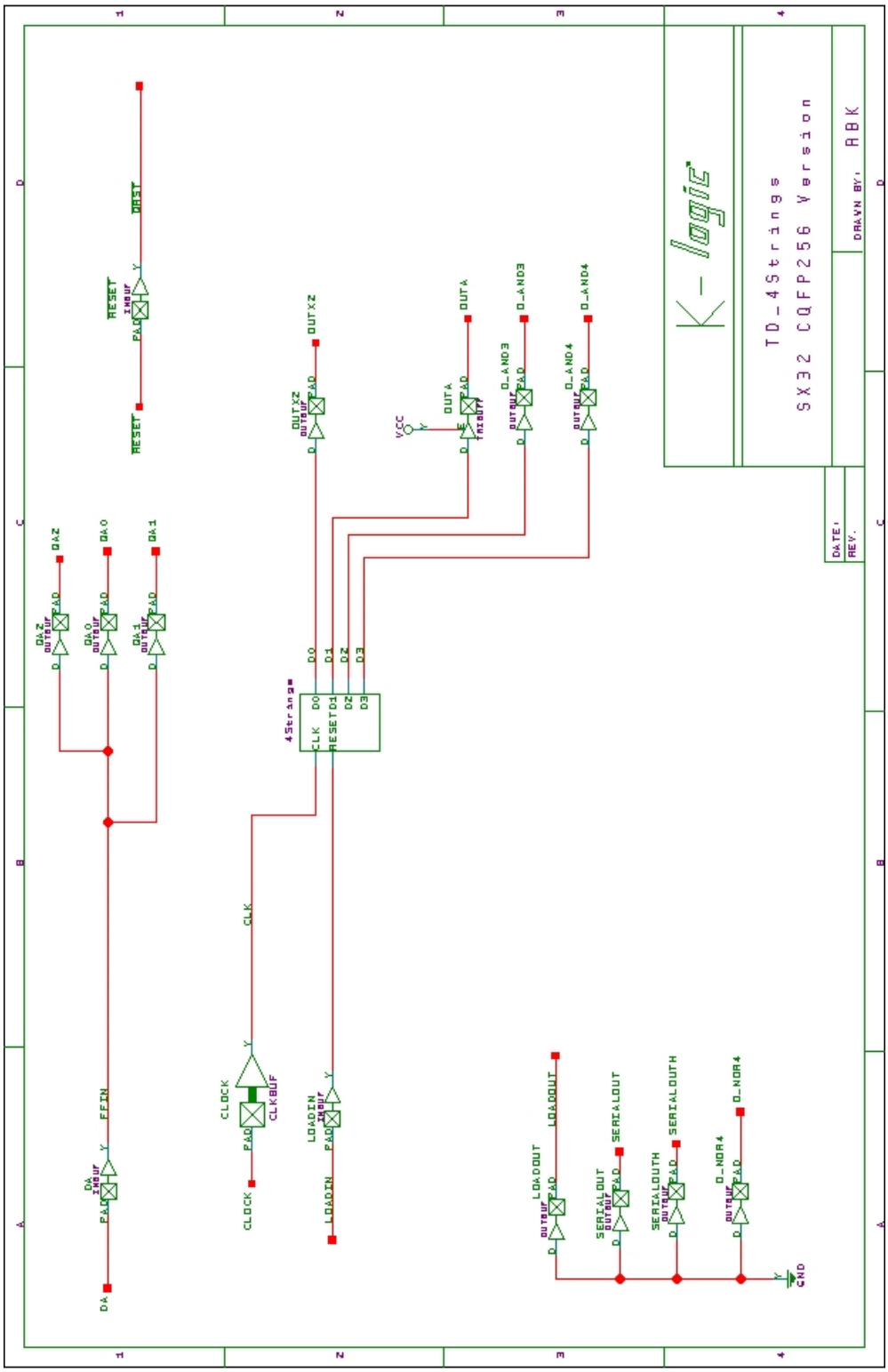
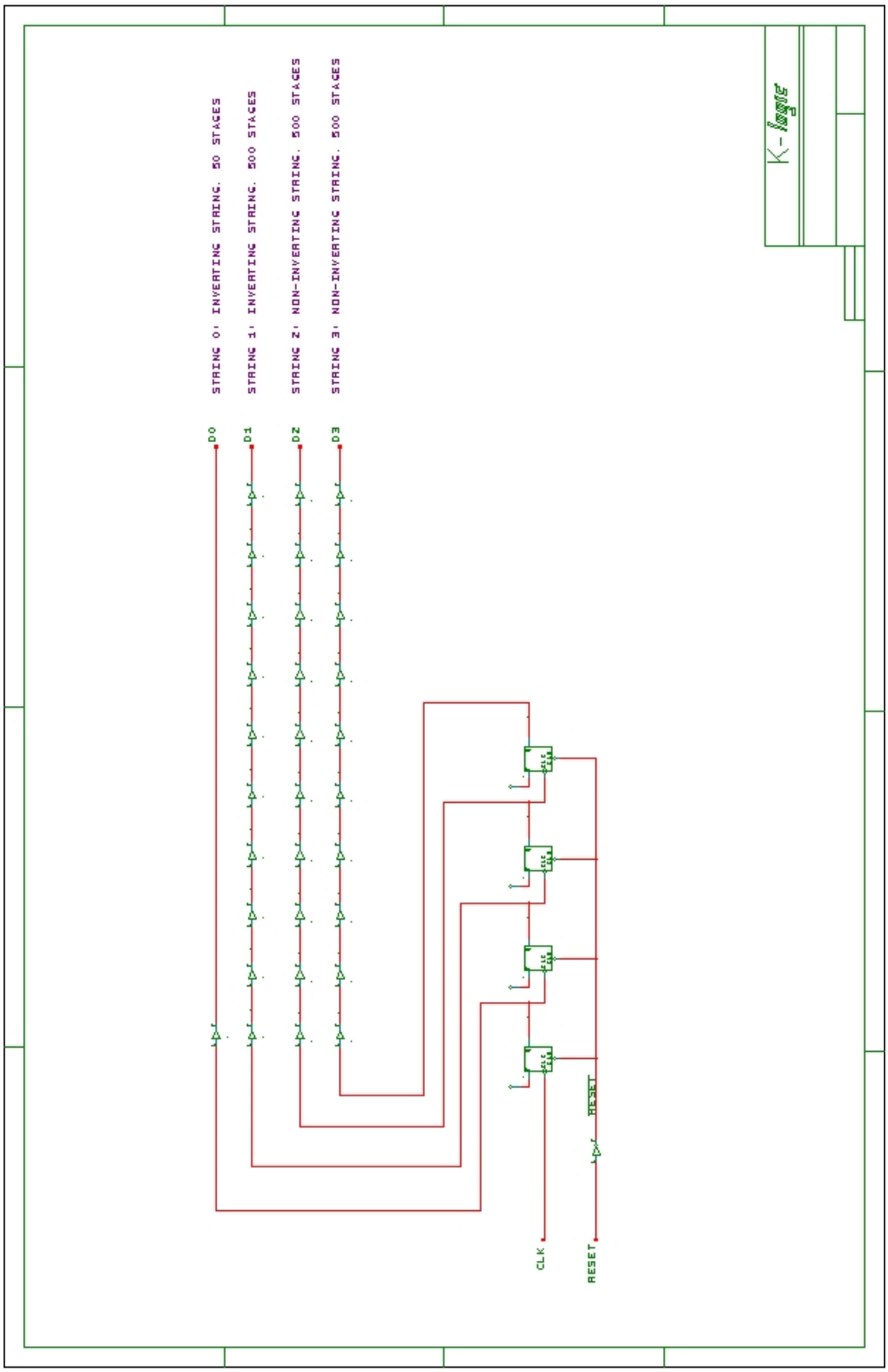


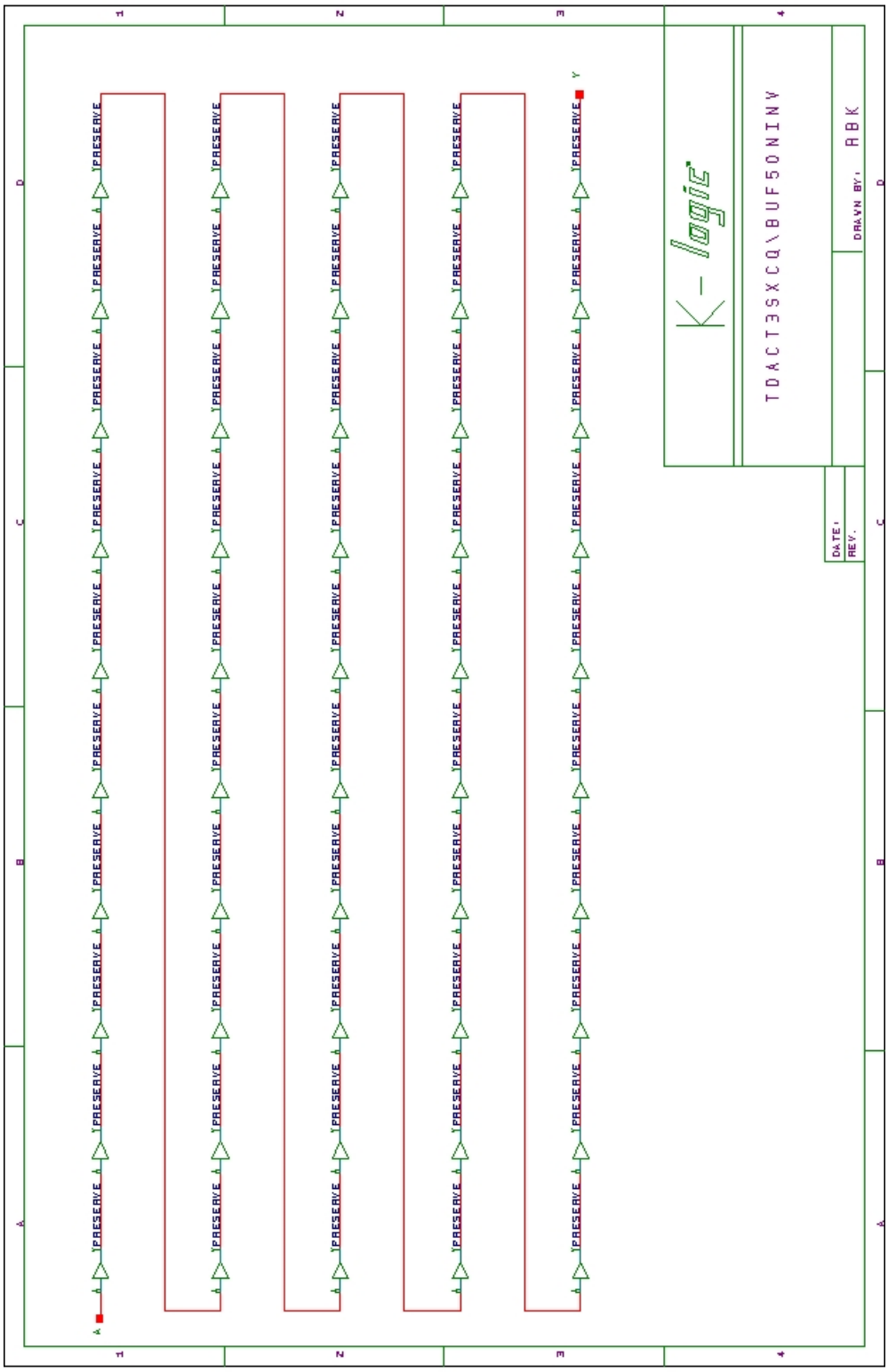
Fig 15b The post-irradiation power up transient

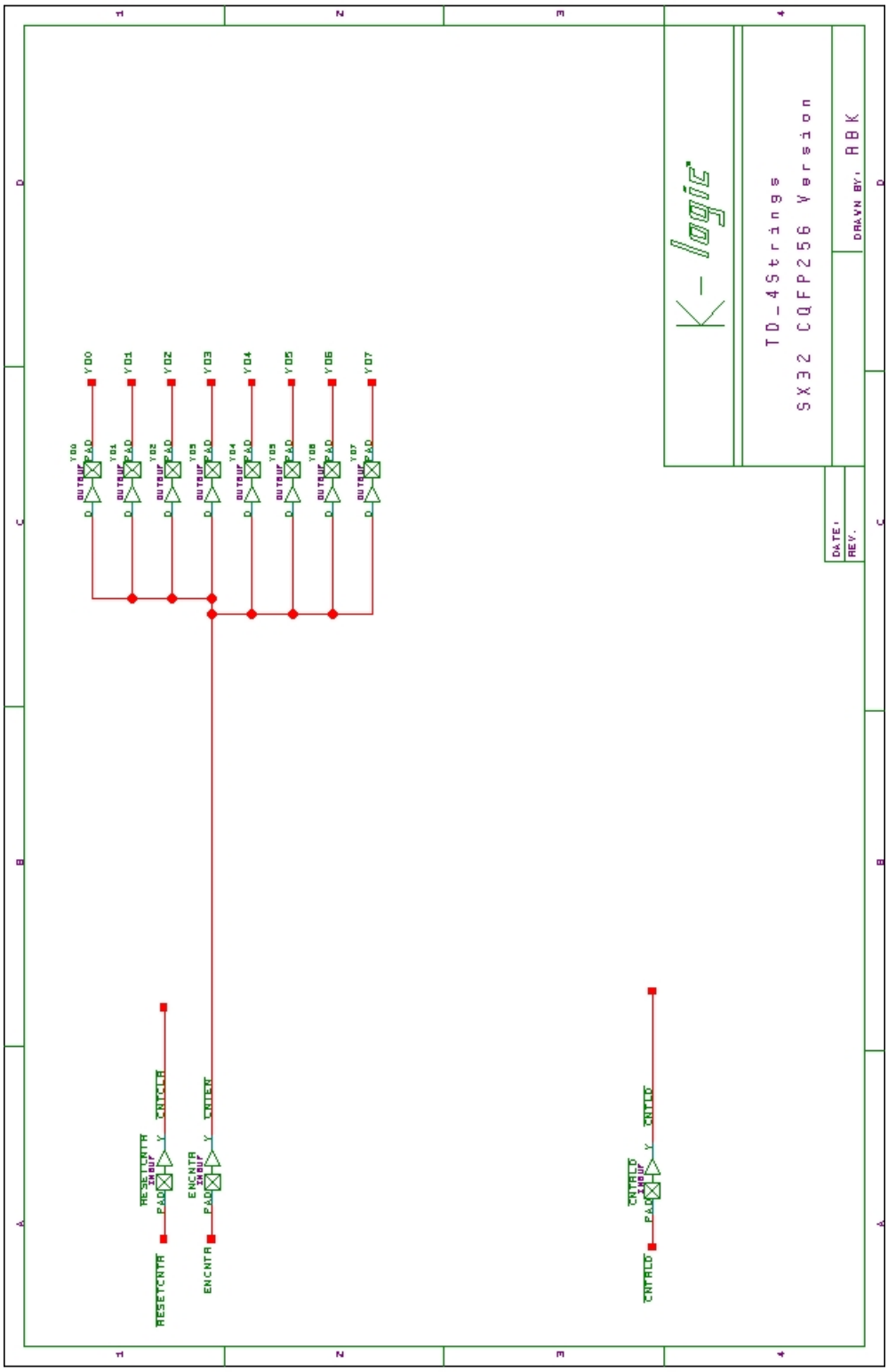
APPENDIX A DUT DESIGN SCHEMATICS

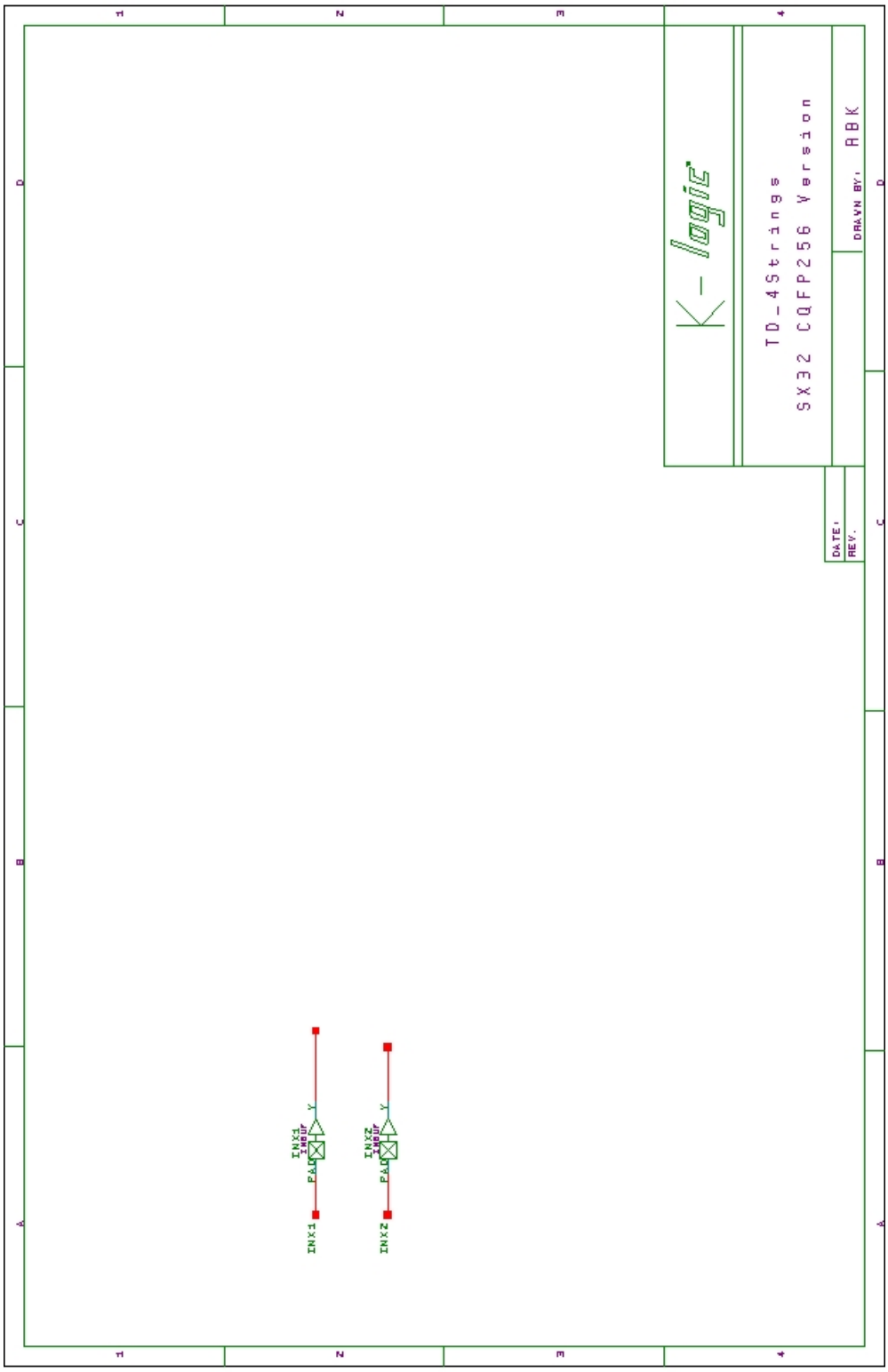


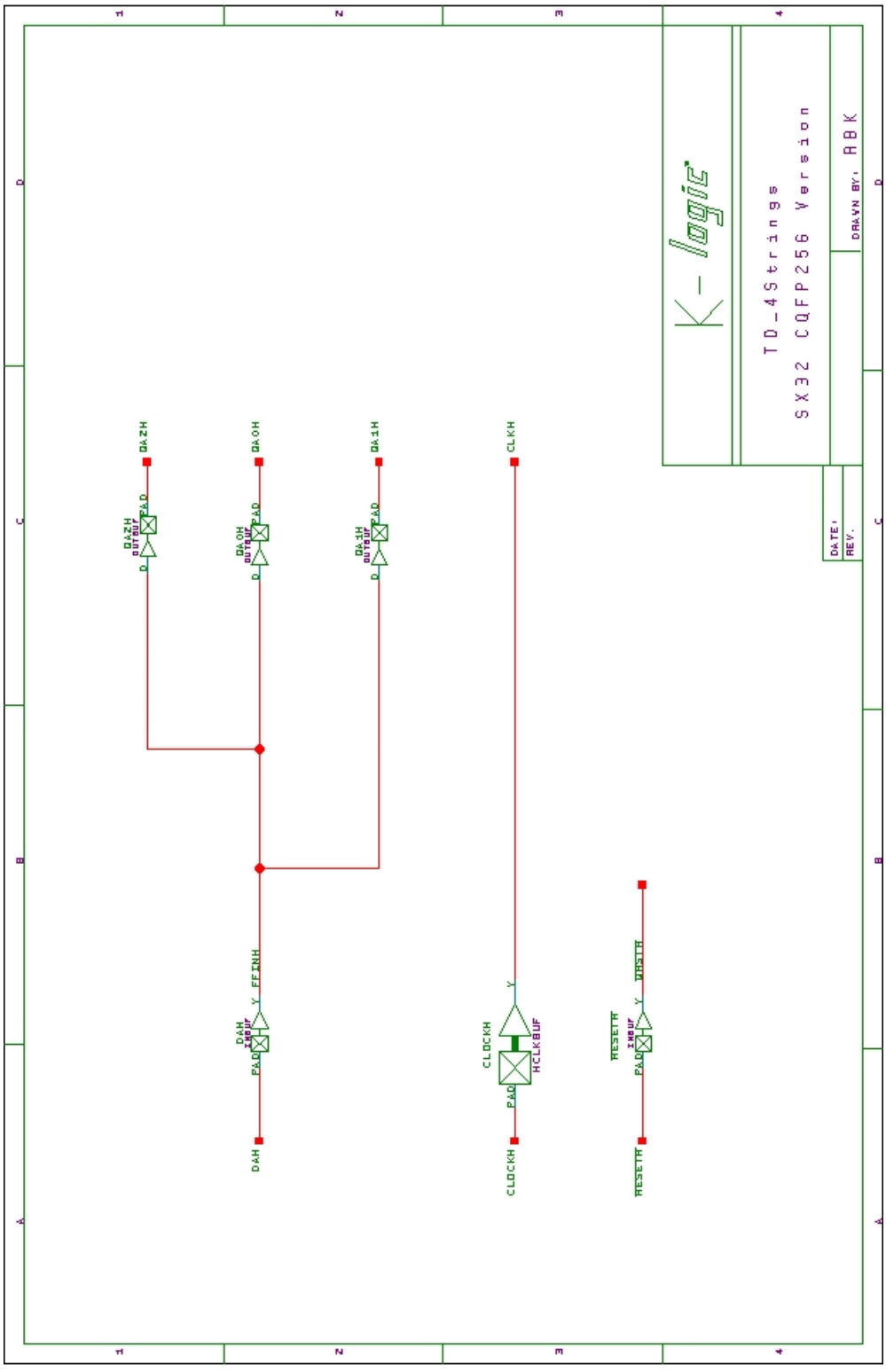

K-logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
RESET
DRST
DUTXZ
OUTA
D_AND3
D_AND4
VCC
DA2
DA0
DA1
4Strange
CLK
RESET
D0
D1
D2
D3
CLOCK
CLKBUF
LOADIN
DA
FFIN
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
GND

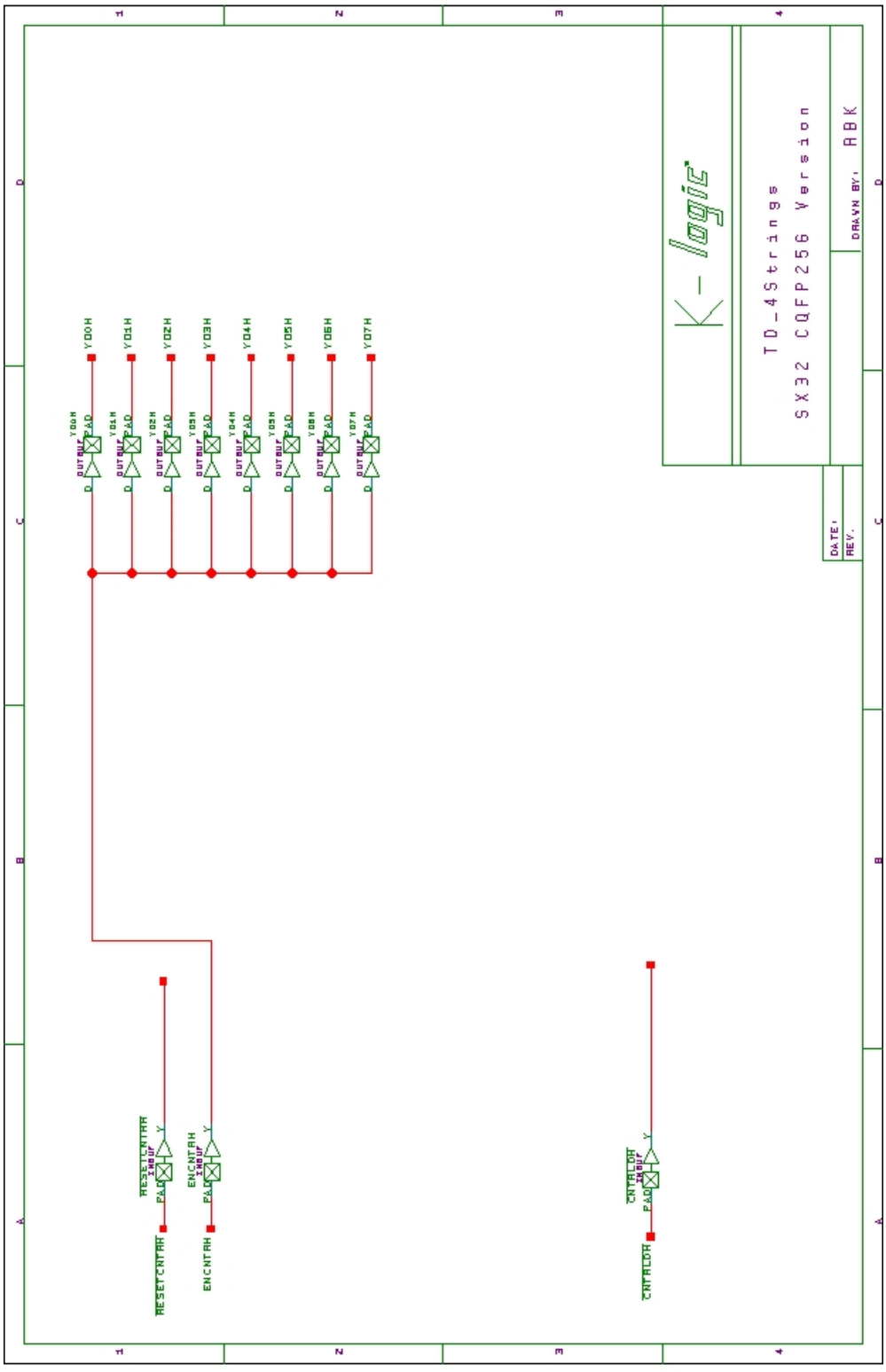

STRING 0: INVERTING STRING. 50 STAGES
STRING 1: INVERTING STRING. 500 STAGES
STRING 2: NON-INVERTING STRING. 500 STAGES
STRING 3: NON-INVERTING STRING. 500 STAGES
D0
D1
D2
D3
CLK
RESET
RESET
K-Logic

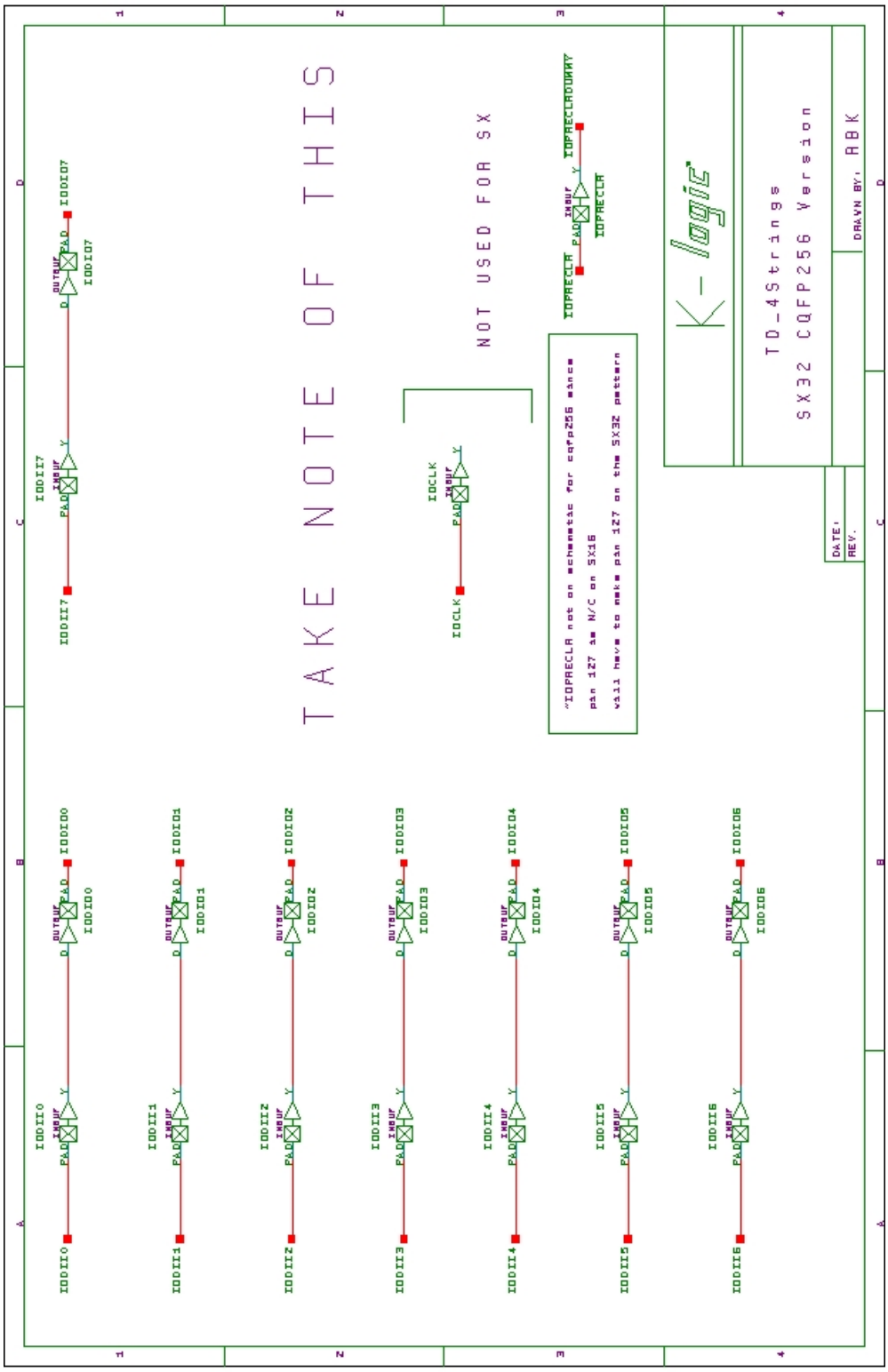

K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE

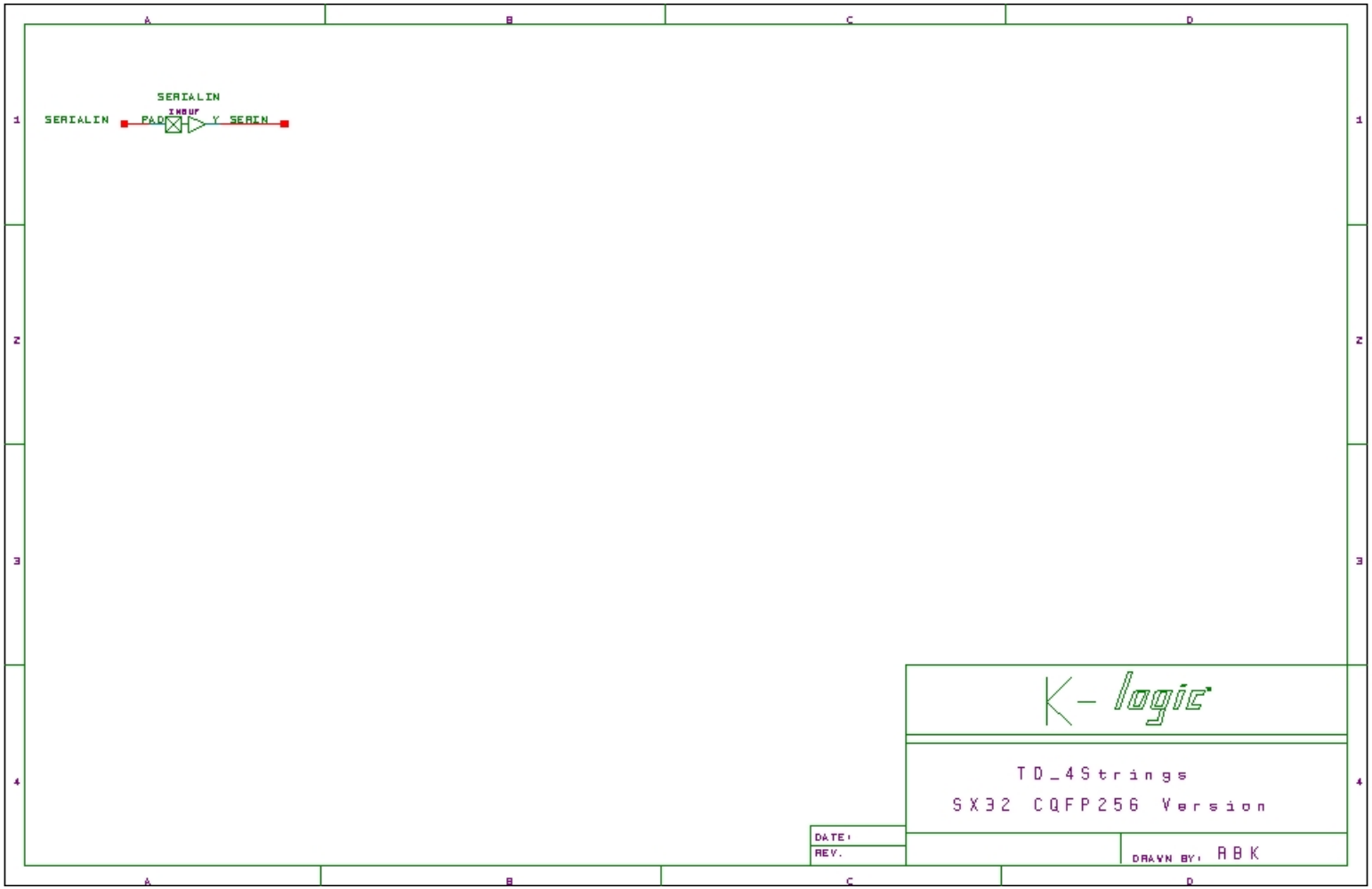

K- logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
YD0
YD1
YD2
YD3
YD4
YD5
YD6
YD7
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRCLR
CNTRLOC
INBUF

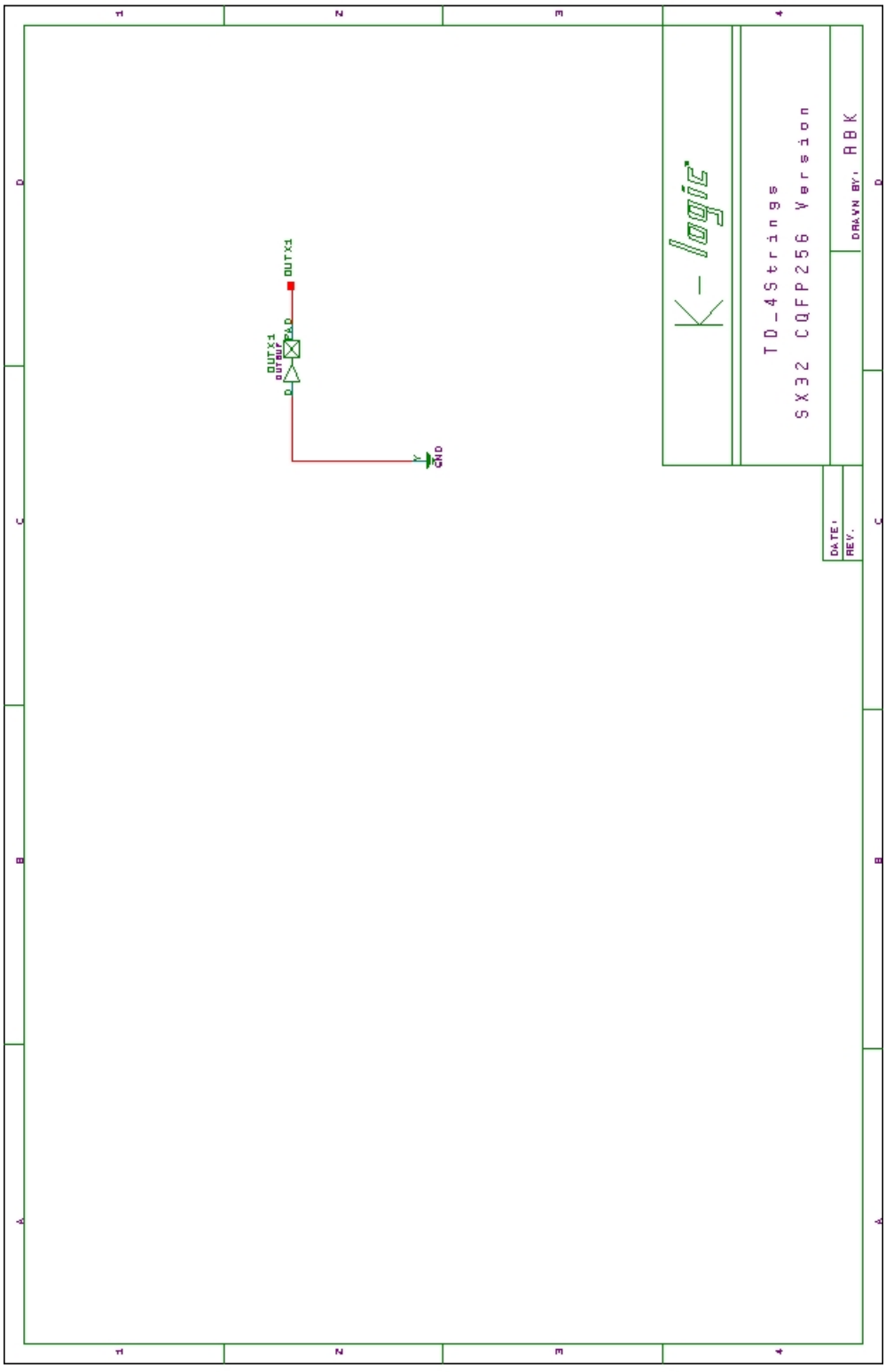

K- logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
INX1
INX2

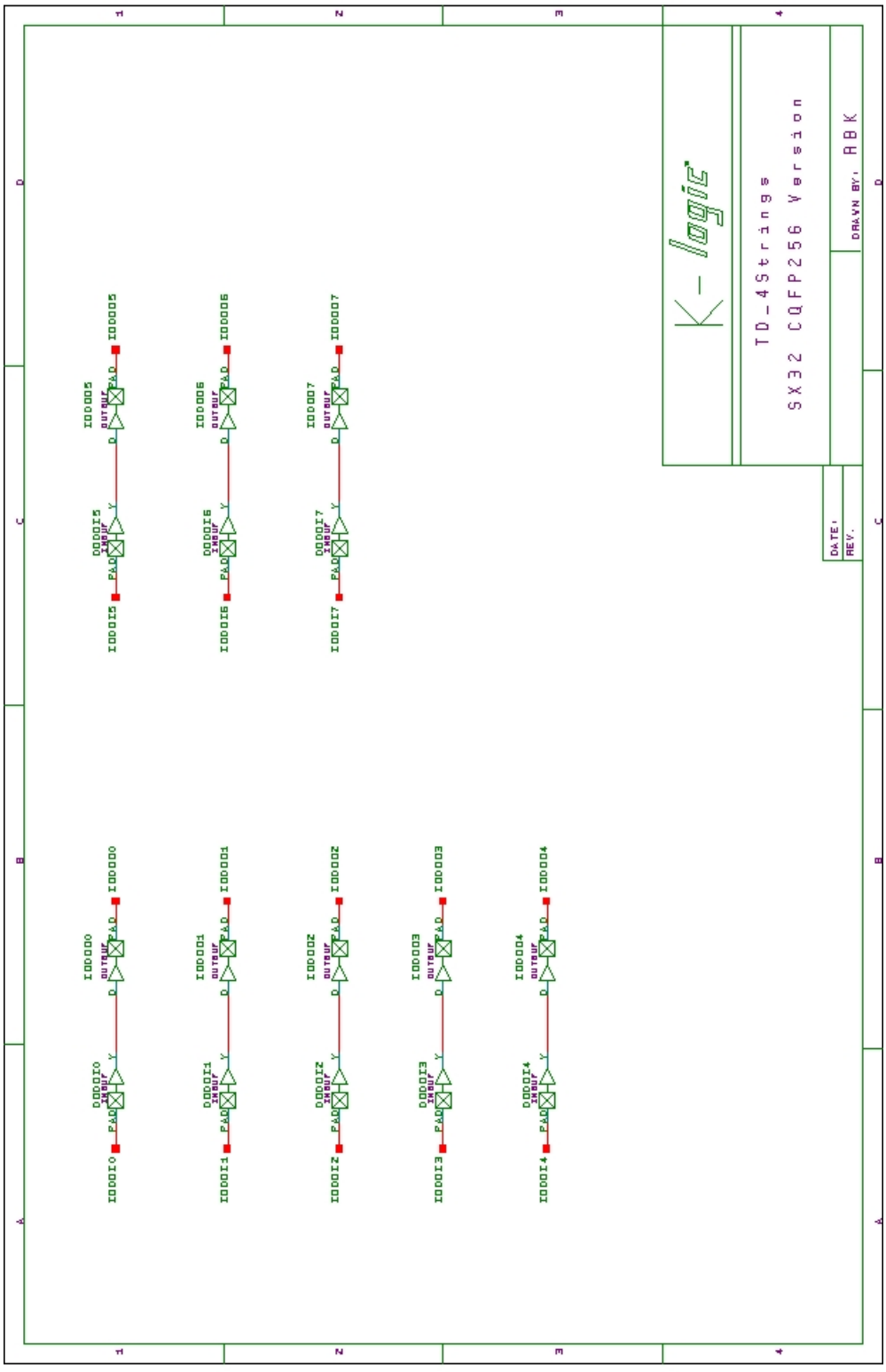

K-logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH
INBUF
Y FFINH
CLOCKH
HCLKBUF
Y
RESETH
WRSTH
DAH
CLOCKH
RESETH


K- logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTAR
ENCNTAR
CNTALOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TD_45trings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRDUMMY
IOII0
IOII1
IOII2
IOII3
IOII4
IOII5
IOII6
IOII7
IOIO0
IOIO1
IOIO2
IOIO3
IOIO4
IOIO5
IOIO6
IOIO7


A
B
C
D
1
2
3
4
SERIALIN
SERIALIN
IMBUF
PAD
Y
SERIN
K- logic
TD_4Strings
SX32 CQFP256 Version
DATE:
REV.
DRAWN BY: ABK


OUTX1
OUTX1
PAD
O
GND
K- logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.


K- logic
TD_4Strings
SX32 CQFP256 Version
DRAWN BY: ABK
DATE:
REV.
IOOOOO
IOOOO1
IOOOO2
IOOOO3
IOOOO4
IOOOO5
IOOOO6
IOOOO7
IOOOIO
IOOOI1
IOOOI2
IOOOI3
IOOOI4
IOOOI5
IOOOI6
IOOOI7
OUTBUF
XHBUF
PAD