Microsemi

Total Ionizing Dose Test Report

No. 13T-RTAX4000S-CQ352-D3LG61

March 28, 2013

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I. Summary Table

The TID tolerance for each tested parameter is summarized below in Table 1. The overall tolerance is limited by the standby power-supply current (ICC). The room temperature annealing allowed by 1019.8 to anneal down ICC is performed for approximately 7 days. Every DUT passes the major specifications listed in the table for 200 krad (SiO2) of irradiation.

Table 1 Tolerances for Each Tested Parameter

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
3. Input Threshold (VIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Time	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the basis of an extensive database (see, for example, TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 2 lists the DUT and irradiation parameters. During irradiation all inputs are grounded except for the inputs Burnin, oe_EAQ, enable_HSB and the utilized clocks (Rclock1-3 and Hclock1-4). The inputs Burnin, oe_EAQ and enable_HSB are set high to 3.3 V and a 1 KHz clock is provided to all clocks in order for the design to remain stable during irradiation. During anneal each input and output is tied to ground or VCCI through a 4.7 kΩ resistor. Appendix A contains the schematics of irradiation-bias circuits.

Table 2 DUT and Irradiation Parameters

Part Number	**RTAX4000S**
Package	CQFP352
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	MASTER_RTAX4000S_DESIGN_80_SP1
Die Lot Number	D3LG61
Quantity Tested	6
Serial Number	300 krad: 18267, 18268, 18270 200 krad: 18273, 18279, 18281
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V / 1.5 V
I/O Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

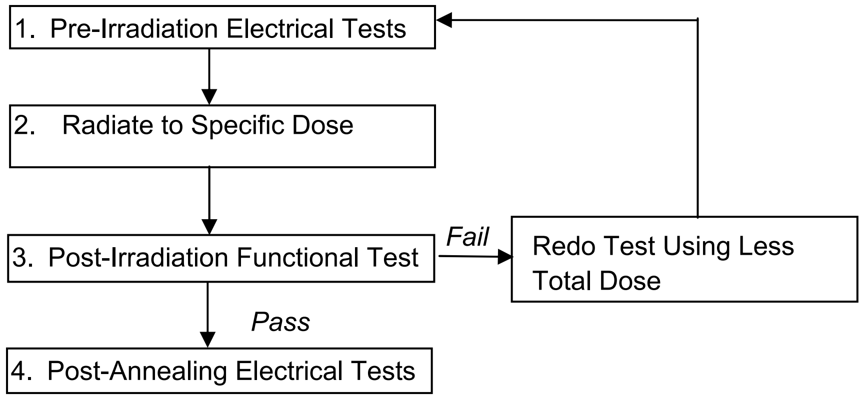

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi SoC Products Group products manufactured by sub-micron CMOS technology. Elevated temperature annealing actually reduces the effects originated from radiation-induced leakages. As indicated by testing data in the following sections, the predominant radiation effects in RTAX4000S are due to radiation-induced leakages.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization generic design (Master_RTAX4000S_Design_80_SP1) to evaluate total dose effects for typical space applications. The schematics of this design are documented in Appendix B.

The functionality is measured at 1 MHz and 50 MHz using the minimum and maximum power specifications shown in Table 3.

Table 3 Minimum and Maximum Power Specifications for RTAX-D Devices

Supply Voltage	Minimum	Recommended	Maximum
1.5 V Core	1.4 V	1.5 V	1.6 V
3.3 V I/O	3.0 V	3.3 V	3.6 V
3.3 V VCCDA I/O	3.0 V	3.3 V	3.6 V

The functionality test design is subdivided into two blocks, the EAQ (Enhanced Antifuse Qualification) and the QBI (Qualification Burn-In). The EAQ block includes three 1458-bit shift registers and tests the I/Os (1560 I/O registers and 520 I/Os) and RAM (1x16384 RAM). The QBI block tests all offered macros and I/O standards. The results from the functional tests are obtained from the following outputs: IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI. Details on the Functionality Test are shown in Appendix B.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is tested on single-ended inputs Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, and A_Pattern_Length_0. The output-drive voltage (VOL/VOH) is measured on single-ended outputs Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8.

The propagation delays are measured on the outputs of five delay strings; each one comprises of 1,170 NAND4-inverters. There are 6 delay measurements: one measurement for each delay string and a total delay measurement obtained from cascading all the delay strings. The propagation delay is defined as the time delay from the triggering edge at the HClock1 input to the switching edge at the output. The transition characteristics, measured on the output delay_out_SEU4, are shown as oscilloscope captures.

Table 4 lists measured electrical parameters and the corresponding logic design.

Table 4 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	IO_Monitor_EAQ, RAM_Monitor_EAQ, Array_Monitor_EAQ, Global_Monitor_EAQ, C_test_mon_QBI, ALU_test_mon_QBI, Global_mon_QBI_TP, and Global_mon_QBI_BI
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (Shiftin1, Shiftin2, Shiftin3, Shiftin4, Shiftin5, Shiftin7, Shiftin8, zoom_sel_n_1, zoom_sel_n_0, zoom, TOG_n, SEU_sel, Set_n, Resetn, oe_EAQ, enable_HSB, test_done_sel_2, IO_Pattern_Length_2, IO_Pattern_Length_1, IO_Pattern_Length_0, IO_Johnson, A_Johnson, A_Pattern_Length_1, A_Pattern_Length_0)
4. Output Drive (VOL/VOH)	Single-ended outputs (Array_out_EAQ_0, Array_out_EAQ_1, Array_out_EAQ_2, Global_Monitor_EAQ, Shiftout3, Shiftout7, Shiftout8, RAM_Monitor_EAQ, RAM_out_EAQ_0, RAM_out_EAQ_4, RAM_out_EAQ_8)
5. Propagation Delay	String of NAND4-inverters. Measured from output delay_out_SEU4
6. Transition Characteristic	NAND4-inverter output (delay_out_SEU4)

III. Test Results

The test results mainly compare the electrical parameter measured pre-irradiation with the same parameter measured post-irradiation-and-annealing, or post-annealing.

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

The logic-array power supply (VCCA) is 1.5 V, and the IO power supply (VCCI) is 3.3 V. Their standby currents, ICCA and ICCI, are monitored influx. Figure 2-7 show the influx ICCA and ICCI versus total dose for the DUTs.

Referring to TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICC should be defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the *RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs datasheet* posted on the Microsemi SoC Products Group website:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

Therefore, the PIPL for ICCA is 600 mA, and the PIPL for ICCI is 60 mA.

Table 5 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 5 Pre-irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-Irrad.	Post-Irrad.	Post-Ann.	Pre-Irrad.	Post-Irrad.	Post-Ann.
18267	300 krad	5	187	39	9	317	95
18268	300 krad	12	292	56	8	310	110
18270	300 krad	4	205	42	8	305	94
18273	200 krad	15	19	15	9	75	34
18279	200 krad	14	20	12	9	78	30
18281	200 krad	4	11	2	8	73	31

Based on these PIPL, the post-annealing DUT passes both the ICCA and ICCI specification for 200 krad(SiO_2).

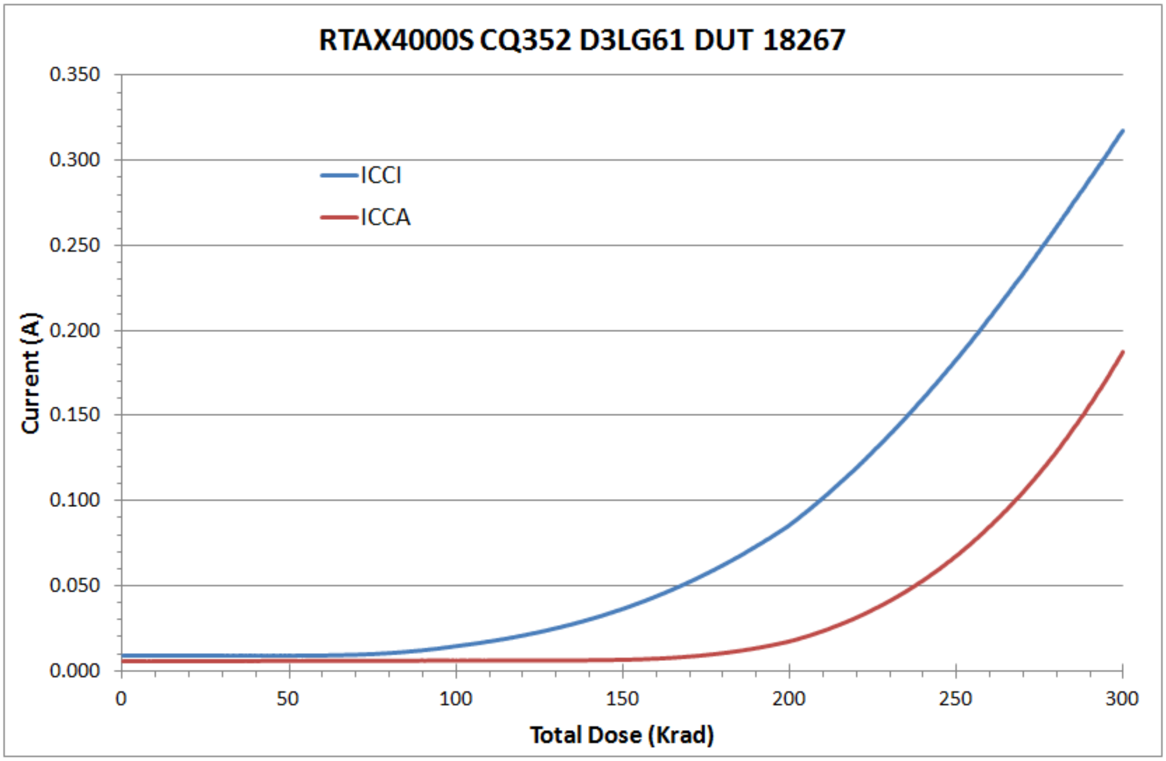

Figure 2 DUT 18267 Influx ICCI and ICCA

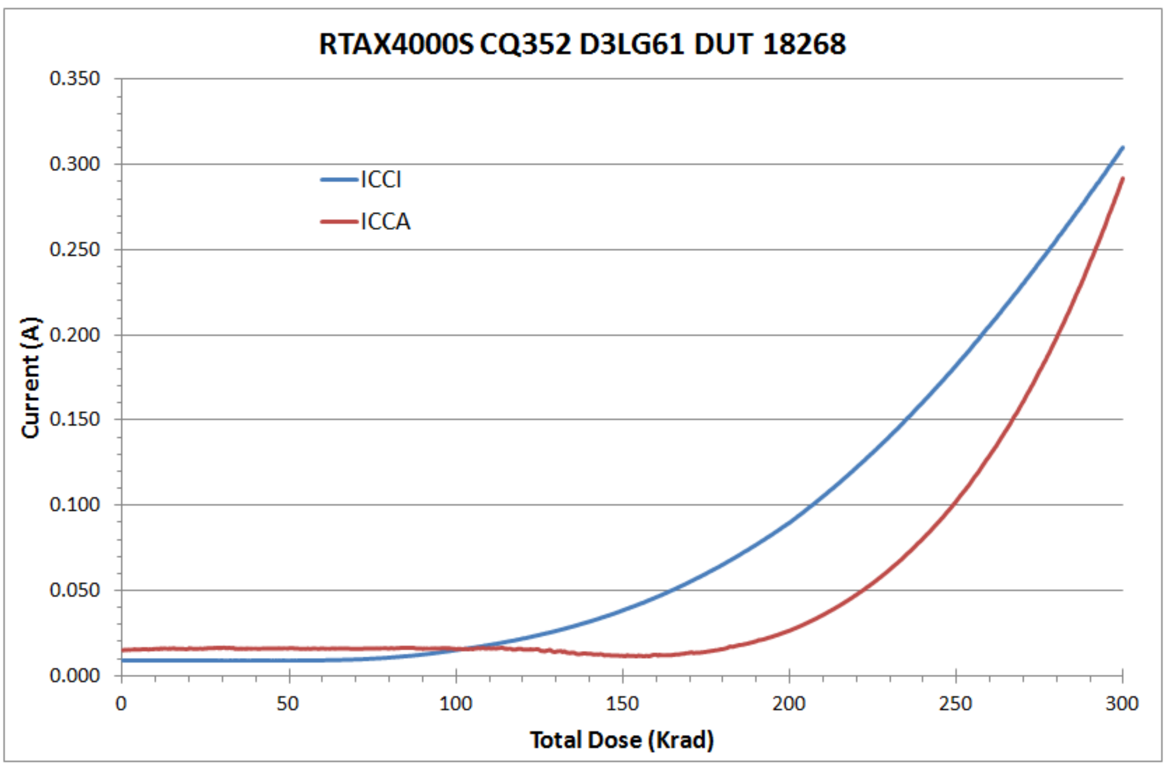

Figure 3 DUT 18268 Influx ICCI and ICCA

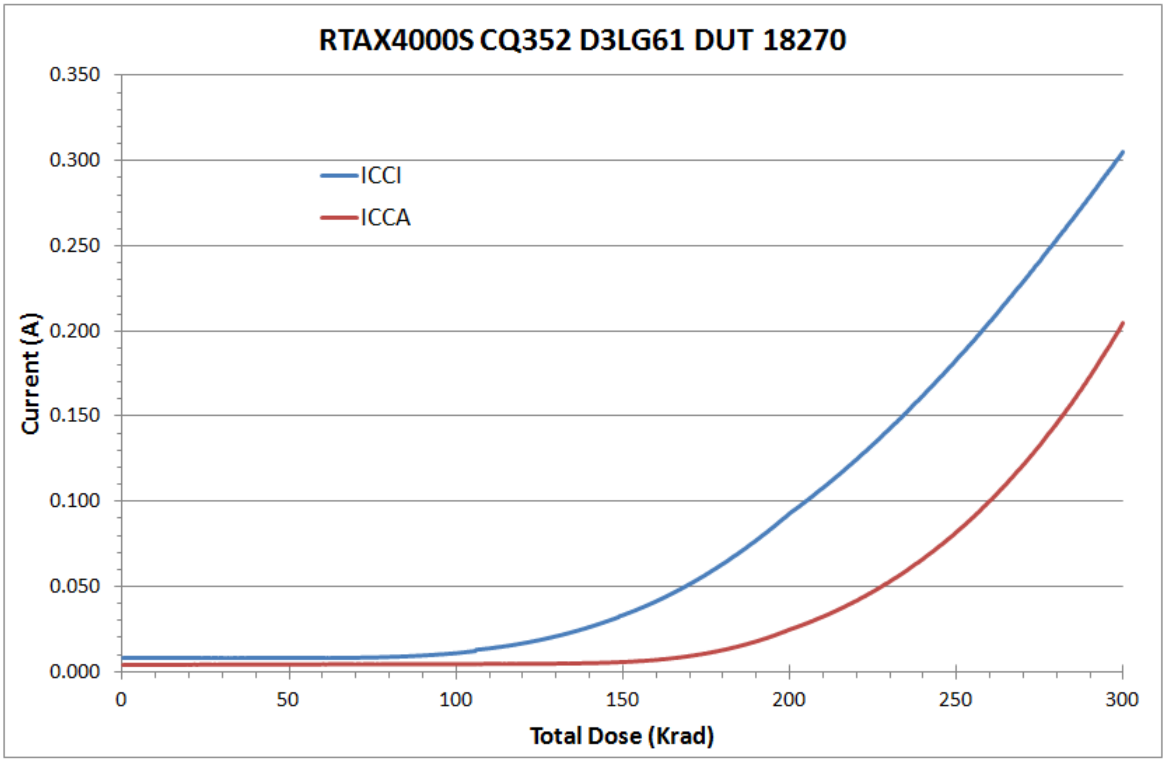

Figure 4 DUT 18270 Influx ICCI and ICCA

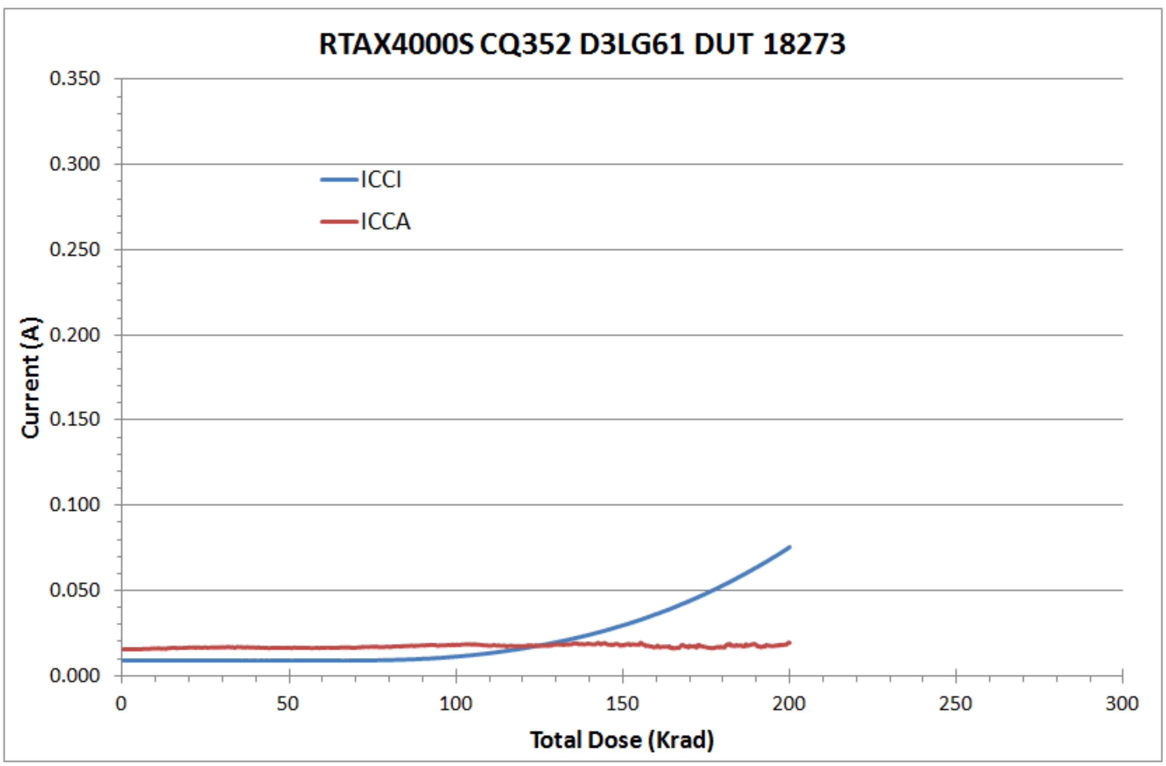

Figure 5 DUT 18273 Influx ICCI and ICCA

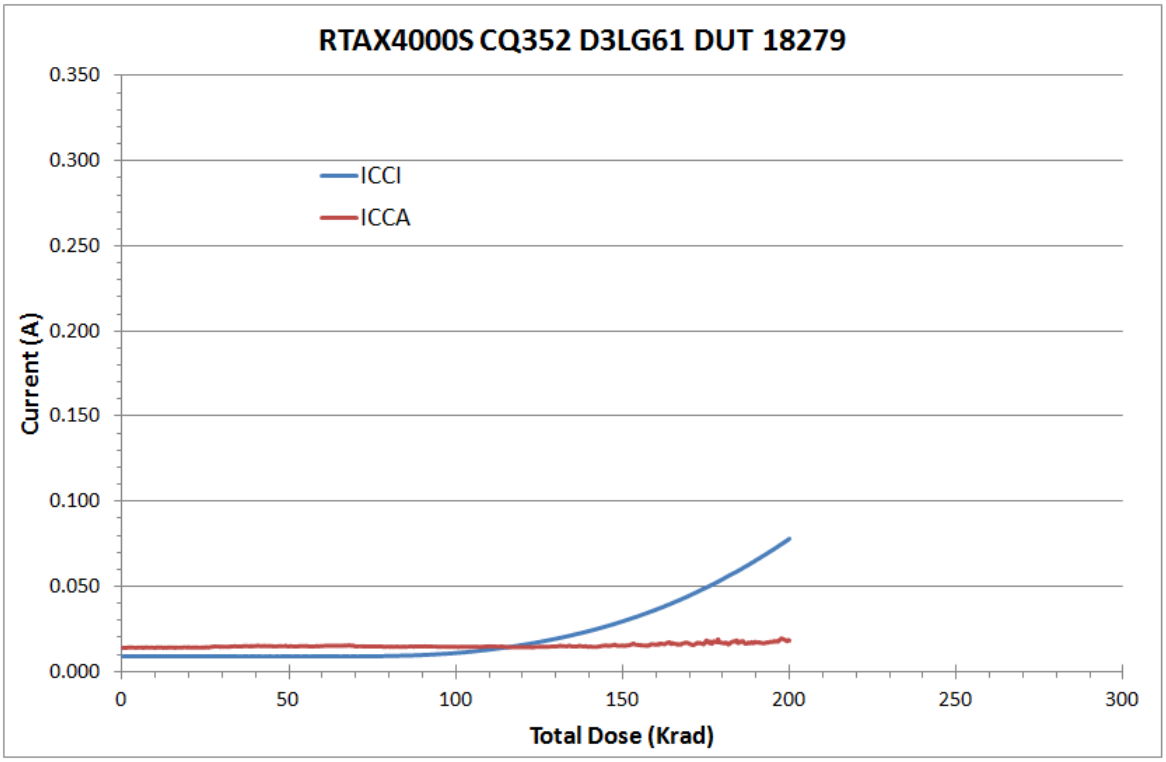

Figure 6 DUT 18279 Influx ICCI and ICCA

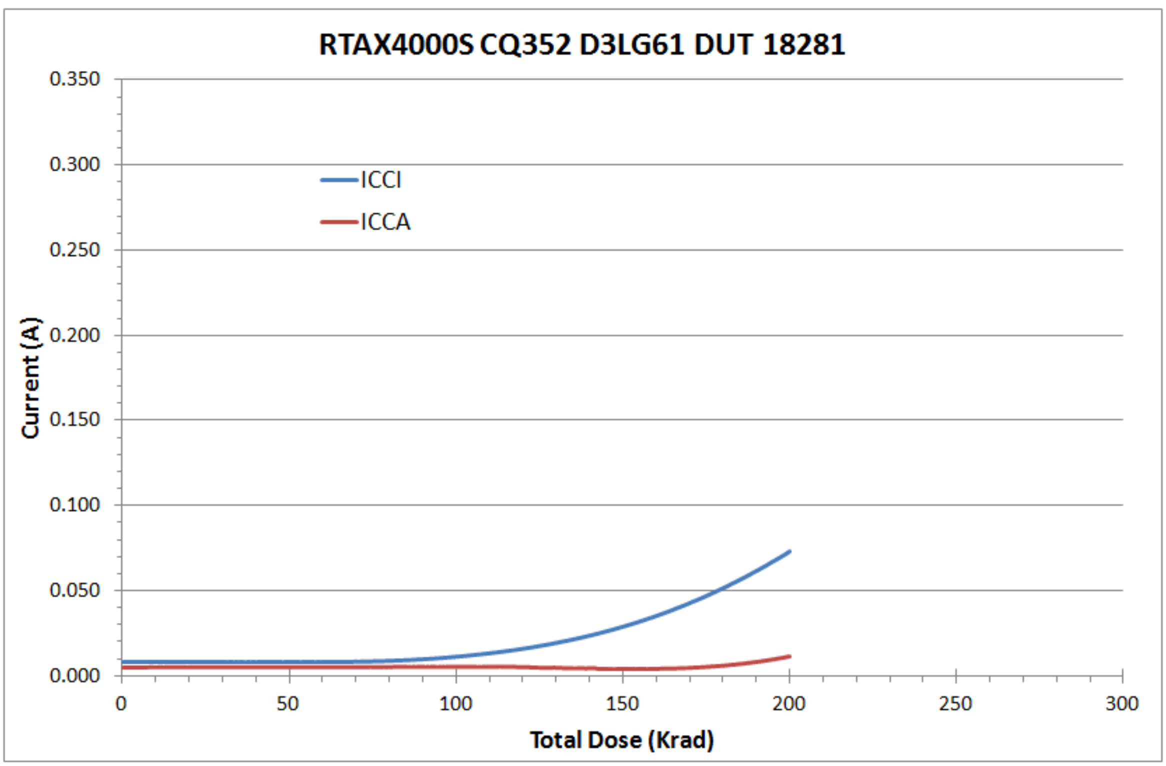

Figure 7 DUT 18281 Influx ICCI and ICCA

C. Single-Ended 3.3 V LVTTL Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design often just input and output buffers starts to switch: VIH is the input trip point when the input is going high to low; VIL is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-annealing data is usually negligibly small.

The pre-irradiation and post-annealing single-ended VIL and VIH are tested and recorded as pass or fail. In each case, the pre-irradiation and post-annealing both passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH are listed in Tables 6 and 7. The post-annealing data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table 6 Pre-Irradiation and Post-Annealing VOL (mV)

Pin \ DUT(Dose)	18267 (300 krad)		18268 (300 krad)		18270 (300 krad)		18273 (200 krad)		18279 (200 krad)		18281 (200 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	155.8	143.9	154.3	143.5	158.6	143.3	156.1	145.6	155.2	145.6	161.2	144.9
Array_out_EAQ_1	189.1	180.4	187.4	179.9	190.9	181.8	187.9	181.5	189.8	183.1	195.7	182.5
Array_out_EAQ_2	186.2	183.0	182.1	182.7	185.4	181.5	184.3	183.8	184.1	184.9	189.6	184.1
Global_Monitor_EAQ	183.0	181.0	180.6	186.6	183.0	177.8	181.8	175.8	181.6	178.4	185.8	167.9
Shiftout3	193.7	175.3	190.7	186.9	193.4	189.9	193.1	185.5	190.0	188.7	191.5	188.6
Shiftout7	203.3	190.9	200.3	190.0	202.6	194.1	202.8	198.3	199.5	195.9	201.2	194.7
Shiftout8	205.5	192.0	206.1	193.6	210.0	195.6	203.4	191.5	206.7	194.1	205.0	196.2
RAM_Monitor_EAQ	189.4	176.1	186.9	172.8	189.1	177.0	188.4	180.5	188.6	178.7	192.4	186.4
RAM_out_EAQ_0	191.6	179.0	192.2	180.6	196.8	181.6	190.0	180.3	195.3	182.2	198.2	182.9
RAM_out_EAQ_4	155.1	144.8	154.8	144.8	156.9	145.9	155.0	145.1	154.4	146.4	154.0	146.4
RAM_out_EAQ_8	191.5	208.4	188.5	208.1	192.4	206.1	189.8	224.3	190.7	213.0	197.8	208.4

Table 7 Pre-Irradiation and Post-Annealing VOH (V)

Pin \ DUT(Dose)	18267 (300 krad)		18268 (300 krad)		18270 (300 krad)		18273 (200 krad)		18279 (200 krad)		18281 (200 krad)	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
Array_out_EAQ_0	2.75	2.75	2.76	2.75	2.75	2.75	2.75	2.76	2.75	2.76	2.75	2.76
Array_out_EAQ_1	2.72	2.72	2.72	2.72	2.72	2.71	2.72	2.72	2.72	2.72	2.71	2.72
Array_out_EAQ_2	2.72	2.71	2.73	2.72	2.72	2.71	2.72	2.72	2.72	2.72	2.72	2.72
Global_Monitor_EAQ	2.73	2.72	2.73	2.73	2.73	2.72	2.73	2.72	2.73	2.72	2.73	2.72
Shiftout3	2.71	2.71	2.72	2.70	2.72	2.73	2.72	2.71	2.72	2.71	2.72	2.71
Shiftout7	2.71	2.70	2.71	2.70	2.71	2.72	2.71	2.70	2.71	2.70	2.71	2.70
Shiftout8	2.70	2.70	2.70	2.70	2.69	2.70	2.70	2.70	2.70	2.70	2.70	2.70
RAM_Monitor_EAQ	2.72	2.71	2.72	2.72	2.72	2.73	2.72	2.72	2.72	2.72	2.72	2.71
RAM_out_EAQ_0	2.72	2.72	2.72	2.72	2.71	2.71	2.72	2.72	2.71	2.72	2.71	2.72
RAM_out_EAQ_4	2.76	2.76	2.76	2.76	2.76	2.76	2.76	2.76	2.76	2.76	2.76	2.76
RAM_out_EAQ_8	2.72	2.69	2.72	2.69	2.72	2.69	2.72	2.69	2.72	2.69	2.71	2.70

E. Propagation Delay

Table 8 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below 10%.

Table 8 Radiation-Induced Propagation Delay Degradations

Delay (μs)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
18267	300 krad	6.360	6.330	6.330	6.500	6.465
18268	300 krad	6.550	6.500	6.550	6.735	6.575
18270	300 krad	6.610	6.570	6.580	6.745	6.590
18273	200 krad	6.375	6.340	6.485	-	6.260
18279	200 krad	6.465	6.435	6.440	-	6.355
18281	200 krad	7.050	7.005	7.015	-	6.925

Radiation Δ (%)

DUT	Total Dose	Pre-rad.	Post-100krad	Post-200krad	Post-300krad	Post-ann.
18267	300 krad	-	-0.5%	-0.5%	2.2%	1.7%
18268	300 krad	-	-0.8%	0.0%	2.8%	0.4%
18270	300 krad	-	-0.6%	-0.5%	2.0%	-0.3%
18273	200 krad	-	-0.5%	1.7%	-	-1.8%
18279	200 krad	-	-0.5%	-0.4%	-	-1.7%
18281	200 krad	-	-0.6%	-0.5%	-	-1.8%

F. Transition Time

Figure 8a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

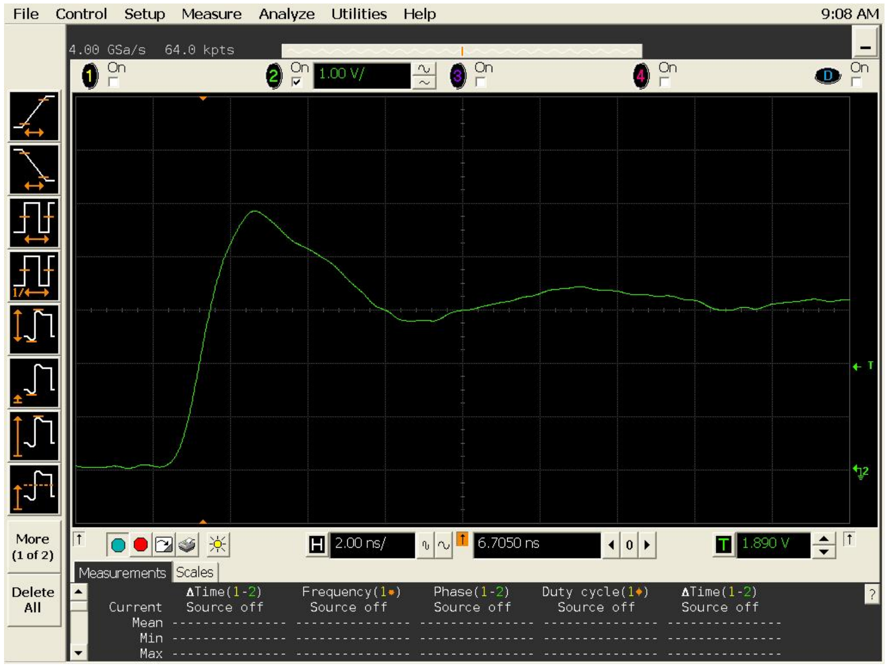

Figure 8a DUT 18267 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

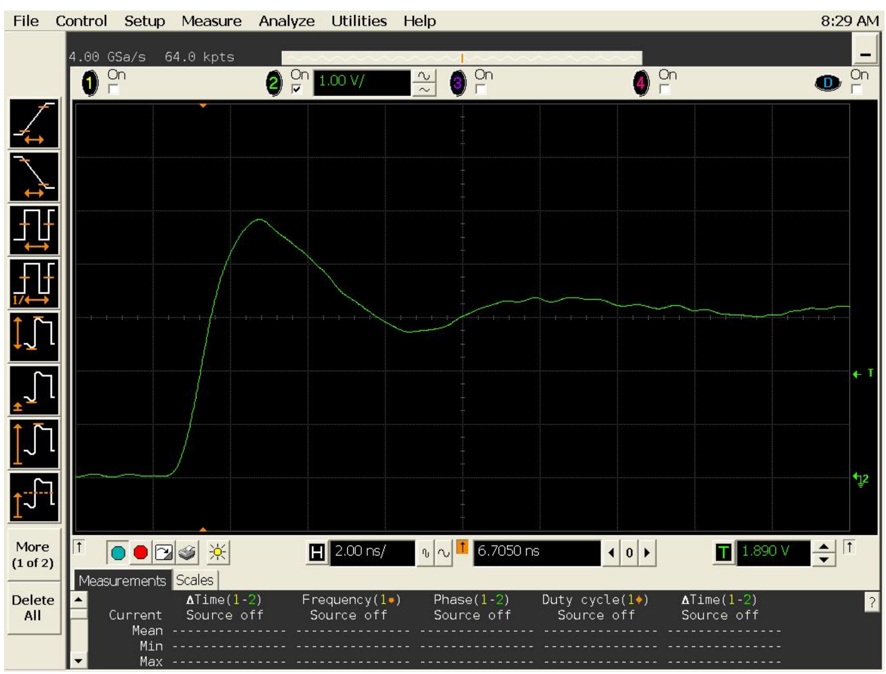

Figure 8b DUT 18267 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

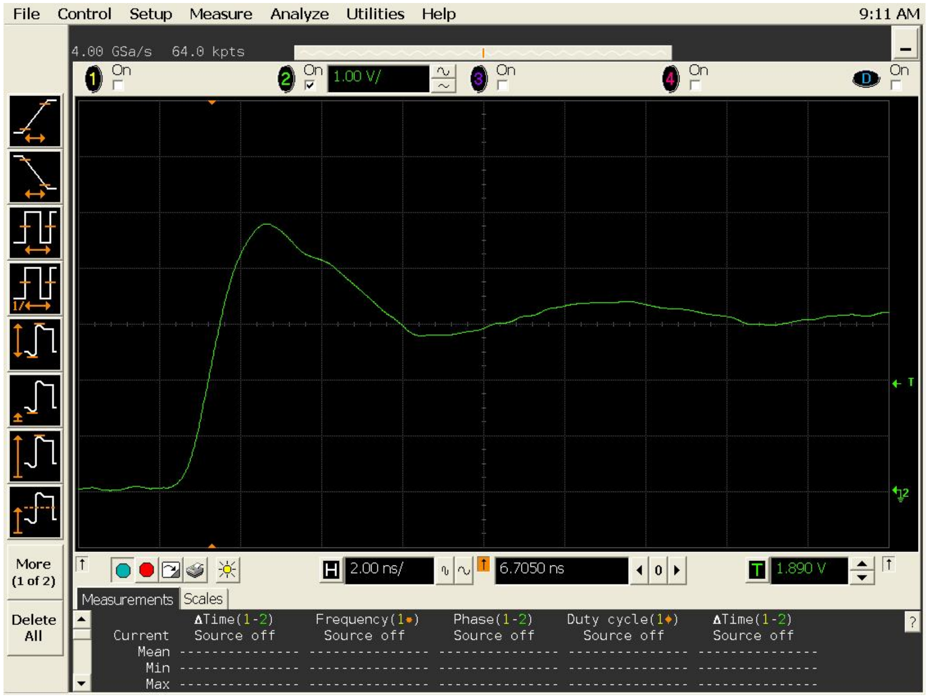

Figure 9a DUT 18268 Pre-irradiation Rising Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

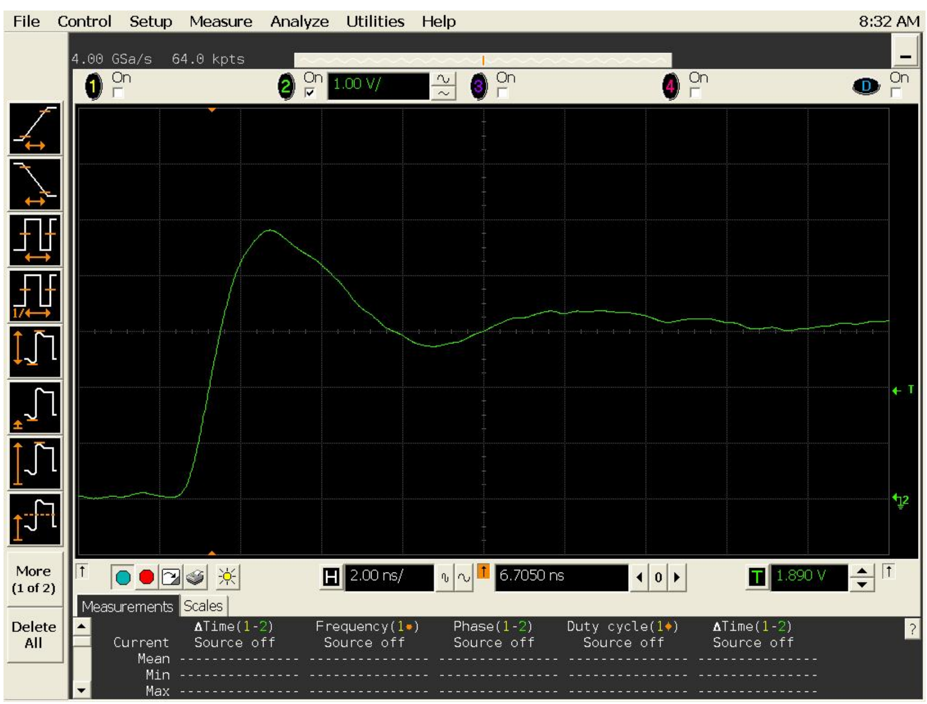

Figure 9b DUT 18268 Post-Annealing Rising Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

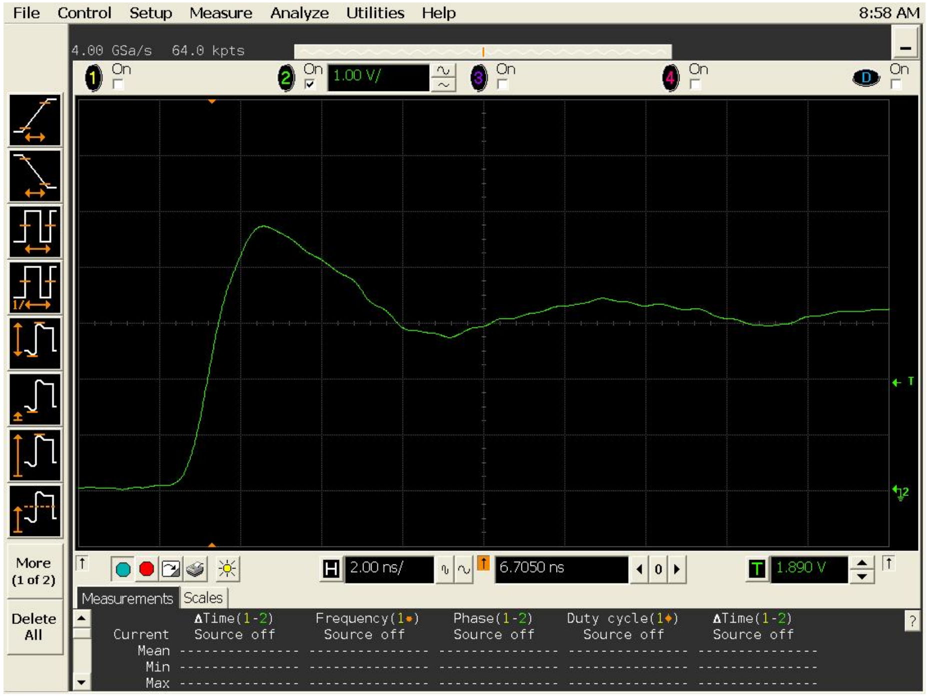

Figure 10a DUT 18270 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

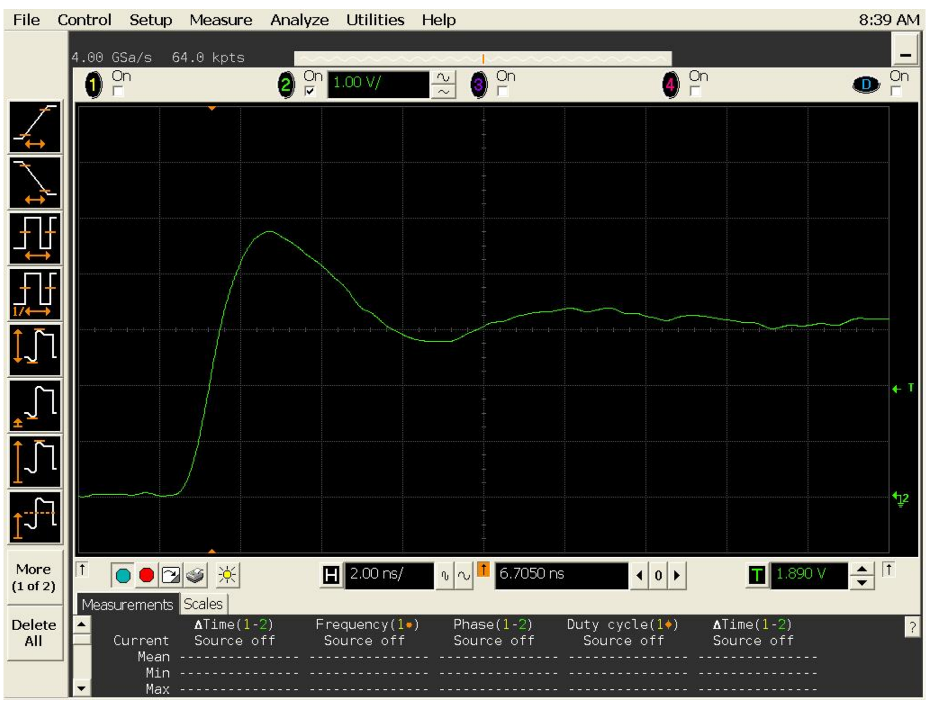

Figure 10b DUT 18270 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

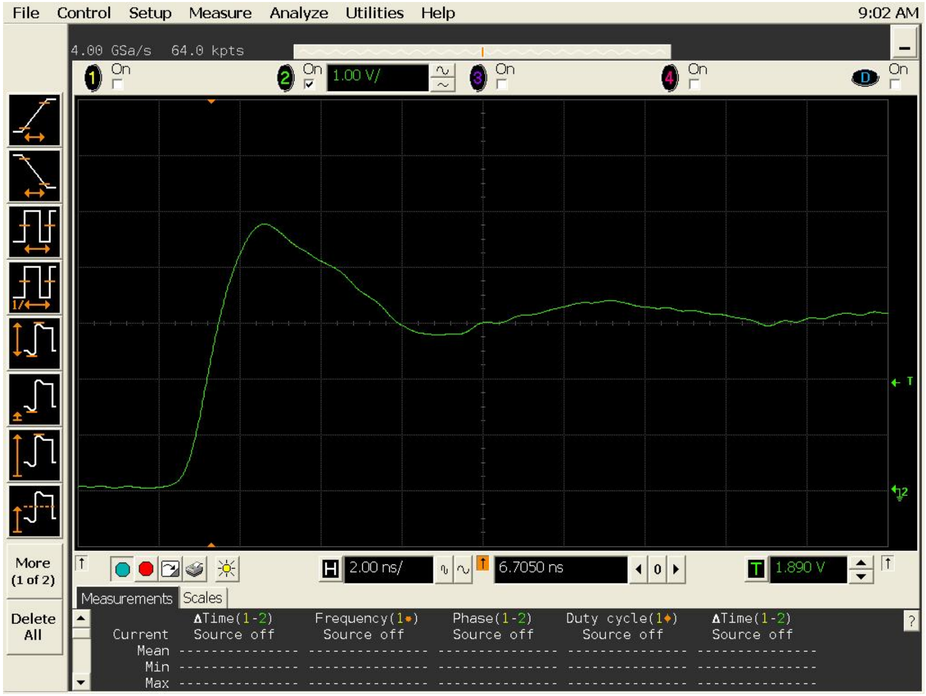

Figure 11a DUT 18273 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

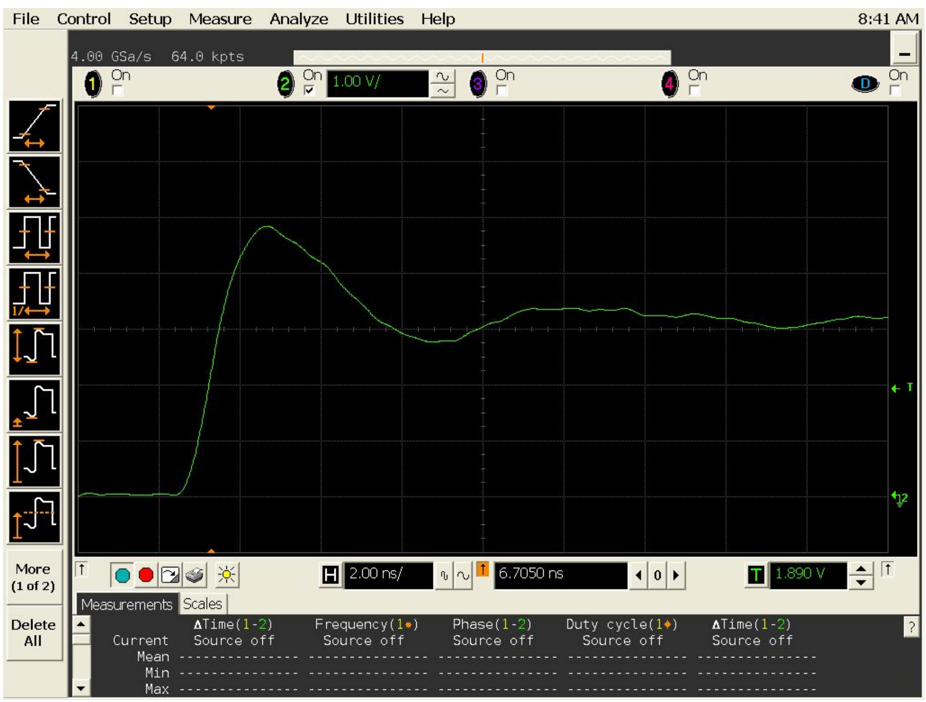

Figure 11b DUT 18273 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

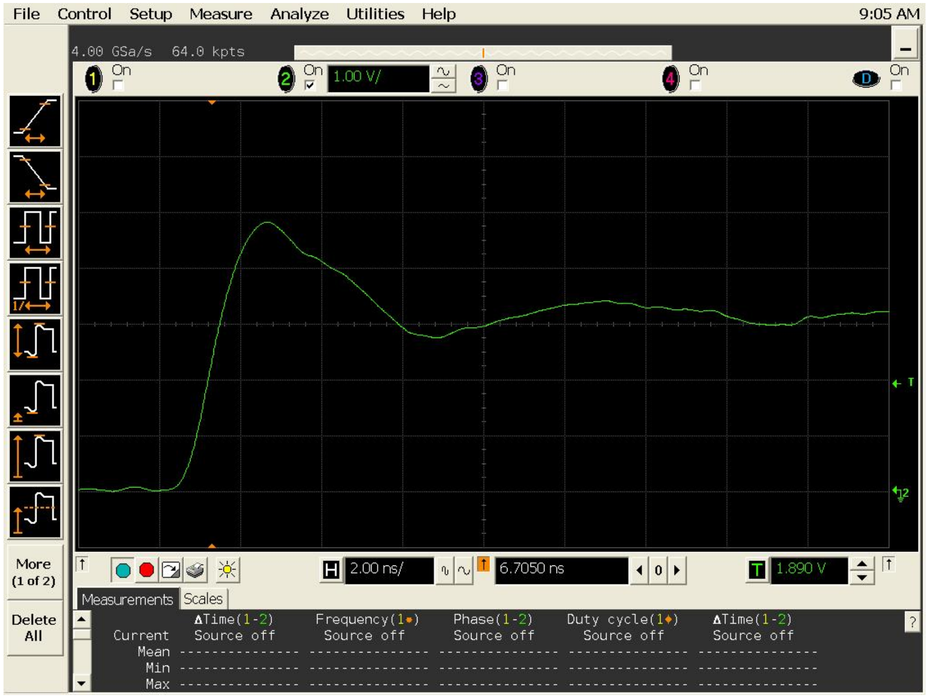

Figure 12a DUT 18279 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

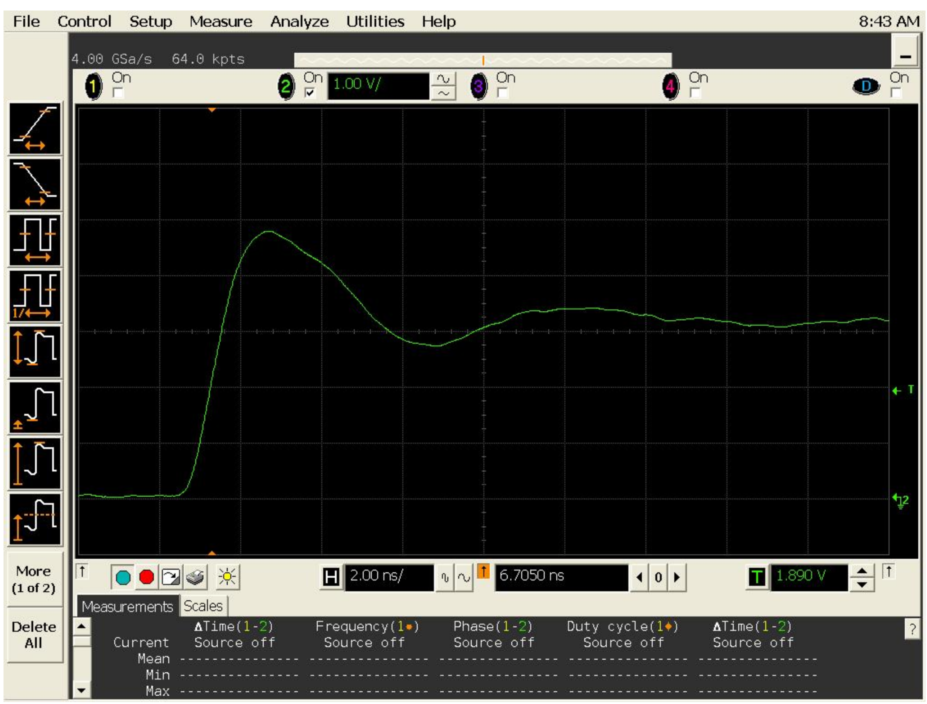

Figure 12b DUT 18279 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

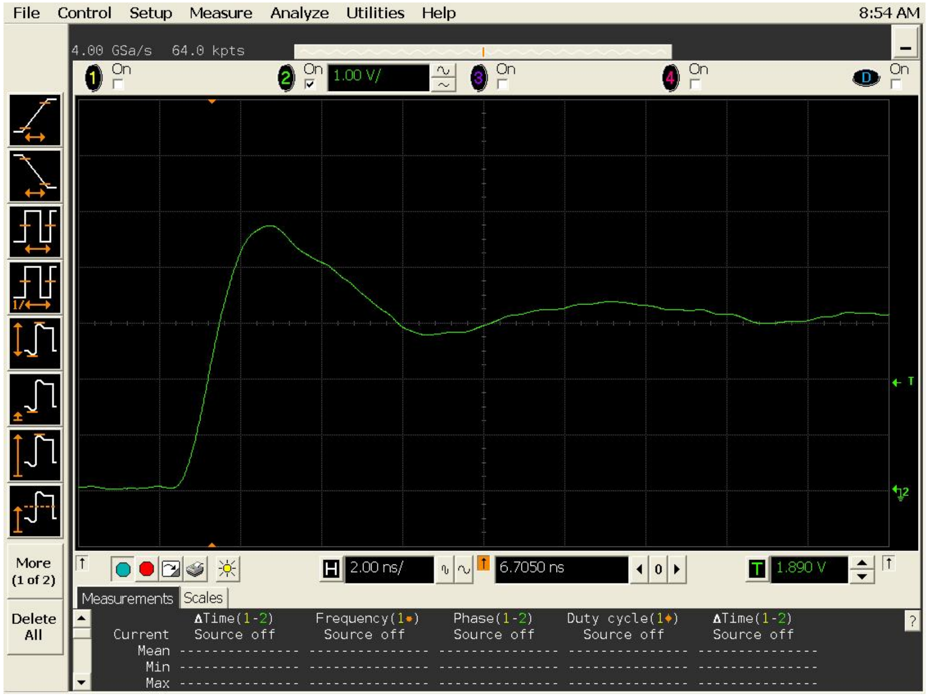

Figure 13a DUT 18281 Pre-Irradiation Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

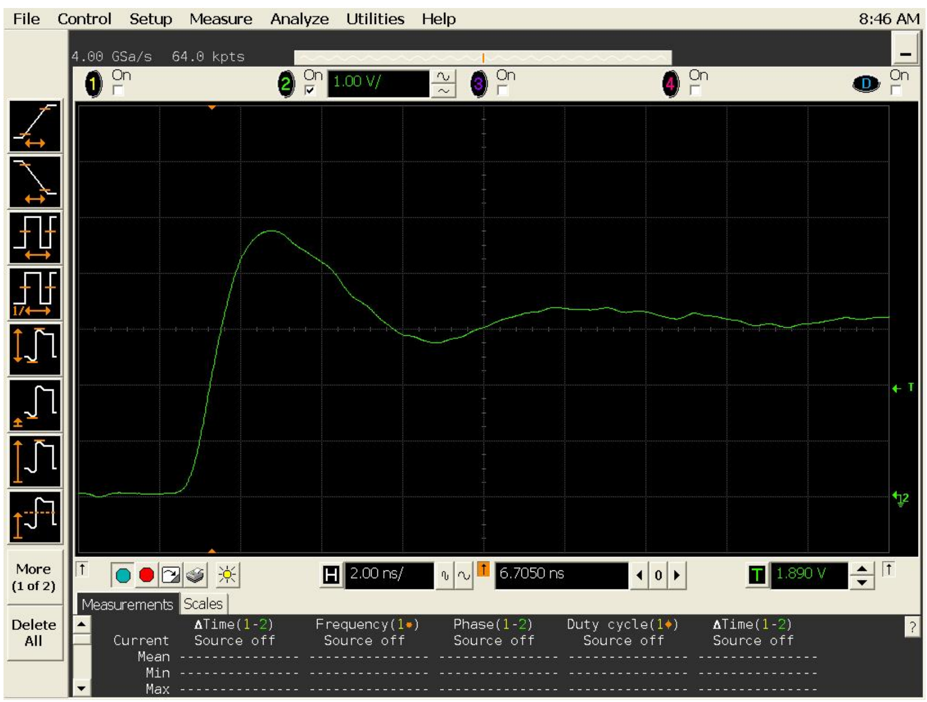

Figure 13b DUT 18281 Post-Annealing Rising Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

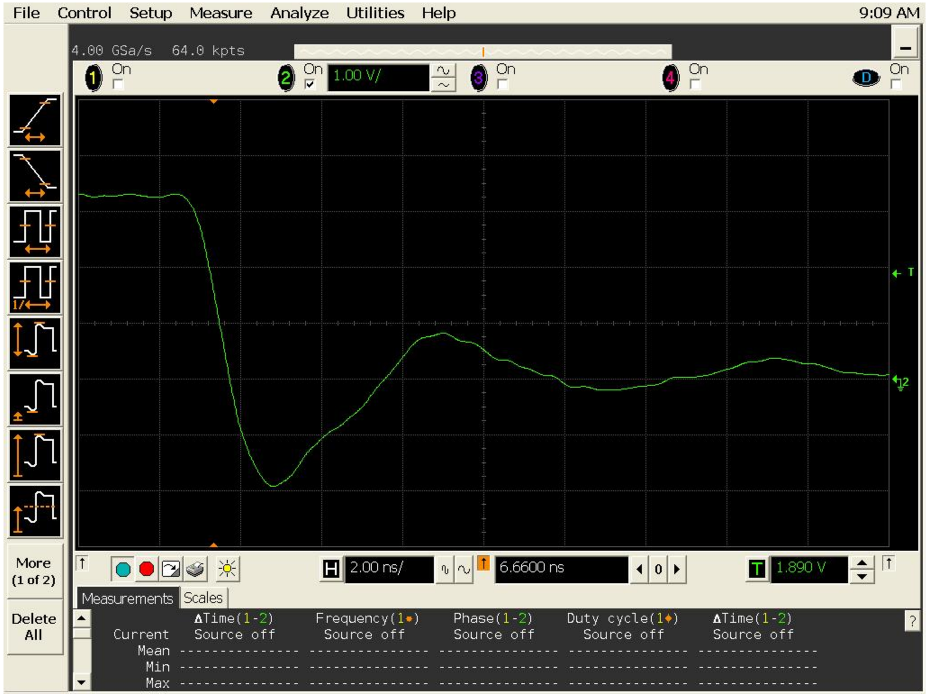

Figure 14a DUT 18267 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

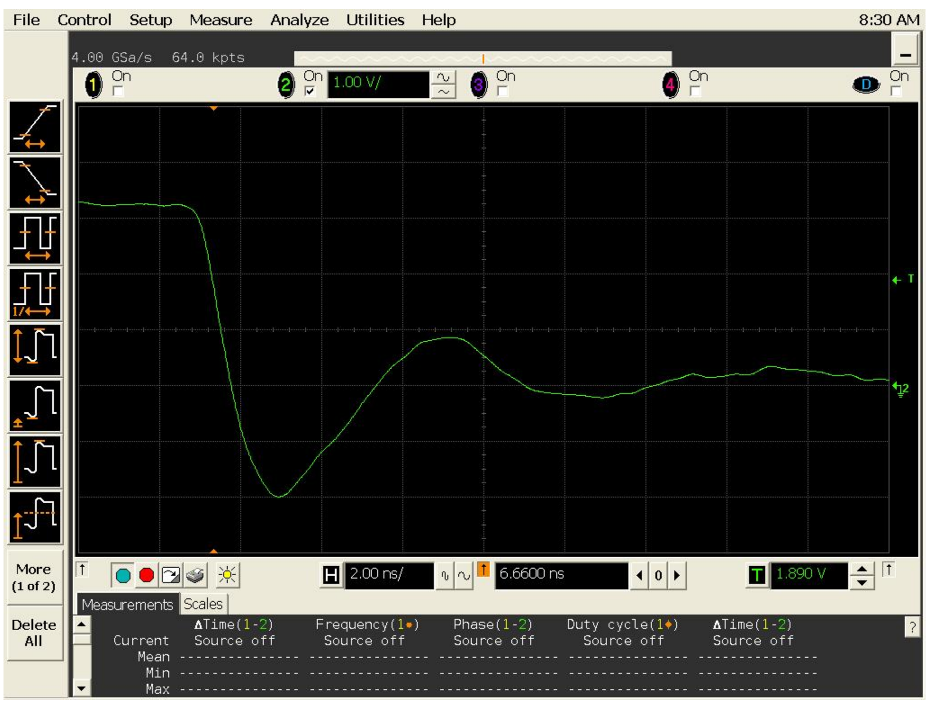

Figure 14b DUT 18267 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

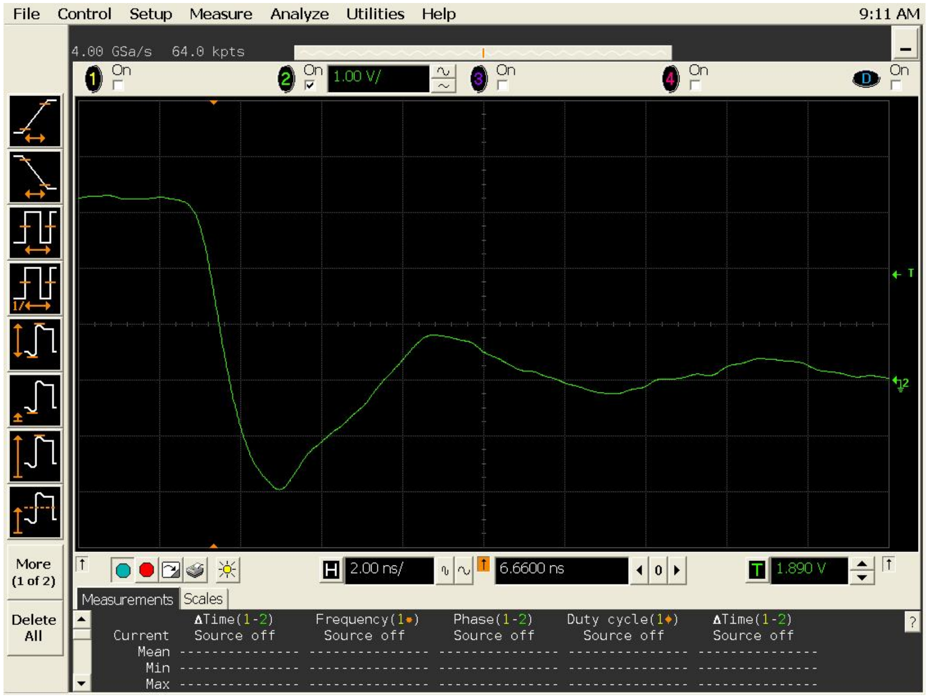

Figure 15a DUT 18268 Pre-Irradiation Falling Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

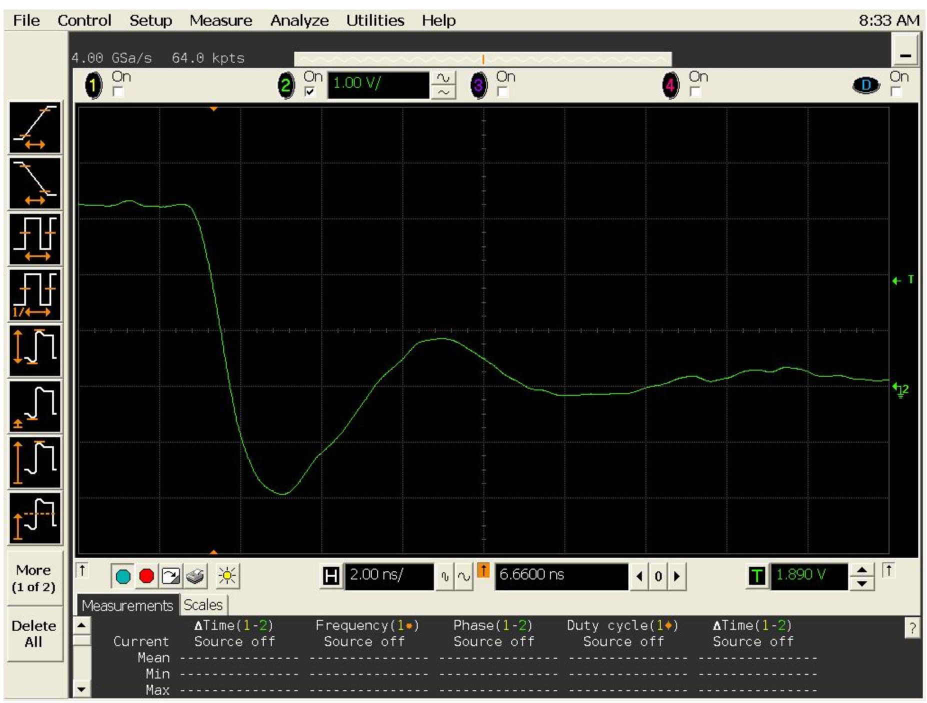

Figure 15b DUT 18268 Post-Annealing Falling Edge,
abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

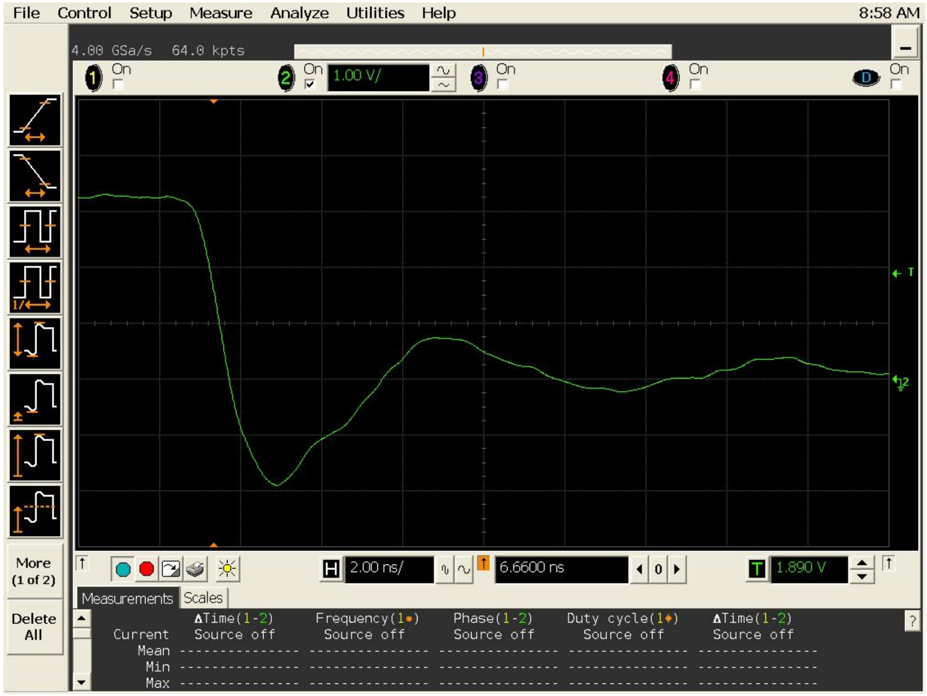

Figure 16a DUT 18270 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

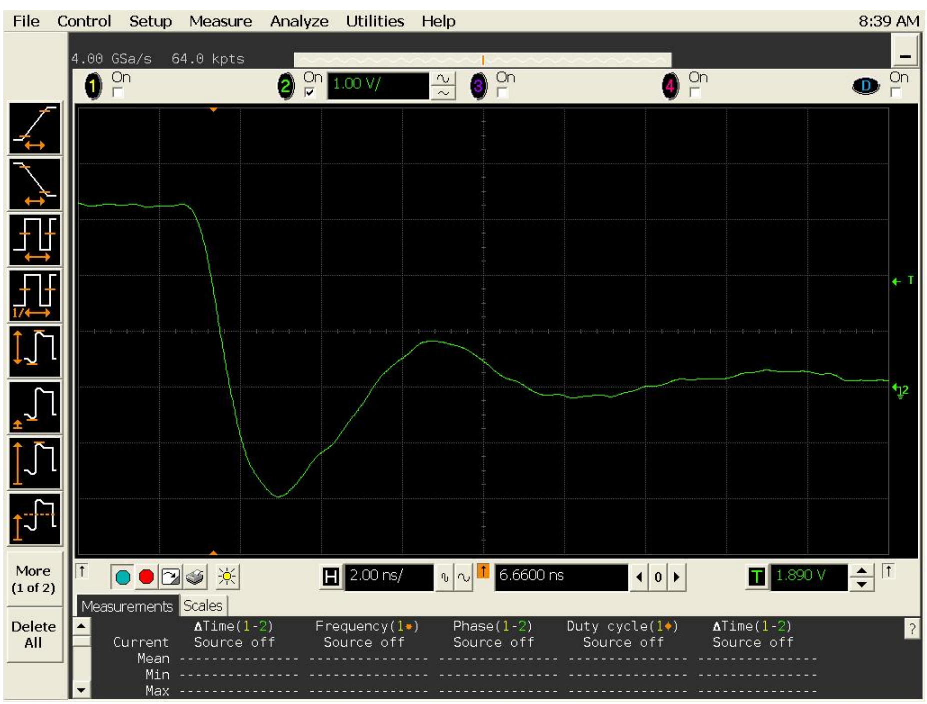

Figure 16b DUT 18270 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

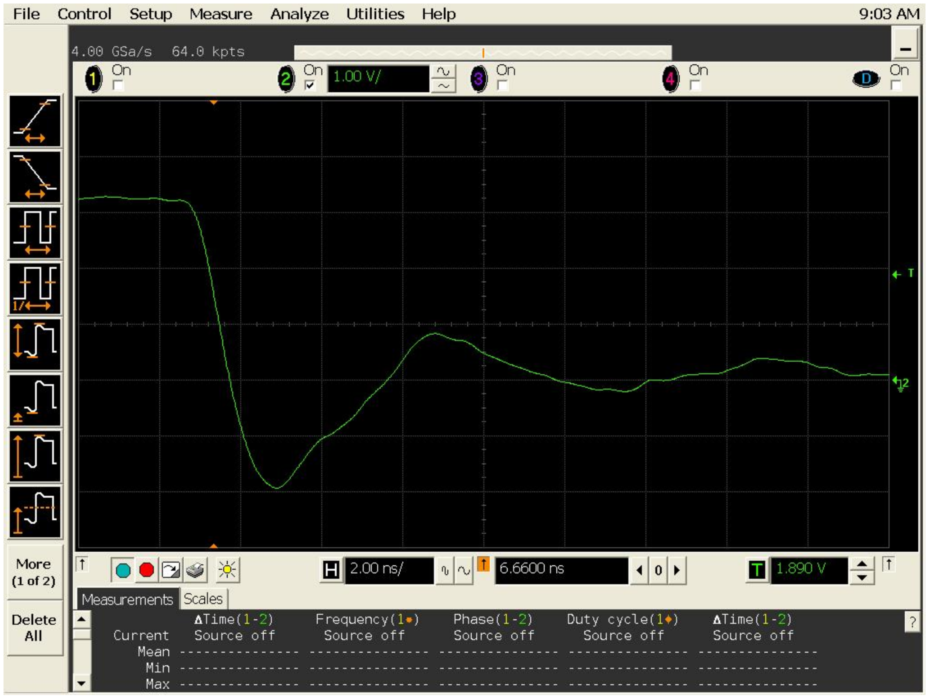

Figure 17a DUT 18273 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

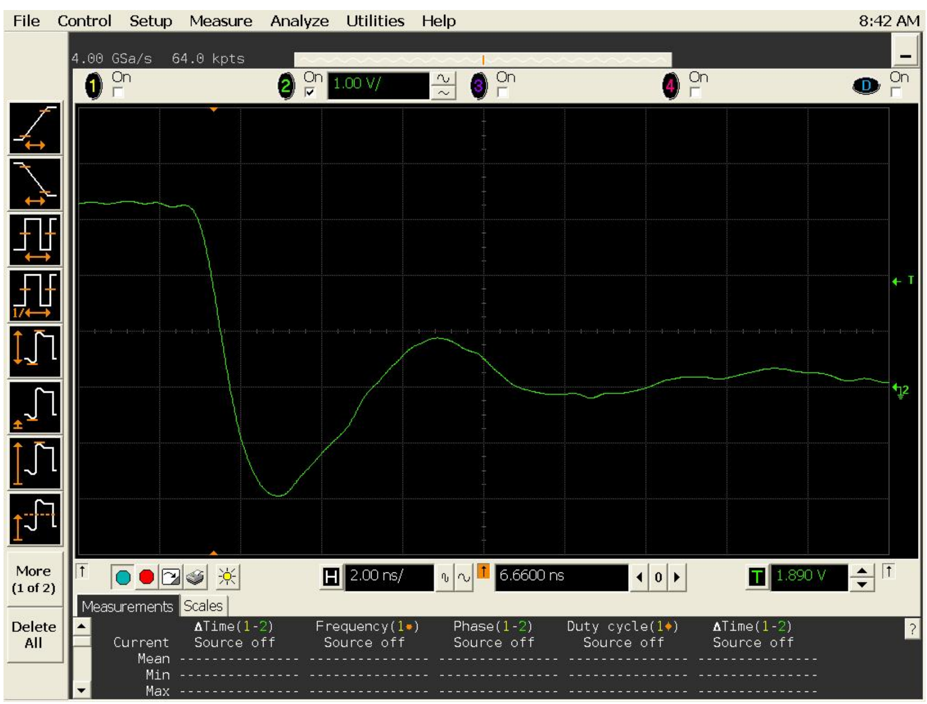

Figure 17b DUT 18273 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

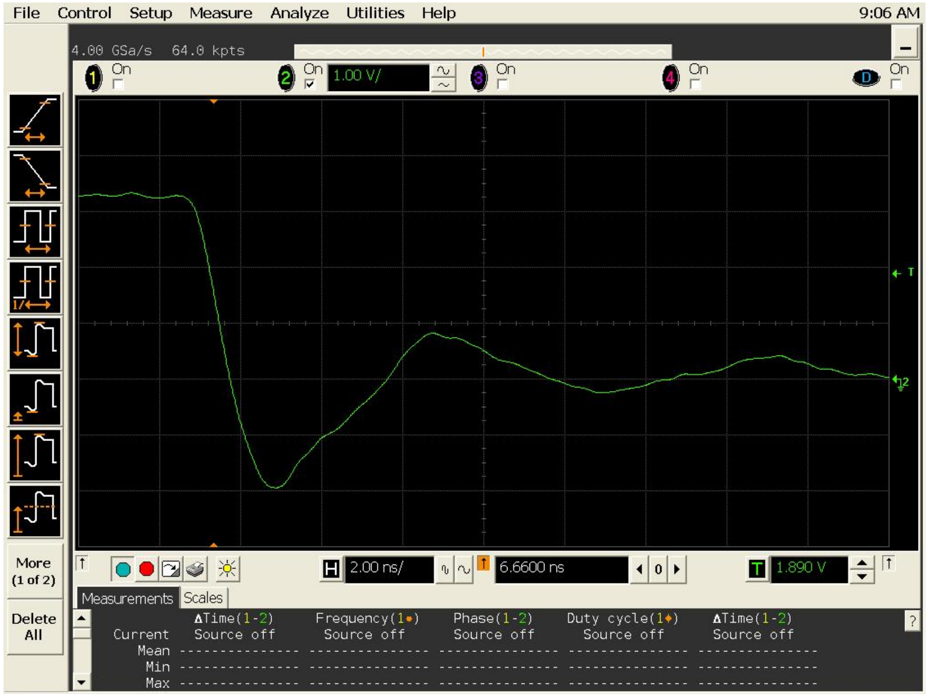

Figure 18a DUT 18279 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

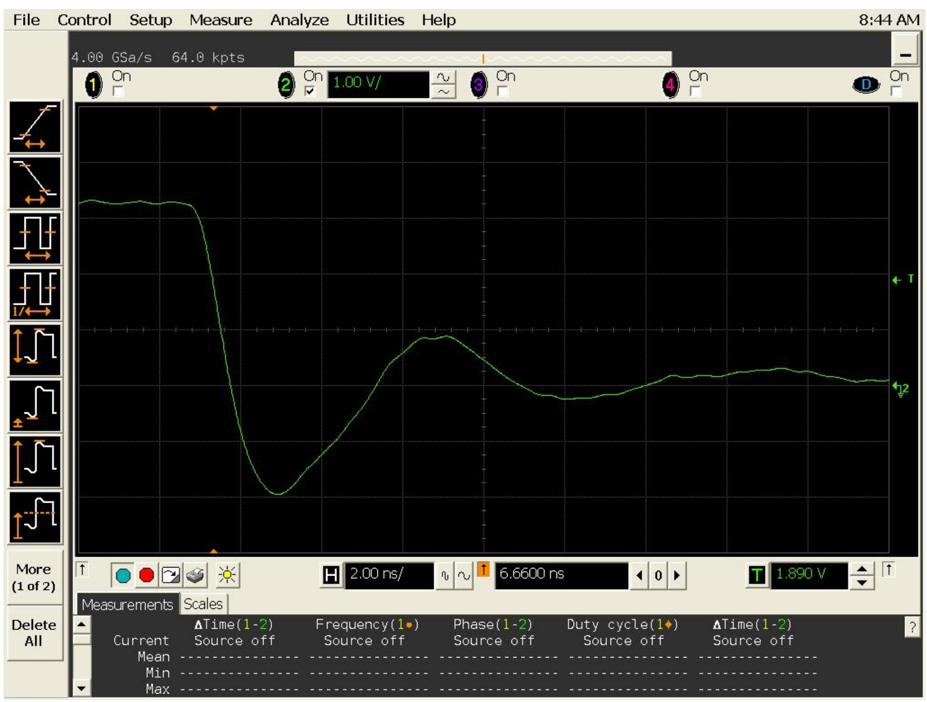

Figure 18b DUT 18279 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

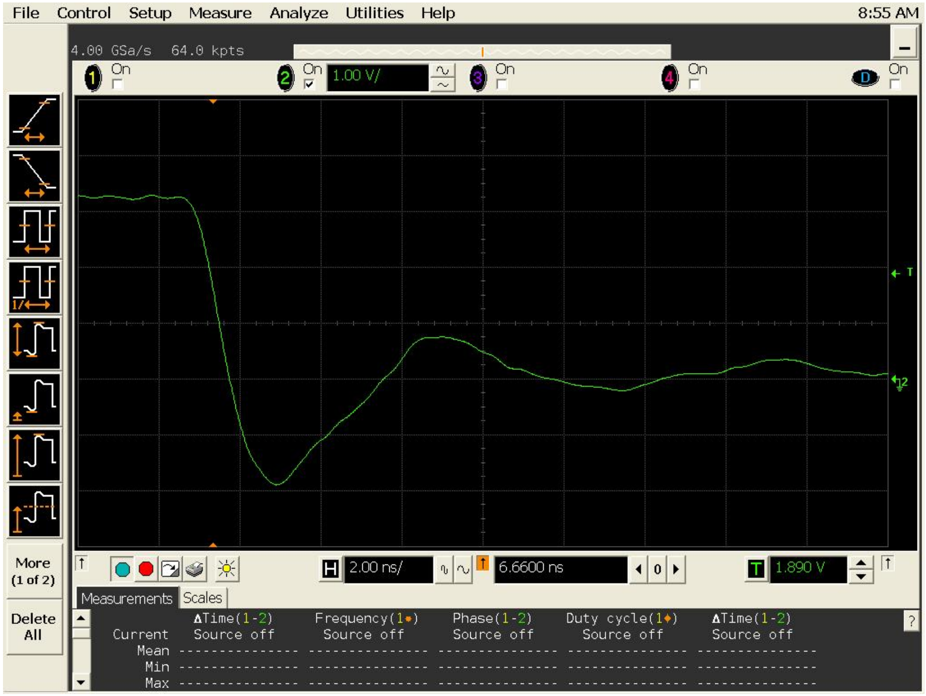

Figure 19a DUT 18281 Pre-Irradiation Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

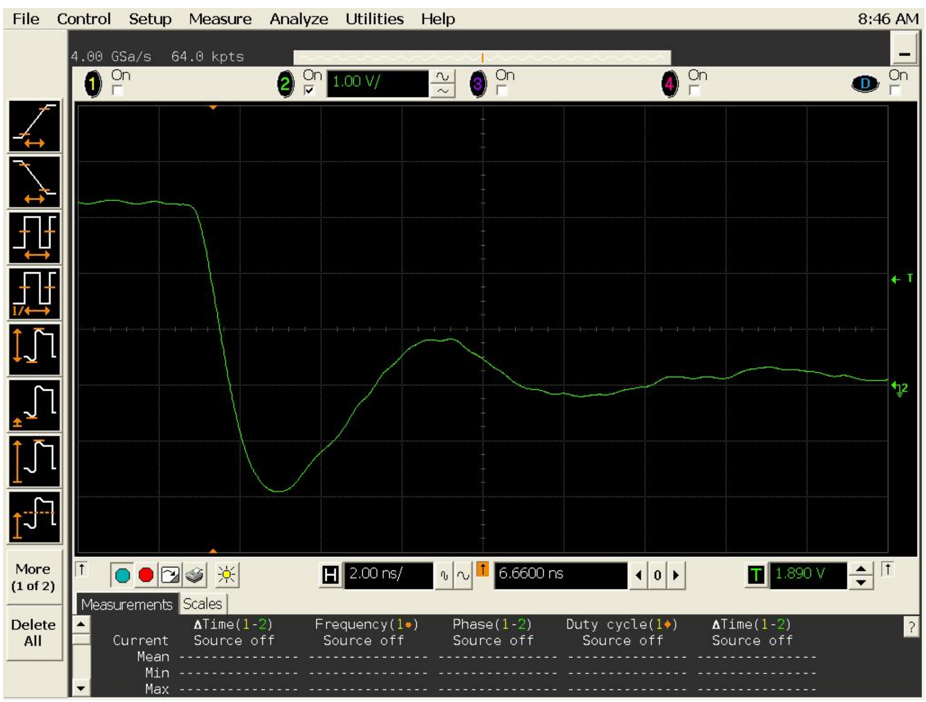

Figure 19b DUT 18281 Post-Annealing Falling Edge, abscissa scale is 1 V/div and ordinate scale is 2 ns/div.

Appendix A: DUT Bias Diagram

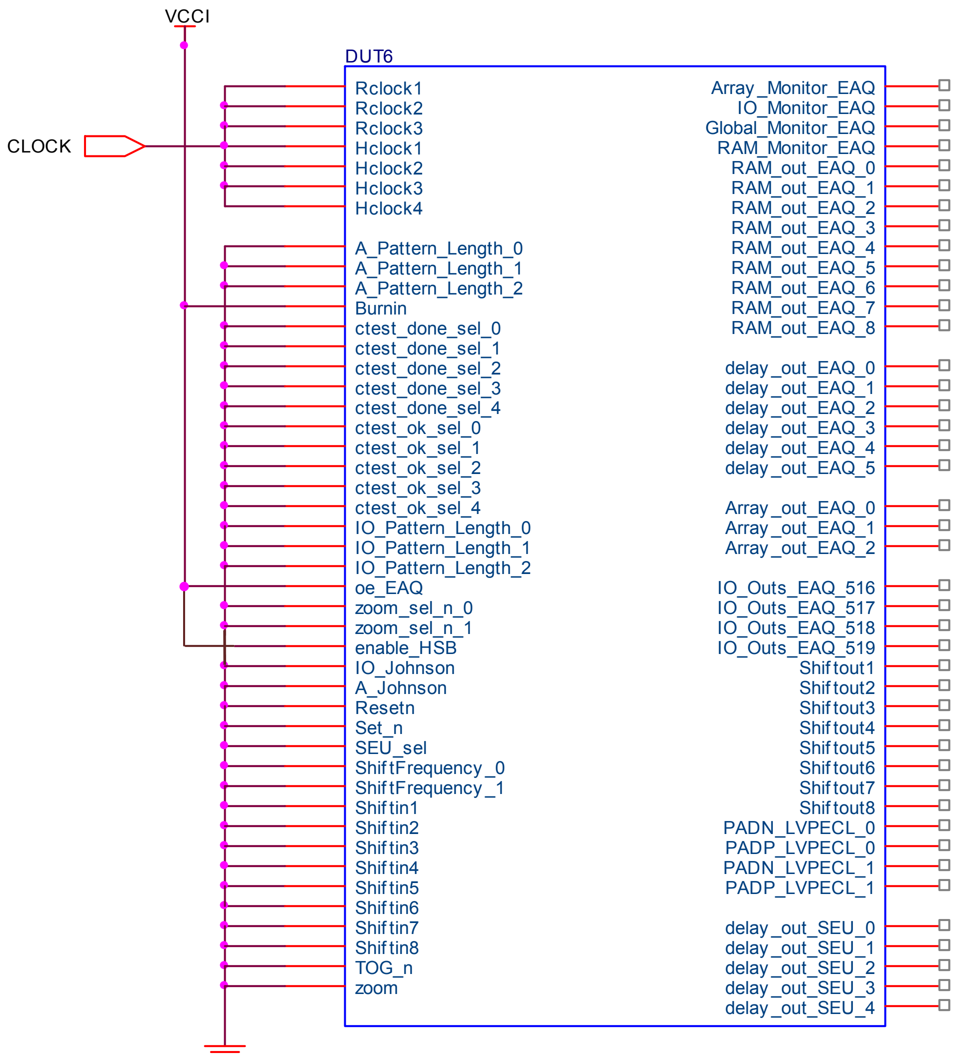

Figure A1 I/O Bias During Irradiation

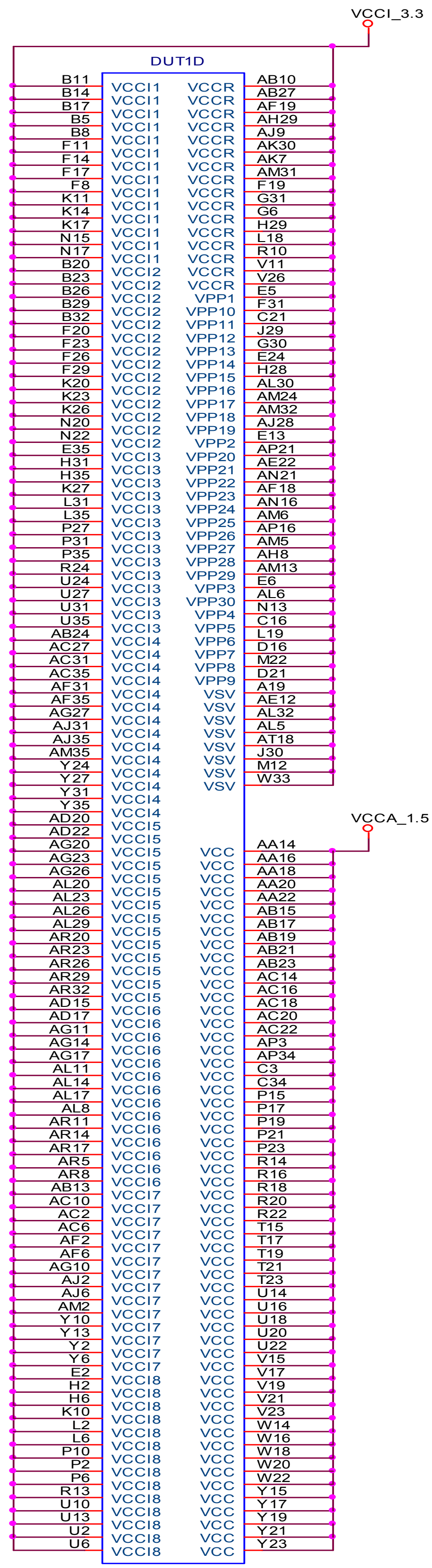

Figure A2 Power supply, Ground and Special Pins Bias During Irradiation

Appendix B: Functionality Tests

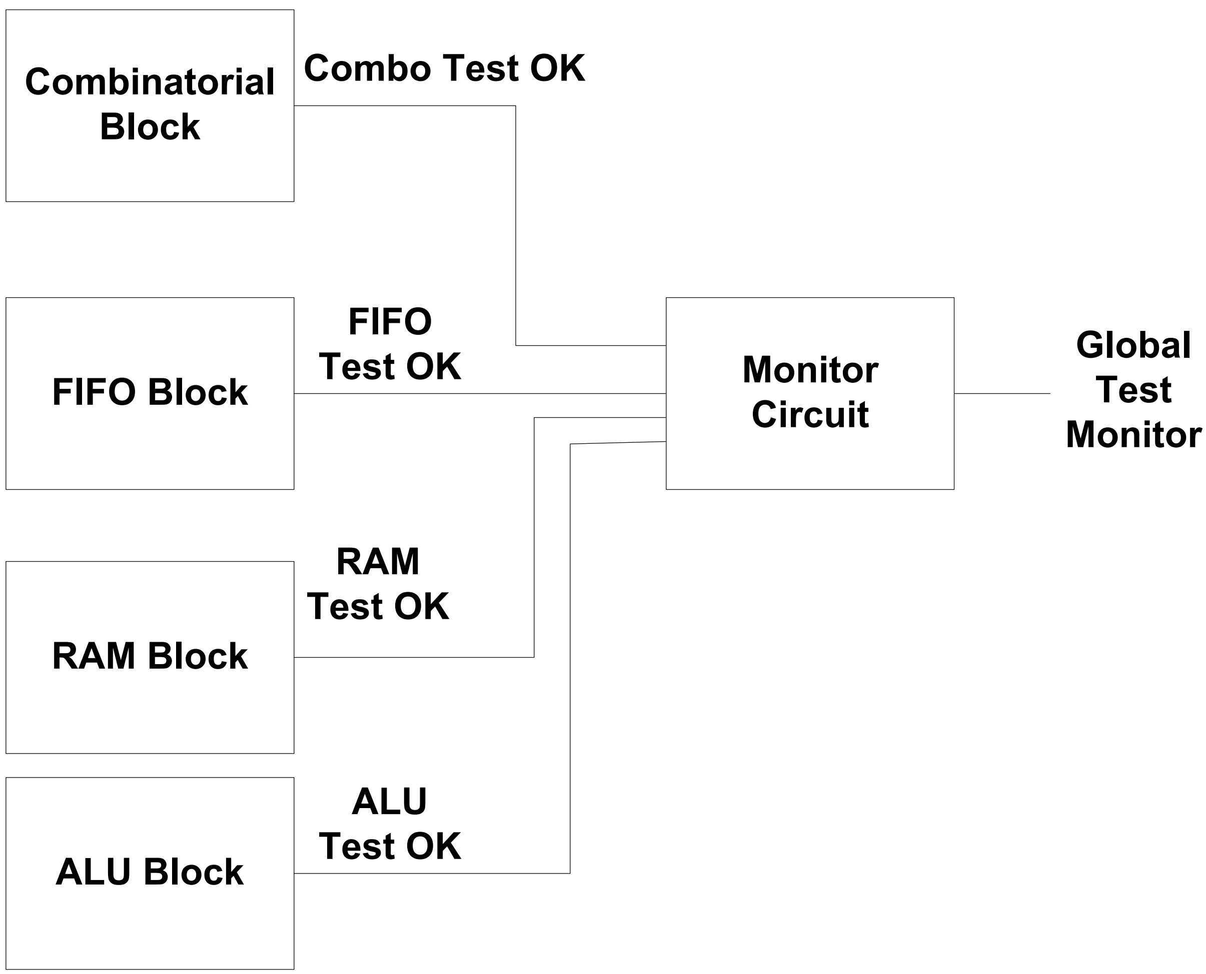

Figure B1 QBI Block – Top-Level Design

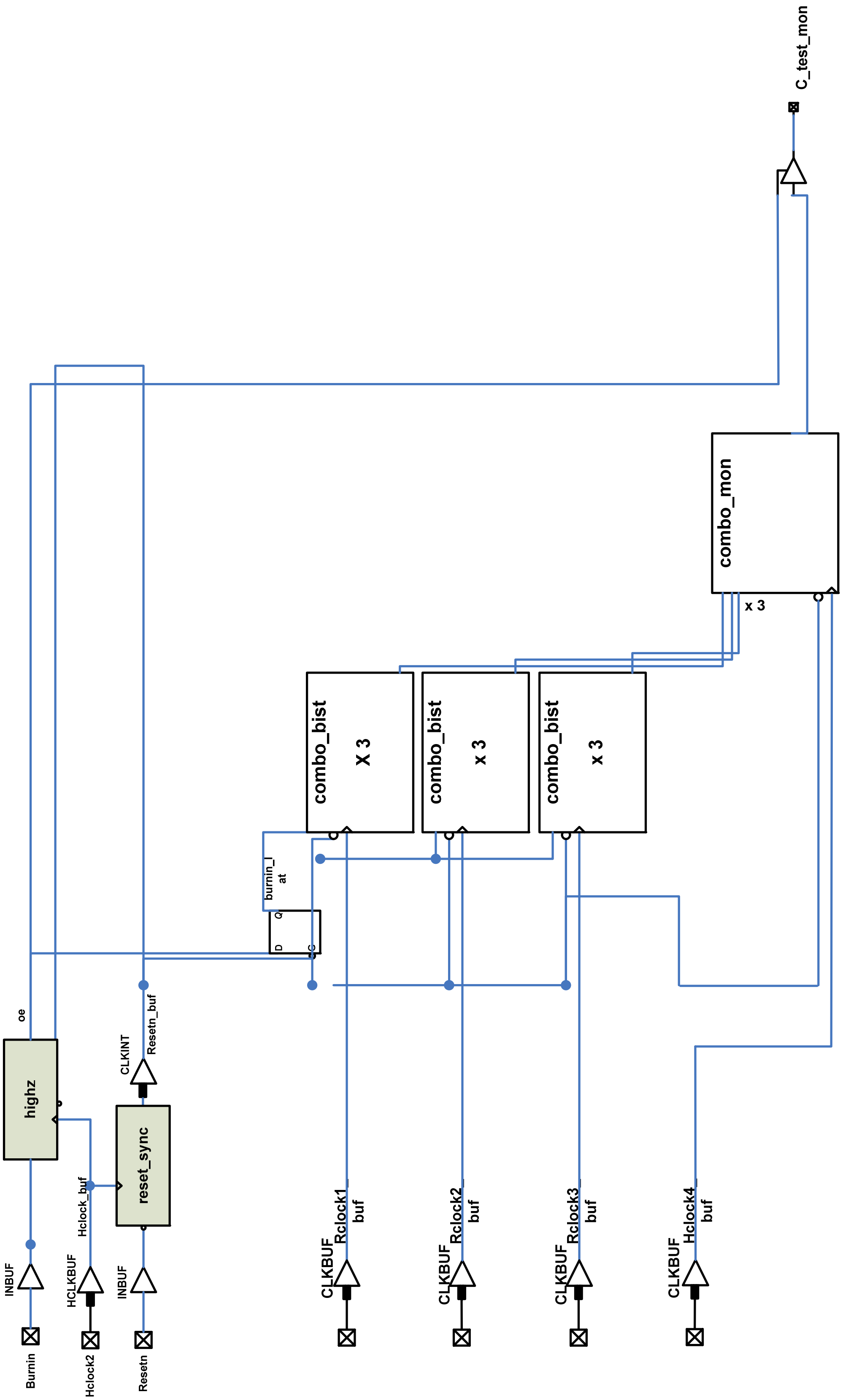

Figure B2 QBI Block – Combinatorial Test (Top Level)

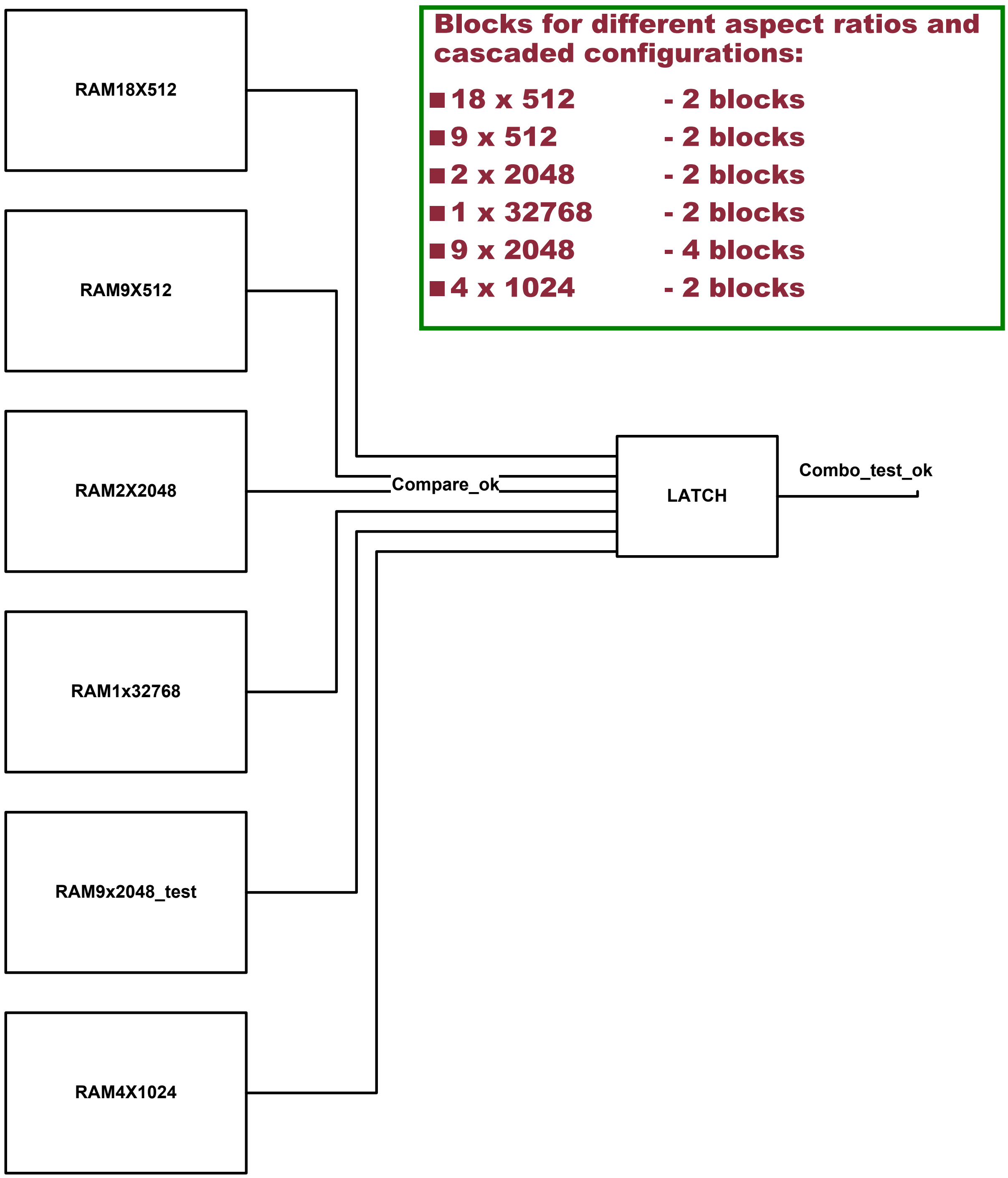

Figure B3 QBI Block – RAM Test (Top Level)

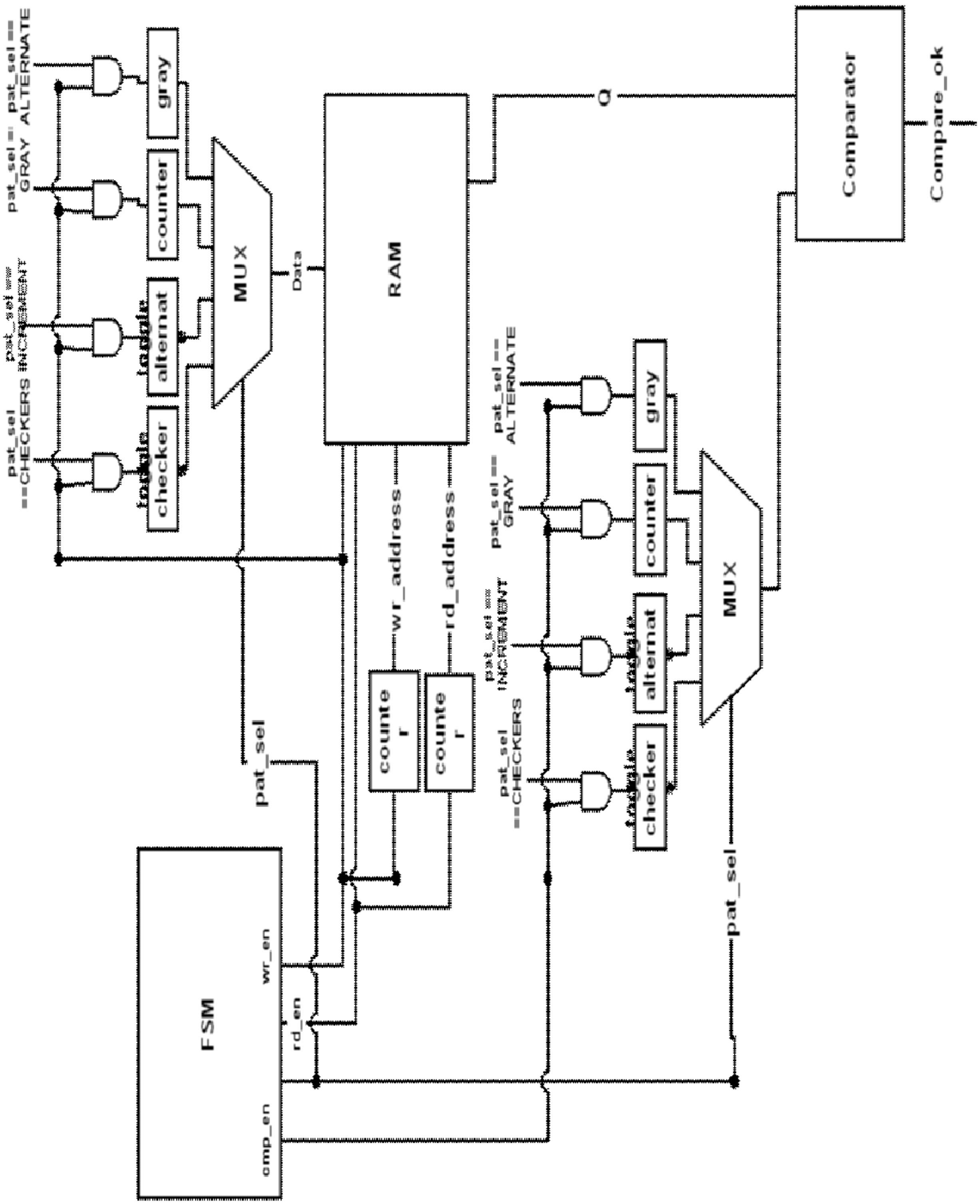

Figure B4 QBI Block – RAM Block

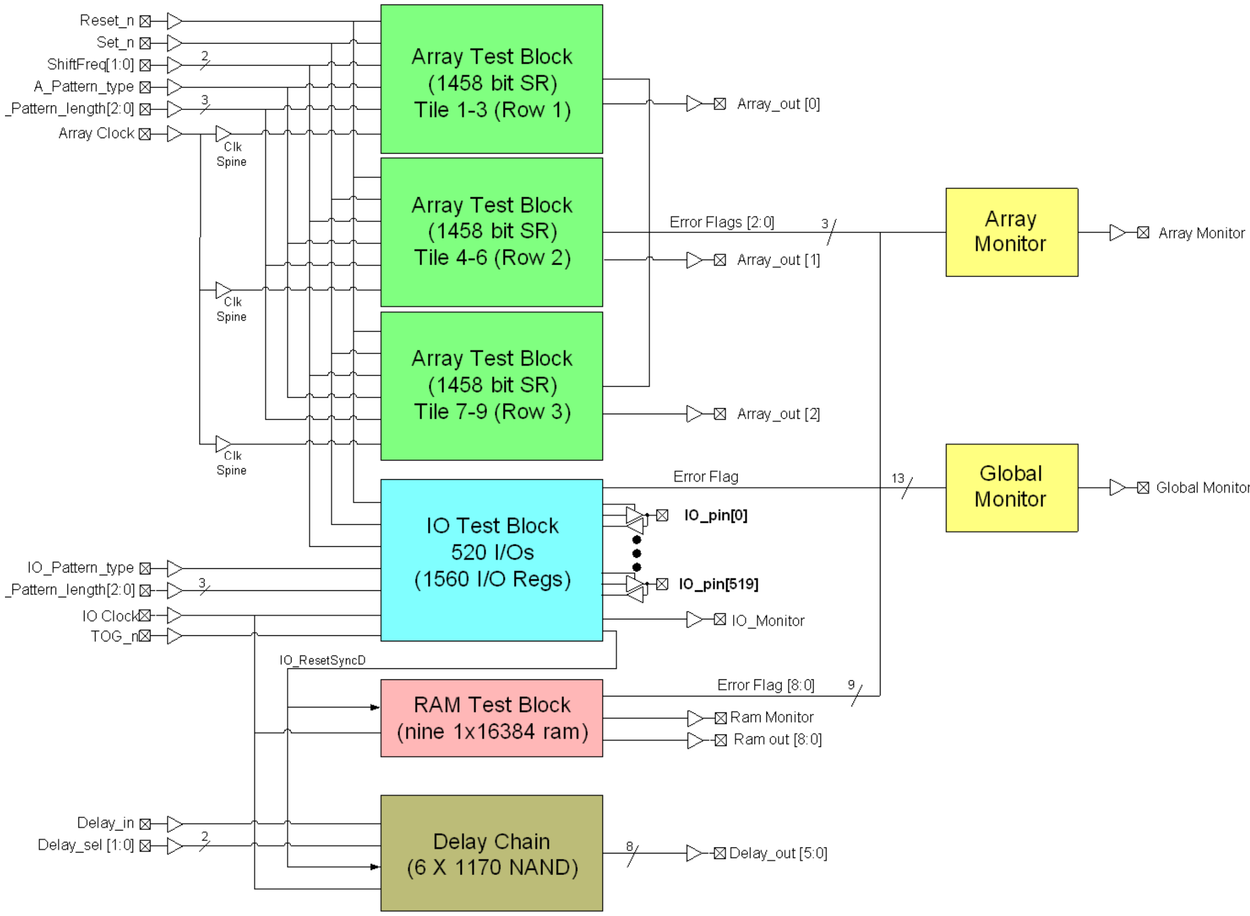

Figure B5 EAQ Block – Top Level

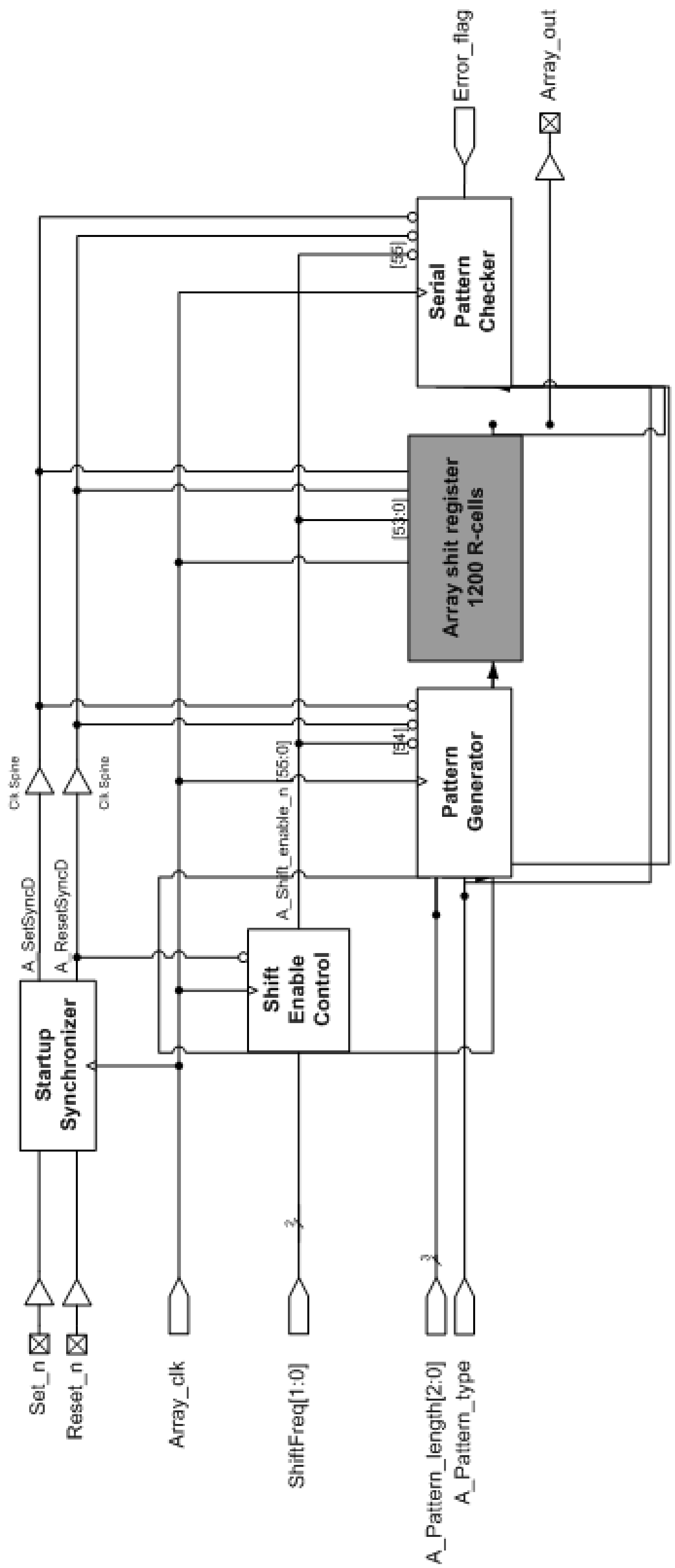

Figure B6 EAQ Block – Array Test (Shift Register)

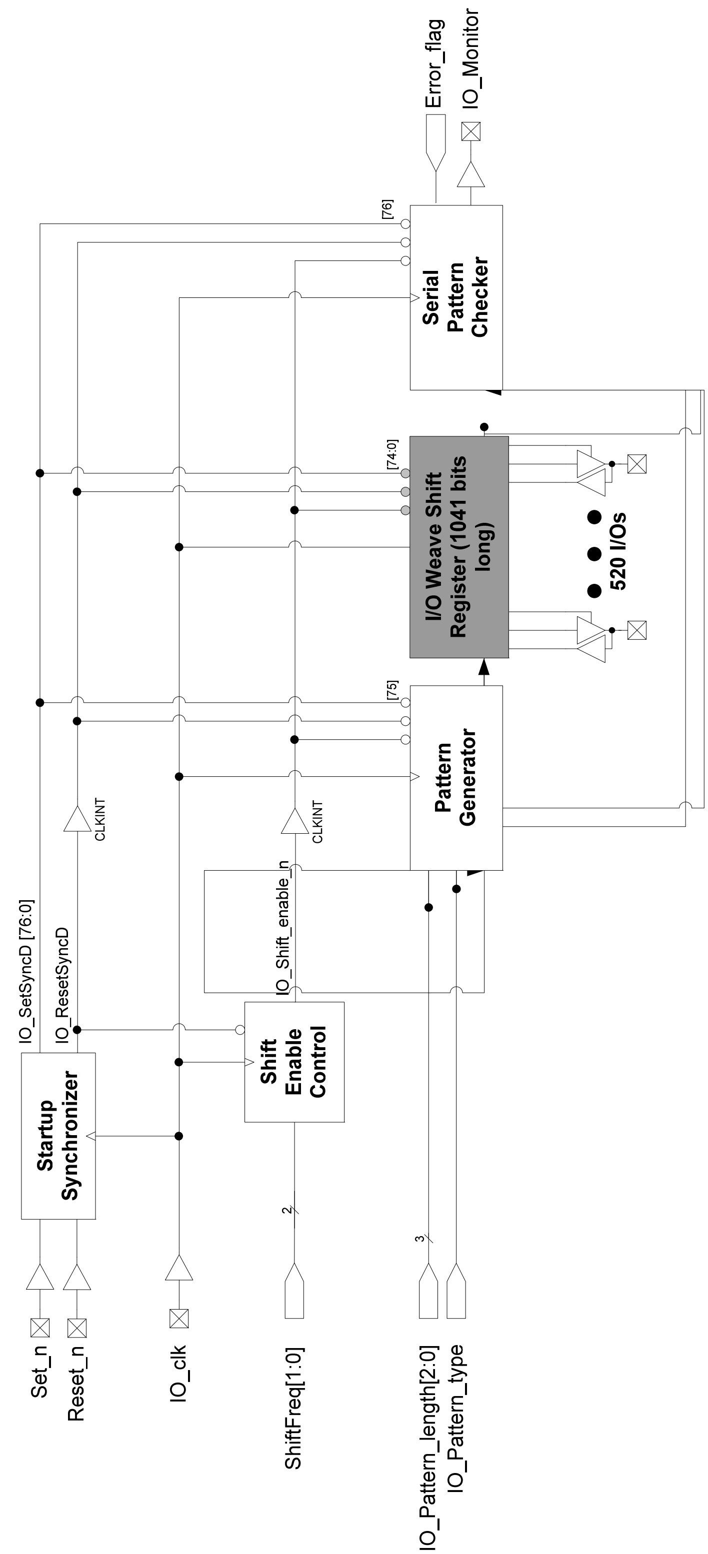

Figure B7 EAQ Block – I/O Test (Top Level)

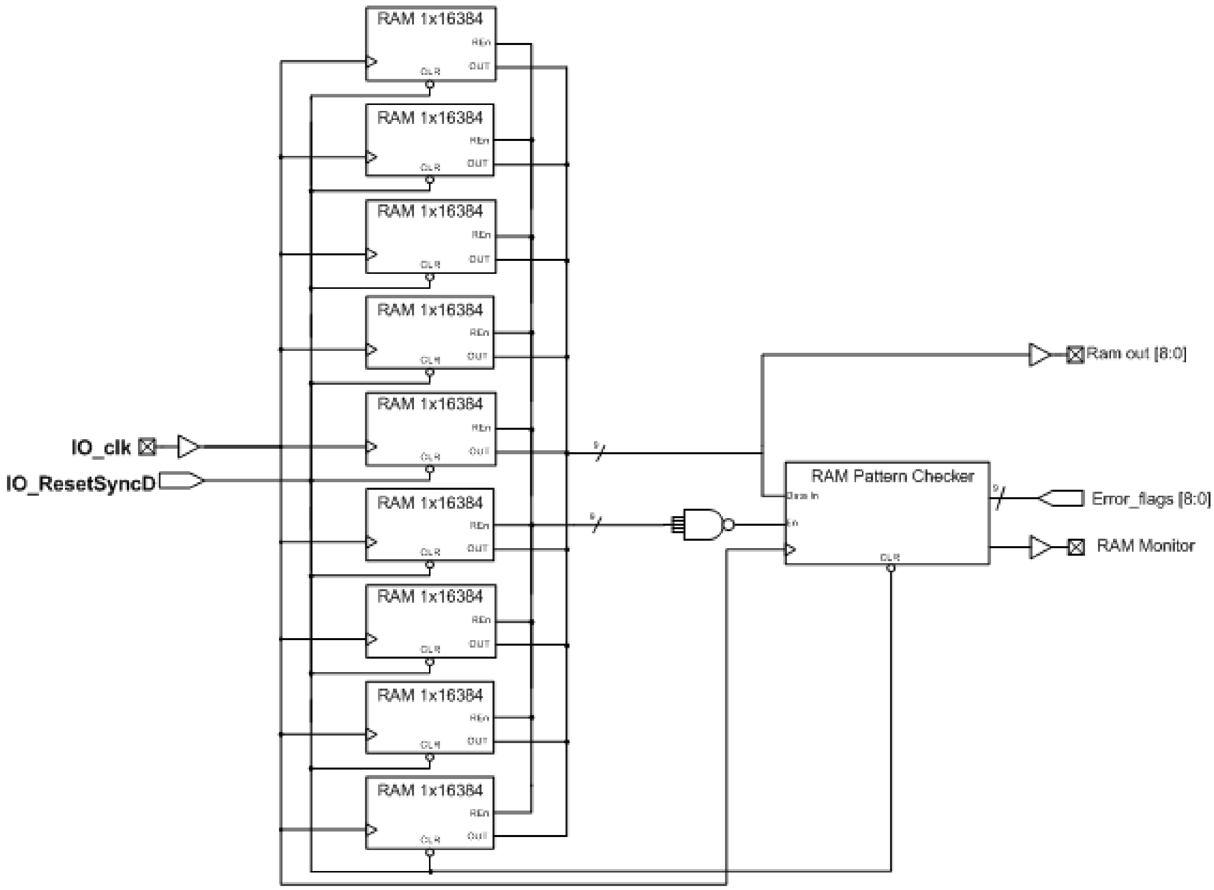

Figure B8 EAQ Block – SRAM Test (Top Level)

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