Total Ionizing Dose Test Report

No. 12T-RTAX2000S-CQ256-D58881

June 29, 2012

Table of Contents

TOTAL IONIZING DOSE TEST REPORT

No. 12T-RTAX2000S-CQ256-D58881

June 29, 2012

CK Huang and J.J. Wang

(408) 643-6136, (408) 643-6302

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 300 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Charateristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGA in http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded through a jumper; during annealing each input or output is tied to the ground or VCCI with a resistor. Appendix A contains the schematics of the irradiation-bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	EAQ_RTAX2000S_rev1
Die Lot Number	D58881
Quantity Tested	5
Serial Number	300 krad(SiO_2): 3000, 3002 200 krad(SiO_2): 3007, 3021, 3023
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	7.5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

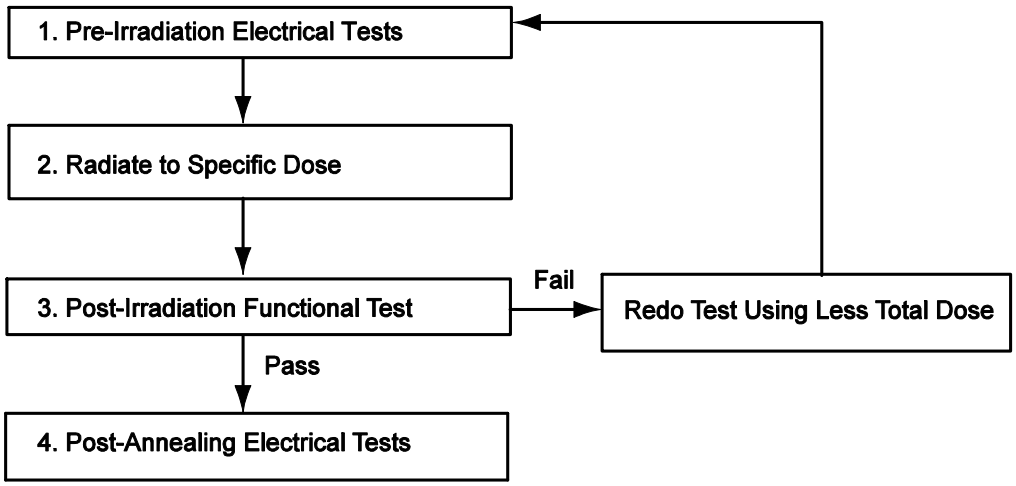


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000S are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization, generic design (EAQ_RTAX2000S_rev1) to evaluate total dose effects for typical space applications. Appendix B contains the schematics that illustrate this design.

Table 2 lists measured electrical parameters and the corresponding logic design. The functionality is measured on the output pins including the embedded RAM.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively.

The input logic threshold (VIL/VIH) is measured on inputs A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2, oe, Reset_n, Set_n, ShiftFrequency_0, ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1.

The output-drive voltage (VOL/VOH) is measured on Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0. The propagation delay is measured on the output of the buffer string; the definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output, are shown as oscilloscope captures.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key logic functions, and outputs of embedded RAM
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Inputs (A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2 , oe, Reset_n, Set_n, ShiftFrequency_0 , ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1)
4. Output Drive (V_{OL}/V_{OH})	Outputs (Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0)
5. Propagation Delay	String of buffers (IO_Clock to delay_out[0])
6. Transition Characteristic	String of buffers output (delay_out[0])

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT. Table 3 summarizes the pre-irradiation, post-irradiation and post-annealing ICC. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

Table 3 Pre-Irradiation, Post-Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad(SiO_2)	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
3000	300 krad	7	67	14	17	116	36
3002	300 krad	7	93	13	16	119	35
3007	200 krad	6	10	9	8	43	18
3021	200 krad	10	16	15	9	46	14
3023	200 krad	7	9	6	8	42	16

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the RTAXS datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT. Based on these PIPL, post-annealed DUT passes both the ICCA and ICCI specification for 300 krad (SiO2).

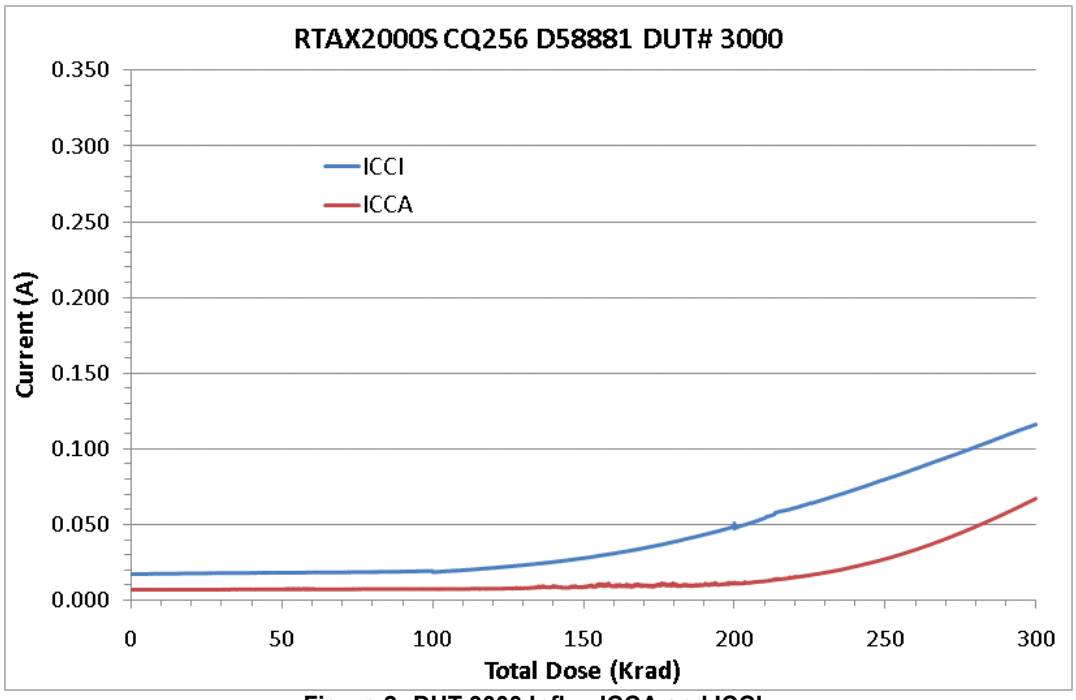


Figure 2 DUT 3000 Influx ICCA and ICCI

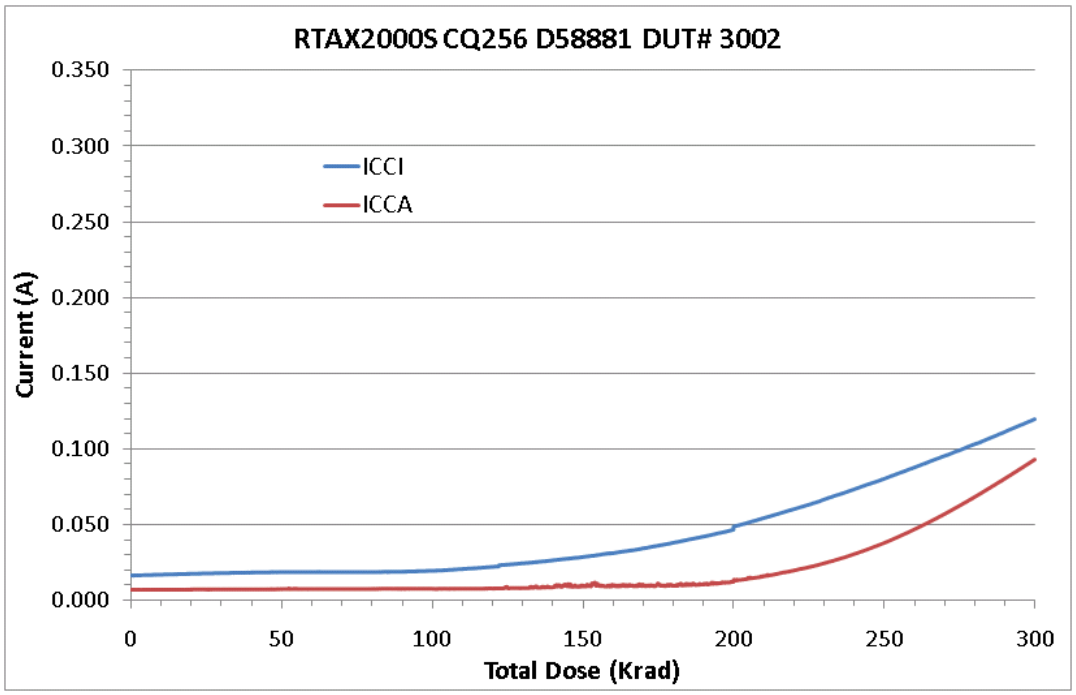


Figure 3 DUT 3002 Influx ICCA and ICCI

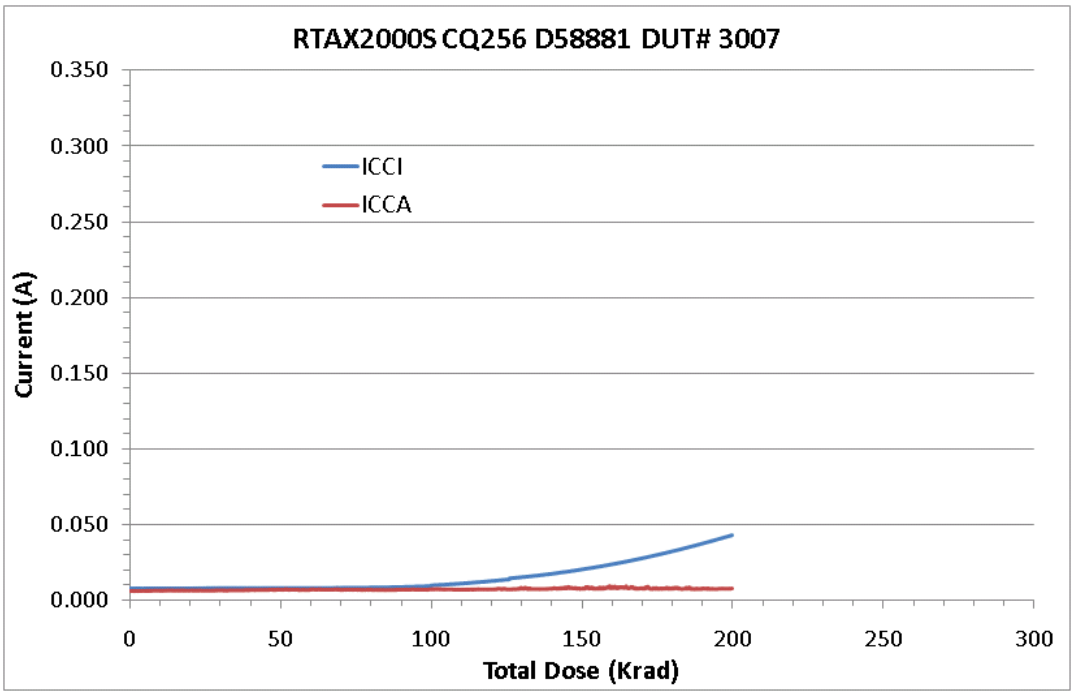


Figure 4 DUT 3007 Influx ICCA and ICCI

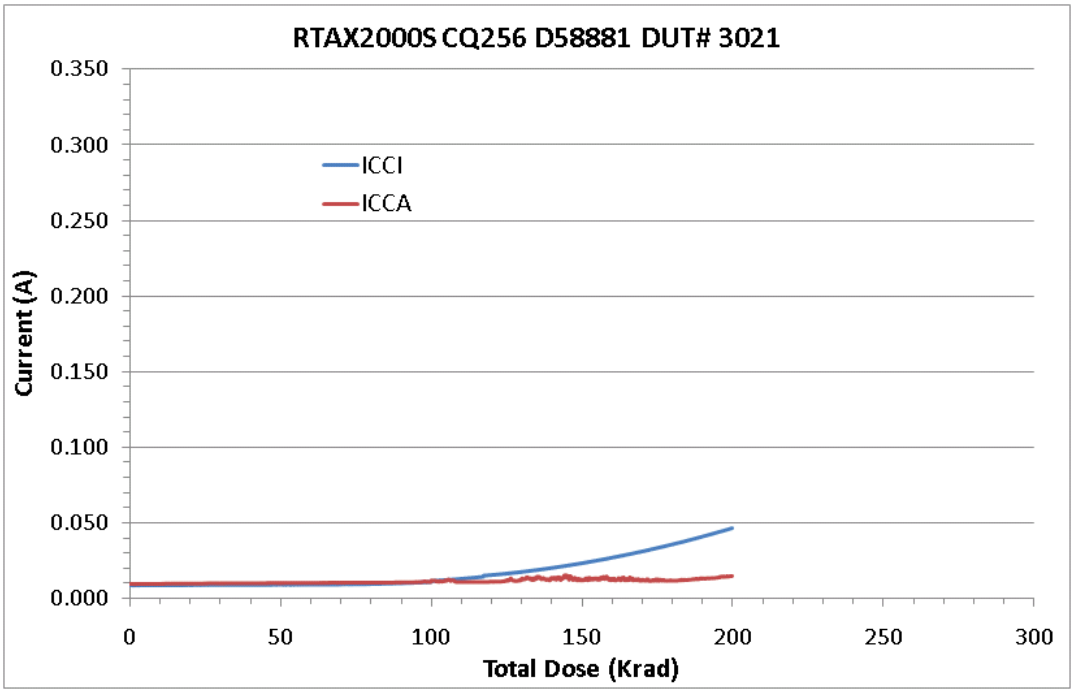


Figure 5 DUT 3021 Influx ICCA and ICCI

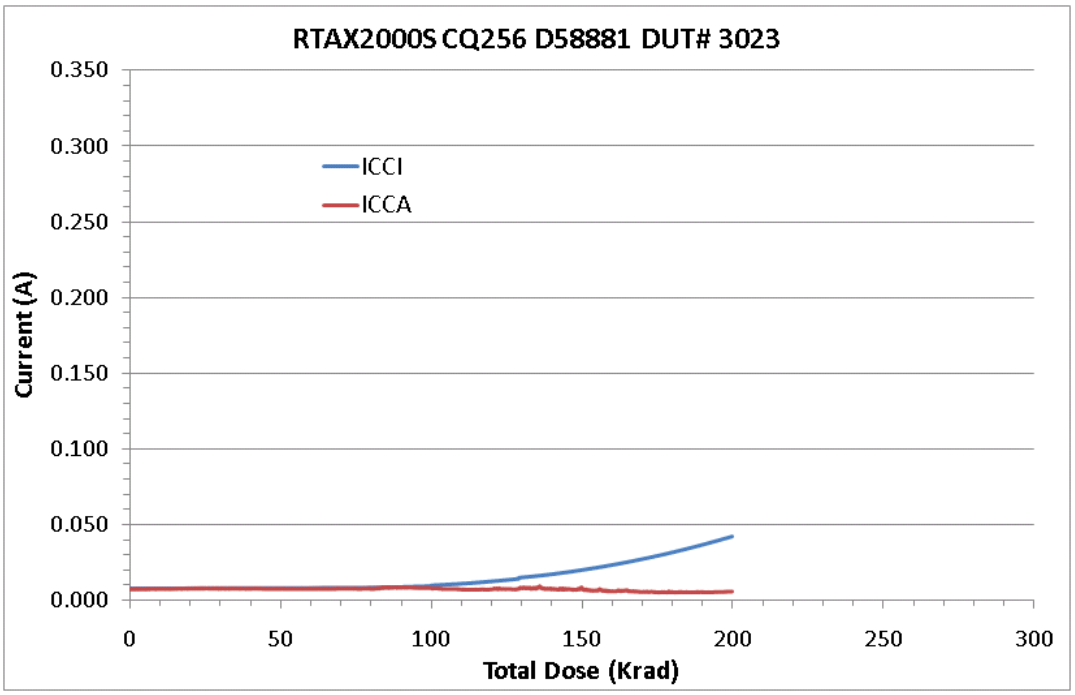


Figure 6 DUT 3023 Influx ICCA and ICCI

C. Input Threshold VIL

Table 4 lists the pre-irradiation and post-annealing single-ended input threshold. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds VIL (mV)

Pin\DUT	3000 (300 krad)		3002 (300 krad)		3007 (200 krad)		3021 (200 krad)		3023 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.375	1.370	1.375	1.370	1.380	1.375	1.380	1.370	1.375	1.370
A_Johnson	1.370	1.365	1.370	1.360	1.380	1.370	1.370	1.365	1.380	1.370
A_Pattern_Length_0	1.380	1.375	1.380	1.370	1.385	1.380	1.380	1.375	1.385	1.380
A_Pattern_Length_1	1.380	1.375	1.385	1.370	1.390	1.380	1.380	1.375	1.390	1.380
A_Pattern_Length_2	1.370	1.365	1.375	1.365	1.380	1.375	1.370	1.365	1.380	1.375
IO_Clock	1.370	1.365	1.370	1.360	1.375	1.370	1.370	1.365	1.370	1.365
IO_Johnson	1.380	1.375	1.385	1.370	1.385	1.380	1.380	1.375	1.390	1.380
IO_Pattern_Length_0	1.370	1.365	1.370	1.360	1.375	1.370	1.370	1.360	1.380	1.370
IO_Pattern_Length_1	1.370	1.360	1.370	1.365	1.375	1.370	1.370	1.365	1.380	1.370
IO_Pattern_Length_2	1.375	1.370	1.375	1.370	1.390	1.380	1.380	1.375	1.385	1.380
oe	1.375	1.370	1.375	1.370	1.380	1.375	1.375	1.370	1.380	1.375
Reset_n	1.375	1.370	1.375	1.370	1.380	1.375	1.375	1.370	1.380	1.375
Set_n	1.365	1.360	1.365	1.360	1.370	1.365	1.365	1.360	1.365	1.360
ShiftFrequency_0	1.380	1.370	1.380	1.370	1.380	1.375	1.375	1.370	1.380	1.375
ShiftFrequency_1	1.375	1.370	1.380	1.370	1.380	1.375	1.380	1.375	1.385	1.375
TOG_n	1.380	1.375	1.380	1.370	1.380	1.375	1.380	1.375	1.380	1.375
zoom	1.385	1.380	1.385	1.380	1.385	1.380	1.390	1.380	1.390	1.380
zoom_sel_n_0	1.370	1.355	1.370	1.355	1.375	1.365	1.370	1.355	1.375	1.360
zoom_sel_n_1	1.370	1.350	1.375	1.350	1.375	1.360	1.370	1.355	1.375	1.360

D. Input Threshold VIH

Table 5 lists the input threshold voltage changes due to irradiations. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing Input Thresholds VIH (mV)

Pin\DUT	3000 (300 krad)		3002 (300 krad)		3007 (200 krad)		3021 (200 krad)		3023 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.640	1.635	1.645	1.630	1.650	1.640	1.645	1.635	1.645	1.635
A_Johnson	1.665	1.655	1.665	1.650	1.670	1.660	1.665	1.655	1.670	1.665
A_Pattern_Length_0	1.650	1.640	1.650	1.635	1.655	1.645	1.650	1.640	1.660	1.650
A_Pattern_Length_1	1.650	1.640	1.655	1.635	1.660	1.650	1.650	1.640	1.660	1.650
A_Pattern_Length_2	1.665	1.655	1.670	1.650	1.670	1.665	1.665	1.655	1.670	1.665
IO_Clock	1.665	1.655	1.665	1.655	1.670	1.660	1.665	1.655	1.665	1.660
IO_Johnson	1.650	1.640	1.655	1.635	1.655	1.650	1.650	1.645	1.660	1.650
IO_Pattern_Length_0	1.660	1.650	1.665	1.645	1.670	1.660	1.660	1.650	1.670	1.660
IO_Pattern_Length_1	1.660	1.650	1.665	1.650	1.670	1.660	1.665	1.655	1.670	1.660
IO_Pattern_Length_2	1.645	1.640	1.645	1.635	1.660	1.650	1.650	1.640	1.655	1.650
oe	1.645	1.635	1.645	1.635	1.650	1.640	1.645	1.635	1.650	1.640
Reset_n	1.640	1.630	1.640	1.635	1.645	1.635	1.645	1.635	1.645	1.635
Set_n	1.655	1.650	1.655	1.650	1.665	1.655	1.660	1.650	1.660	1.650
ShiftFrequency_0	1.645	1.640	1.650	1.635	1.650	1.640	1.650	1.640	1.650	1.640
ShiftFrequency_1	1.645	1.635	1.645	1.635	1.650	1.640	1.645	1.640	1.655	1.645
TOG_n	1.645	1.635	1.650	1.635	1.650	1.640	1.650	1.640	1.650	1.640
zoom	1.655	1.645	1.655	1.645	1.655	1.650	1.660	1.650	1.660	1.650
zoom_sel_n_0	1.660	1.635	1.665	1.635	1.670	1.650	1.660	1.645	1.665	1.650
zoom_sel_n_1	1.660	1.635	1.665	1.635	1.665	1.650	1.660	1.645	1.670	1.650

E. Output-Drive Voltage (VOL)

The pre-irradiation and post-annealing VOL are listed in Table 6. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 6 Pre-Irradiation and Post-Annealing Output-Drive VOL (mV)

Pin\DUT	3000 (300 krad)		3002 (300 krad)		3007 (200 krad)		3021 (200 krad)		3023 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	187.5	181.2	188.7	181.5	190.1	183.5	186.8	181.2	189.9	183.9
Array_out_0	179.9	175.1	181.1	177.4	182.6	178.9	179.7	176.6	182.1	178.0
delay_out_0	190.5	181.7	189.5	181.3	189.8	182.7	184.1	181.1	191.4	183.7
Global_Monitor	188.7	183.2	190.0	184.7	191.2	185.6	188.5	183.2	191.1	185.4
IO_Monitor	183.2	176.6	184.9	178.3	185.9	180.0	183.0	178.3	185.9	180.2
IO_Outs_0	183.0	180.7	183.4	181.3	186.0	183.8	182.3	179.8	186.8	183.8
RAM_Monitor	191.6	184.3	193.8	187.7	194.1	188.0	192.6	187.5	194.0	188.4
RAM_out_0	188.1	198.3	188.8	198.3	189.2	197.5	187.1	197.4	195.8	200.8

F. Output-Drive Voltage (VOH)

The pre-irradiation and post-annealing VOH are listed in Table 7. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 7 Pre-Irradiation and Post-Annealing Output-Drive VOH (mV)

Pin\DUT	3000 (300 krad)		3002 (300 krad)		3007 (200 krad)		3021 (200 krad)		3023 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	2723	2721	2721	2720	2721	2720	2726	2724	2721	2721
Array_out_0	2730	2725	2727	2723	2726	2723	2731	2728	2728	2725
delay_out_0	2724	2723	2724	2723	2724	2724	2727	2727	2722	2723
Global_Monitor	2722	2720	2720	2717	2719	2718	2724	2723	2720	2719
IO_Monitor	2726	2724	2724	2721	2723	2722	2727	2726	2724	2723
IO_Outs_0	2725	2725	2723	2722	2722	2721	2727	2726	2723	2722
RAM_Monitor	2718	2717	2715	2713	2716	2715	2720	2719	2716	2716
RAM_out_0	2726	2712	2725	2711	2723	2708	2728	2715	2724	2711

G. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The irradiation was temporarily stopped at each total-dose increment of 100 krad for the measurement. Each measurement has a 2-minute wait after a DUT is removed from the chamber. The results are plotted in Figure 7, and listed in Table 8. As shown in Figure 7, the propagation delay initially decreases with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots, a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

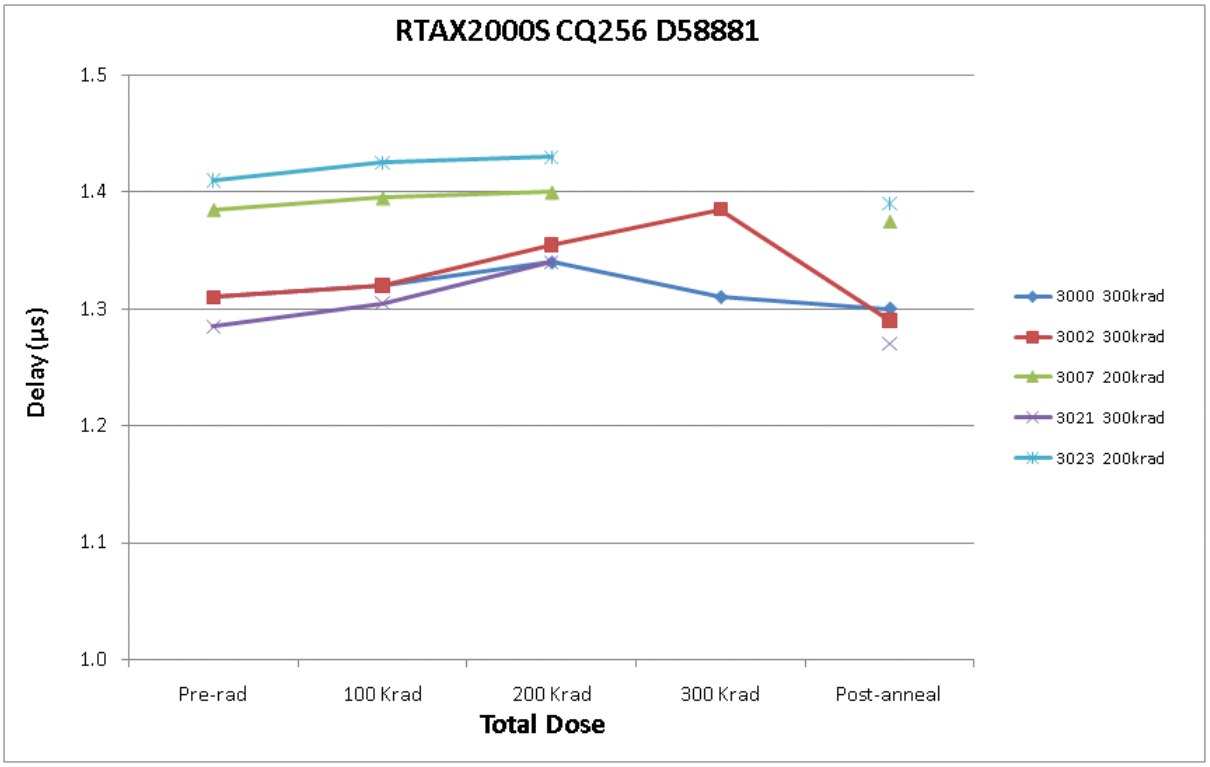


Figure 7 In-Situ Propagation Delay versus Total Dose
The measurement is performed outside the irradiation chamber.

Table 8 Radiation-Induced Propagation-Delay Degradations

	RTAX2000S D58881 CQ256						
Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	3000	300 krad	1.31	1.32	1.34	1.31	1.30
	3002	300 krad	1.31	1.32	1.36	1.39	1.29
	3007	200 krad	1.39	1.40	1.40	-	1.38
	3021	200 krad	1.29	1.31	1.34	-	1.27
	3023	200 krad	1.41	1.43	1.43	-	1.39
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	3000	300 krad	-	0.76%	2.29%	0.00%	-0.76%
	3002	300 krad	-	0.76%	3.44%	5.73%	-1.53%
	3007	200 krad	-	0.72%	1.08%	-	-0.72%
	3021	200 krad	-	1.56%	4.28%	-	-1.17%
	3023	200 krad	-	1.06%	1.42%	-	-1.42%

H. Transition Characteristics

Figure 8a to Figure 17b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

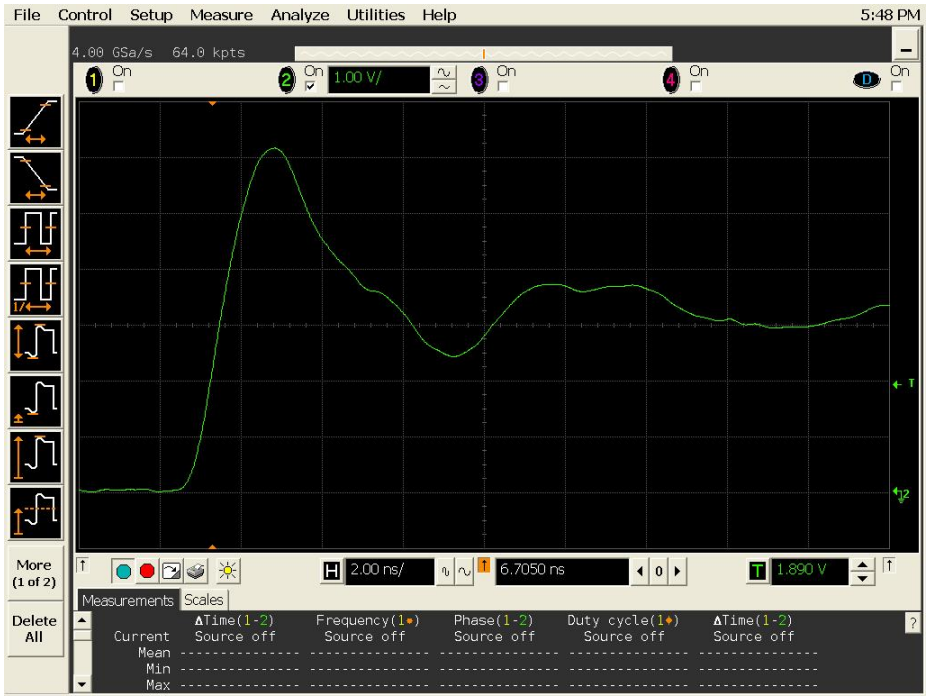


Figure 8a DUT 3000 Pre-Irradiation Rising Edge

Figure 8b DUT 3000 Post-Annealing Rising Edge

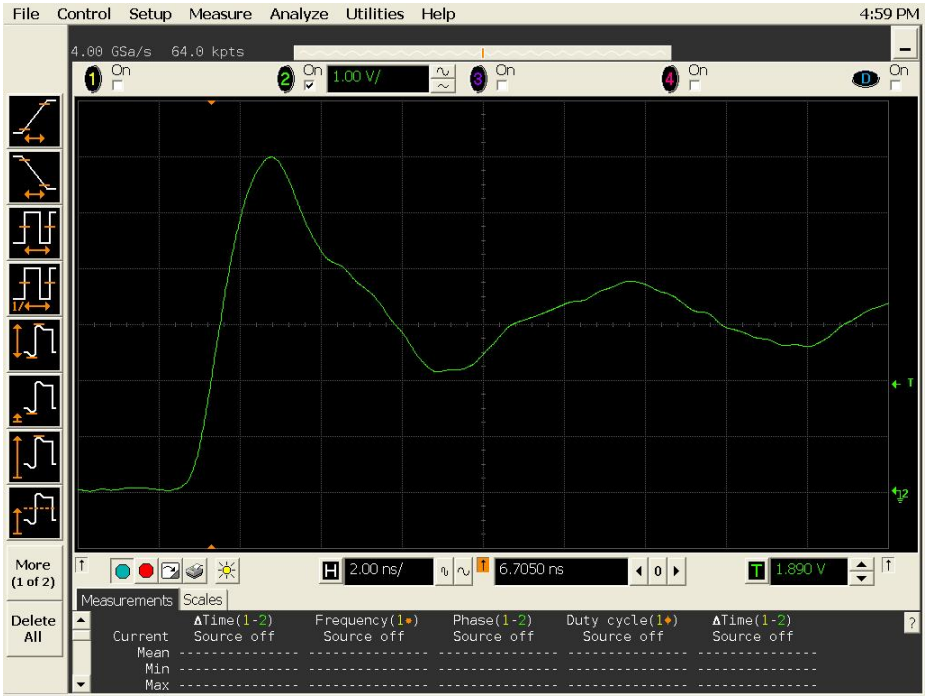


Figure 9a DUT 3002 Pre-Irradiation Rising Edge

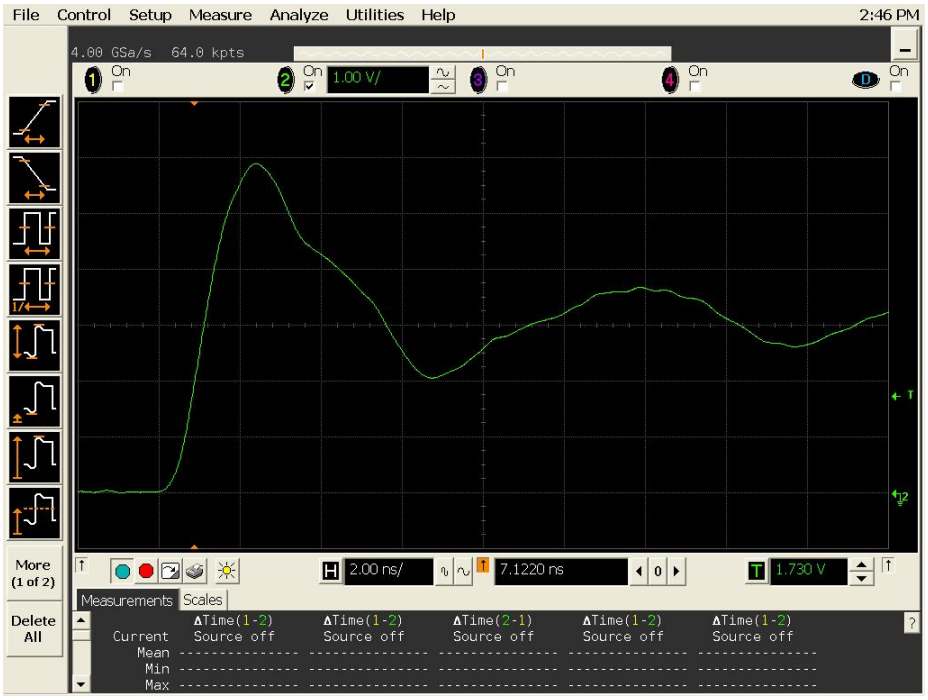


Figure 9b DUT 3002 Post-Annealing Rising Edge

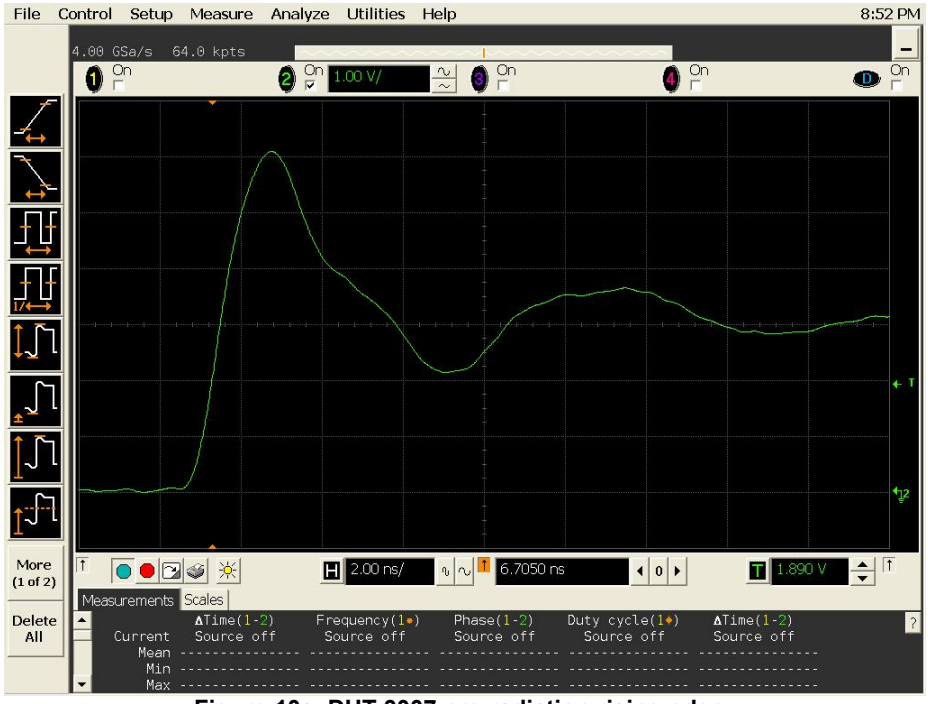


Figure 10a DUT 3007 pre-radiation rising edge.

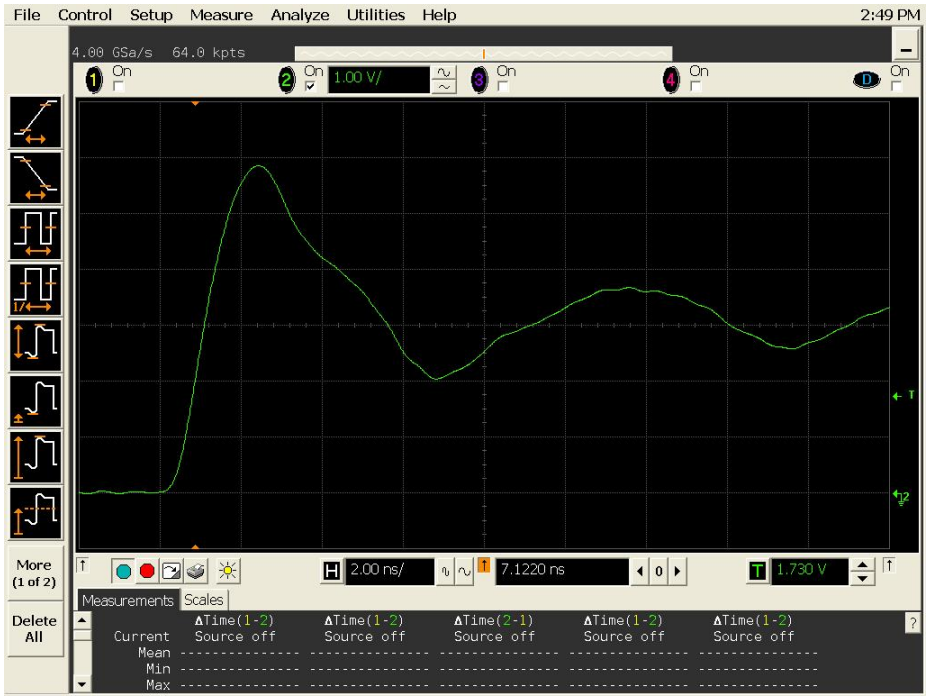


Figure 10b DUT 3007 Post-Annealing Rising Edge

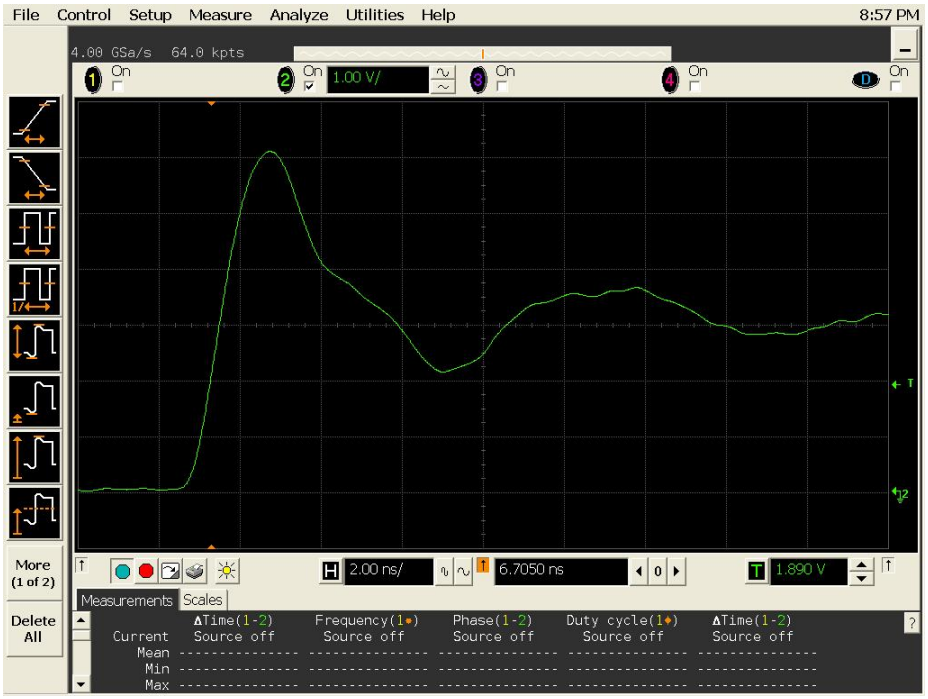


Figure 11a DUT 3021 Pre-Irradiation Rising Edge

Figure 11b DUT 3021 Post-Annealing Rising Edge

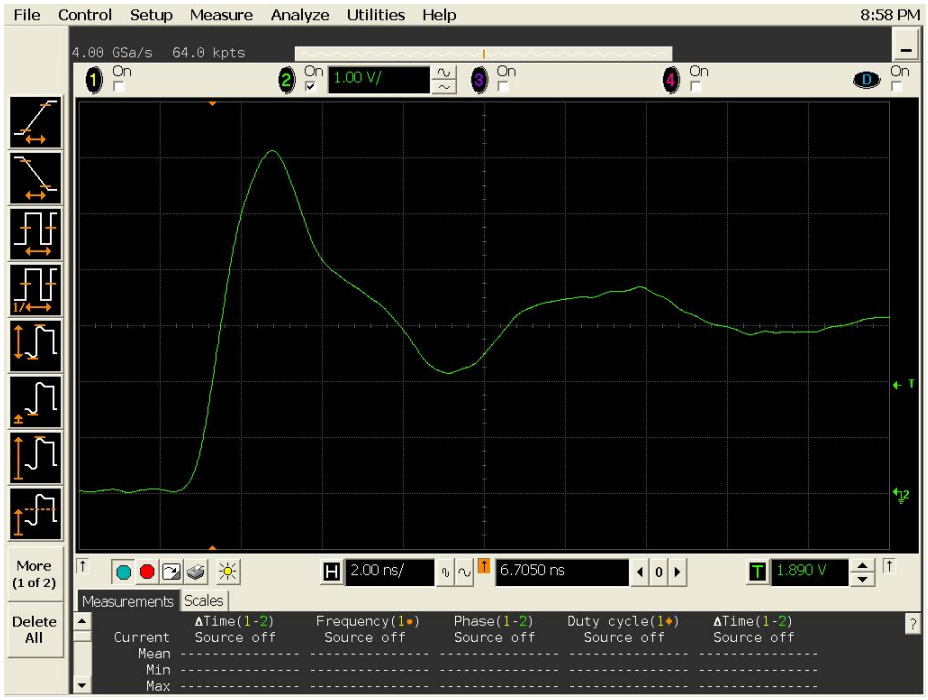


Figure 12a DUT 3023 Pre-Irradiation Rising Edge

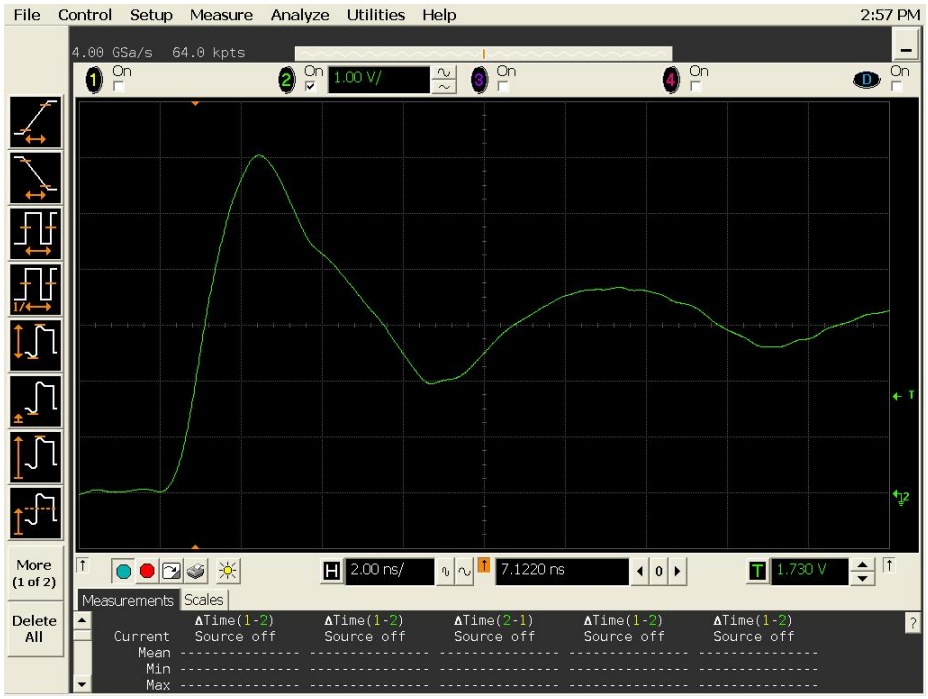


Figure 12b DUT 3023 Post-Annealing Rising Edge

Figure 13a DUT 3000 Pre-Radiation Falling Edge

Figure 13b DUT 3000 Post-Annealing Falling Edge

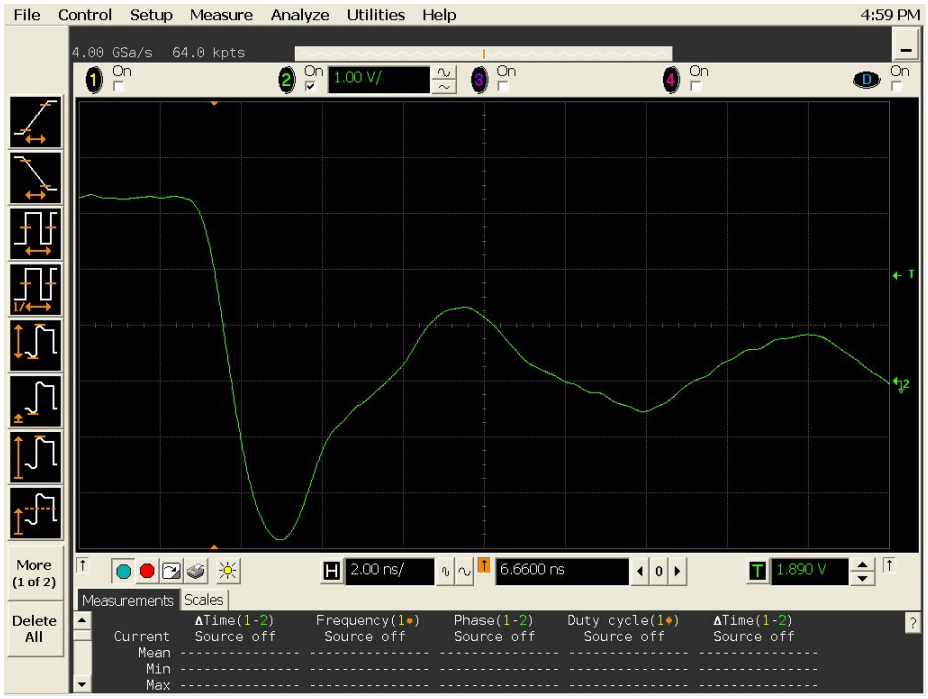


Figure 14a DUT 3002 Pre-Irradiation Falling Edge

Figure 14b DUT 3002 Post-Annealing Falling Edge

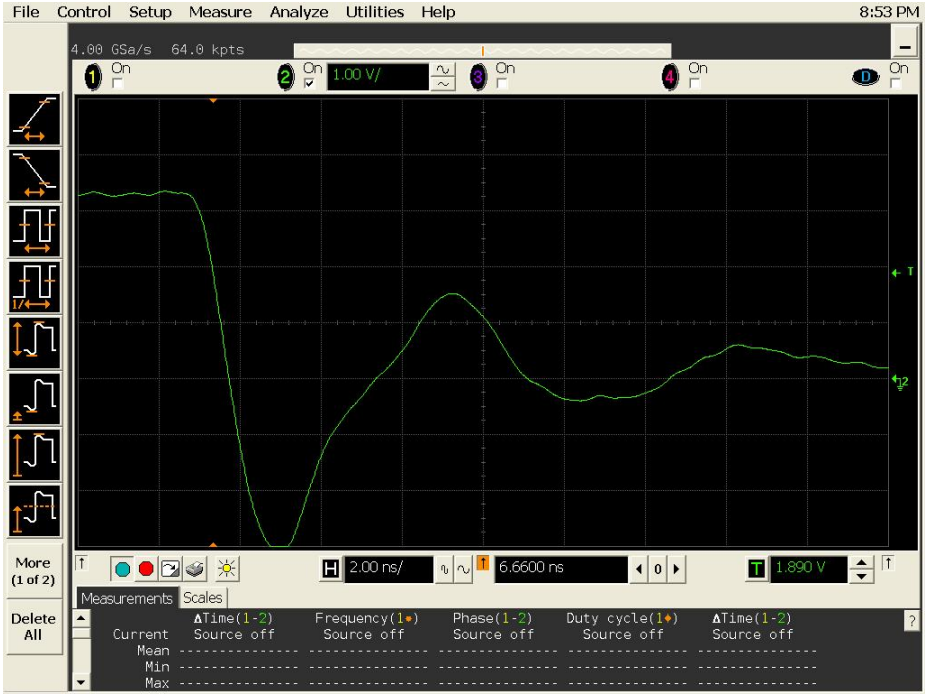


Figure 15a DUT 3007 Pre-Irradiation Falling Edge

Figure 15b DUT 3007 Post-Annealing Falling Edge

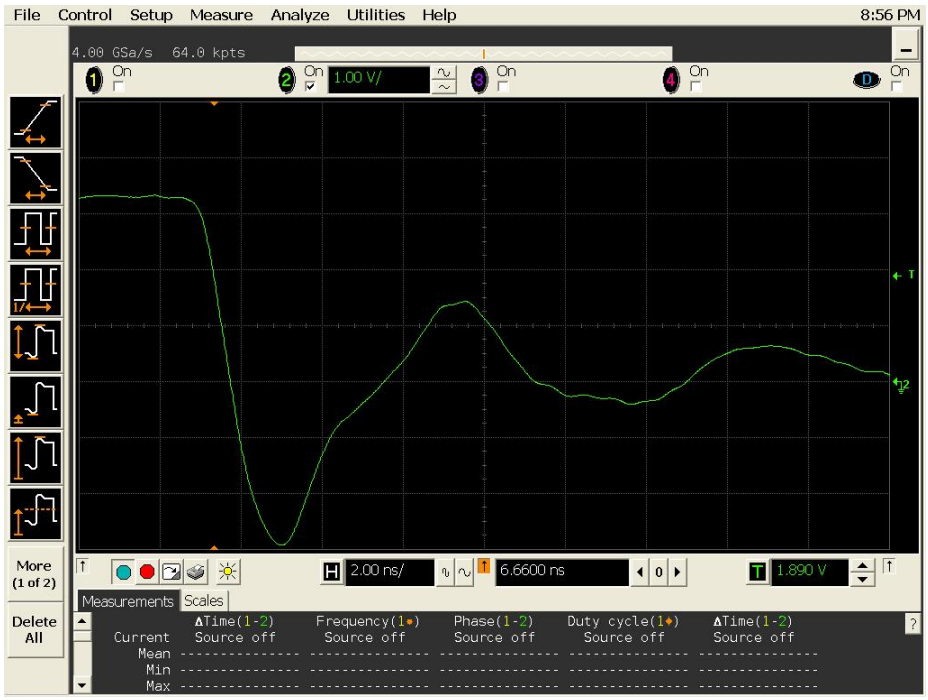


Figure 16a DUT 3021 Pre-Irradiation Falling Edge

Figure 16b DUT 3021 Post-Annealing Falling Edge

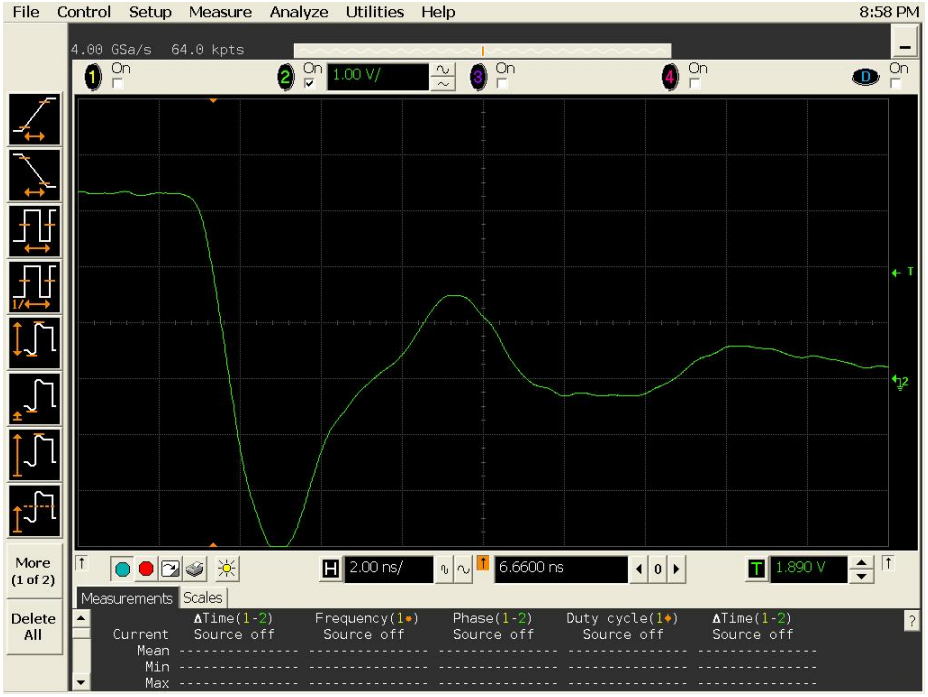


Figure 17a DUT 3023 Pre-Irradiation Falling Edge

Figure 17b DUT 3023 Post-Annealing Falling Edge

Appendix A: DUT Bias

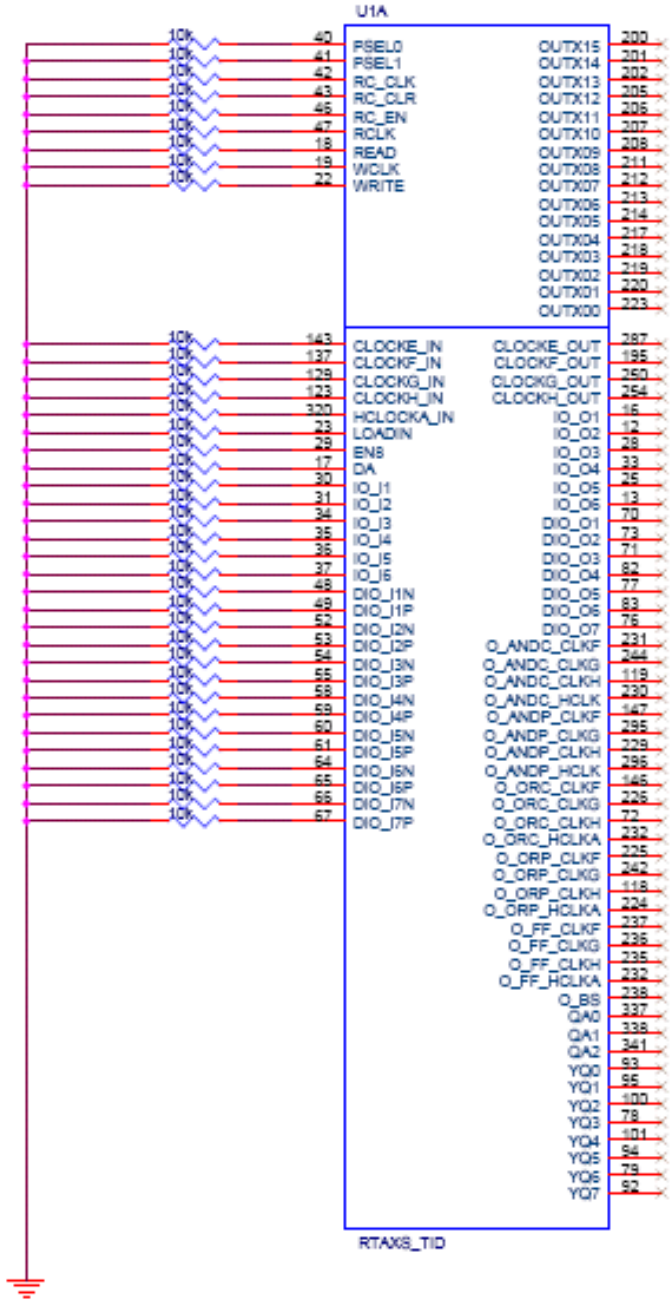


Figure A1 I/O Bias During Irradiation

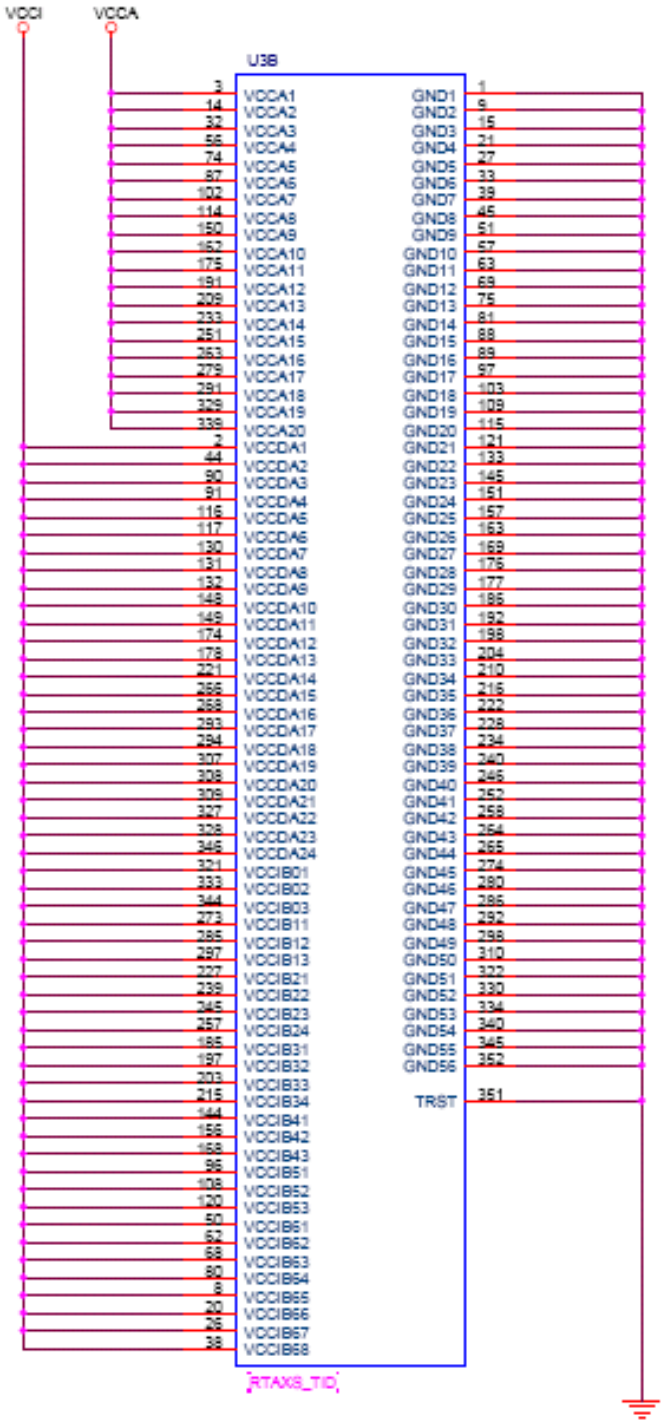
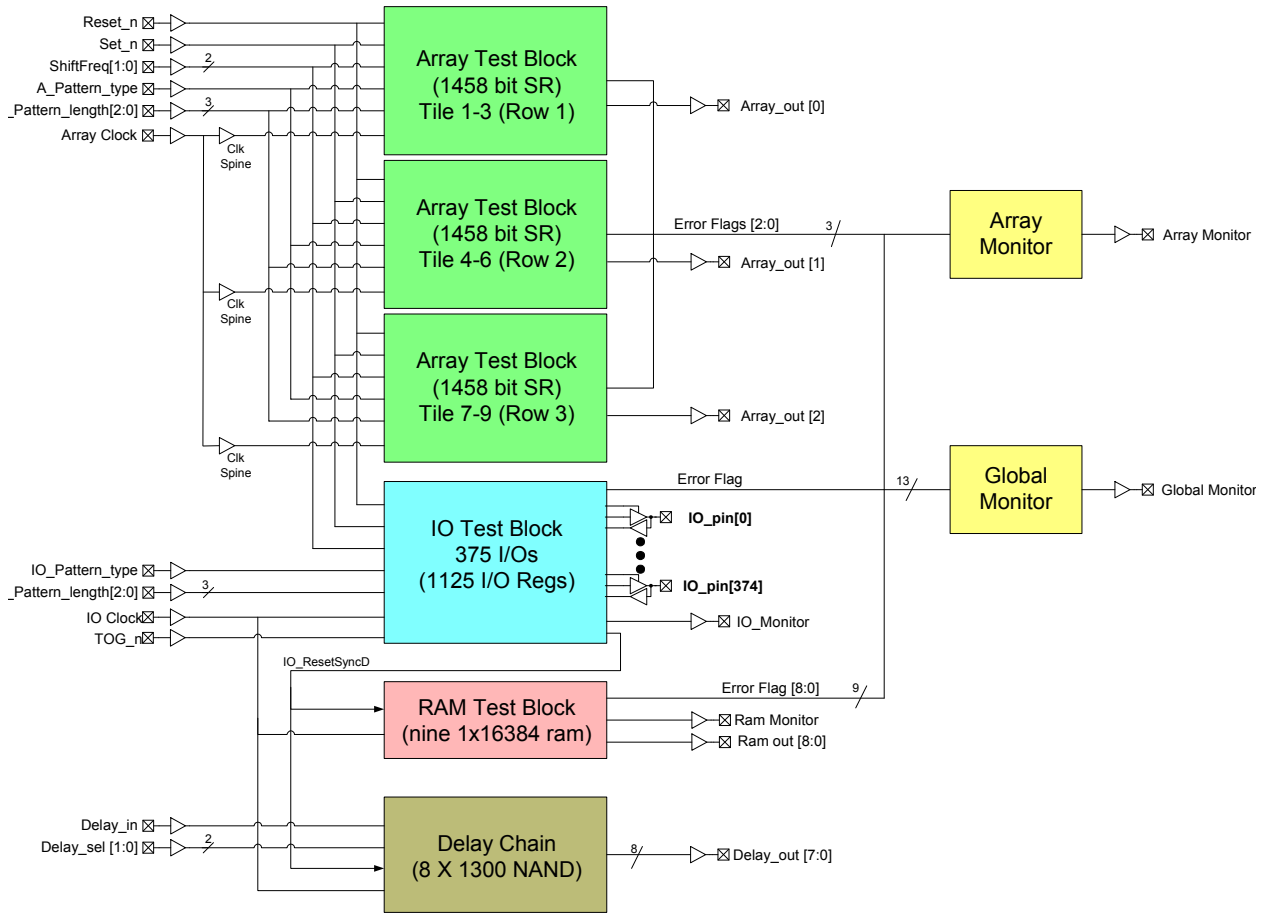


Figure A2 Power Supply, Ground and Special Pins Bias During Irradiation

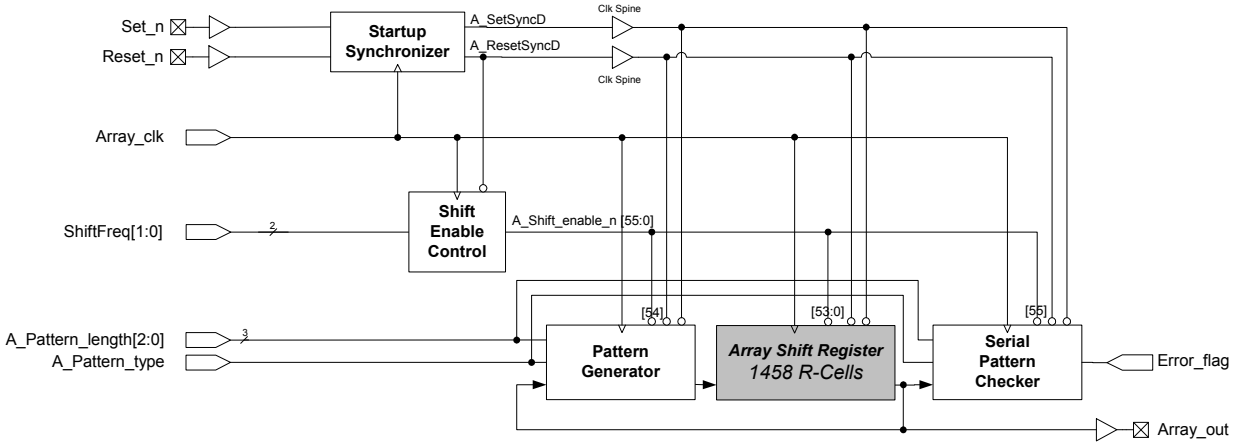
Appendix B: DUT Design Schematics

A. Design Blocks Overview

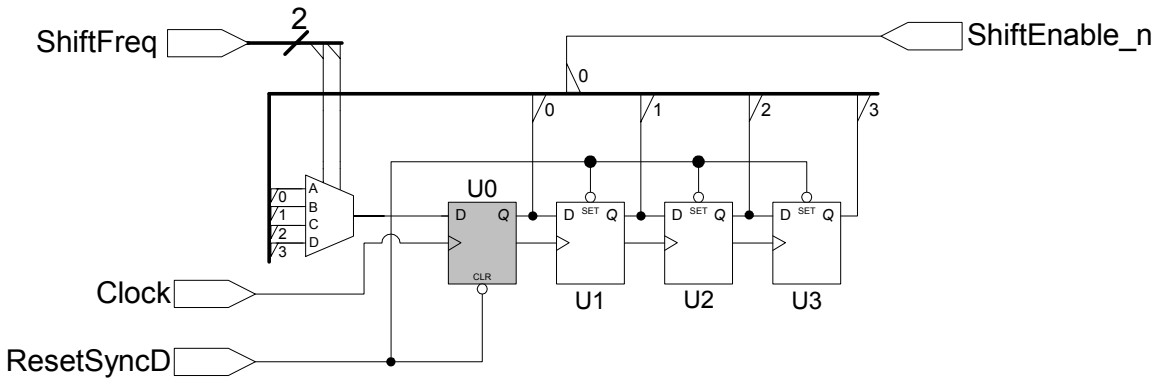
(The diagrams in the following pages schematically illustrate the main blocks of the design. The naming could be different to the final pins)



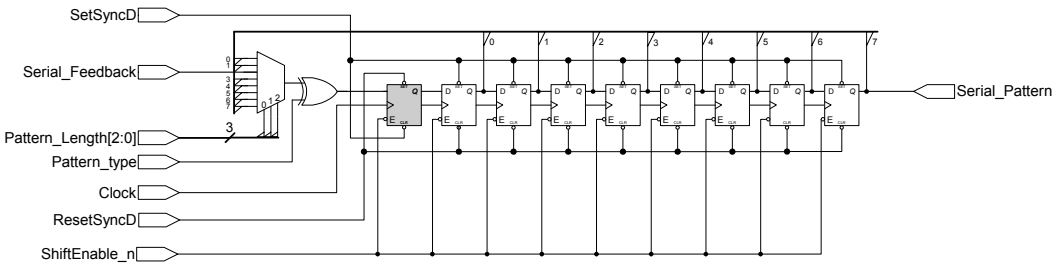
B. Array Test Block



C. Shift Enable Control

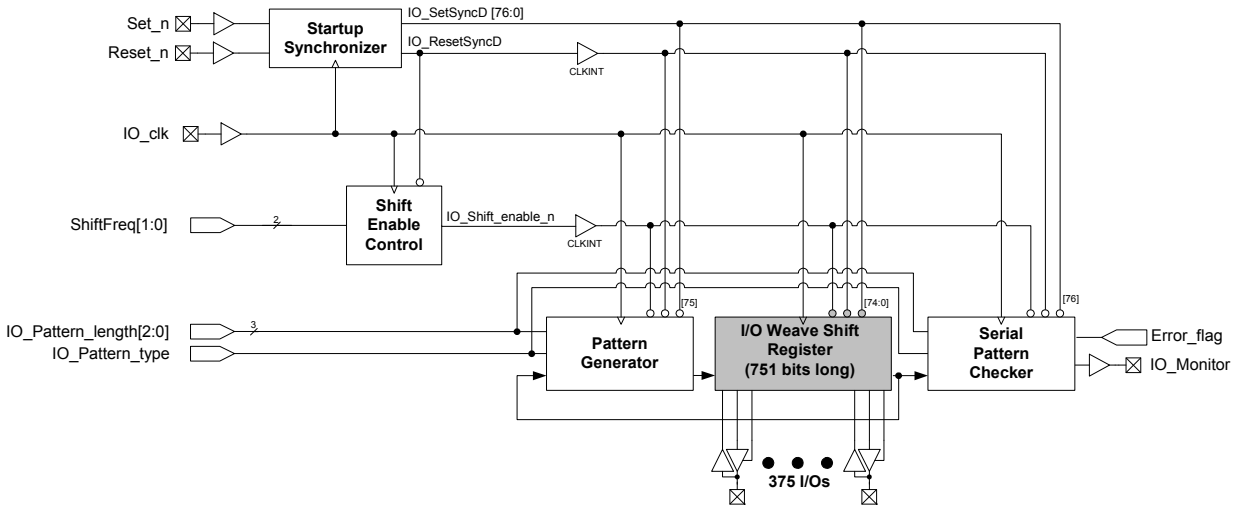


D. Pattern Generator

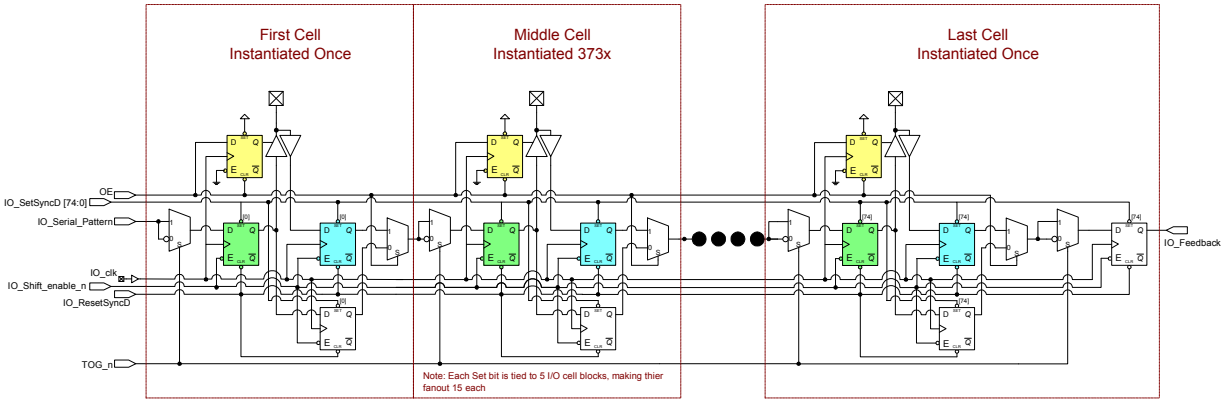


Pattern Type	Pattern Length		Code Length	Δ Bits	Switching Rate
0	000	1 0 ⇨ 0 1 ↰	2	2	100.00%
0	001	1 0 0 ⇨ 0 1 0 ⇨ 0 0 1 ↰	3	2	66.67%
0	010	**One hot I/O at a time switching in entire I/O ring**	#Bits+9	2	N/A
0	011	1 0 0 0 0 ⇨ 0 1 0 0 0 ⇨ 0 0 1 0 0 ⇨ 0 0 0 1 0 ⇨ 0 0 0 0 1 ↰	5	2	40.00%
0	100	1 0 0 0 0 0 ⇨ 0 1 0 0 0 0 ⇨ 0 0 1 0 0 0 ⇨ 0 0 0 1 0 0 ⇨ 0 0 0 0 1 0 ⇨ 0 0 0 0 0 1 ↰	6	2	33.33%
0	101	1 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 ⇨ 0 0 0 1 0 0 0 ⇨ 0 0 0 0 1 0 0 ⇨ 0 0	7	2	28.57%
0	110	1 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 ⇨ 0 0 0 0 1 0	8	2	25.00%
0	111	1 0 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 0 ⇨ 0 0	9	2	22.22%
1	000	1 0 ⇨ 1 1 ⇨ 0 1 ⇨ 0 0 ↰	2	1	50.00%
1	001	1 0 0 ⇨ 1 1 0 ⇨ 1 1 1 ⇨ 0 1 1 ⇨ 0 0 1 ⇨ 0 0 0 ↰	3	1	33.33%
1	010	**Wave of 0's followed by wave of 1's**	#Bits+9	1	N/A
1	011	1 0 0 0 0 ⇨ 1 1 0 0 0 ⇨ 1 1 1 0 0 ⇨ 1 1 1 1 0 ⇨ 1 1 1 1 1 ⇨ 0 1 1 1 1 ⇨ 0 0 1 1 1 ⇨	5	1	20.00%
1	100	1 0 0 0 0 0 ⇨ 1 1 0 0 0 0 ⇨ 1 1 1 0 0 0 ⇨ 1 1 1 1 0 0 ⇨ 1 1 1 1 1 0 ⇨ 1 1 1 1 1 1 ⇨	6	1	16.67%
1	101	1 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 ⇨ 1 1 1 1 0 0 0 ⇨ 1 1 1 1 1 0 0 ⇨ 1 1	7	1	14.29%
1	110	1 0 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 ⇨ 1 1 1 1 1 0	8	1	12.50%
1	111	1 0 0 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 0 ⇨ 1 1	9	1	11.11%

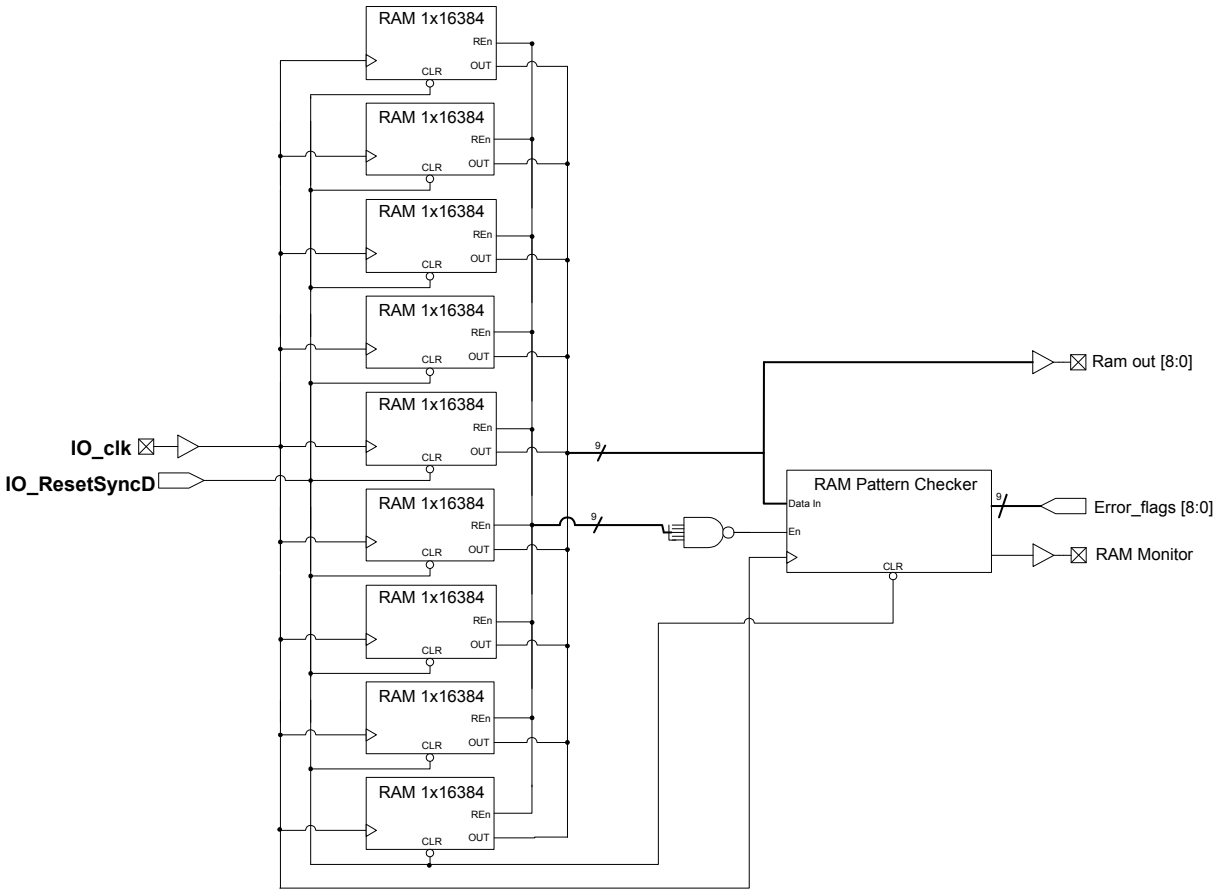
E. I/O Test Block



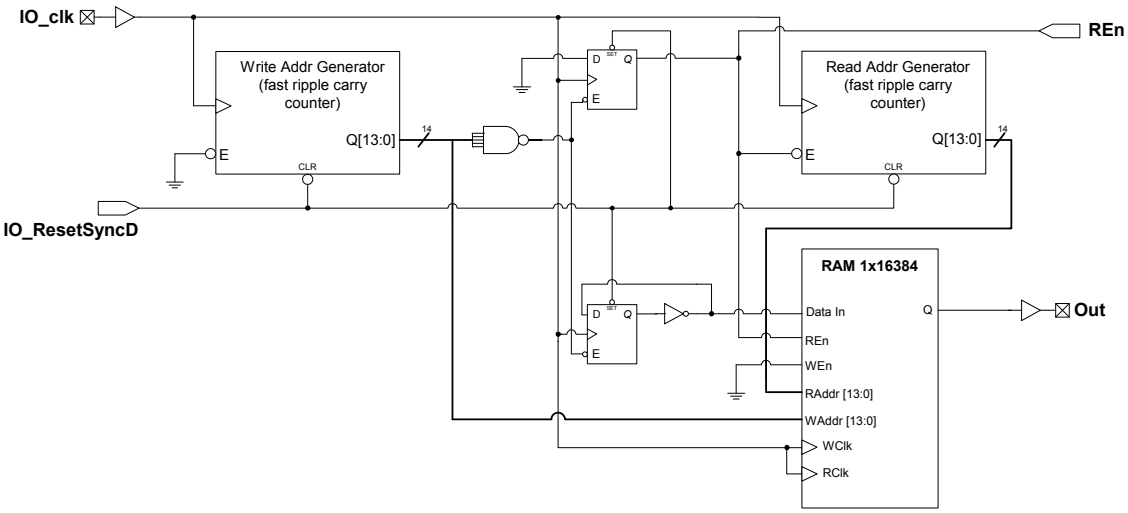
F. I/O Weave Structure



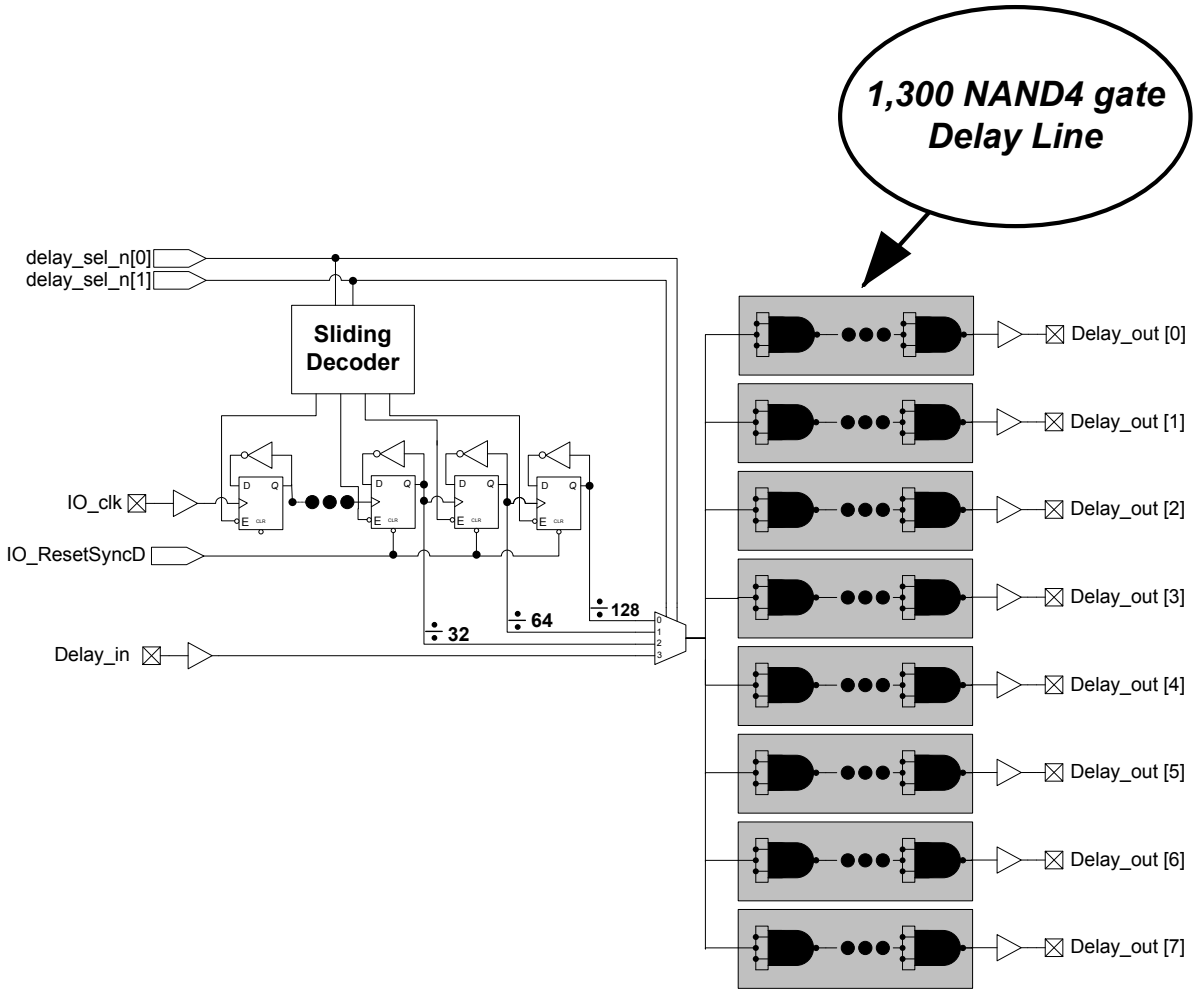
G. RAM Test Block



H. RAM 1x16384



I. Delay Chains



Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (NASDAQ: MSCC) offers a comprehensive portfolio of semiconductor solutions for: aerospace, defense and security; enterprise and communications; and industrial and alternative energy markets. Products include high-performance, high-reliability analog and RF devices, mixed signal and RF integrated circuits, customizable SoCs, FPGAs, and complete subsystems. Microsemi is headquartered in Aliso Viejo, Calif. Learn more at **www.microsemi.com**.