Total Ionizing Dose Test Report

No. 11T-RTAX2000S-CQ256-D54C71

August 23, 2011

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CK Huang and J.J. Wang

(650) 318-4209, (650) 318-4576

chang-kai.huang@microsemi.com, jih-jong.wang@microsemi.com

I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 300 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2) for 10% degradation criterion
6. Transition Charateristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGA in http://www.klabs.org and http://www.actel.com) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded through a jumper; during annealing each input or output is tied to the ground or VCCI with a resistor. Appendix A contains the schematics of the irradiation-bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	EAQ_RTAX2000S_rev1
Die Lot Number	D54C71
Quantity Tested	6
Serial Number	300 krad(SiO_2): 3531, 3532, 3541 200 krad(SiO_2): 3542, 3556, 3557
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

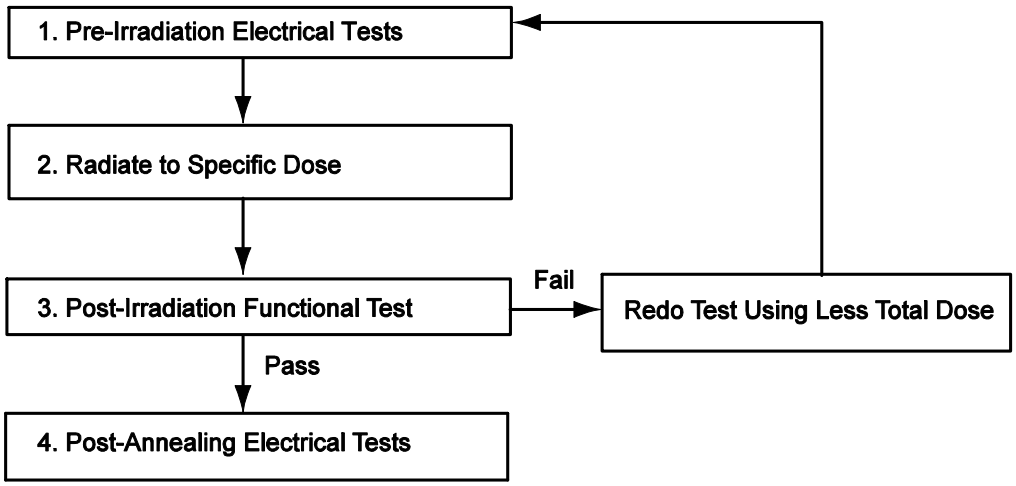


Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8 is unnecessary because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000S are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 3.5 days.

C. Design and Parametric Measurements

The DUT uses a high utilization, generic design (EAQ_RTAX2000S_rev1) to evaluate total dose effects for typical space applications. Appendix B contains the schematics that illustrate this design.

Table 2 lists measured electrical parameters and the corresponding logic design. The functionality is measured on the output pins including the embedded RAM.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively.

The input logic threshold (VIL/VIH) is measured on inputs A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2, oe, Reset_n, Set_n, ShiftFrequency_0, ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1.

The output-drive voltage (VOL/VOH) is measured on Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0. The propagation delay is measured on the output of the buffer string; the definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output, are shown as oscilloscope captures.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key logic functions, and outputs of embedded RAM
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Inputs (A_Clock A_Johnson, A_Pattern_Length_0, A_Pattern_Length_1, A_Pattern_Length_2, IO_Clock, IO_Johnson, IO_Pattern_Length_0, IO_Pattern_Length_1, IO_Pattern_Length_2 , oe, Reset_n, Set_n, ShiftFrequency_0 , ShiftFrequency_1, TOG_n, zoom, zoom_sel_n_0, zoom_sel_n_1)
4. Output Drive (V_{OL}/V_{OH})	Outputs (Array_Monitor, Array_out_0, delay_out_0, Global_Monitor, IO_Monitor, IO_Outs_0, RAM_Monitor, RAM_out_0)
5. Propagation Delay	String of buffers (IO_Clock to delay_out[0])
6. Transition Characteristic	String of buffers output (delay_out[0])

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 7 plot the influx standby ICCA and ICCI versus total dose for each DUT. Table 3 summarizes the pre-irradiation, post-irradiation and post-annealing ICC. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

Table 3 Pre-Irradiation, Post-Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad(SiO_2)	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
3531	300krad	5	27	7	7	111	46
3532	300krad	3	31	8	8	128	54
3541	300krad	1	25	5	8	121	45
3542	200krad	6	11	6	3	36	16
3556	200krad	6	9	4	8	29	22
3557	200krad	3	7	4	6	33	15

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-4 of the RTAXS datasheet:

http://www.actel.com/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to 35 + 10 + 3.13 × 7 = 66.91 (mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT. Based on these PIPL, post-annealed DUT passes both the ICCA and ICCI specification for 300 krad (SiO2).

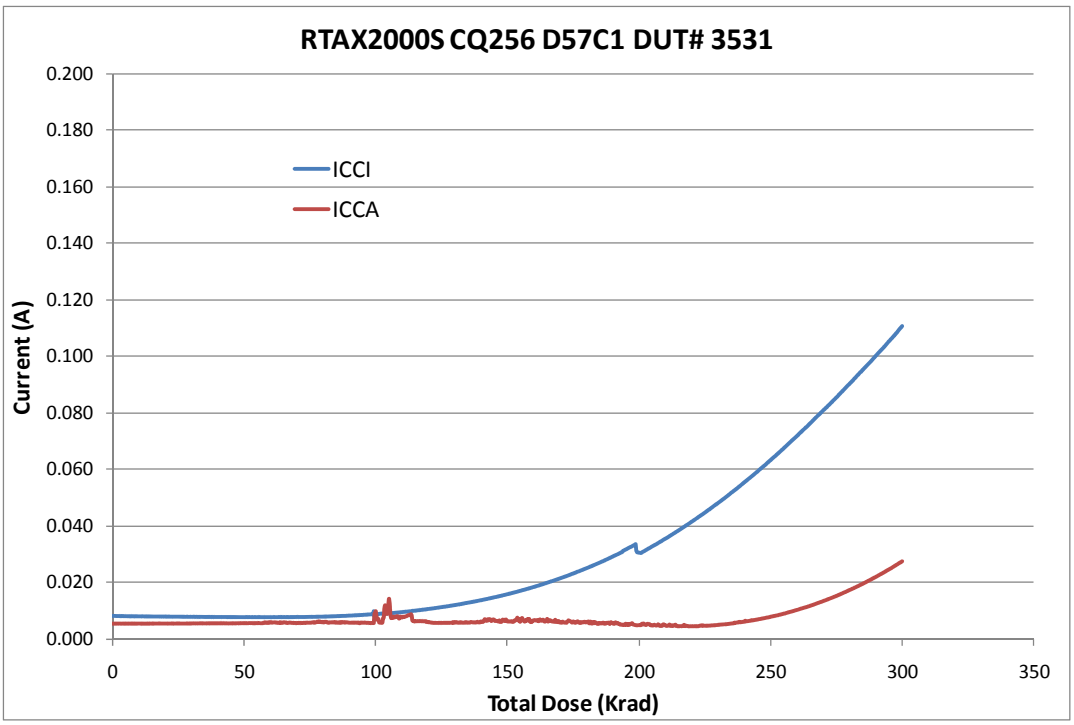


Figure 2 DUT 3531 Influx ICCA and ICCI

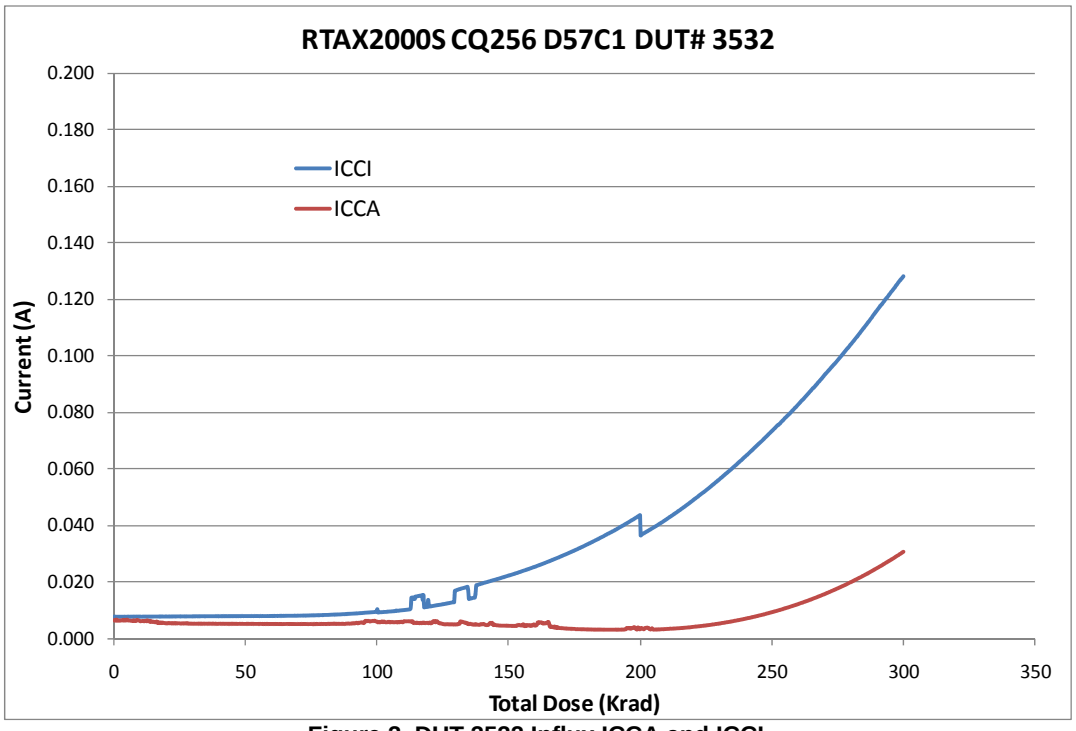


Figure 3 DUT 3532 Influx ICCA and ICCI

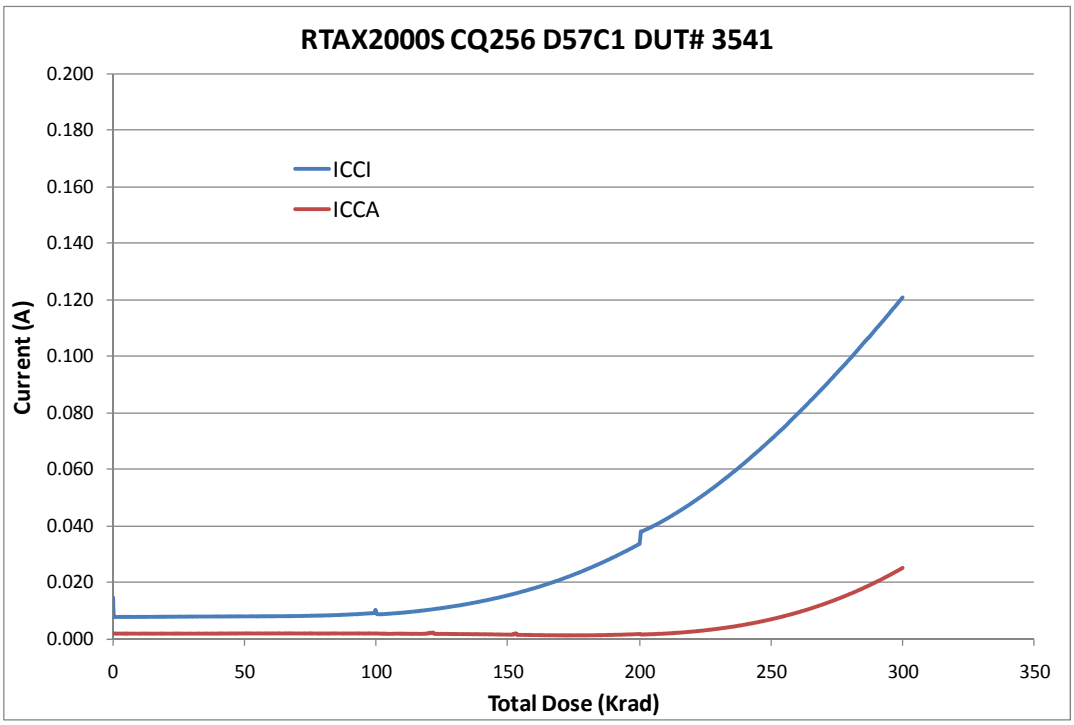


Figure 4 DUT 3541 Influx ICCA and ICCI

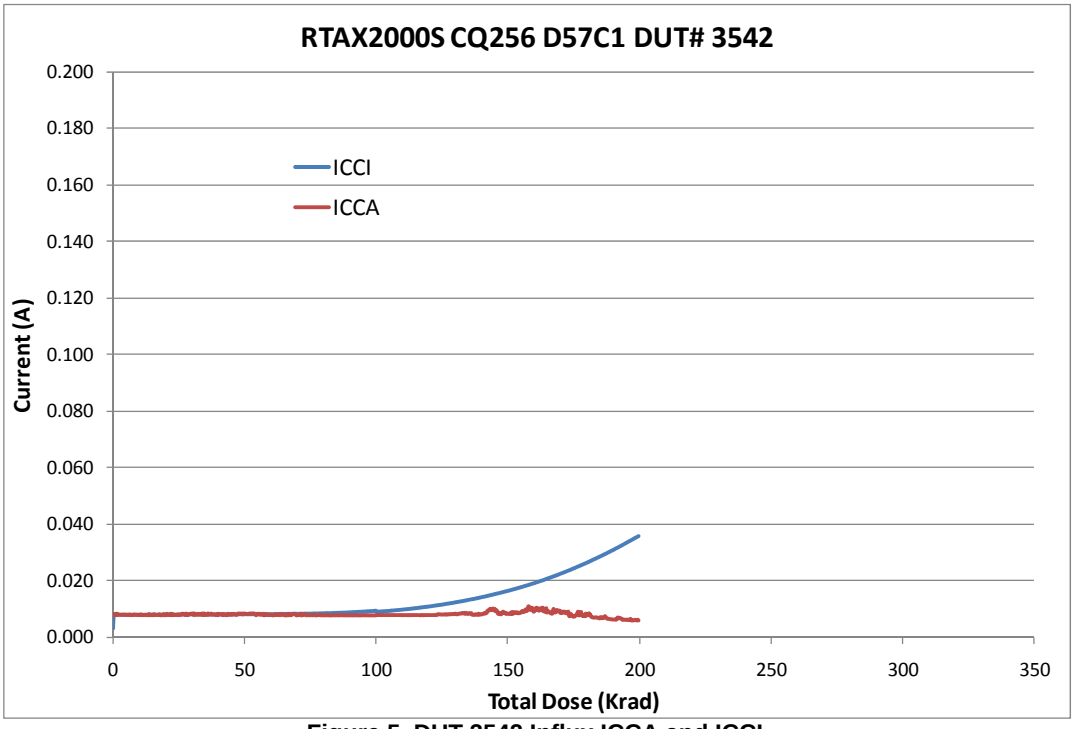


Figure 5 DUT 3542 Influx ICCA and ICCI

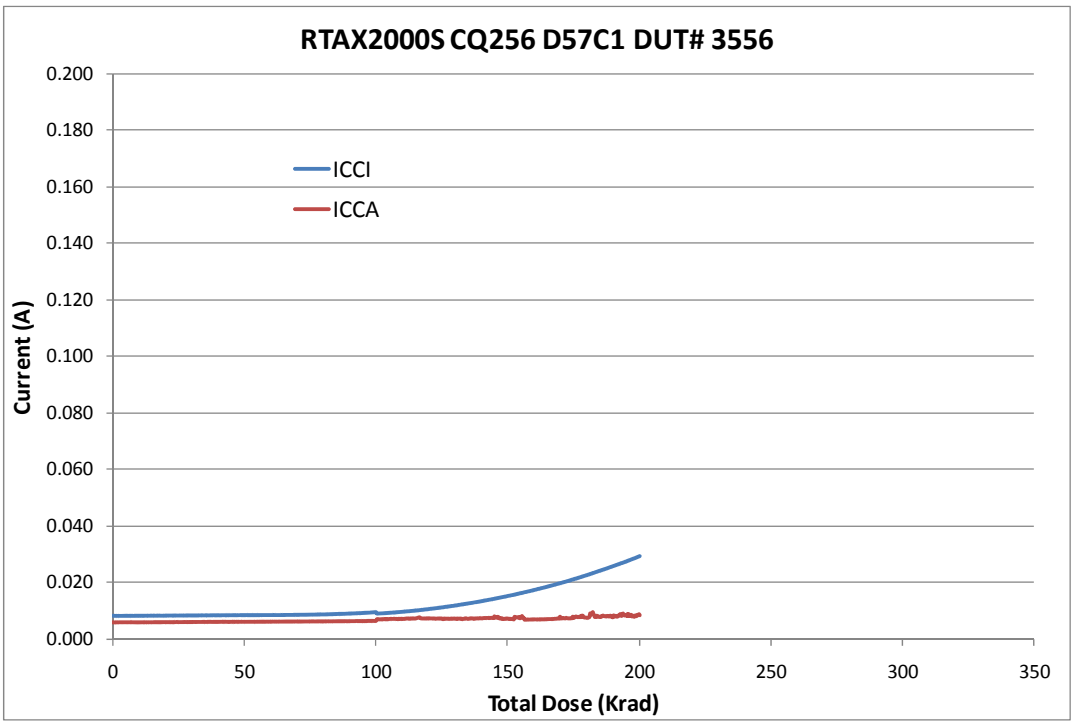


Figure 6 DUT 3556 Influx ICCA and ICCI

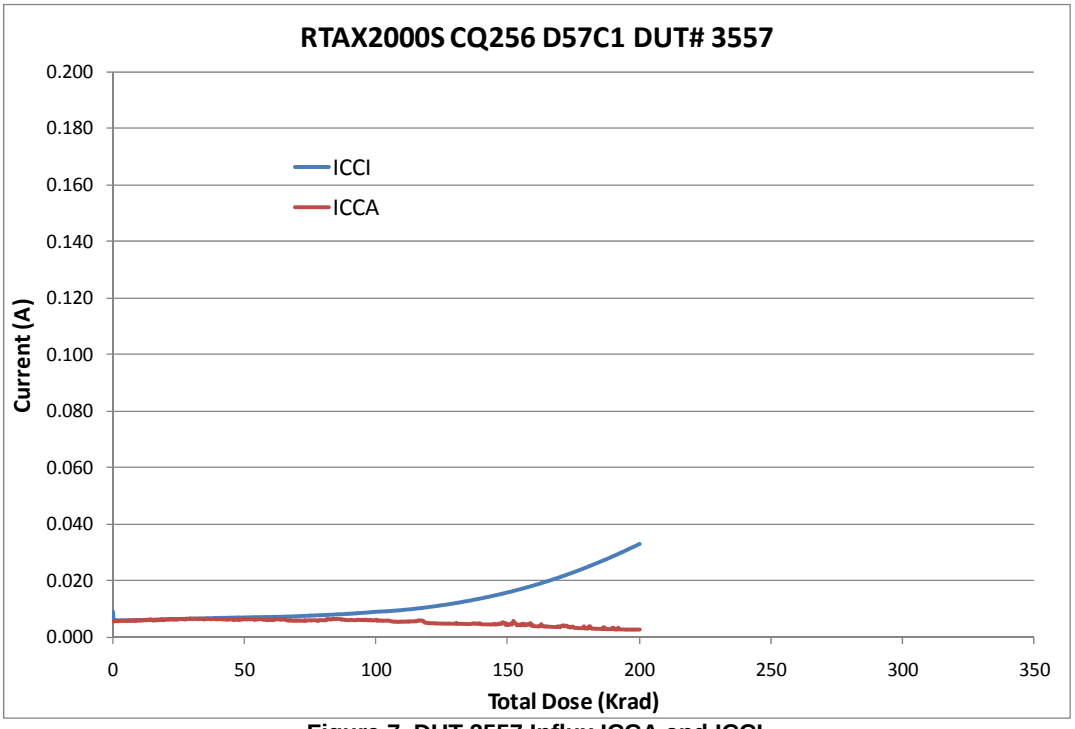


Figure 7 DUT 3557 Influx ICCA and ICCI

C. Input Threshold VIL

Table 4 lists the pre-irradiation and post-annealing single-ended input threshold. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds VIL (mV)

Pin\DUT	3531 (300 krad)		3532 (300 krad)		3541 (300 krad)		3542 (200 krad)		3556 (200 krad)		3557 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.3750	1.3750	1.3750	1.3750	1.3750	1.3750	1.3700	1.3750	1.3750	1.3700	1.3750	1.3750
A_Johnson	1.3700	1.3700	1.3700	1.3650	1.3650	1.3650	1.3700	1.3700	1.3700	1.3650	1.3650	1.3700
A_Pattern_Length_0	1.3800	1.3800	1.3750	1.3750	1.3750	1.3750	1.3750	1.3800	1.3800	1.3750	1.3750	1.3750
A_Pattern_Length_1	1.3800	1.3800	1.3750	1.3800	1.3750	1.3750	1.3750	1.3800	1.3800	1.3750	1.3800	1.3800
A_Pattern_Length_2	1.3700	1.3700	1.3700	1.3700	1.3650	1.3650	1.3700	1.3700	1.3700	1.3650	1.3700	1.3700
IO_Clock	1.3700	1.3700	1.3650	1.3700	1.3650	1.3650	1.3650	1.3700	1.3700	1.3600	1.3650	1.3650
IO_Johnson	1.3750	1.3750	1.3800	1.3750	1.3750	1.3750	1.3750	1.3800	1.3800	1.3750	1.3750	1.3800
IO_Pattern_Length_0	1.3700	1.3650	1.3650	1.3650	1.3600	1.3650	1.3650	1.3700	1.3750	1.3600	1.3650	1.3700
IO_Pattern_Length_1	1.3700	1.3650	1.3700	1.3650	1.3600	1.3650	1.3700	1.3700	1.3700	1.3650	1.3650	1.3650
IO_Pattern_Length_2	1.3750	1.3750	1.3750	1.3750	1.3700	1.3750	1.3750	1.3750	1.3800	1.3700	1.3750	1.3800
oe	1.3750	1.3750	1.3700	1.3750	1.3700	1.3700	1.3650	1.3750	1.3750	1.3650	1.3700	1.3750
Reset_n	1.3750	1.3750	1.3750	1.3750	1.3750	1.3750	1.3700	1.3750	1.3750	1.3650	1.3750	1.3750
Set_n	1.3650	1.3700	1.3650	1.3650	1.3650	1.3650	1.3600	1.3650	1.3650	1.3600	1.3600	1.3650
ShiftFrequency_0	1.3750	1.3700	1.3750	1.3750	1.3700	1.3750	1.3700	1.3750	1.3750	1.3700	1.3750	1.3750
ShiftFrequency_1	1.3800	1.3750	1.3750	1.3750	1.3700	1.3700	1.3700	1.3750	1.3750	1.3650	1.3700	1.3750
TOG_n	1.3800	1.3750	1.3750	1.3750	1.3700	1.3750	1.3700	1.3750	1.3800	1.3700	1.3750	1.3750
zoom	1.3850	1.3800	1.3800	1.3800	1.3750	1.3750	1.3800	1.3850	1.3800	1.3750	1.3850	1.3800
zoom_sel_n_0	1.3700	1.3650	1.3700	1.3550	1.3500	1.3600	1.3650	1.3700	1.3700	1.3500	1.3600	1.3600
zoom_sel_n_1	1.3700	1.3650	1.3650	1.3550	1.3500	1.3550	1.3650	1.3700	1.3700	1.3450	1.3550	1.3600

D. Input Threshold VIH

Table 5 lists the input threshold voltage changes due to irradiations. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 5 Pre-Irradiation and Post-Annealing Input Thresholds VIH (mV)

Pin\DUT	3531 (300 krad)		3532 (300 krad)		3541 (300 krad)		3542 (200 krad)		3556 (200 krad)		3557 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
A_Clock	1.640	1.645	1.640	1.635	1.635	1.635	1.635	1.645	1.645	1.630	1.635	1.635
A_Johnson	1.660	1.660	1.660	1.655	1.650	1.655	1.660	1.660	1.660	1.655	1.655	1.655
A_Pattern_Length_0	1.645	1.650	1.645	1.640	1.640	1.635	1.645	1.645	1.650	1.635	1.640	1.640
A_Pattern_Length_1	1.650	1.650	1.645	1.640	1.640	1.640	1.645	1.650	1.650	1.635	1.640	1.645
A_Pattern_Length_2	1.660	1.660	1.660	1.655	1.655	1.655	1.660	1.665	1.660	1.650	1.660	1.655
IO_Clock	1.660	1.665	1.660	1.655	1.660	1.655	1.655	1.660	1.660	1.650	1.655	1.655
IO_Johnson	1.650	1.645	1.645	1.640	1.640	1.640	1.650	1.650	1.650	1.640	1.640	1.645
IO_Pattern_Length_0	1.660	1.655	1.655	1.650	1.650	1.650	1.655	1.660	1.660	1.650	1.655	1.655
IO_Pattern_Length_1	1.660	1.655	1.660	1.655	1.650	1.655	1.660	1.660	1.660	1.650	1.655	1.655
IO_Pattern_Length_2	1.645	1.645	1.645	1.640	1.635	1.640	1.645	1.645	1.650	1.635	1.640	1.645
oe	1.645	1.640	1.640	1.635	1.630	1.635	1.635	1.645	1.645	1.625	1.635	1.635
Reset_n	1.640	1.645	1.640	1.635	1.635	1.630	1.635	1.645	1.640	1.625	1.635	1.635
Set_n	1.655	1.660	1.655	1.650	1.655	1.650	1.650	1.655	1.655	1.645	1.650	1.650
ShiftFrequency_0	1.645	1.640	1.640	1.635	1.635	1.635	1.635	1.645	1.645	1.630	1.640	1.640
ShiftFrequency_1	1.645	1.640	1.640	1.640	1.635	1.635	1.635	1.645	1.645	1.625	1.635	1.640
TOG_n	1.650	1.640	1.645	1.640	1.635	1.635	1.640	1.645	1.645	1.630	1.635	1.640
zoom	1.650	1.650	1.650	1.645	1.640	1.640	1.650	1.655	1.650	1.640	1.650	1.645
zoom_sel_n_0	1.660	1.655	1.660	1.640	1.635	1.645	1.655	1.660	1.655	1.635	1.645	1.640
zoom_sel_n_1	1.660	1.655	1.655	1.640	1.635	1.640	1.655	1.660	1.660	1.630	1.645	1.645

E. Output-Drive Voltage (VOL)

The pre-irradiation and post-annealing VOL are listed in Table 6. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 6 Pre-Irradiation and Post-Annealing Output-Drive VOL (mV)

Pin\DUT	3531 (300 krad)		3532 (300 krad)		3541 (300 krad)		3542 (200 krad)		3556 (200 krad)		3557 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	186	193	187	177	182	178	187	188	188	178	180	181
Array_out_0	179	185	179	170	175	172	179	181	181	170	173	173
delay_out_0	187	193	187	178	182	179	186	188	188	176	179	179
Global_Monitor	188	195	188	180	184	182	188	190	189	181	183	183
IO_Monitor	183	191	183	173	179	176	183	184	185	174	176	177
IO_Outs_0	183	183	180	180	180	177	181	185	182	177	181	178
RAM_Monitor	193	199	192	183	187	183	192	192	194	181	183	186
RAM_out_0	191	192	189	181	184	182	190	191	190	182	183	183

F. Output-Drive Voltage (VOH)

The pre-irradiation and post-annealing VOH are listed in Table 7. All pins show negligible changes after irradiation, and their post-annealing data are within the specification limits.

Table 7 Pre-Irradiation and Post-Annealing Output-Drive VOH (mV)

Pin\DUT	3531 (300 krad)		3532 (300 krad)		3541 (300 krad)		3542 (200 krad)		3556 (200 krad)		3557 (200 krad)	
	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann	Pre-rad	Post-ann
Array_Monitor	2722	2716	2721	2723	2716	2724	2720	2722	2719	2720	2724	2721
Array_out_0	2727	2723	2727	2727	2722	2730	2726	2727	2724	2726	2729	2727
delay_out_0	2724	2719	2725	2725	2720	2727	2725	2726	2722	2726	2729	2725
Global_Monitor	2720	2715	2719	2719	2713	2722	2718	2720	2717	2717	2722	2718
IO_Monitor	2723	2718	2723	2724	2718	2726	2721	2724	2719	2722	2727	2722
IO_Outs_0	2721	2720	2725	2724	2723	2728	2723	2722	2722	2725	2725	2725
RAM_Monitor	2714	2709	2715	2715	2709	2719	2714	2716	2712	2715	2720	2716
RAM_out_0	2721	2720	2720	2720	2722	2723	2721	2722	2720	2721	2723	2721

G. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The irradiation was temporarily stopped at each total-dose increment of 100 krad for the measurement. Each measurement has a 2-minute wait after a DUT is removed from the chamber. The results are plotted in Figure 8, and listed in Table 8. As shown in Figure 8, the propagation delay initially decreases with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots, a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. User can take the worst case for the design-margin consideration.

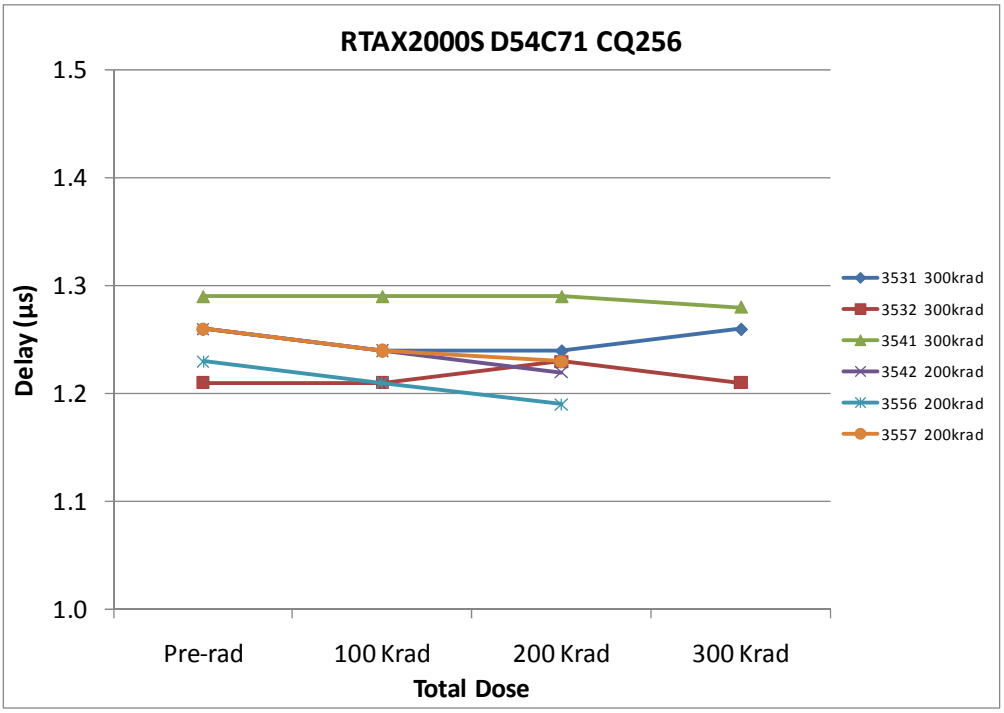


Figure 8 In-Situ Propagation Delay versus Total Dose
The measurement is performed outside the irradiation chamber.

Table 8 Radiation-Induced Propagation-Delay Degradations

	RTAX2000S D54C71 CQ256						
Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	3531	300krad	1.26	1.24	1.24	1.26	1.24
	3532	300krad	1.21	1.21	1.23	1.21	1.20
	3541	300krad	1.29	1.29	1.29	1.28	1.27
	3542	200krad	1.26	1.24	1.22	-	1.22
	3556	200krad	1.23	1.21	1.19	-	1.19
	3557	200krad	1.26	1.24	1.23	-	1.23
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	3531	300krad	-	-1.61%	-1.61%	0.00%	-1.61%
	3532	300krad	-	0.00%	1.65%	0.00%	-0.83%
	3541	300krad	-	0.00%	0.00%	-0.81%	-1.61%
	3542	200krad	-	-1.59%	-3.17%	-	-3.17%
	3556	200krad	-	-1.60%	-3.20%	-	-3.20%
	3557	200krad	-	-1.53%	-2.29%	-	-2.29%

H. Transition Characteristics

Figure 9a to Figure 20b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

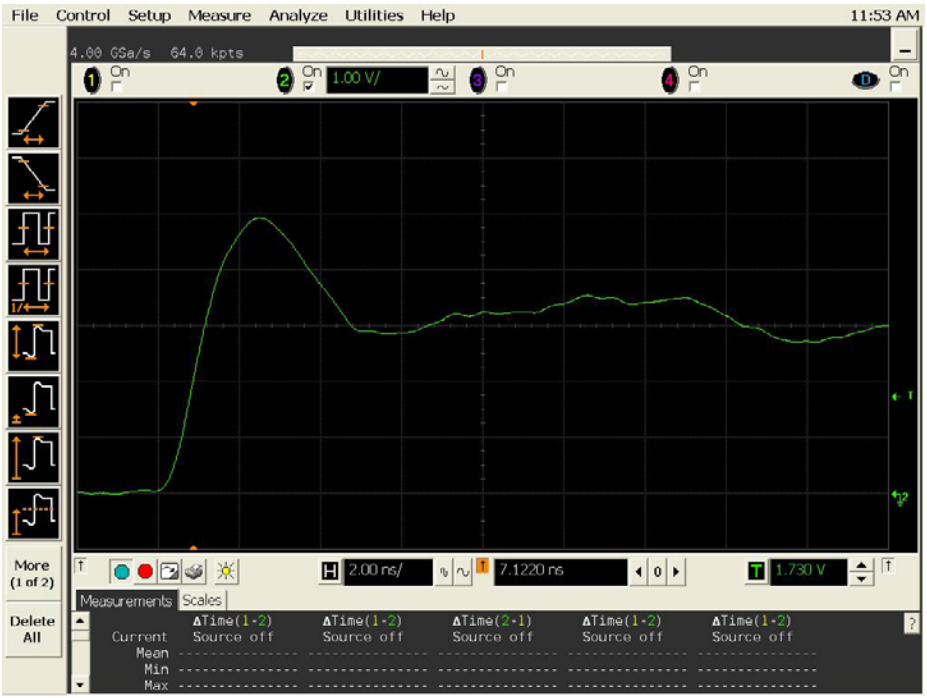


Figure 9a DUT 3531 Pre-Irradiation Rising Edge

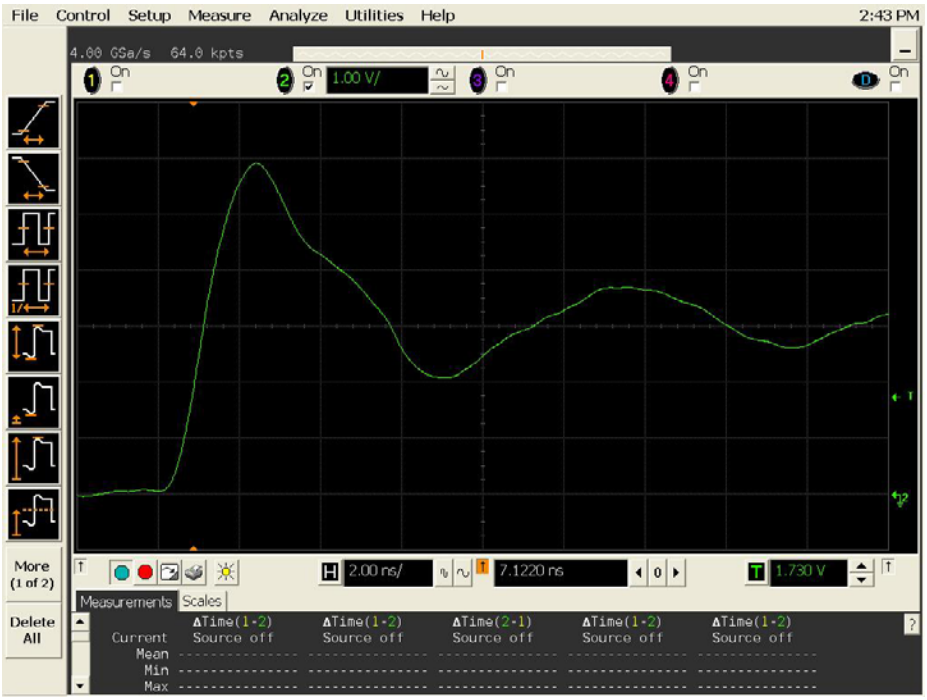


Figure 9b DUT 3531 Post-Annealing Rising Edge

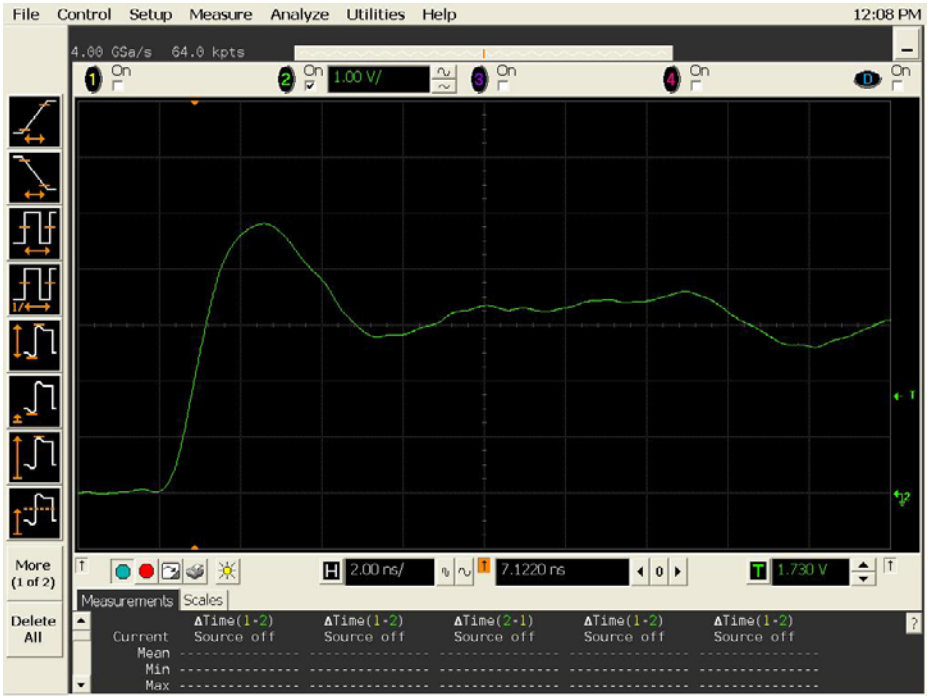


Figure 10a DUT 3532 Pre-Irradiation Rising Edge

Figure 10b DUT 3532 Post-Annealing Rising Edge

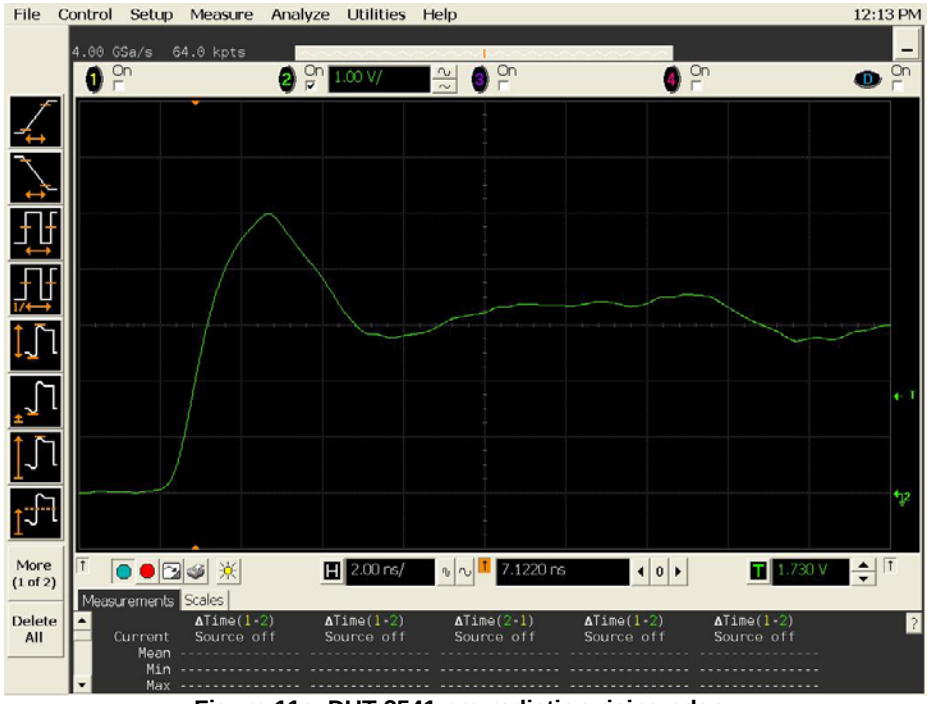


Figure 11a DUT 3541 pre-radiation rising edge.

Figure 11b DUT 3541 Post-Annealing Rising Edge

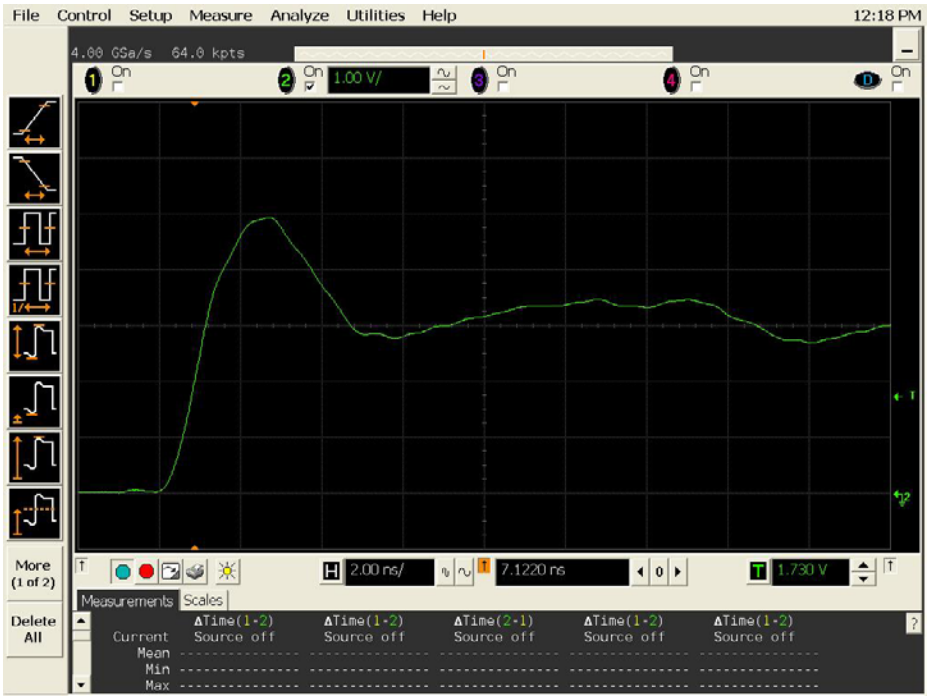


Figure 12a DUT 3542 Pre-Irradiation Rising Edge

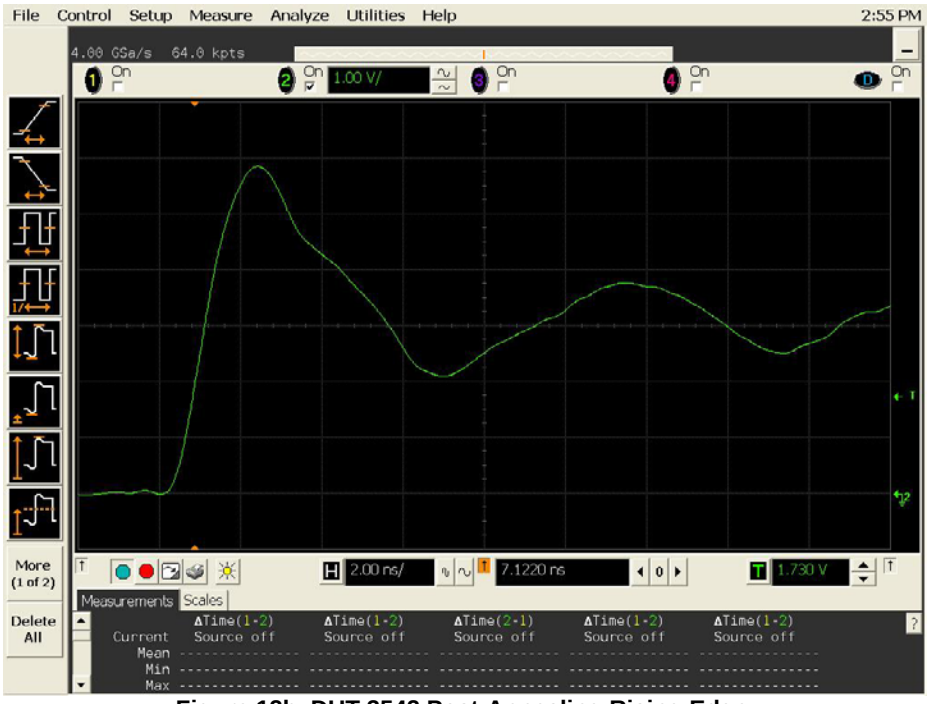


Figure 12b DUT 3542 Post-Annealing Rising Edge

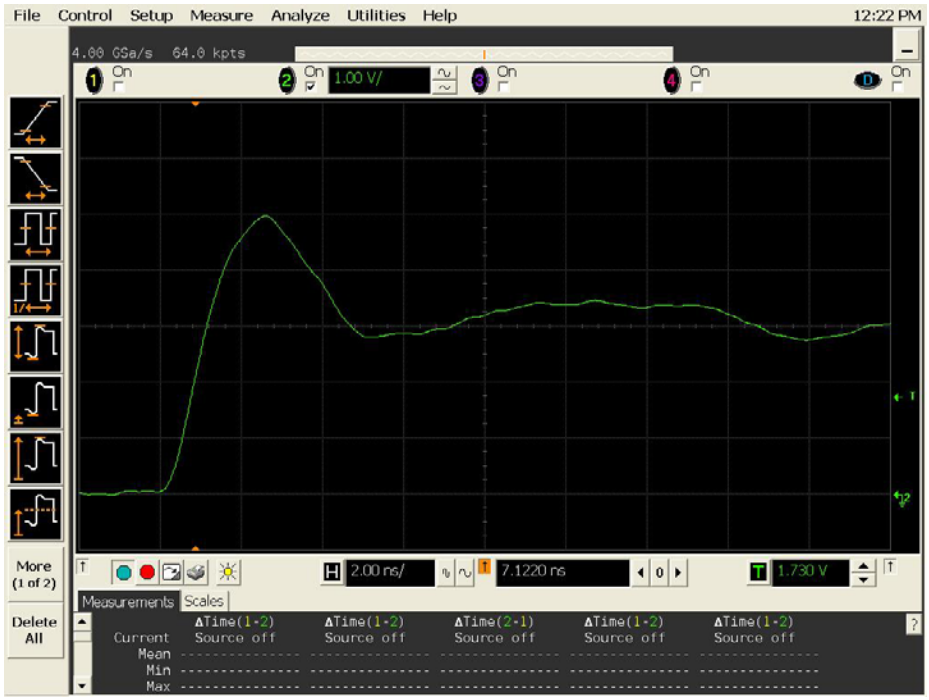


Figure 13a DUT 3556 Pre-Irradiation Rising Edge

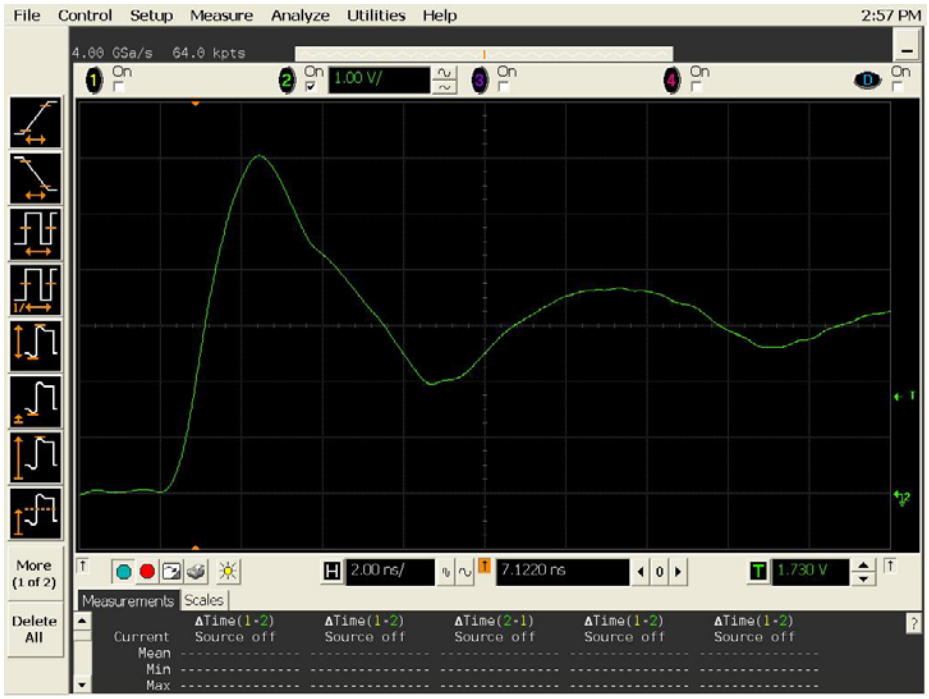


Figure 13b DUT 3556 Post-Annealing Rising Edge

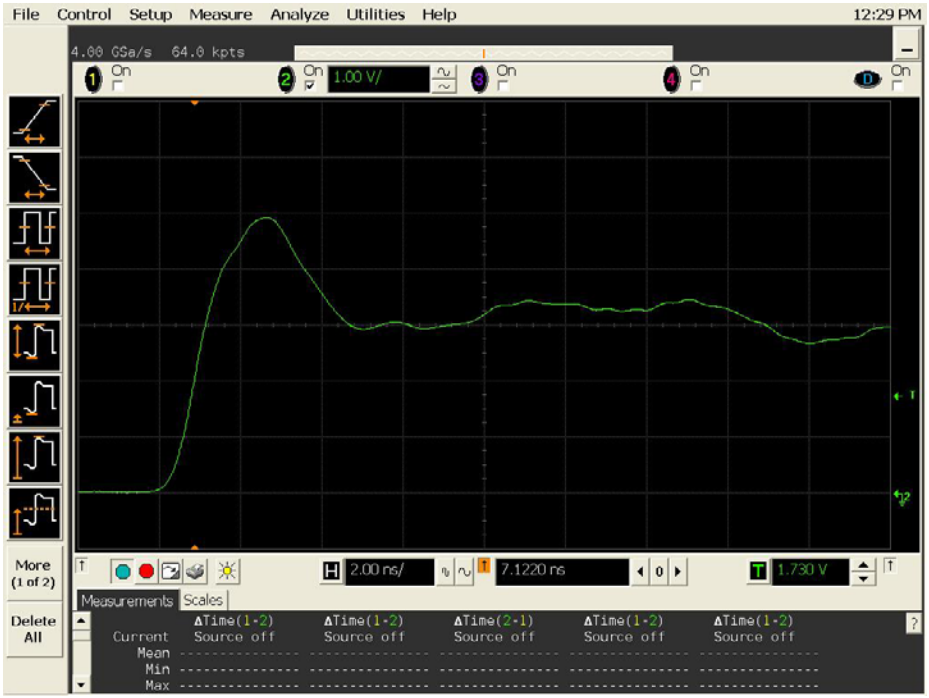


Figure 14a DUT 3557 Pre-Irradiation Rising Edge

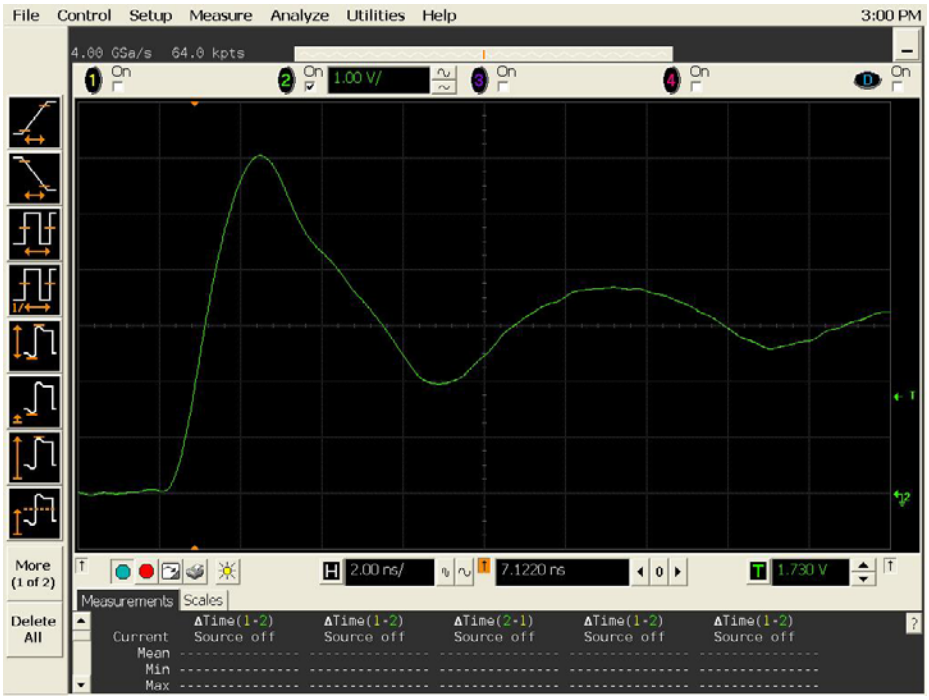


Figure 14b DUT 3557 Post-Annealing Rising Edge

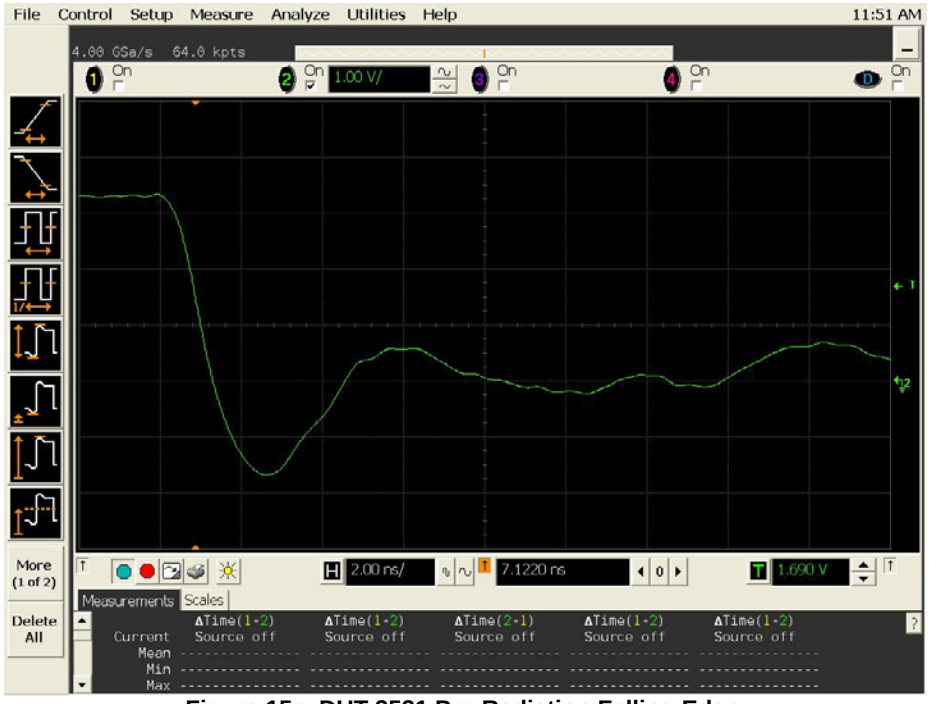


Figure 15a DUT 3531 Pre-Radiation Falling Edge

Figure 15b DUT 3531 Post-Annealing Falling Edge

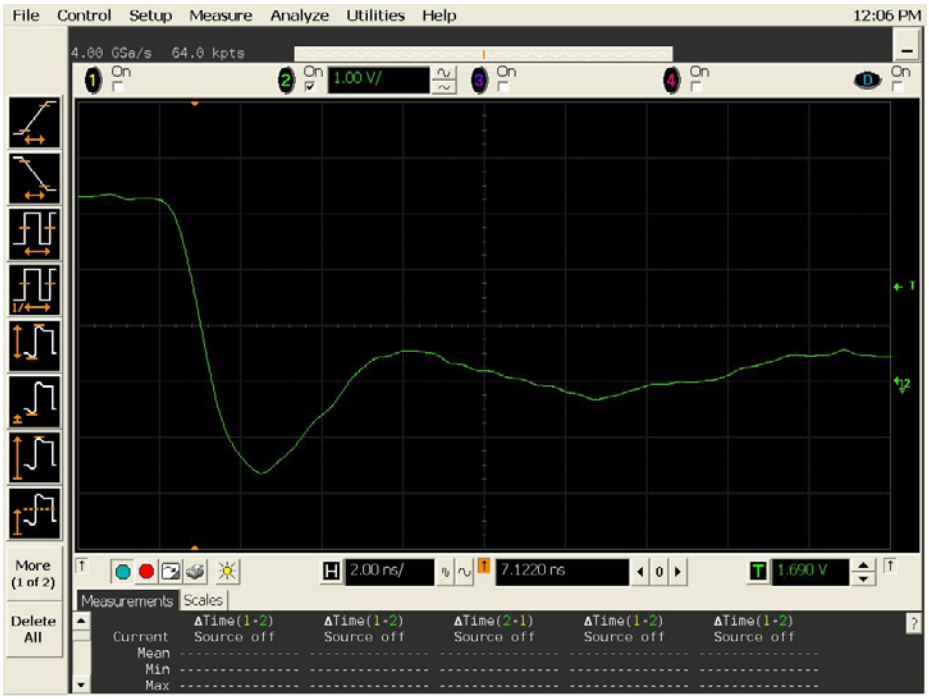


Figure 16a DUT 3532 Pre-Irradiation Falling Edge

Figure 16b DUT 3532 Post-Annealing Falling Edge

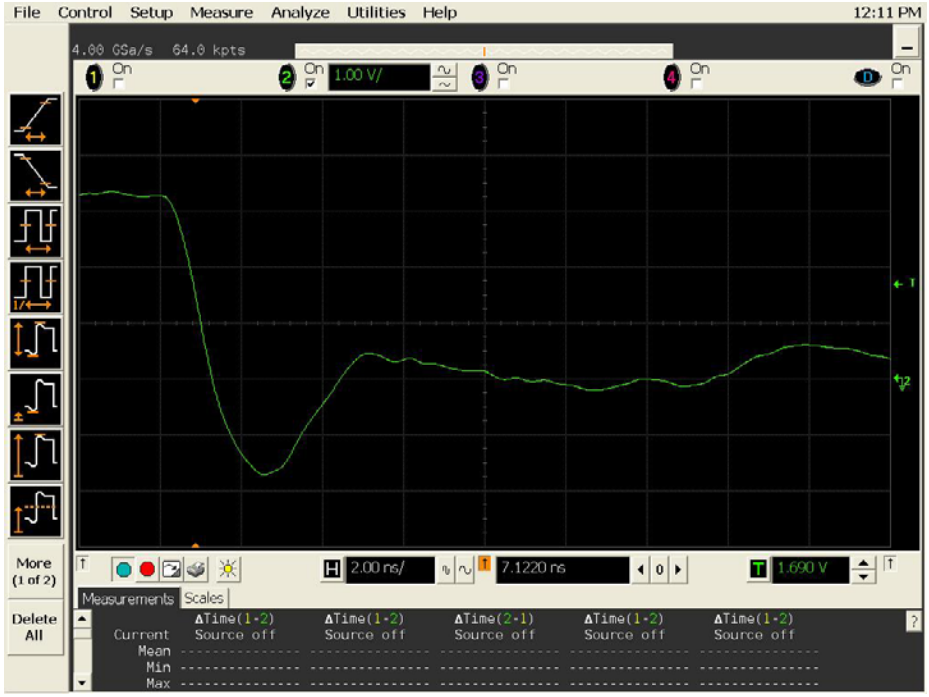


Figure 17a DUT 3541 Pre-Irradiation Falling Edge

Figure 17b DUT 3541 Post-Annealing Falling Edge

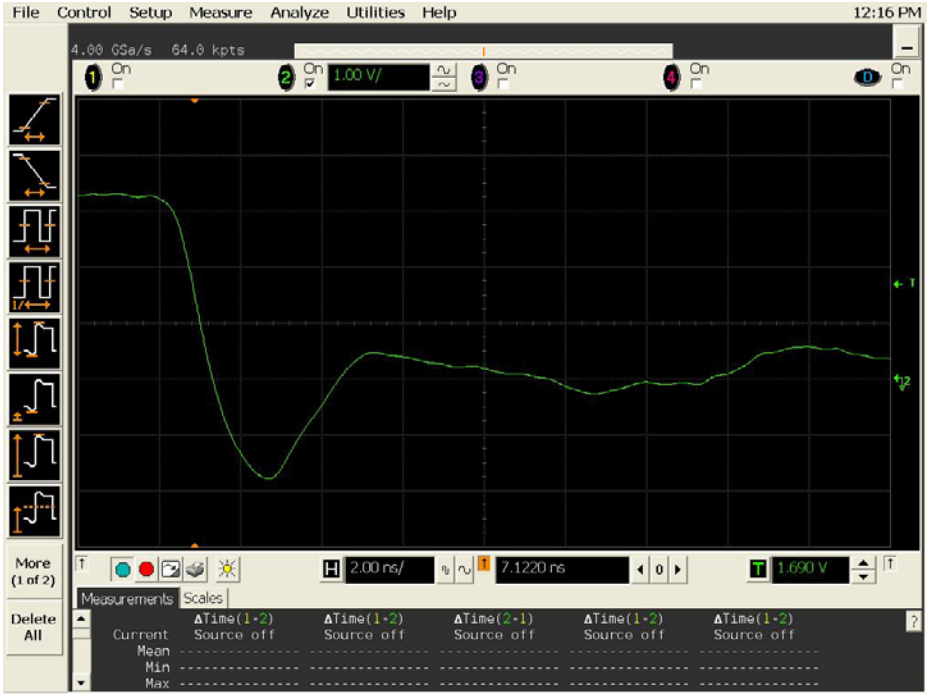


Figure 18a DUT 3542 Pre-Irradiation Falling Edge

Figure 18b DUT 3542 Post-Annealing Falling Edge

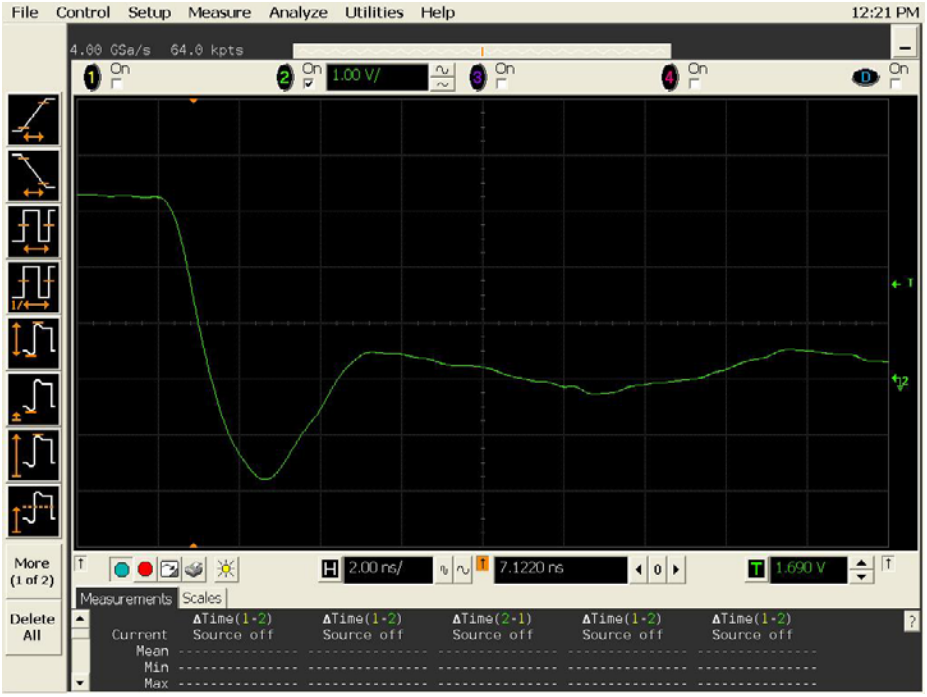


Figure 19a DUT 3556 Pre-Irradiation Falling Edge

Figure 19b DUT 3556 Post-Annealing Falling Edge

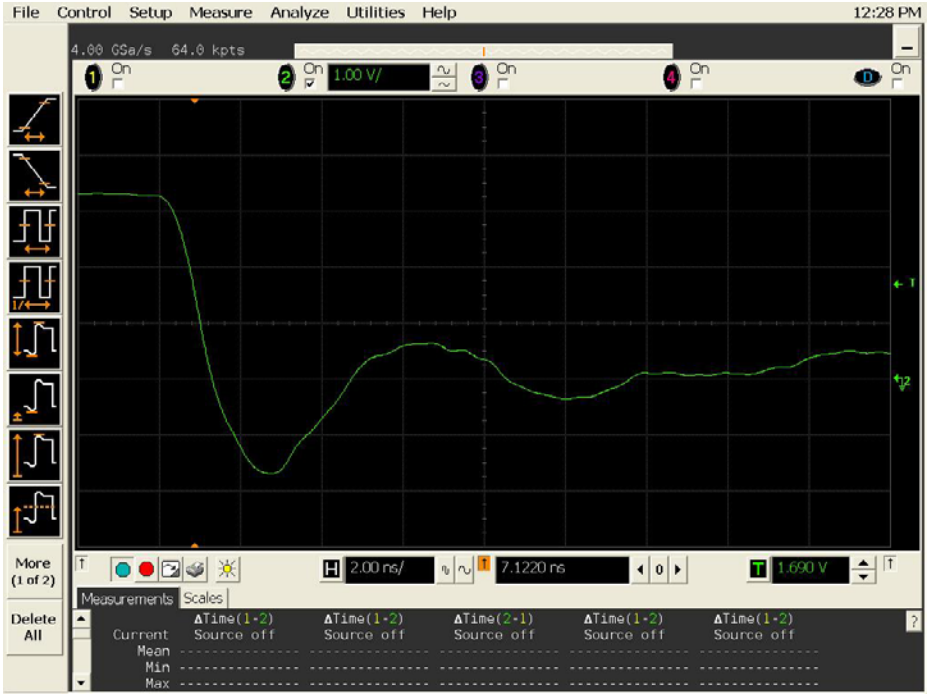


Figure 20a DUT 3557 Pre-Irradiation Falling Edge

Figure 20b DUT 3557 Post-Annealing Falling Edge

Appendix A DUT Bias

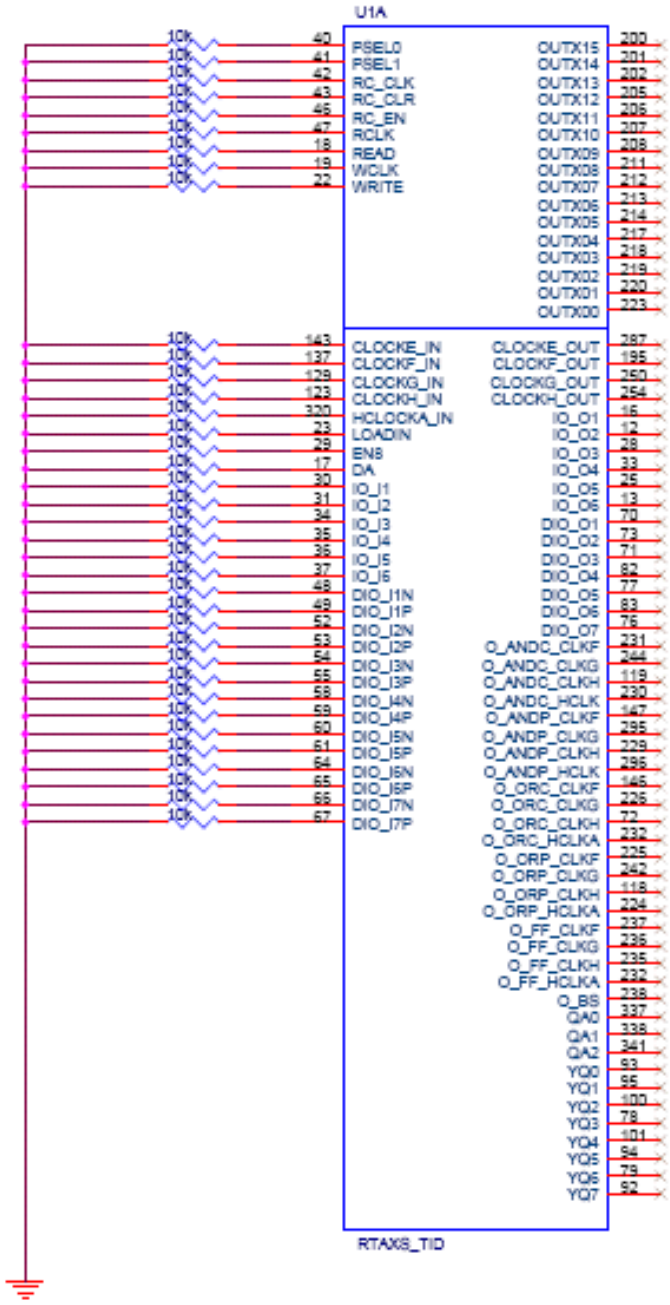


Figure A1 I/O Bias During Irradiation

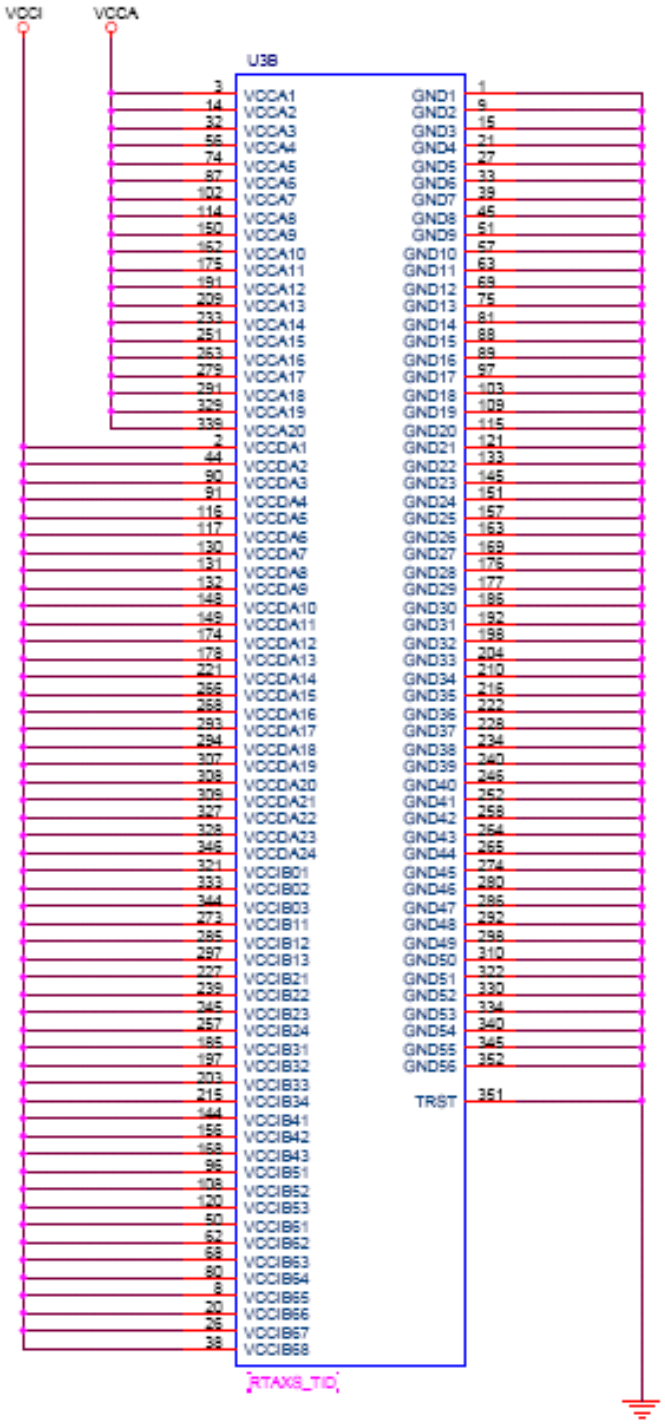
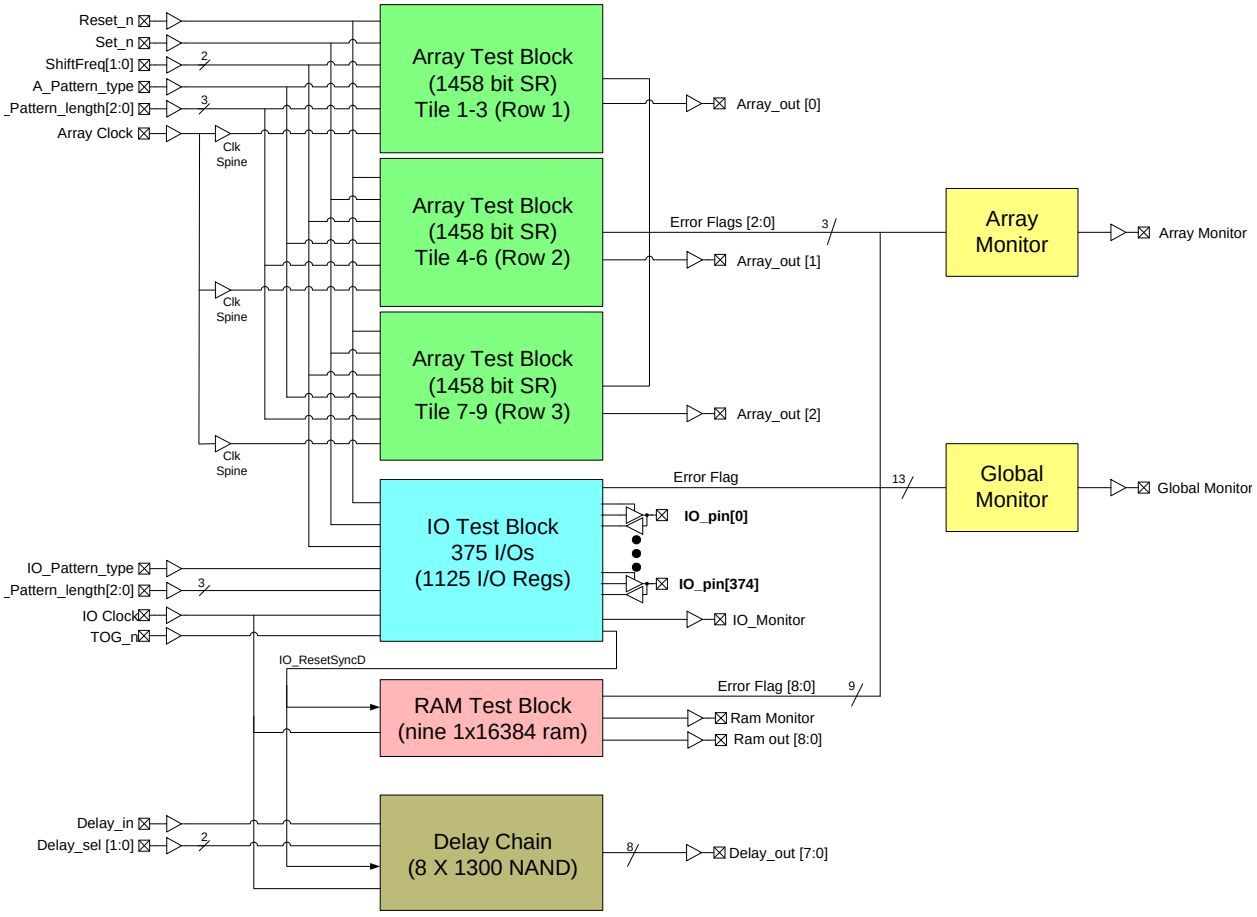


Figure A2 Power Supply, Ground, and Special Pins Bias During Irradiation

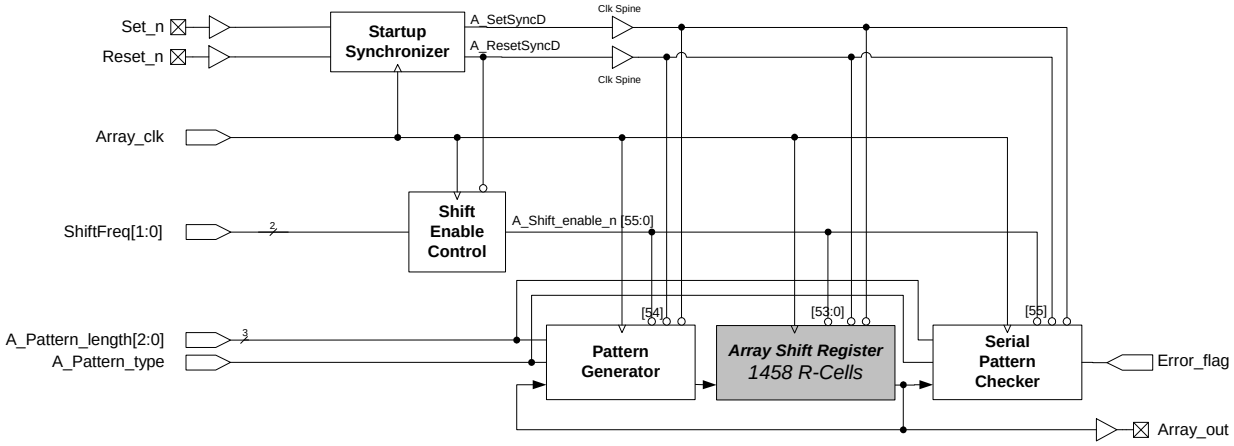
Appendix B DUT Design Schematics

A. Design Blocks Overview

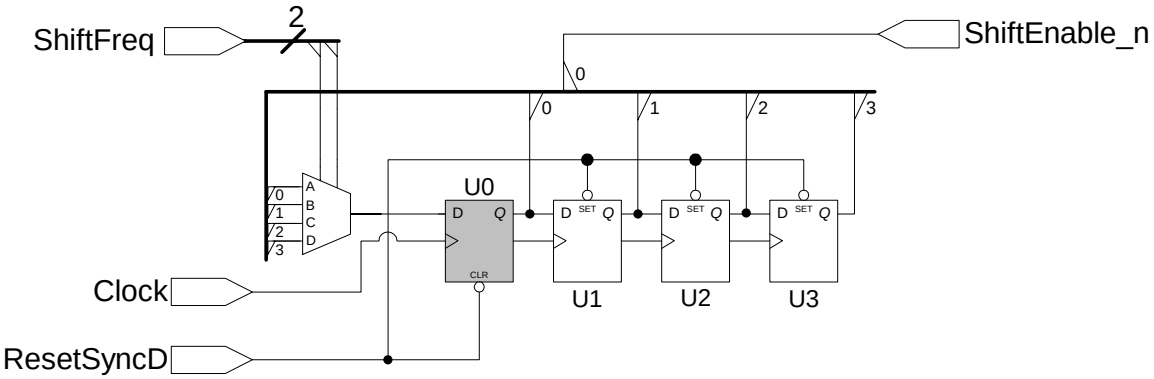
(The diagrams in the following pages schematically illustrate the main blocks of the design. The naming could be different as to the final pins.)



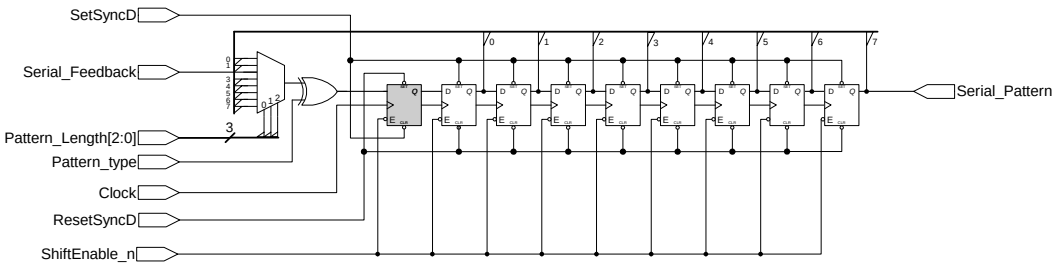
B. Array Test Block



C. Shift Enable Control

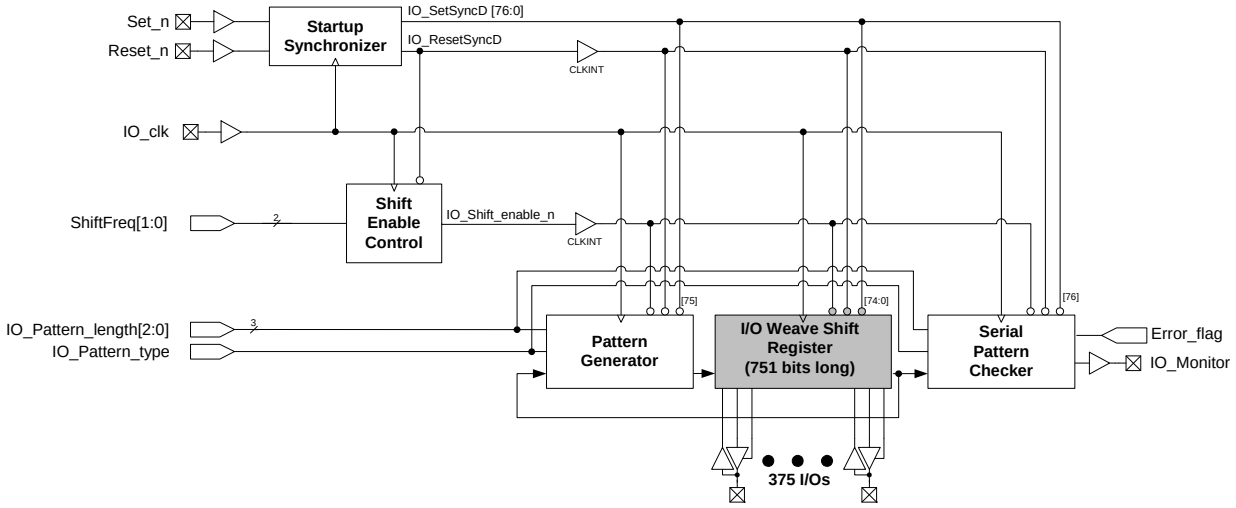


D. Pattern Generator

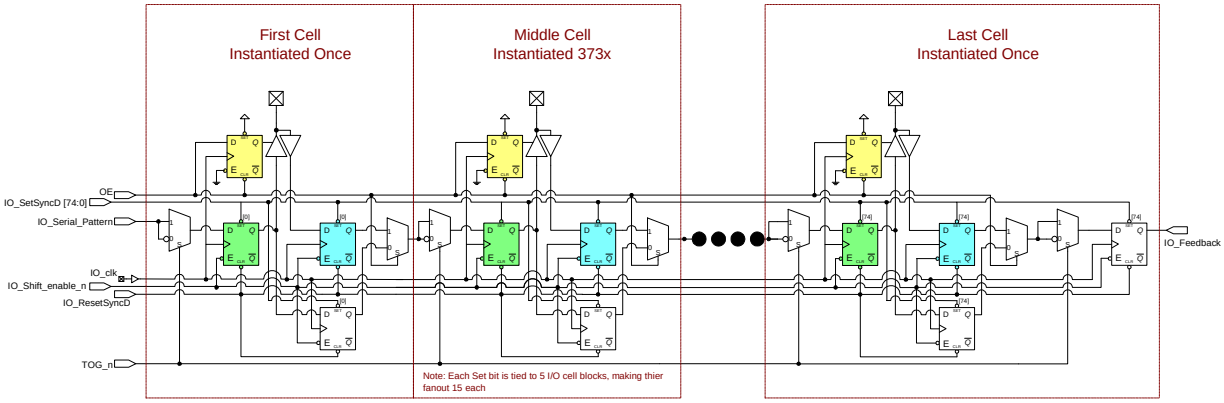


Pattern Type	Pattern Length		Code Length	Δ Bits	Switching Rate
0	000	1 0 ⇨ 0 1 ↰	2	2	100.00%
0	001	1 0 0 ⇨ 0 1 0 ⇨ 0 0 1 ↰	3	2	66.67%
0	010	**One hot I/O at a time switching in entire I/O ring**	#Bits+9	2	N/A
0	011	1 0 0 0 0 ⇨ 0 1 0 0 0 ⇨ 0 0 1 0 0 ⇨ 0 0 0 1 0 ⇨ 0 0 0 0 1 ↰	5	2	40.00%
0	100	1 0 0 0 0 0 ⇨ 0 1 0 0 0 0 ⇨ 0 0 1 0 0 0 ⇨ 0 0 0 1 0 0 ⇨ 0 0 0 0 1 0 ⇨ 0 0 0 0 0 1 ↰	6	2	33.33%
0	101	1 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 ⇨ 0 0 0 1 0 0 0 ⇨ 0 0 0 0 1 0 0 ⇨ 0 0	7	2	28.57%
0	110	1 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 ⇨ 0 0 0 0 1 0	8	2	25.00%
0	111	1 0 0 0 0 0 0 0 0 ⇨ 0 1 0 0 0 0 0 0 0 ⇨ 0 0 1 0 0 0 0 0 0 ⇨ 0 0 0 1 0 0 0 0 0 ⇨ 0 0	9	2	22.22%
1	000	1 0 ⇨ 1 1 ⇨ 0 1 ⇨ 0 0 ↰	2	1	50.00%
1	001	1 0 0 ⇨ 1 1 0 ⇨ 1 1 1 ⇨ 0 1 1 ⇨ 0 0 1 ⇨ 0 0 0 ↰	3	1	33.33%
1	010	**Wave of 0's followed by wave of 1's**	#Bits+9	1	N/A
1	011	1 0 0 0 0 ⇨ 1 1 0 0 0 ⇨ 1 1 1 0 0 ⇨ 1 1 1 1 0 ⇨ 1 1 1 1 1 ⇨ 0 1 1 1 1 ⇨ 0 0 1 1 1 ⇨	5	1	20.00%
1	100	1 0 0 0 0 0 ⇨ 1 1 0 0 0 0 ⇨ 1 1 1 0 0 0 ⇨ 1 1 1 1 0 0 ⇨ 1 1 1 1 1 0 ⇨ 1 1 1 1 1 1 ⇨	6	1	16.67%
1	101	1 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 ⇨ 1 1 1 1 1 0 0 ⇨ 1 1	7	1	14.29%
1	110	1 0 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 ⇨ 1 1 1 1 1 0	8	1	12.50%
1	111	1 0 0 0 0 0 0 0 0 0 ⇨ 1 1 0 0 0 0 0 0 0 ⇨ 1 1 1 0 0 0 0 0 0 ⇨ 1 1 1 1 0 0 0 0 0 ⇨ 1 1	9	1	11.11%

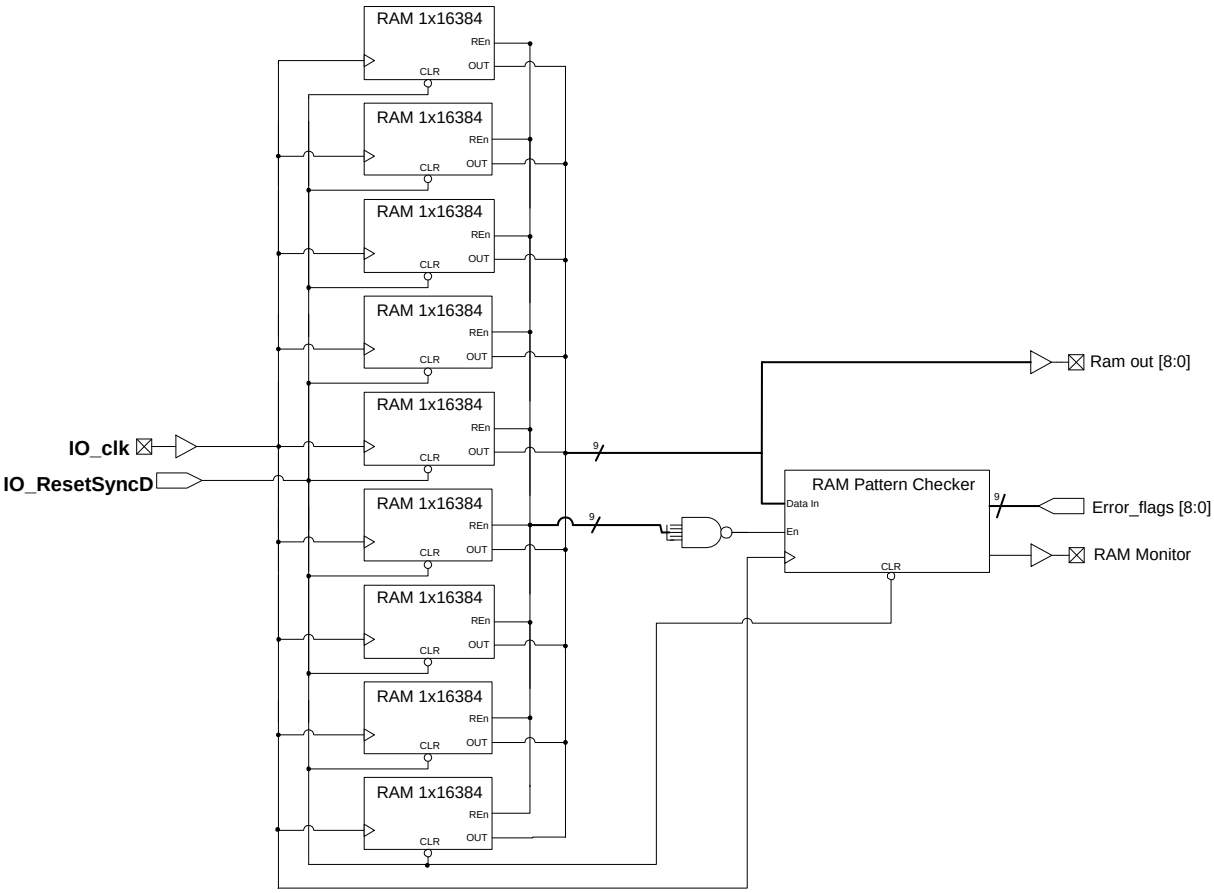
E. I/O Test Block



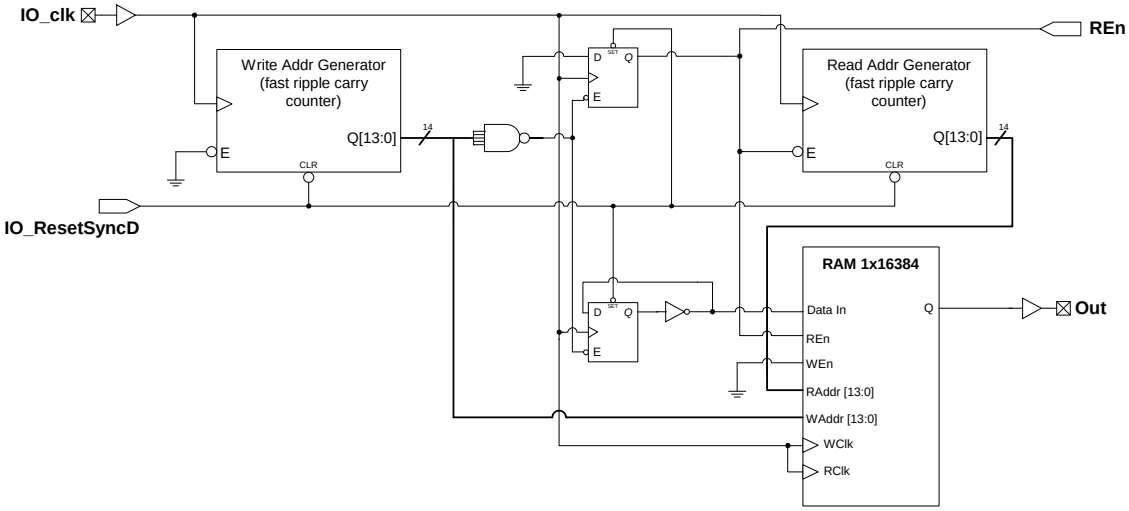
F. I/O Weave Structure



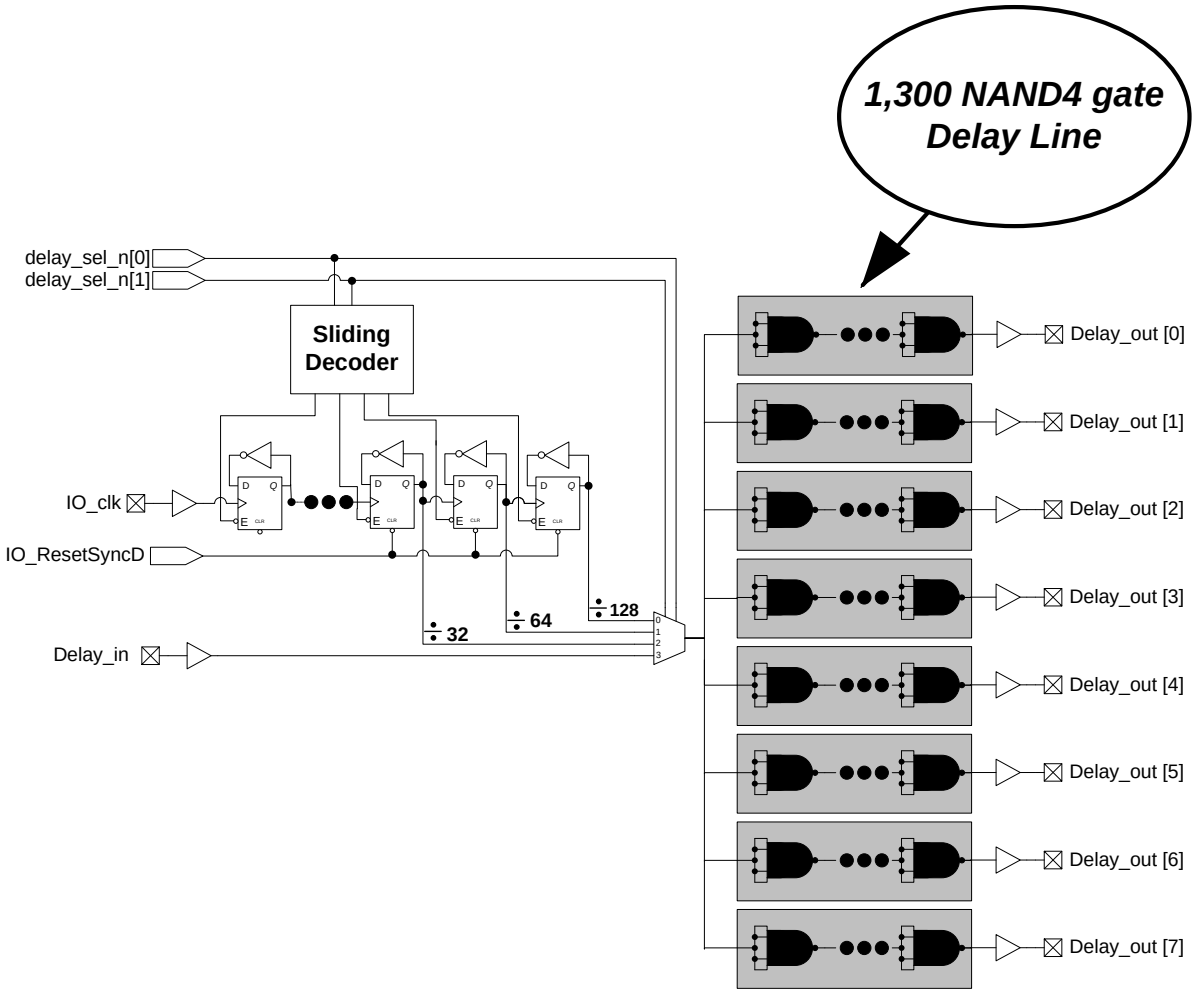
G. RAM Test Block



H. RAM 1x16384



I. Delay Chains



Microsemi Corporate Headquarters
2381 Morse Avenue, Irvine, CA 92614
Phone; 949.221.7100 · Fax: 949.756.0308
www.microsemi.com

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