Actel
POWER MATTERS

TOTAL IONIZING DOSE TEST REPORT

No. 10T-RTSX72SU-CQ256-D1SG11
March 26, 2010
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 60 krad (Si) per 25-mA spec after 7-day room temperature annealing.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10%-degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 μm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1SG11
Quantity Tested	6
Serial Number	40 krad: 436, 445 60 krad: 431, 435 100 krad: 424, 429
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

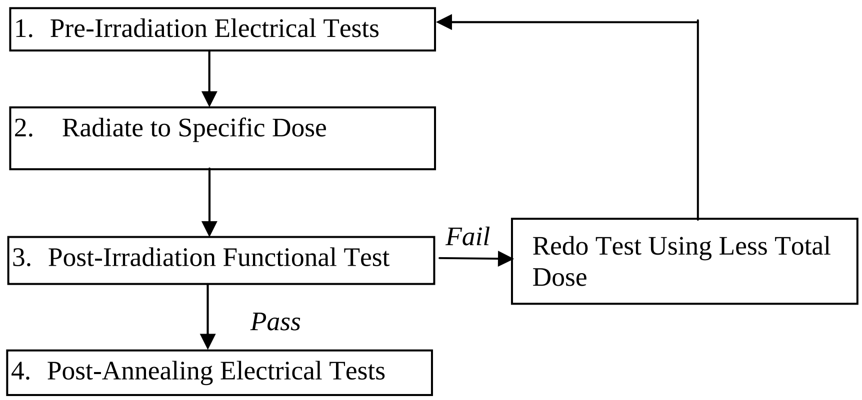


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. Every DUT is annealed for approximately 7 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{IL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{IL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Table 3 shows the post-annealing I_{CC} (I_{CCA} + I_{CCI}) for 60 krad(SiO_2)-irradiated DUTs, DUT 431 and 435, nearly pass the spec of 25 mA. Therefore, it is estimated that this lot should pass I_{CC} spec at least for 60 krad(SiO_2).

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-rad	Post-rad	Post-ann	Pre-rad	Post-rad	Post-ann
424	100 krad	1.30	263	159	0.8	197	69
429	100 krad	1.30	263	128	0.8	196	65
431	60 krad	1.37	21	17	0.8	22.6	10
435	60 krad	1.30	22	18	0.8	26	12
436	40 krad	1.30	3.3	4	0.8	16	2
445	40 krad	1.40	3.2	3	0.9	15.7	2

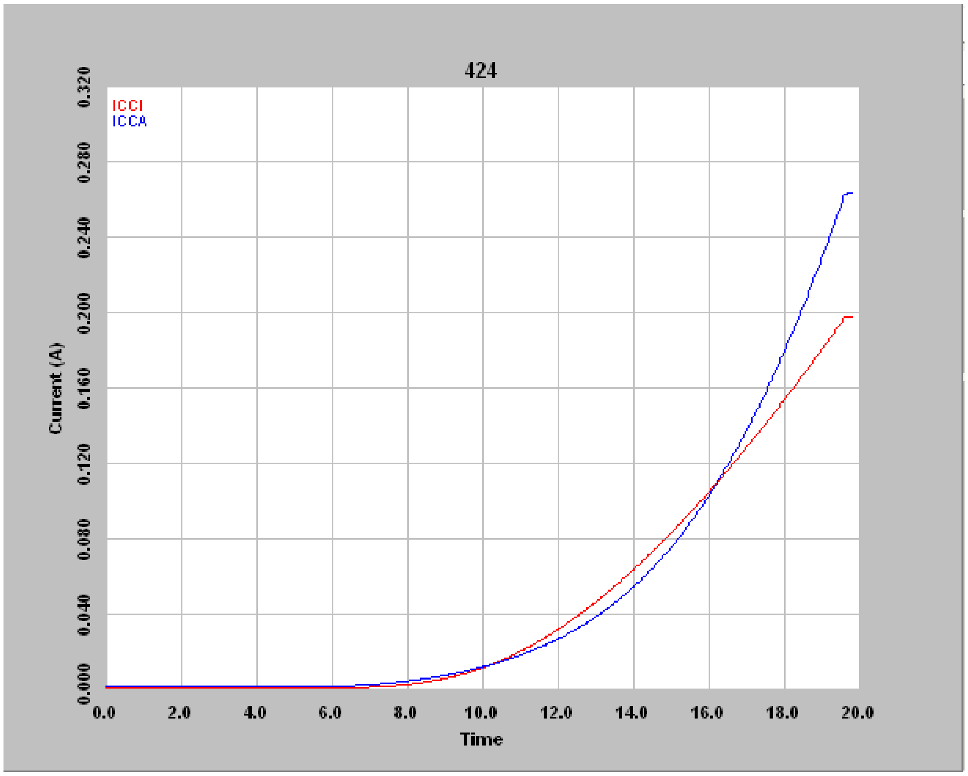


Figure 2 DUT 424 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

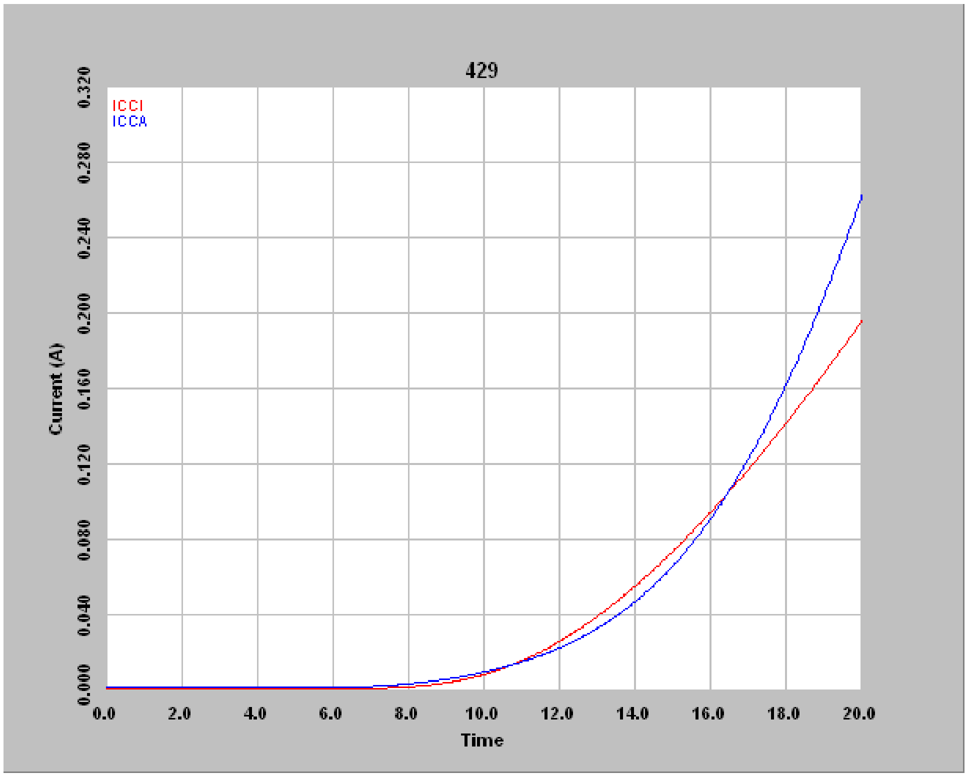


Figure 3 DUT 429 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

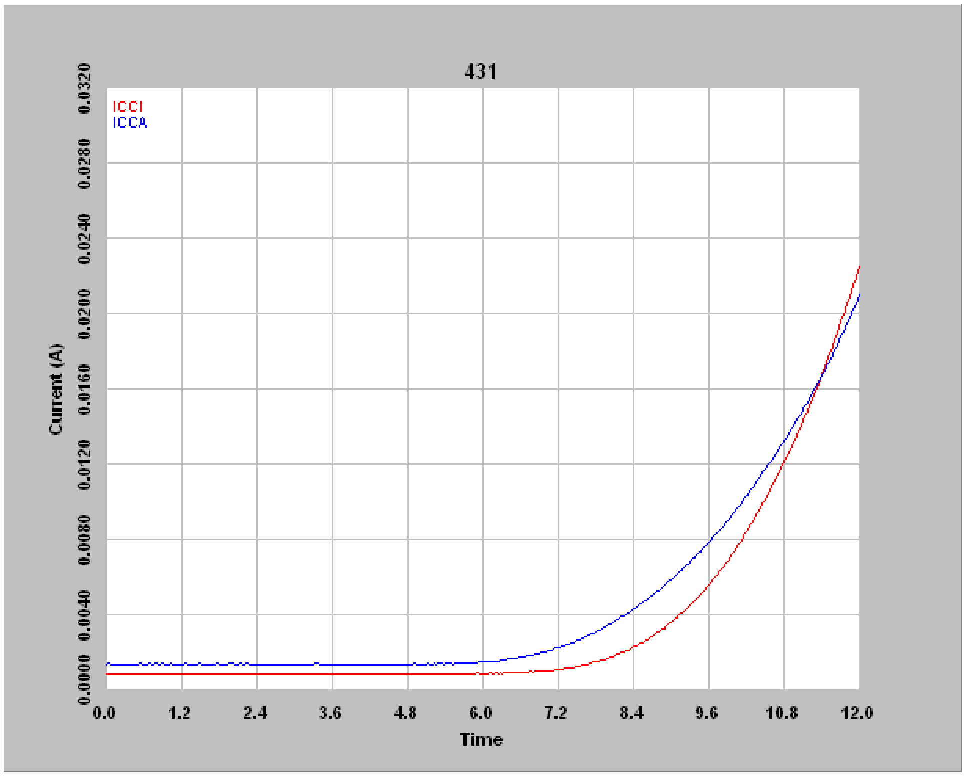


Figure 4 DUT 431 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

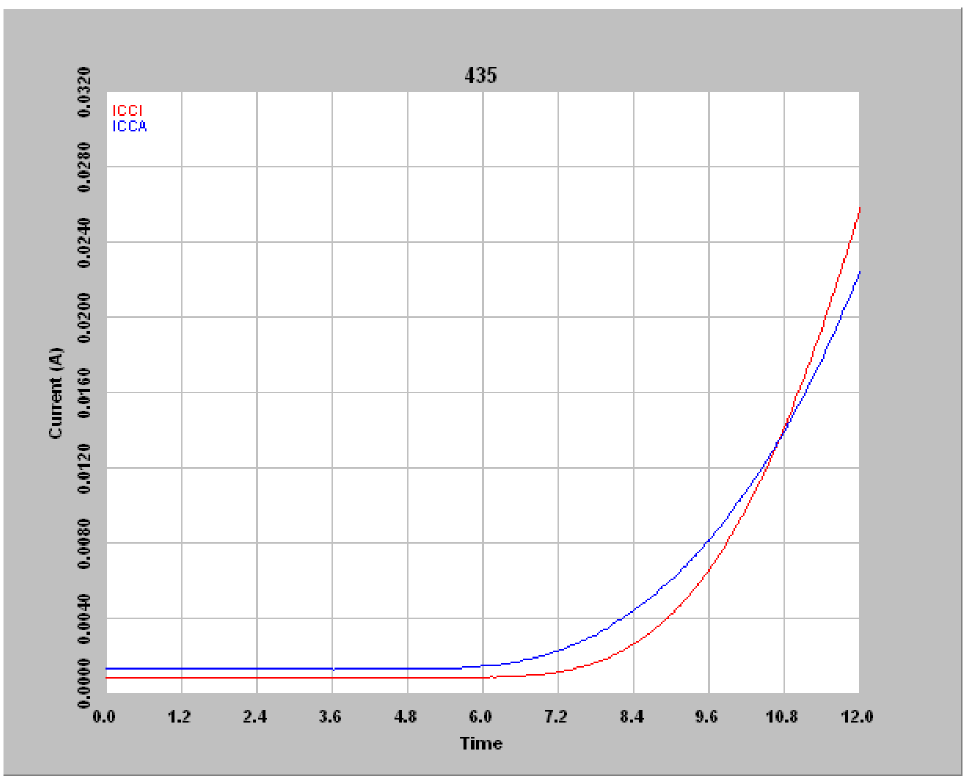


Figure 5 DUT 435 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

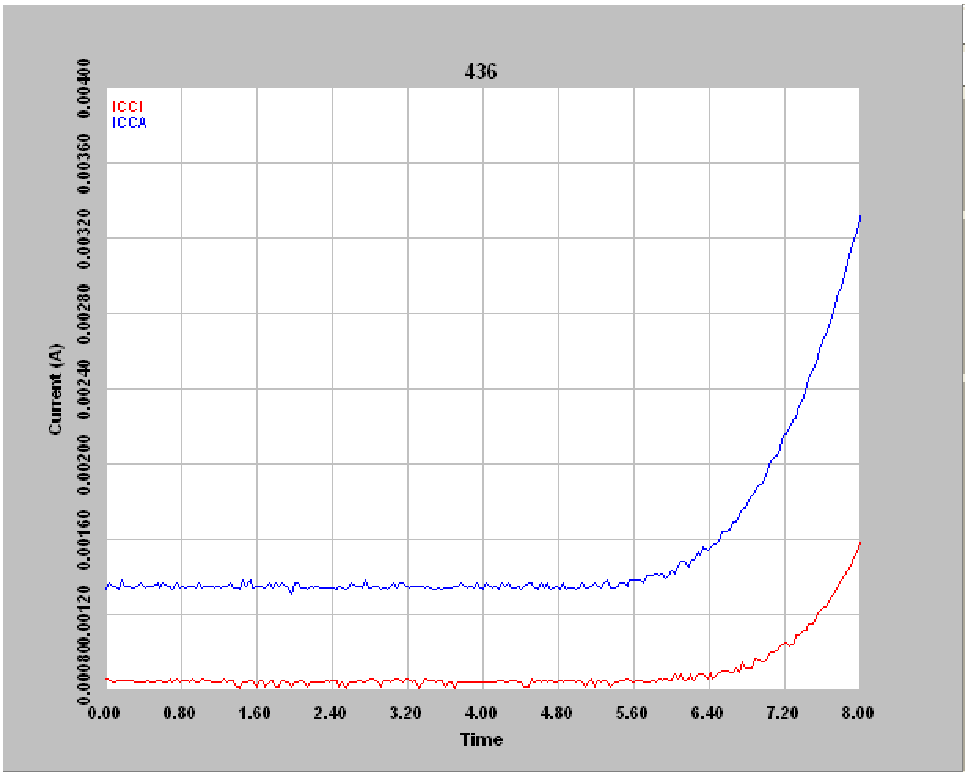


Figure 6 DUT 436 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

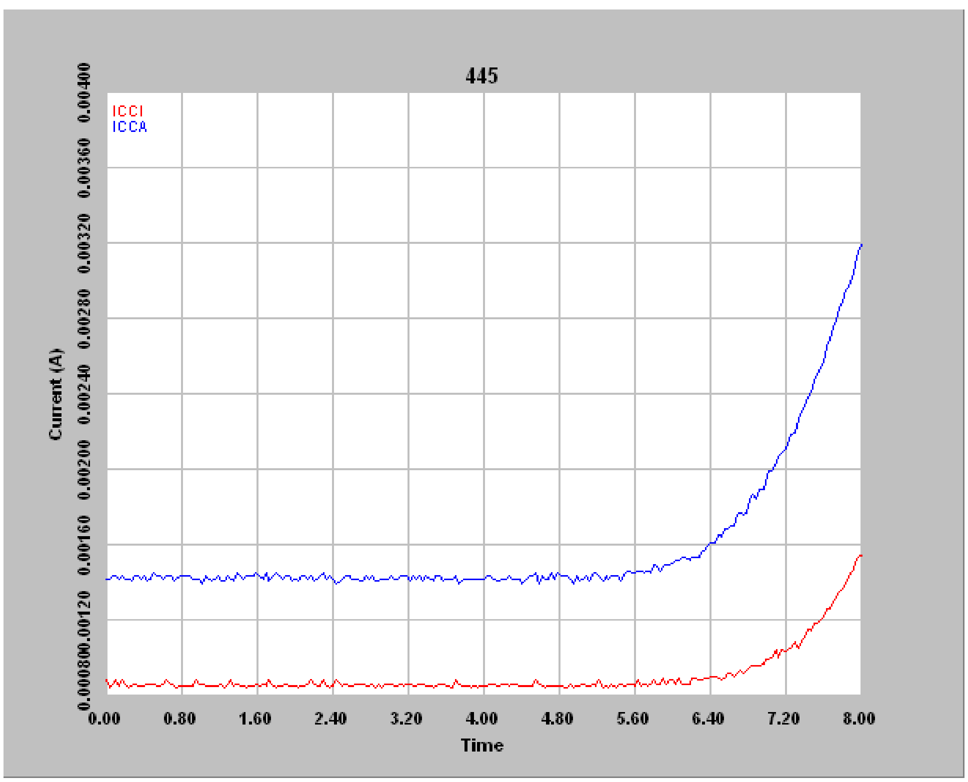


Figure 7 DUT 445 in-flux I_{CCA} and I_{CCI}. The time scale converts to total dose by applying equation: 1 min × 5 krad/min = 5 krad.

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits; for each measurement, the post-annealing value is within ±10% of pre-irradiated value.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA/QA0				DAH/QA0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.55	1.66	1.31	1.28	1.46	1.59	1.37	1.52
429	100 krad	1.56	1.63	1.31	1.38	1.47	1.60	1.37	1.47
431	60 krad	1.55	1.52	1.30	1.33	1.47	1.55	1.37	1.31
435	60 krad	1.57	1.58	1.30	1.27	1.48	1.55	1.36	1.31
436	40 krad	1.56	1.54	1.31	1.28	1.48	1.53	1.38	1.31
445	40 krad	1.56	1.54	1.30	1.28	1.47	1.53	1.37	1.30

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTRH/YO0H				IDII0/IDIO0			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.45	1.58	1.39	1.37	1.54	1.66	1.32	1.20
429	100 krad	1.45	1.50	1.37	1.41	1.55	1.60	1.32	1.43
431	60 krad	1.46	1.54	1.39	1.30	1.61	1.56	1.26	1.26
435	60 krad	1.46	1.55	1.35	1.30	1.60	1.56	1.25	1.31
436	40 krad	1.45	1.53	1.35	1.31	1.58	1.57	1.28	1.28
445	40 krad	1.45	1.52	1.39	1.31	1.55	1.55	1.32	1.29

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII1/IDIO1			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.46	1.57	1.30	1.31
429	100 krad	1.50	1.58	1.31	1.42
431	60 krad	1.48	1.56	1.25	1.27
435	60 krad	1.47	1.57	1.25	1.27
436	40 krad	1.48	1.57	1.26	1.25
445	40 krad	1.47	1.55	1.32	1.28

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2/IDIO2				IDII3/IDIO3			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.56	1.57	1.31	1.33	NA	NA	NA	NA
429	100 krad	1.55	1.59	1.31	1.40	1.56	1.56	1.32	1.36
431	60 krad	1.62	1.57	1.25	1.26	1.59	1.56	1.24	1.26
435	60 krad	1.59	1.57	1.25	1.27	1.58	1.57	1.23	1.26
436	40 krad	1.64	1.58	1.26	1.27	1.61	1.56	1.23	1.26
445	40 krad	1.56	1.52	1.31	1.31	1.62	1.55	1.23	1.27

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4/IDIO4				IDII5/IDIO5			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.49	1.49	1.30	1.32	1.45	1.54	1.37	1.34
429	100 krad	1.45	1.51	1.30	1.35	1.45	1.58	1.34	1.35
431	60 krad	1.49	1.46	1.31	1.30	1.47	1.49	1.36	1.32
435	60 krad	1.48	1.47	1.30	1.30	1.46	1.49	1.36	1.29
436	40 krad	1.50	1.46	1.28	1.28	1.47	1.50	1.37	1.30
445	40 krad	1.46	1.46	1.30	1.32	1.44	1.52	1.36	1.28

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6/IDIO6				IDII7/IDIO7			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
424	100 krad	1.45	1.58	1.35	1.29	1.44	1.46	1.35	1.36
429	100 krad	1.55	1.60	1.32	1.42	1.46	1.50	1.36	1.40
431	60 krad	1.61	1.56	1.25	1.26	1.48	1.47	1.37	1.38
435	60 krad	1.63	1.58	1.22	1.27	1.47	1.46	1.36	1.37
436	40 krad	1.64	1.58	1.24	1.26	1.52	1.57	1.27	1.26
445	40 krad	1.62	1.57	1.26	1.27	1.52	1.45	1.32	1.37

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies within ±10% with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
424	100 krad	0.0098	0.0241	0.104	0.122	0.173	0.193	0.434	0.464	0.951	0.941
429	100 krad	0.0109	0.0260	0.109	0.141	0.180	0.225	0.452	0.546	1.192	1.122
431	60 krad	0.0107	0.0111	0.107	0.108	0.177	0.179	0.445	0.449	0.914	0.920
435	60 krad	0.0107	0.0112	0.107	0.108	0.176	0.178	0.443	0.445	0.910	0.913
436	40 krad	0.0108	0.0092	0.108	0.106	0.179	0.178	0.449	0.448	0.924	0.920
445	40 krad	0.0106	0.0092	0.107	0.106	0.177	0.176	0.445	0.444	0.916	0.913

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
424	100 krad	4.988	4.988	4.864	4.863	4.654	4.639	4.062	4.028	2.684	2.548
429	100 krad	4.988	4.984	4.864	4.861	4.647	4.642	4.060	4.054	2.721	2.741
431	60 krad	4.989	4.986	4.866	4.863	4.651	4.646	4.070	4.060	2.740	2.721
435	60 krad	4.988	4.986	4.864	4.862	4.647	4.643	4.056	4.048	2.684	2.663
436	40 krad	4.988	4.989	4.865	4.866	4.649	4.651	4.063	4.068	2.734	2.751
445	40 krad	4.989	4.987	4.866	4.866	4.652	4.653	4.075	4.007	2.781	2.781

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. All DUTs pass the 10%-degradation criterion. The small negative degradations for 40 krad and 60 krad data are probably mostly due to the measurement inaccuracy.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (μs)	Post-Annealing (μs)	Degradation (%)
424	100 krad	1.34180	1.40150	4.45%
429	100 krad	1.34595	1.39095	3.34%
431	60 krad	1.32885	1.32730	-0.12%
435	60 krad	1.35630	1.35350	-0.21%
436	40 krad	1.31645	1.31030	-0.47%
445	40 krad	1.29820	1.29225	-0.46%

F. *Transition Time*

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

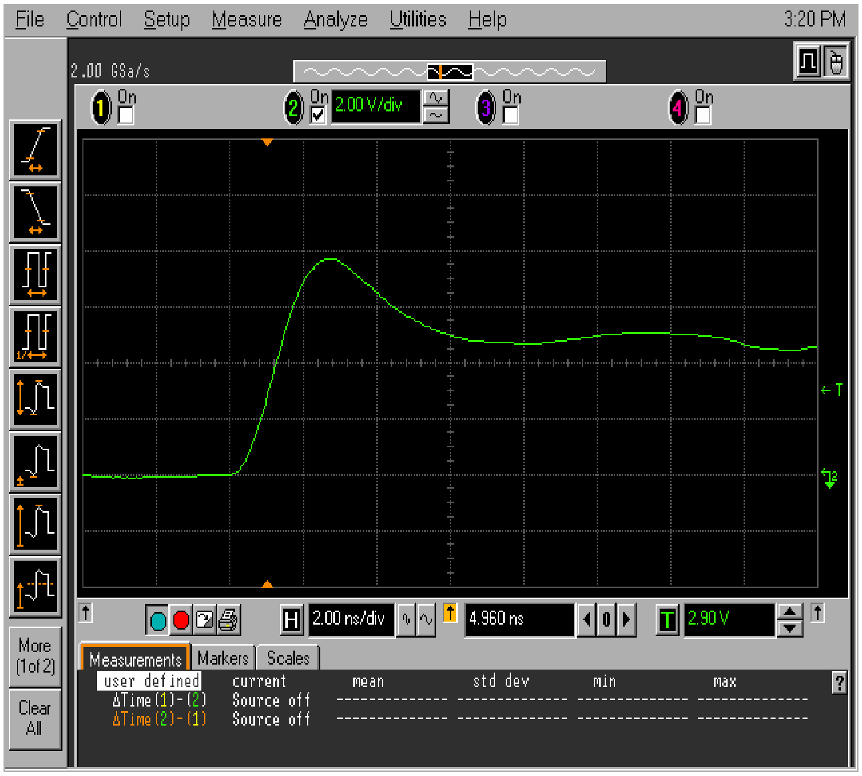


Figure 8(a) DUT 424 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

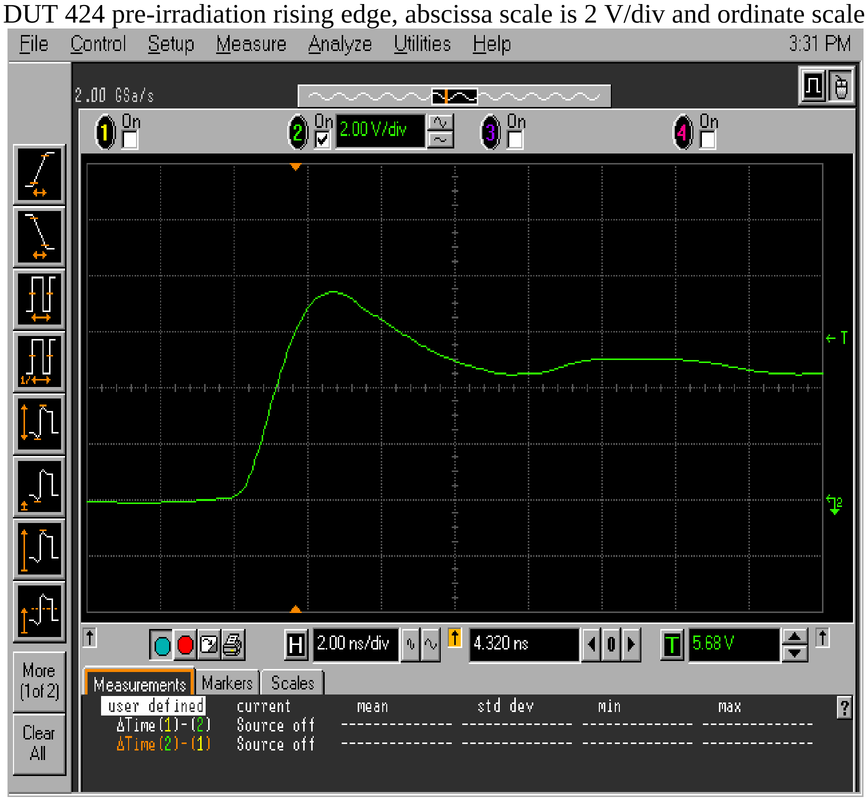


Figure 8(b) DUT 424 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

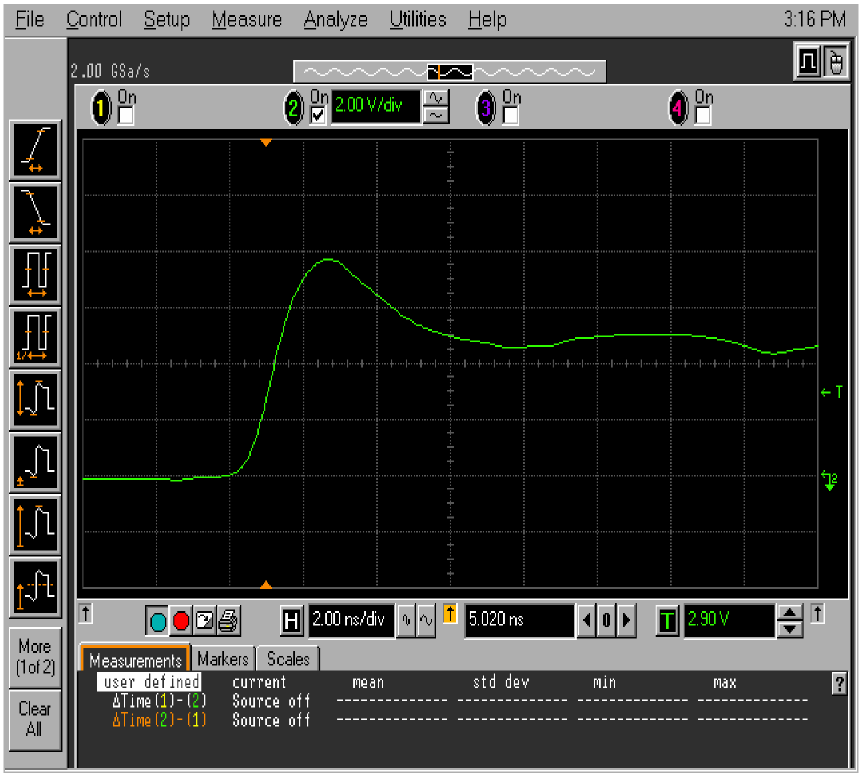


Figure 9(a) DUT 429 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

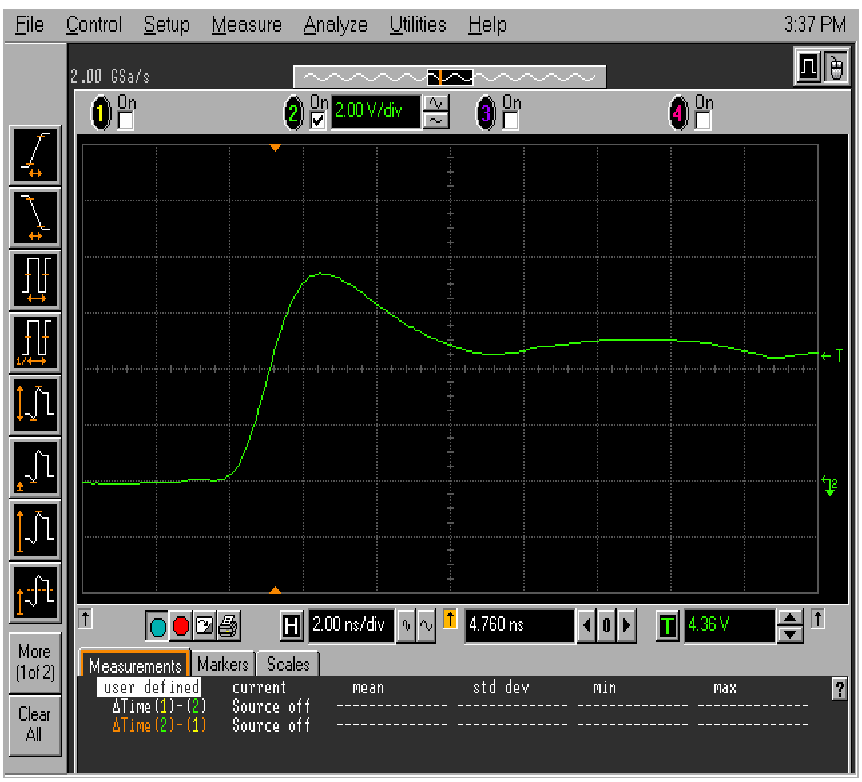


Figure 9(b) DUT 429 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

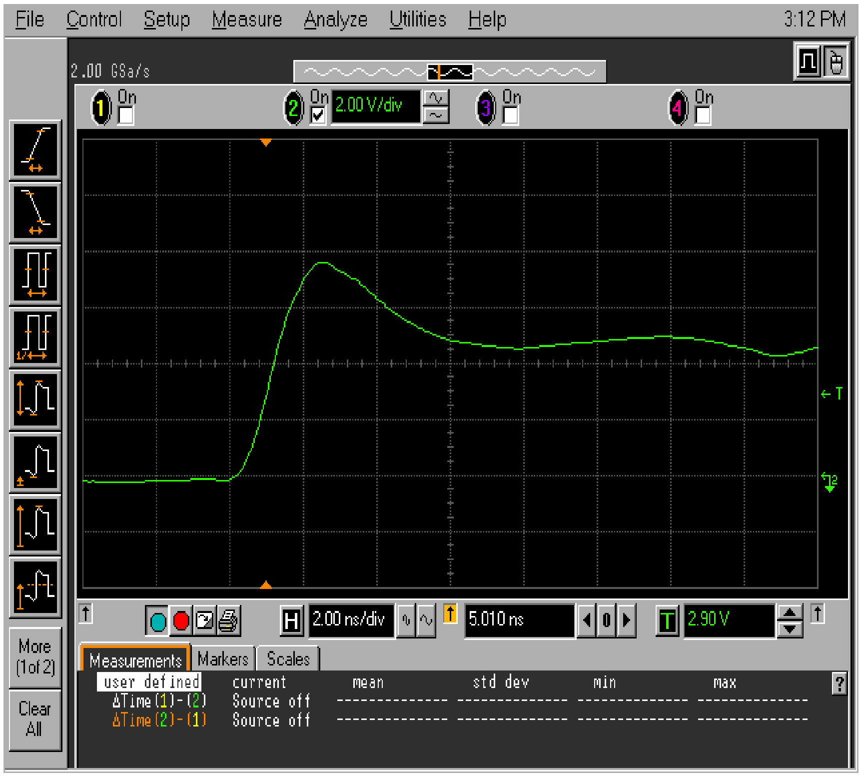


Figure 10(a) DUT 431 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

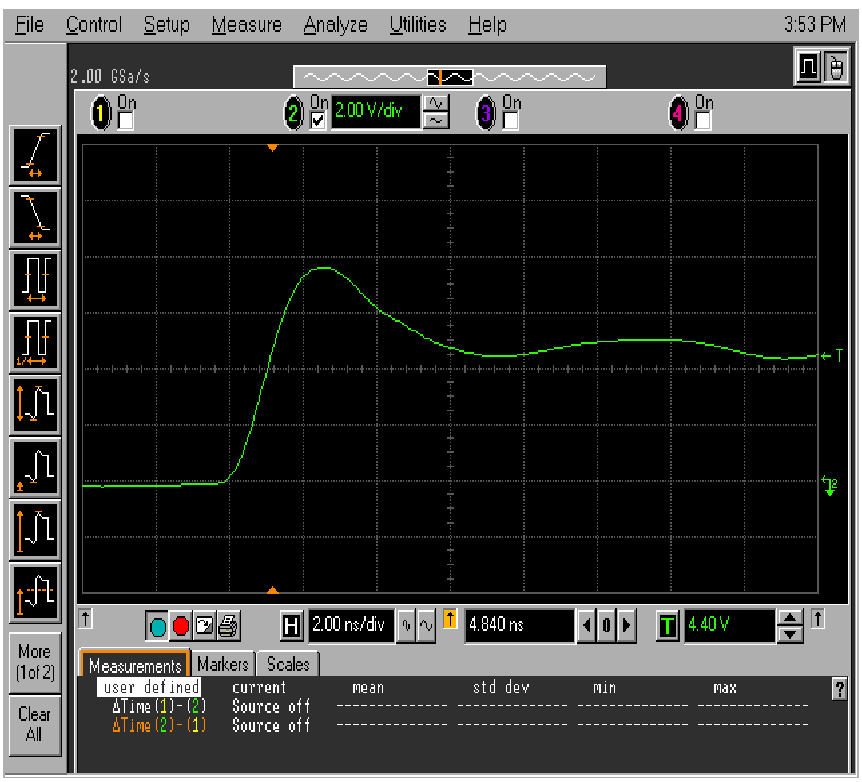


Figure 10(b) DUT 431 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

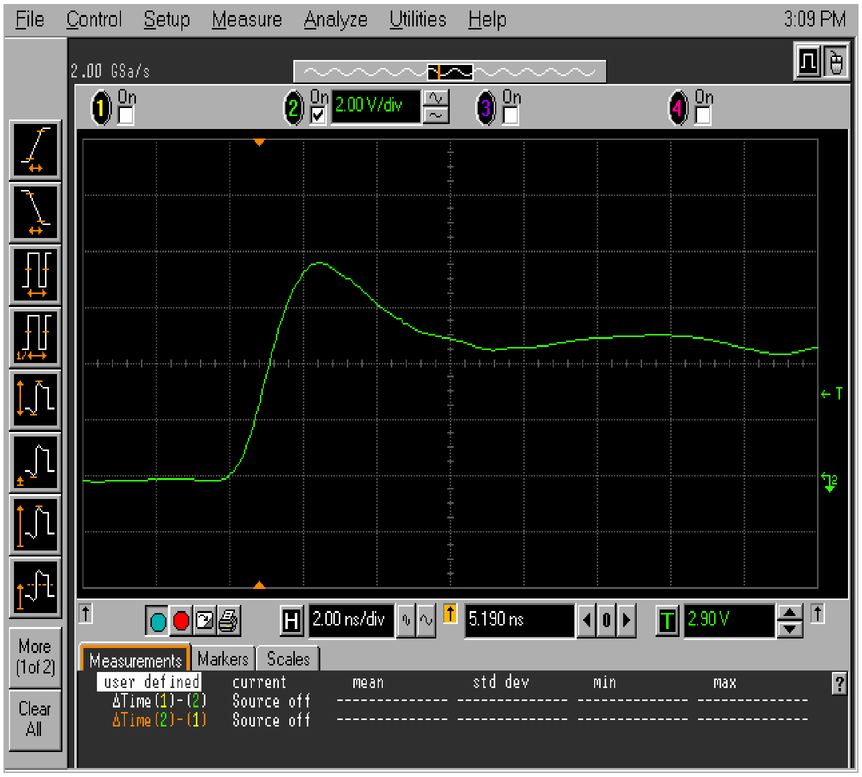


Figure 11(a) DUT 435 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

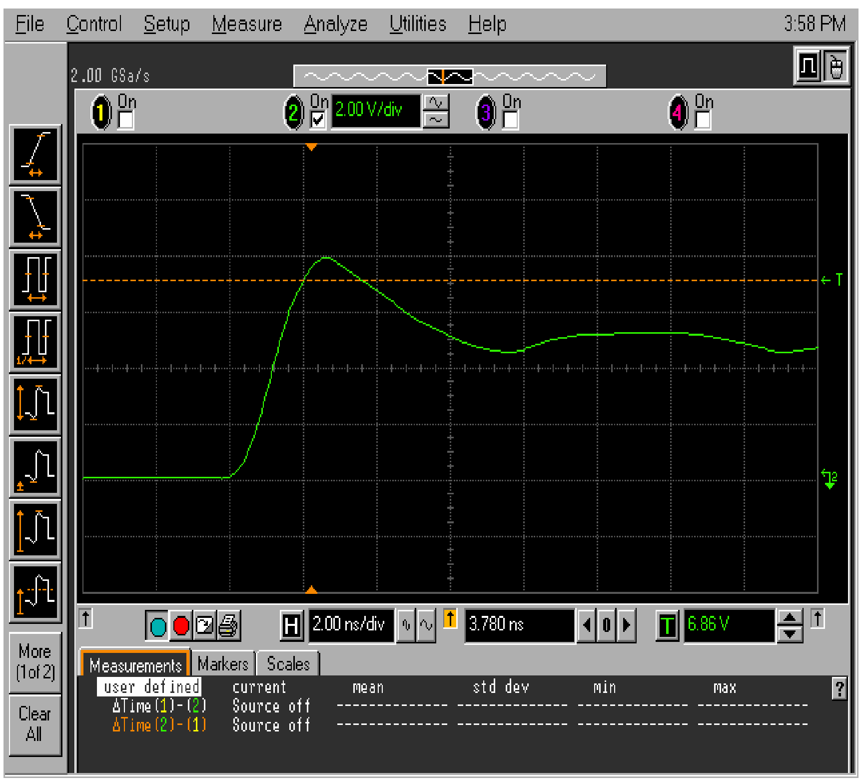


Figure 11(b) DUT 435 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

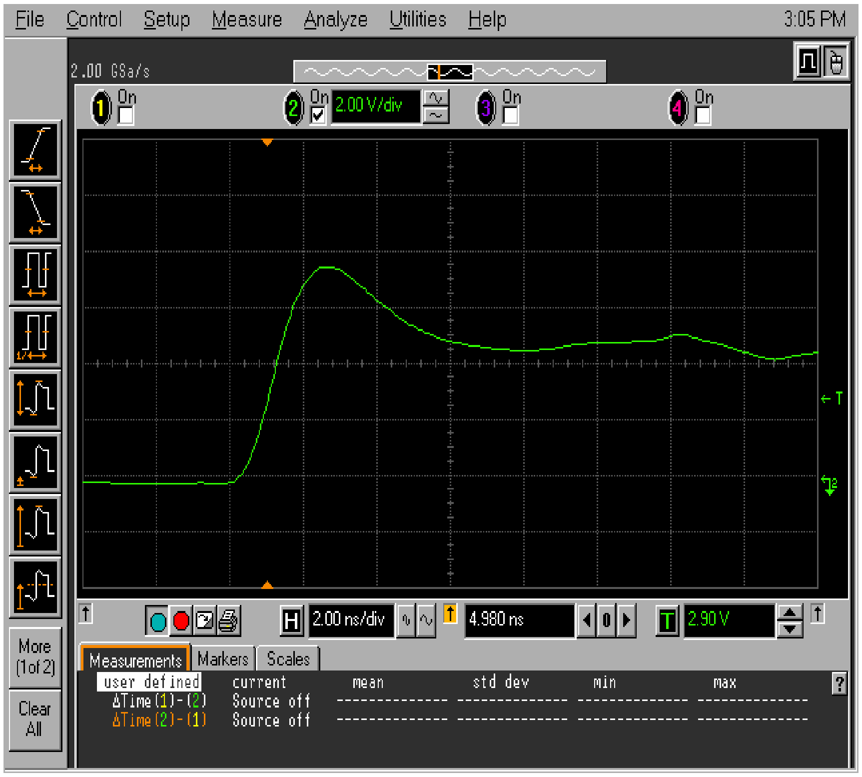


Figure 12(a) DUT 436 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

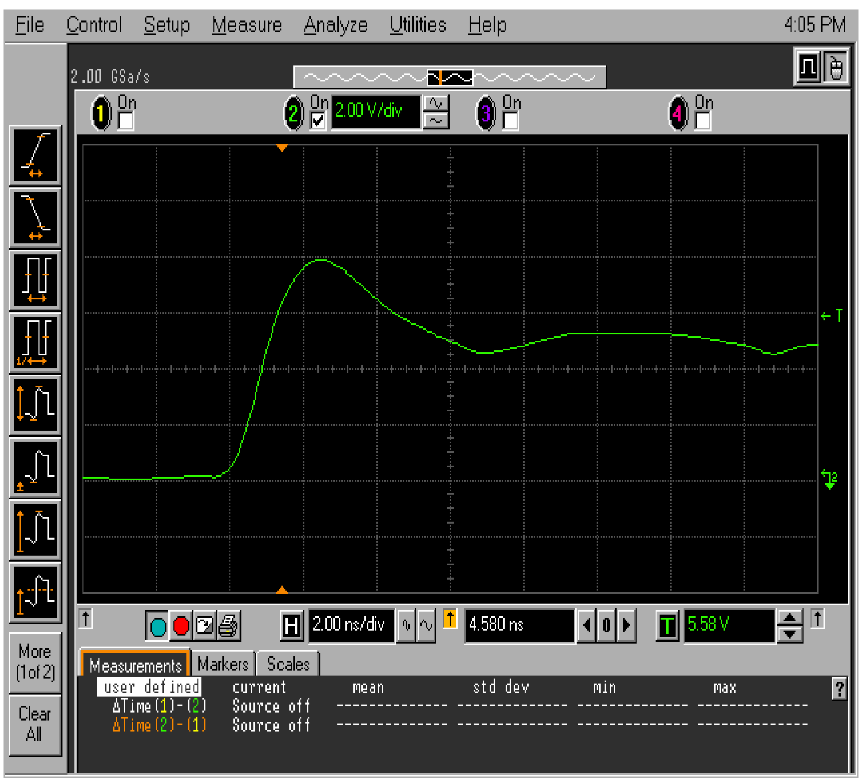


Figure 12(b) DUT 436 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

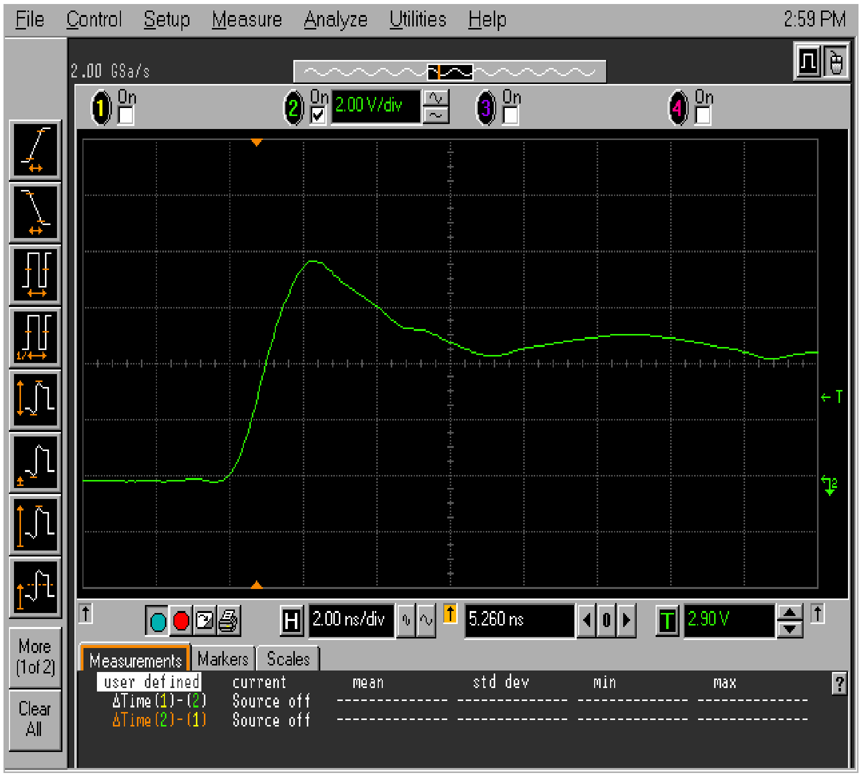


Figure 13(a) DUT 445 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

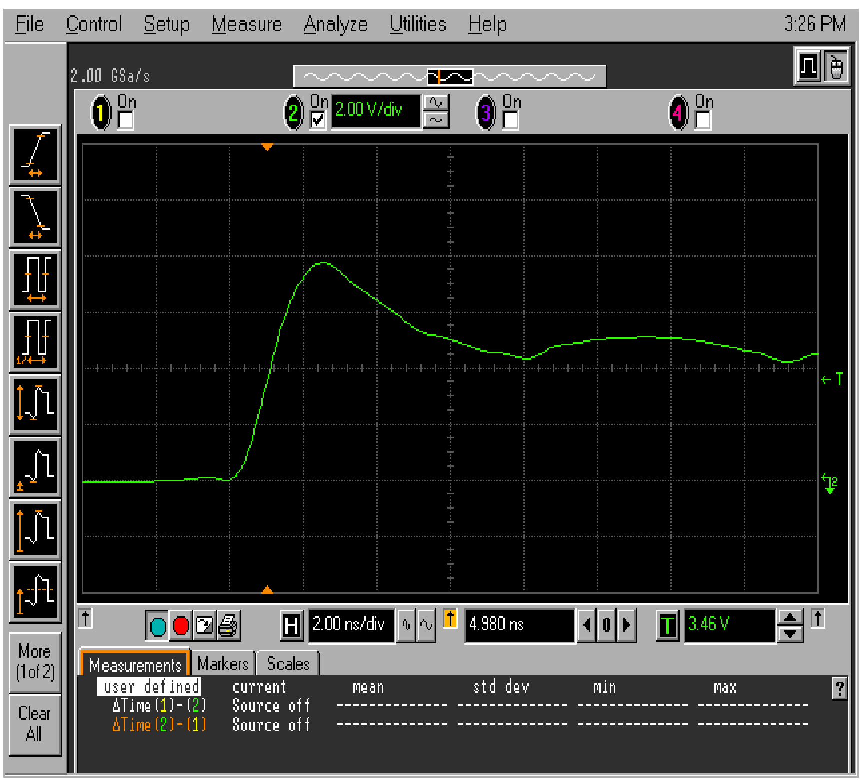


Figure 13(b) DUT 445 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

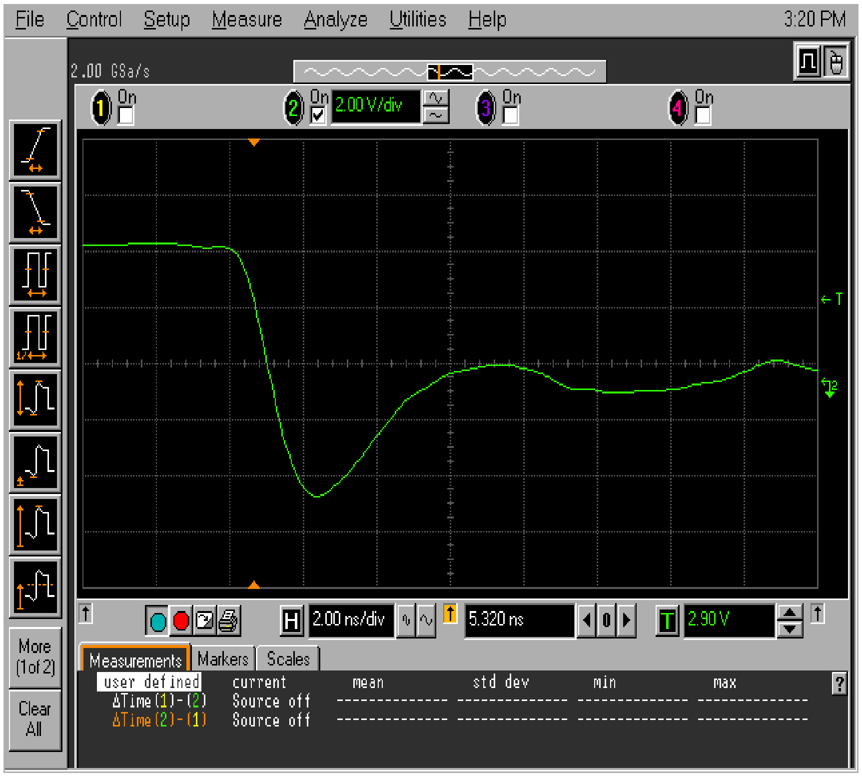


Figure 14(a) DUT 424 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

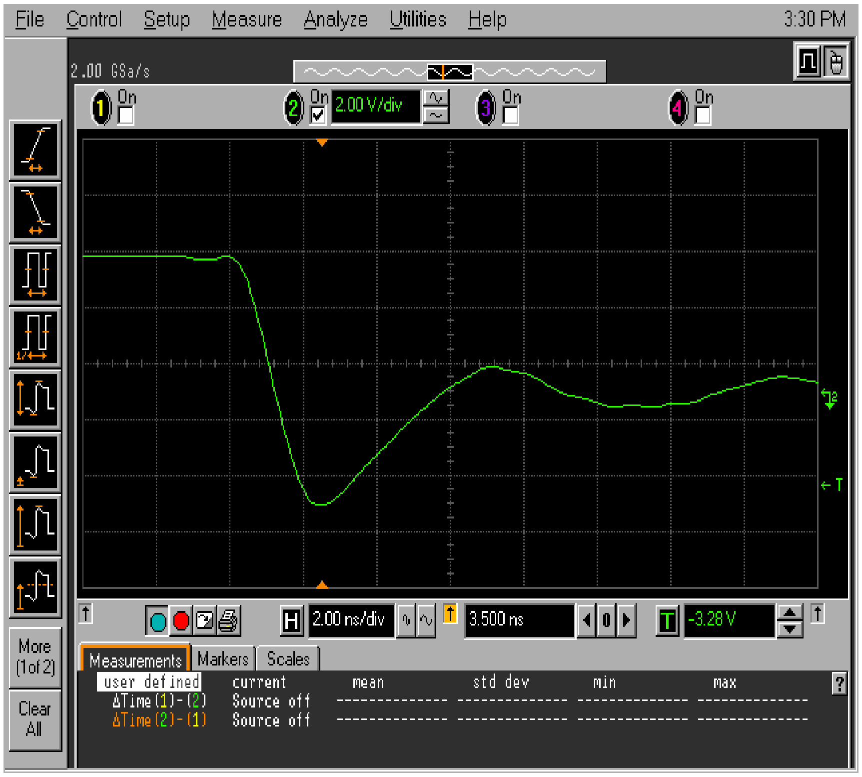


Figure 14(b) DUT 424 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

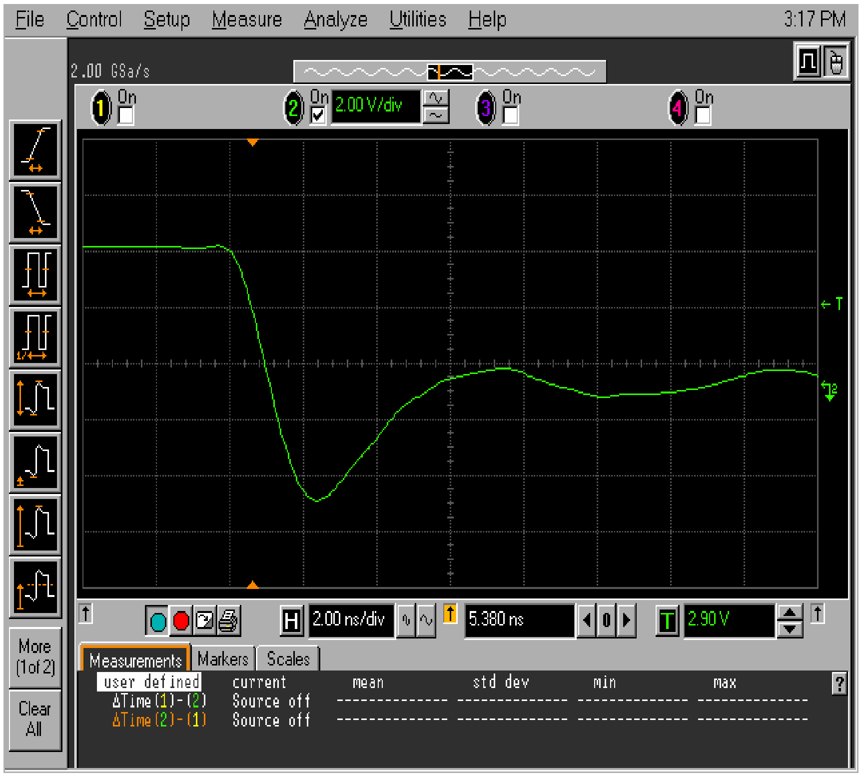


Figure 15(a) DUT 429 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

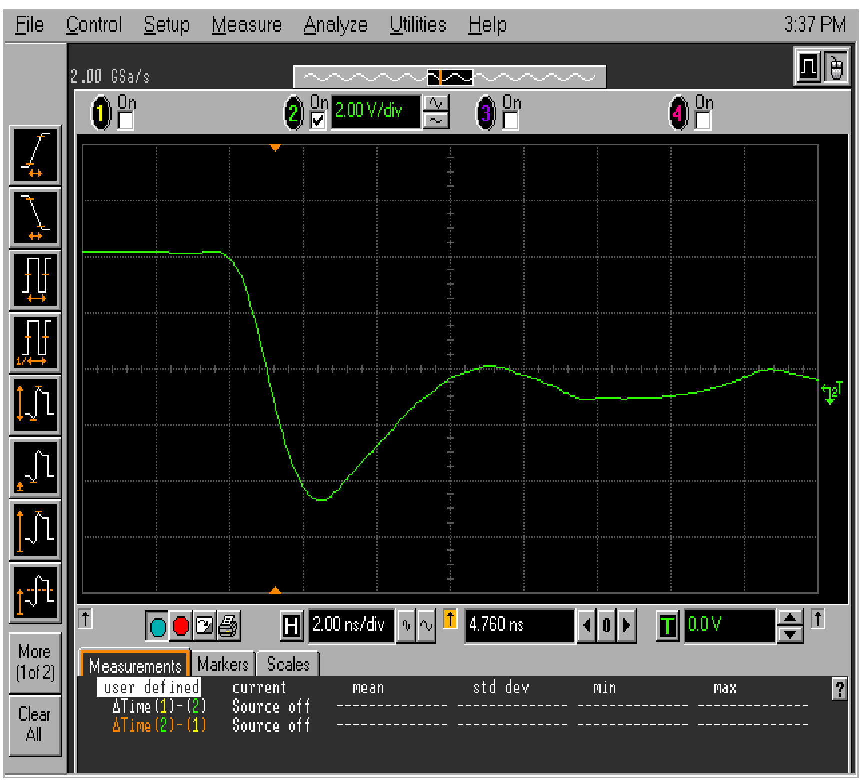


Figure 15(b) DUT 429 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

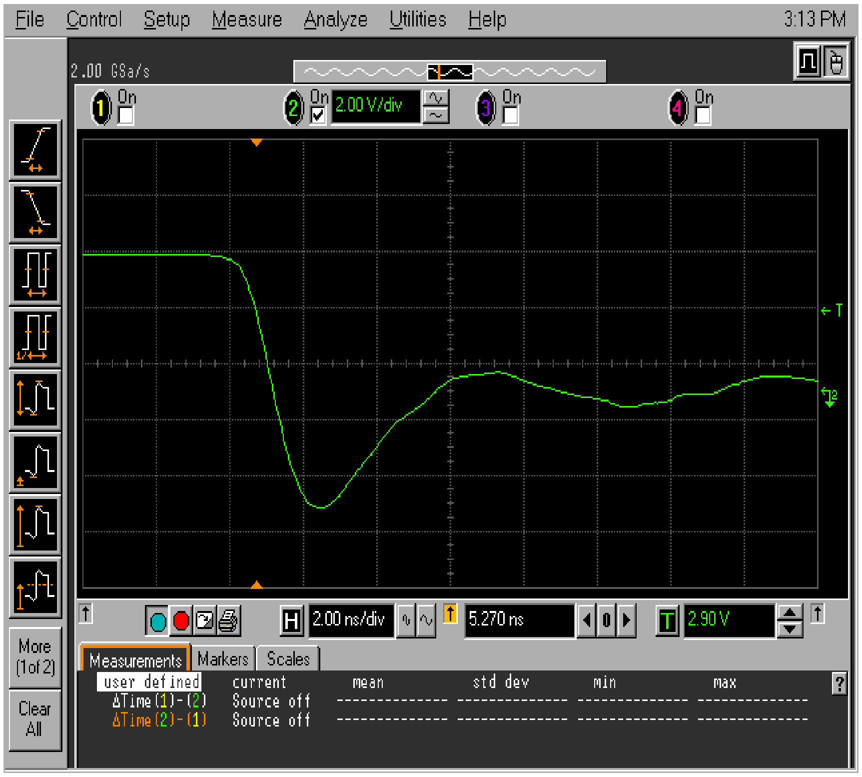


Figure 16(a) DUT 431 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

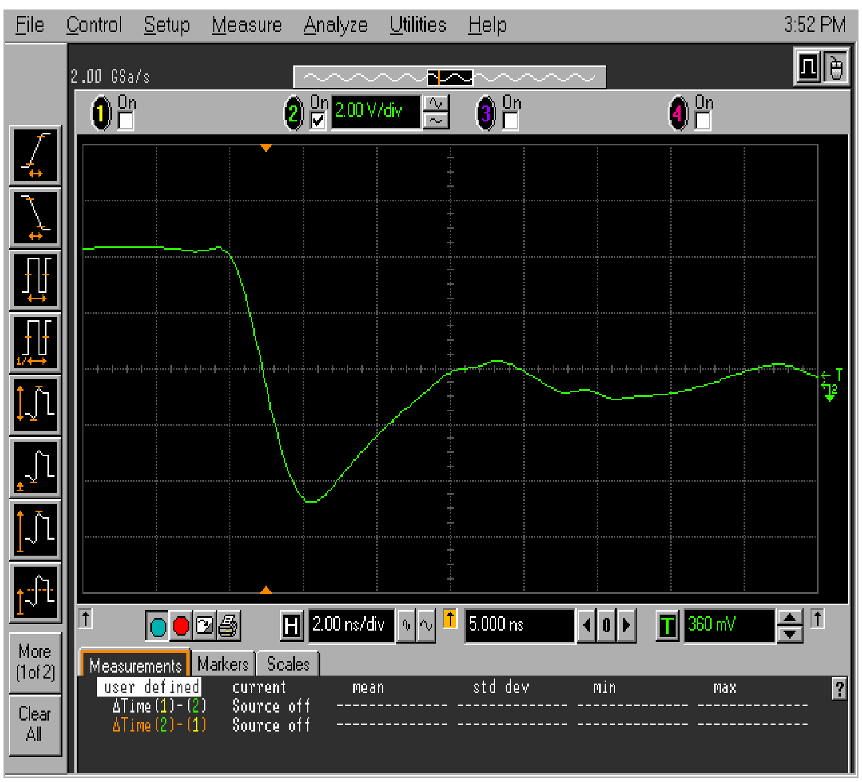


Figure 16(b) DUT 431 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

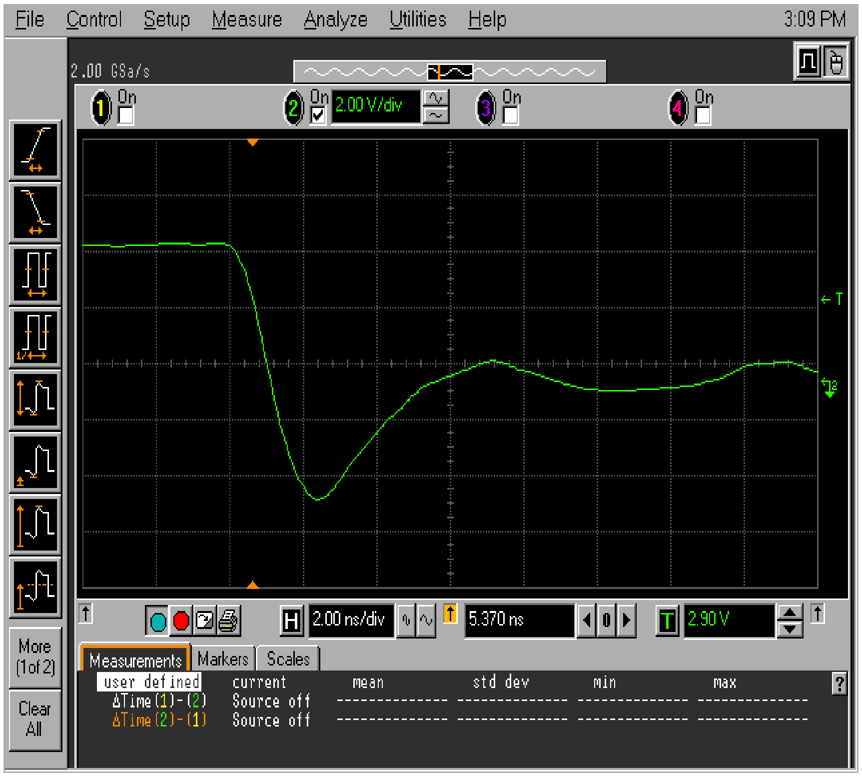


Figure 17(a) DUT 435 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

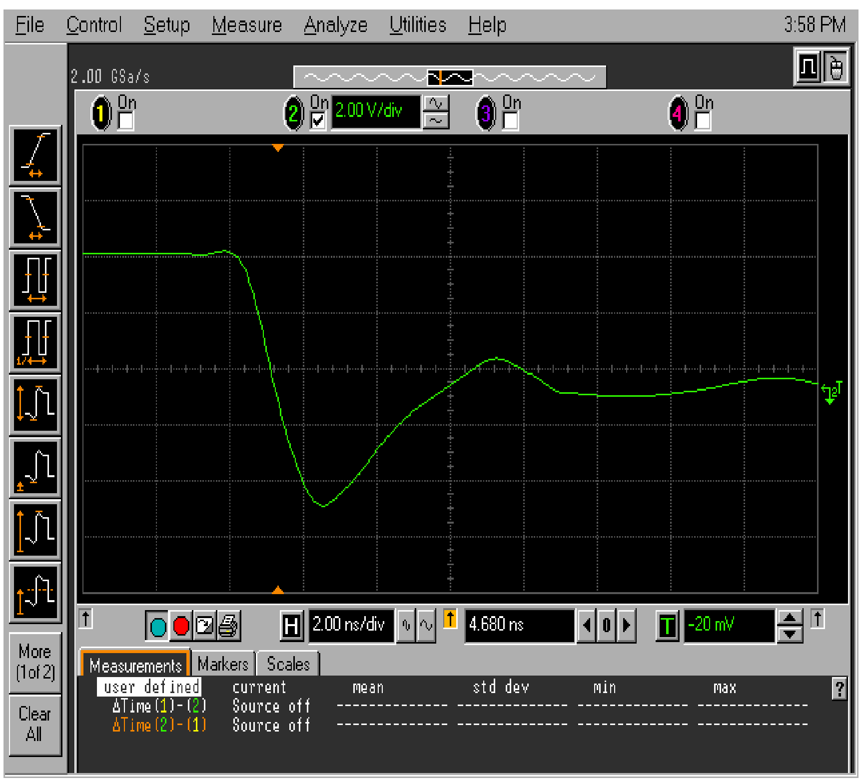


Figure 17(b) DUT 435 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

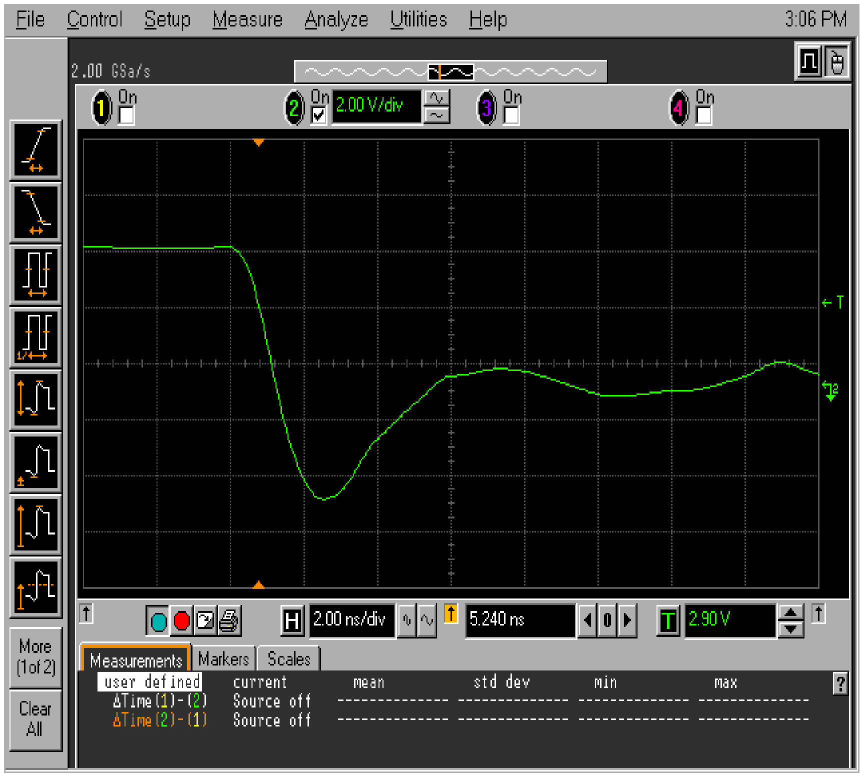


Figure 18(a) DUT 436 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

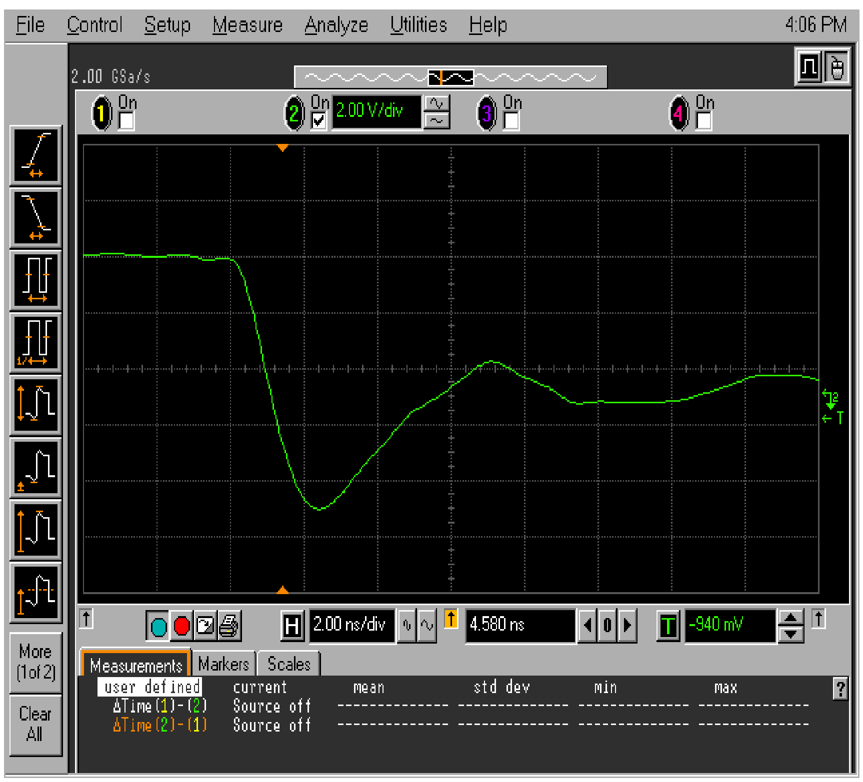


Figure 18(b) DUT 436 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

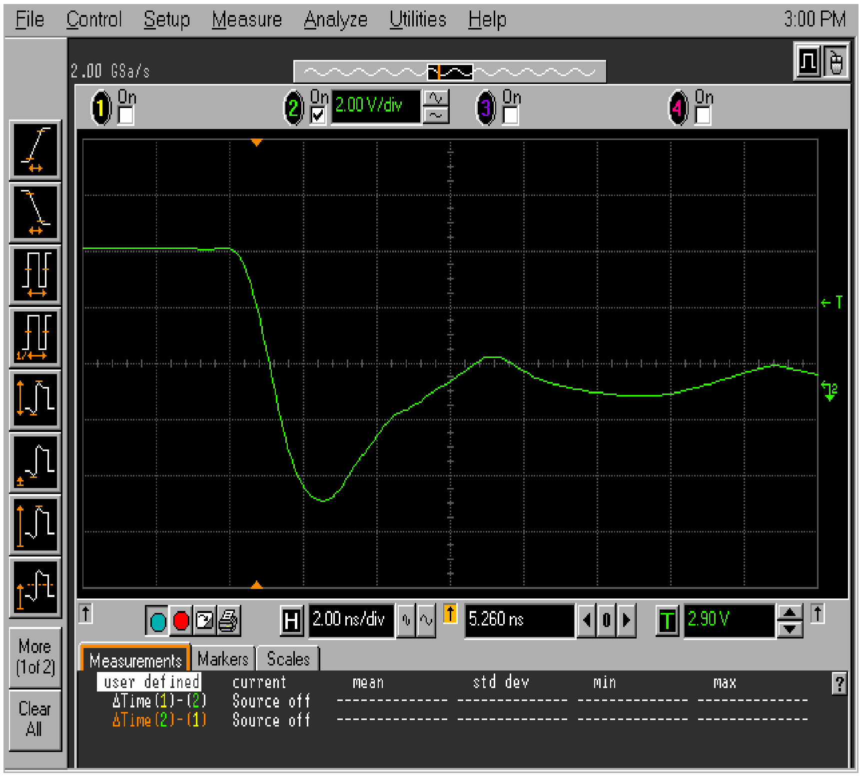


Figure 19(a) DUT 445 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

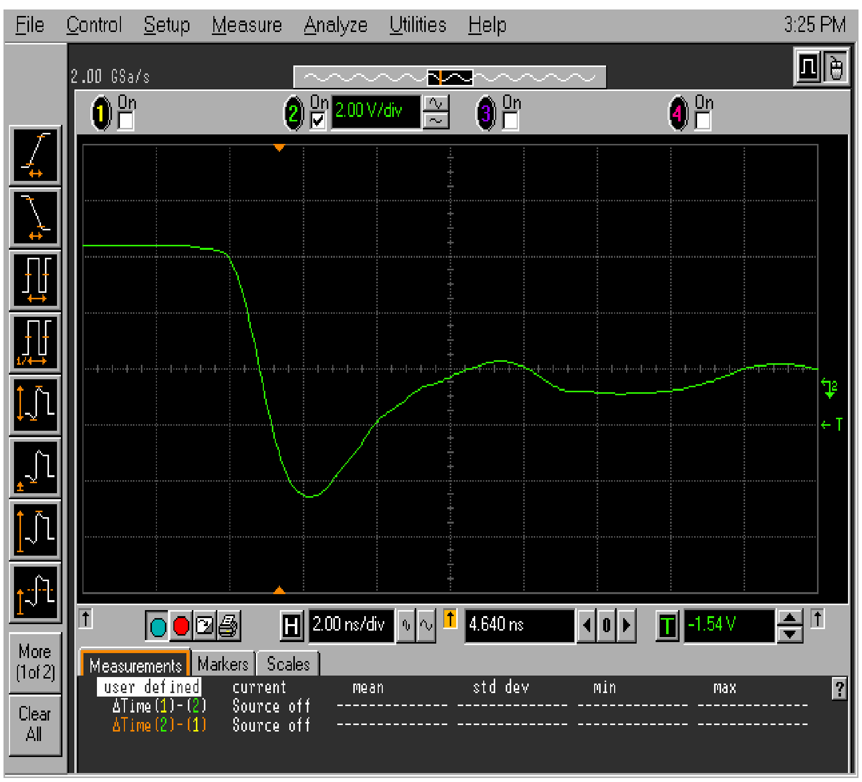
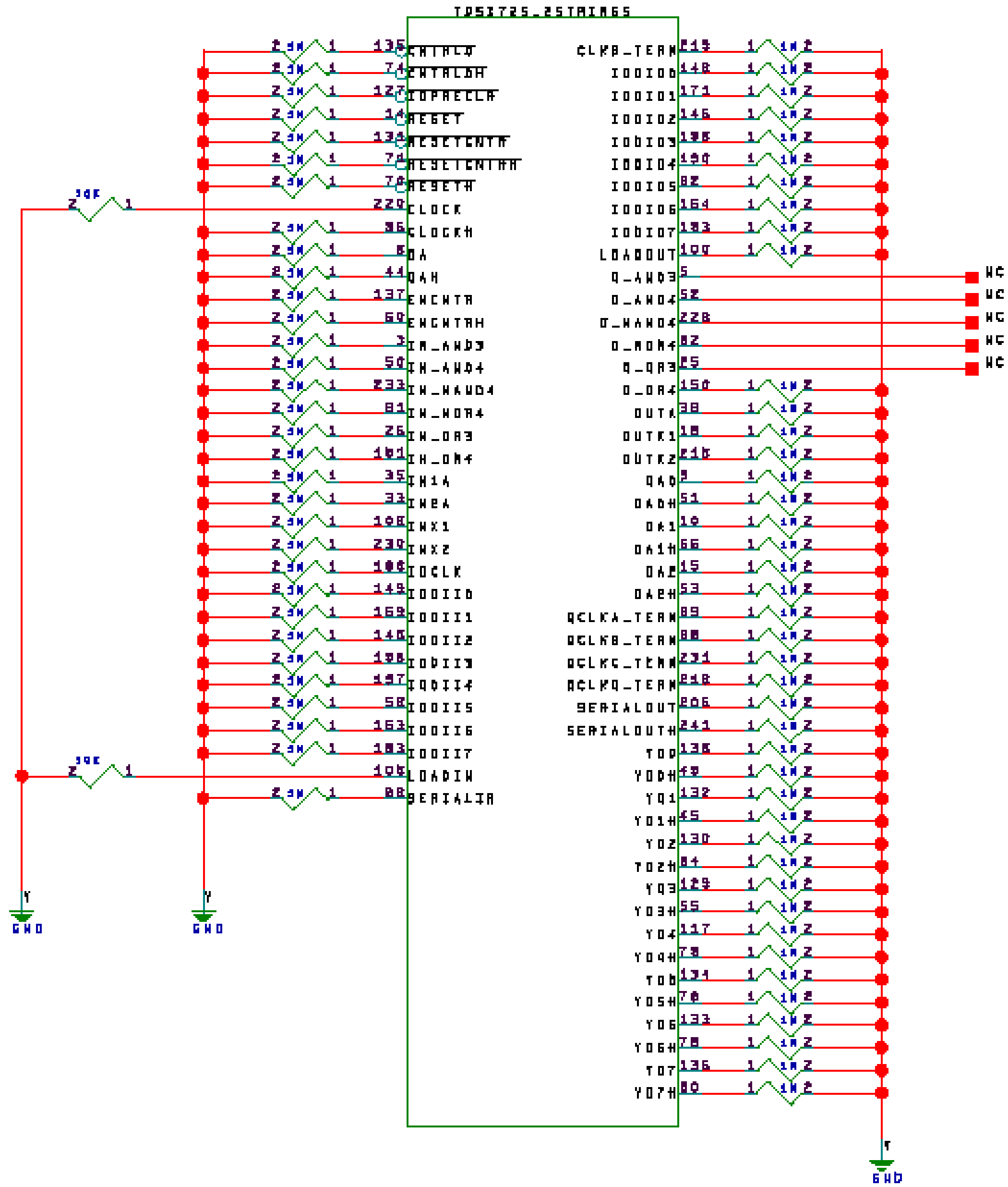
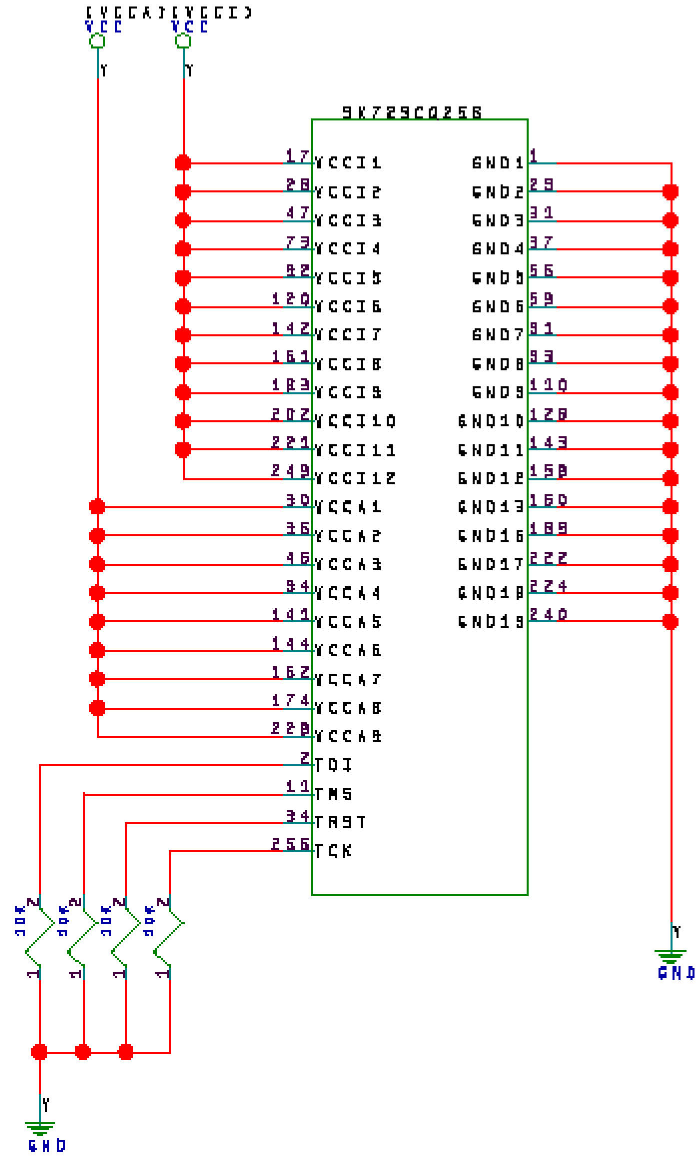


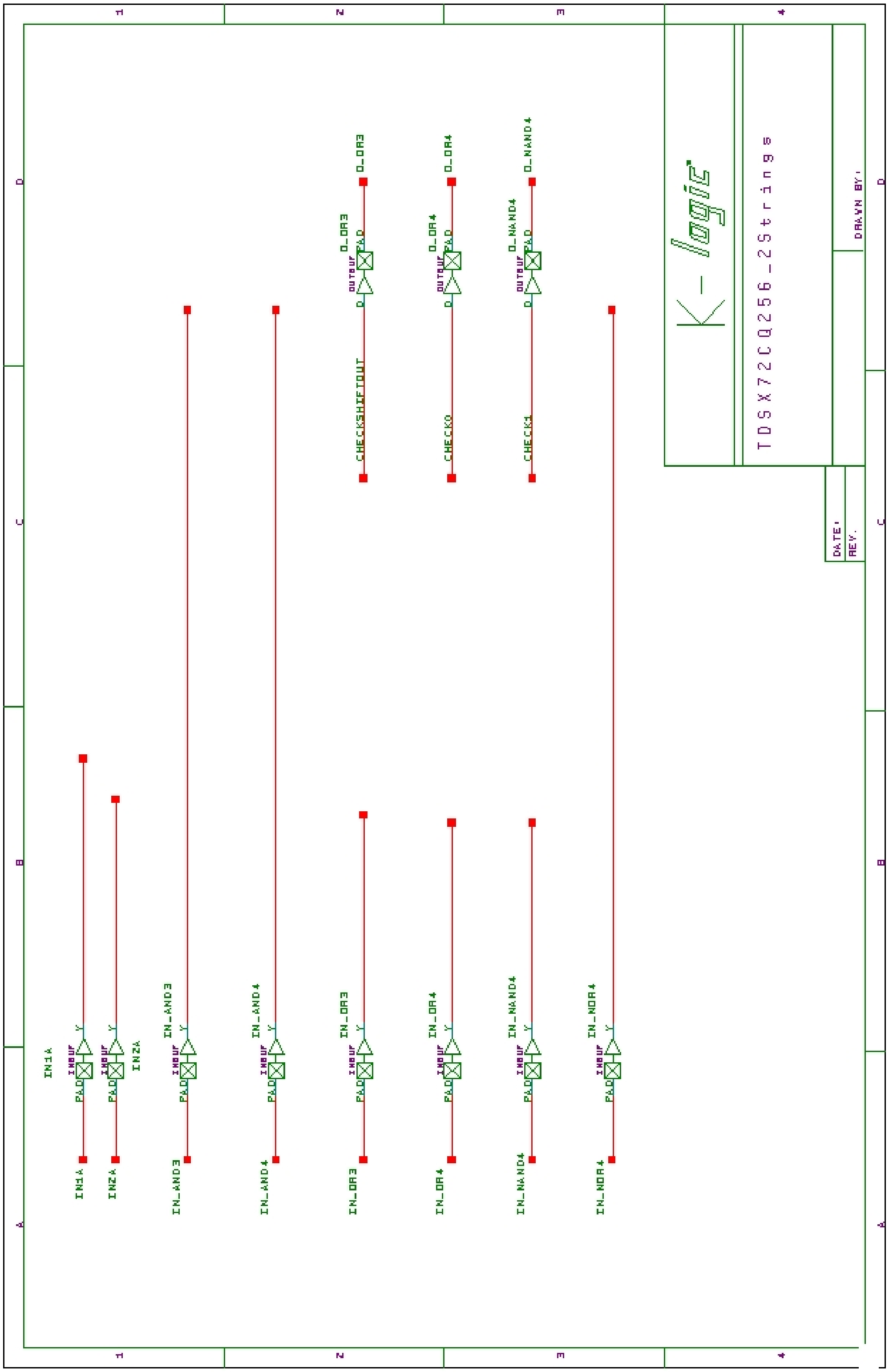
Figure 19(b) DUT 445 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

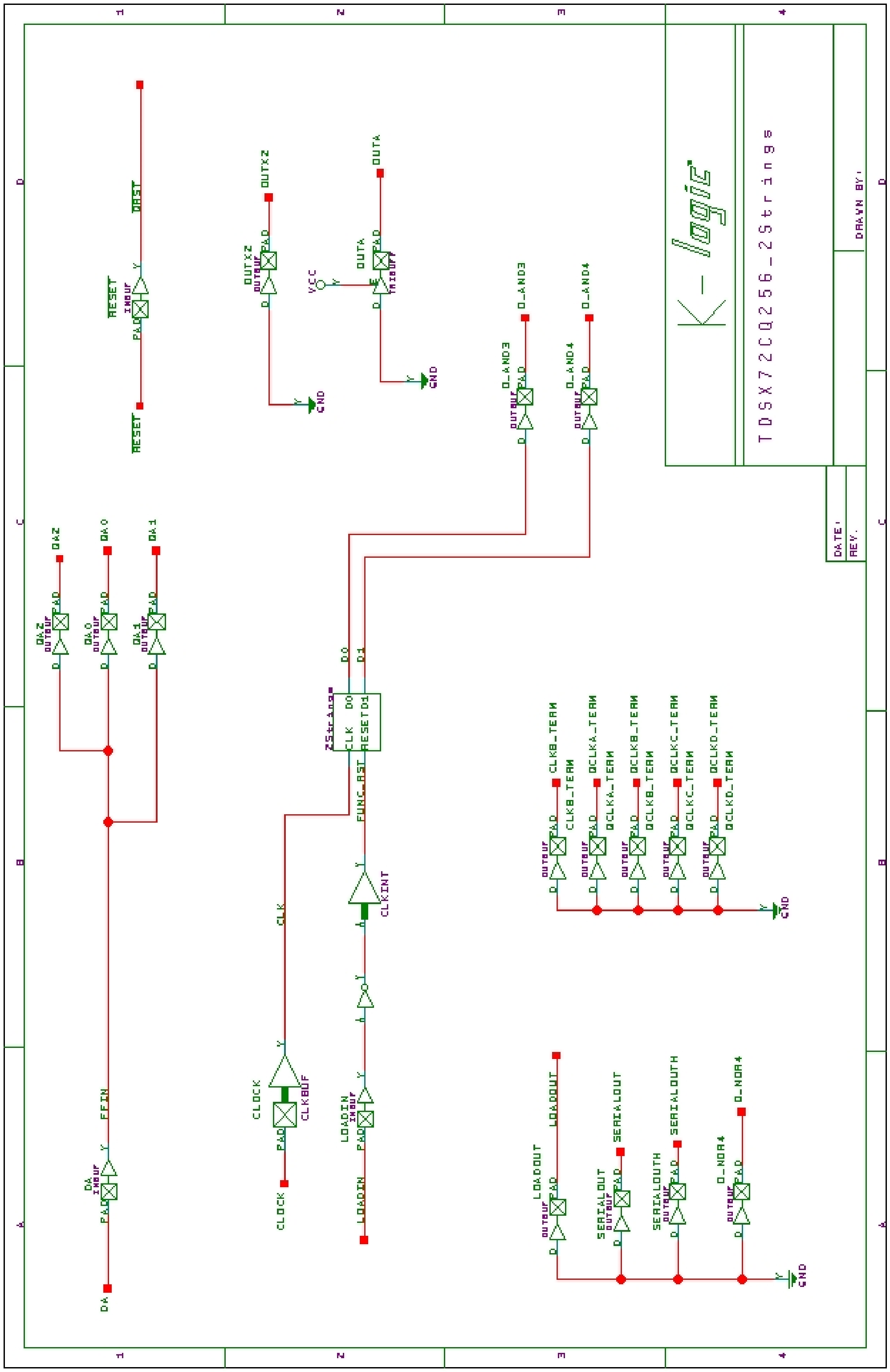
Appendix A DUT Bias

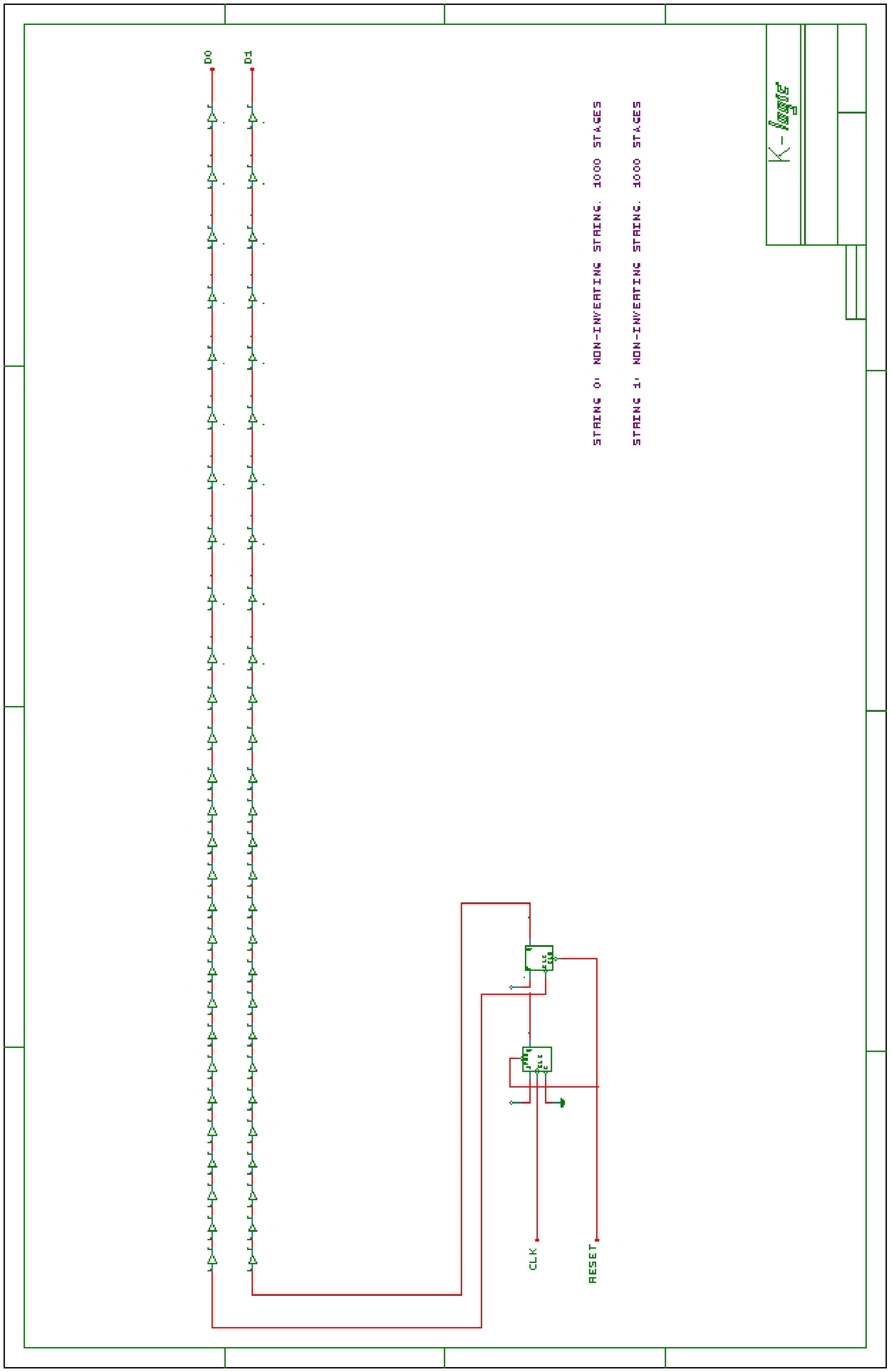


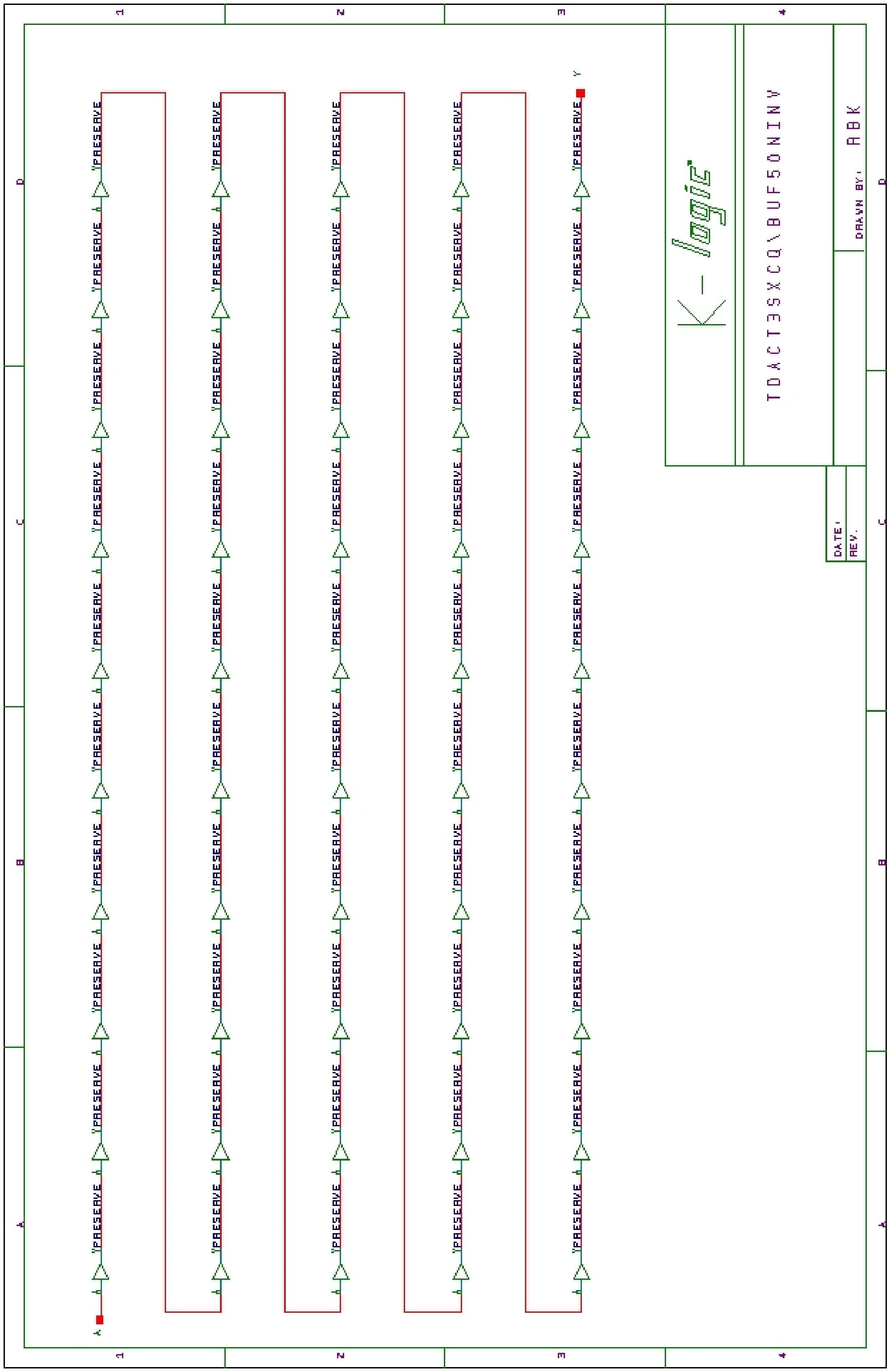

[VCCA][VCCI]
VCC
VCC
9K729CQ256
17 VCCI1
28 VCCI2
47 VCCI3
73 VCCI4
92 VCCI5
120 VCCI6
142 VCCI7
161 VCCI8
183 VCCI9
202 VCCI10
221 VCCI11
249 VCCI12
30 VCCA1
36 VCCA2
46 VCCA3
94 VCCA4
141 VCCA5
144 VCCA6
162 VCCA7
174 VCCA8
228 VCCA9
2 TDI
11 TMS
34 TRST
256 TCK
GND1 1
GND2 29
GND3 31
GND4 37
GND5 56
GND6 59
GND7 91
GND8 93
GND9 110
GND10 128
GND11 143
GND12 158
GND13 160
GND16 189
GND17 222
GND18 224
GND19 240
10K
10K
10K
10K
GND
GND

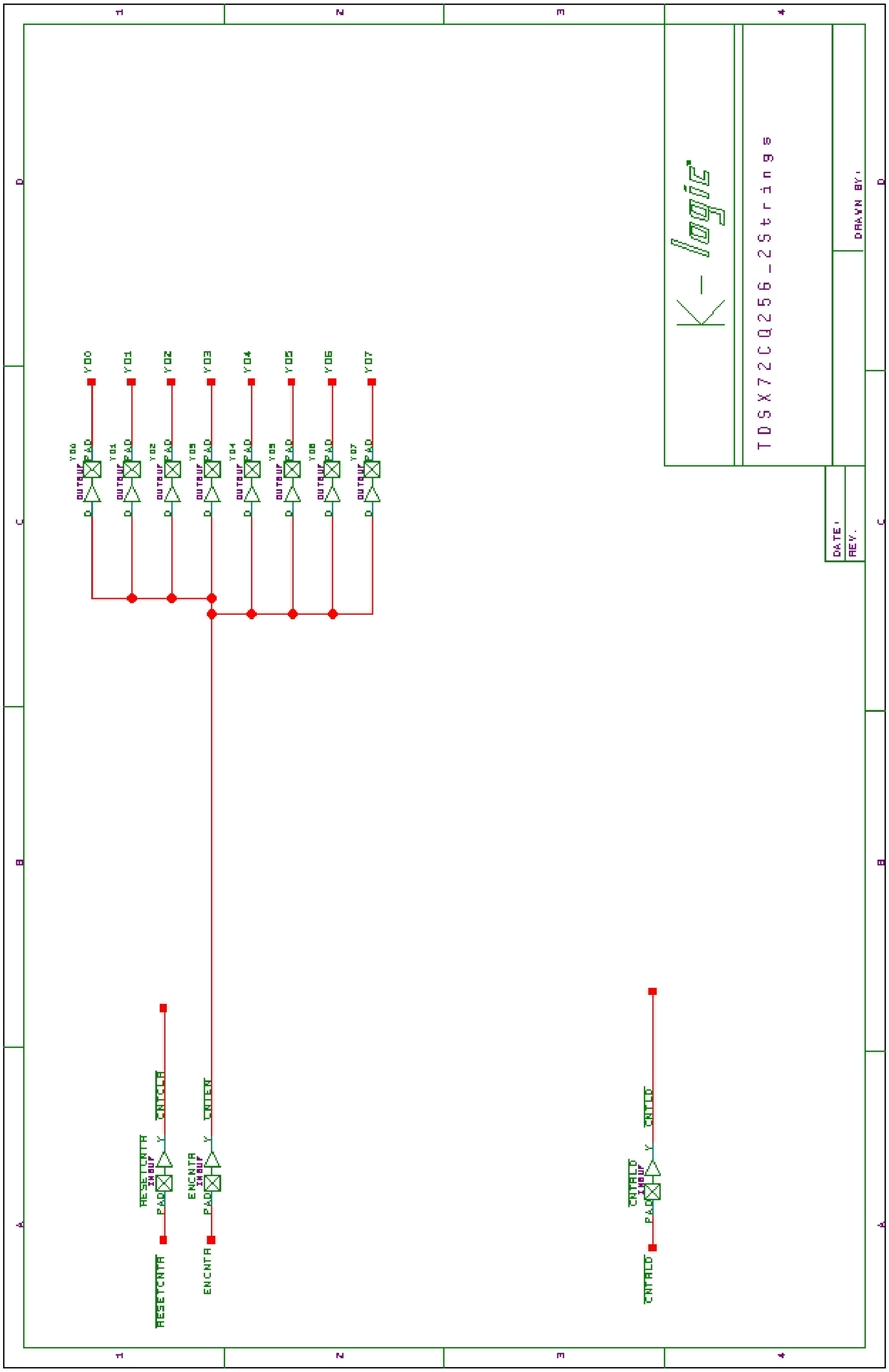
Appendix B DUT Design Schematics

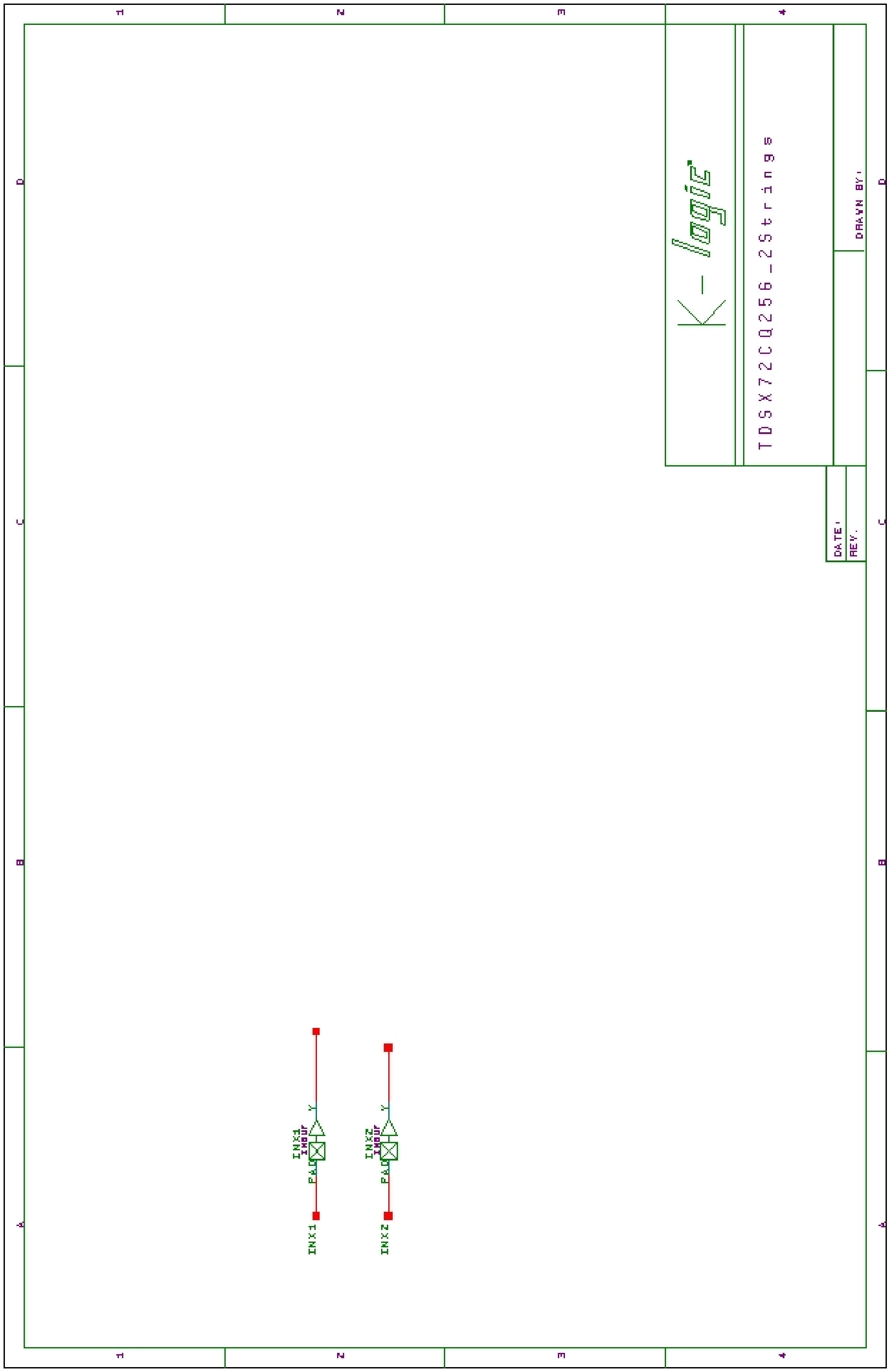


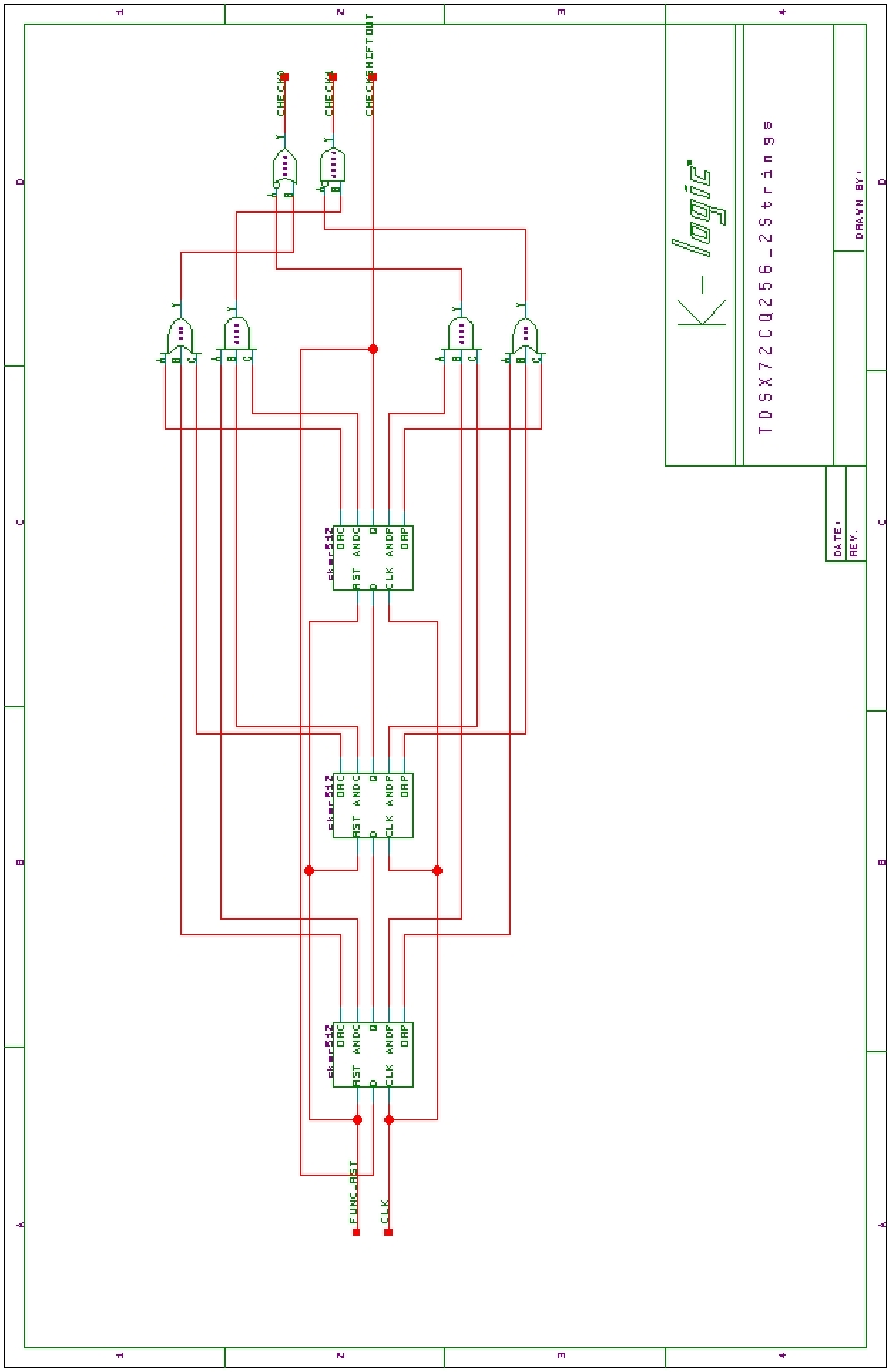

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
QRST
OUTX2
OUTA
VCC
GND
D_AND3
D_AND4
QA2
QA0
QA1
2Strings
CLK
RESET
D0
D1
FUNC_RST
CLK
CLKINT
CLOCK
CLKBUF
LOADIN
DA
FFIN
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

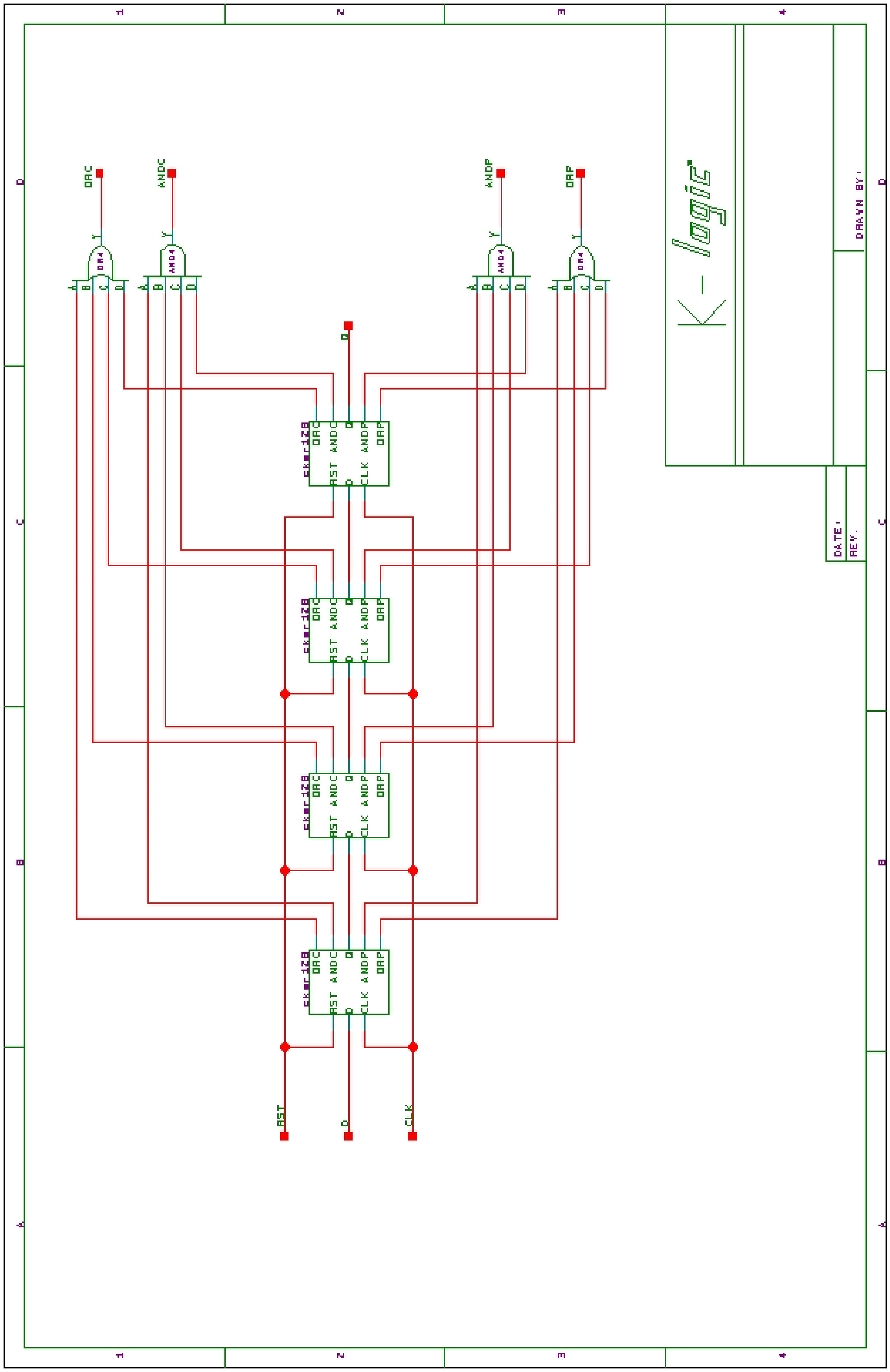

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
CLK
RESET

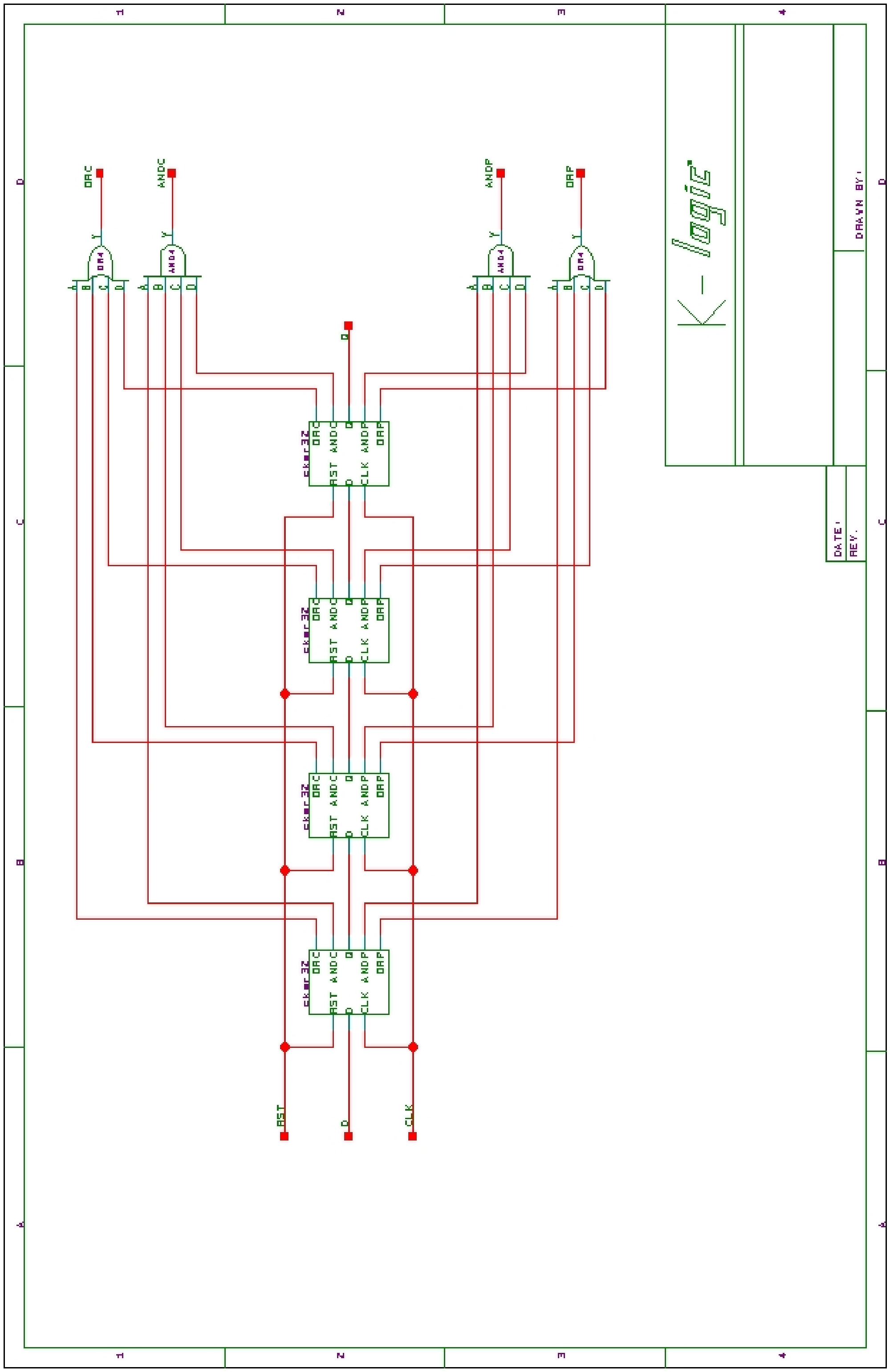

TDACT3SXCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.

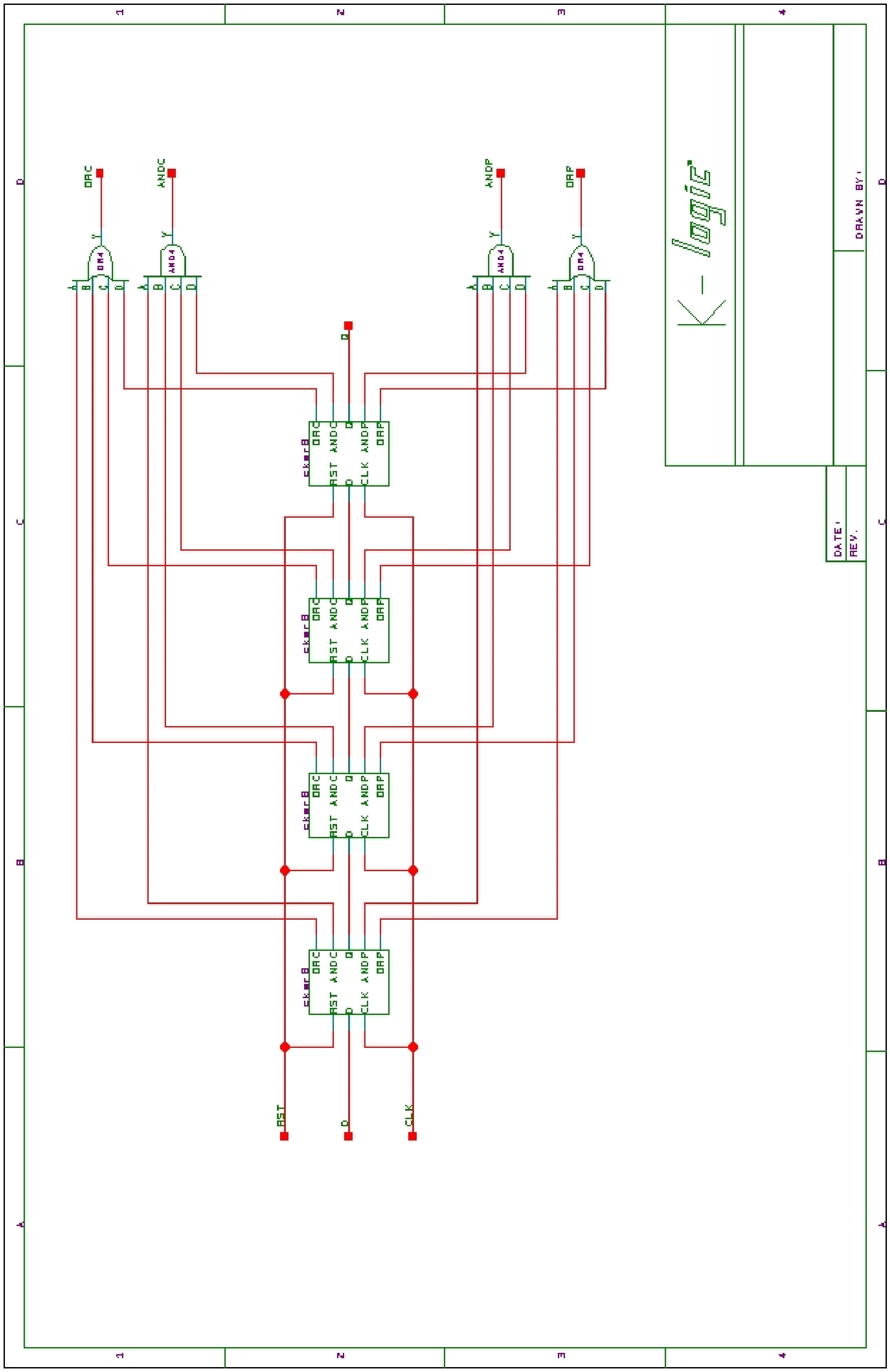

TDSX72CQ256_2Strings
K-logic
DRAWN BY:
DATE:
REV.
YO0
YO1
YO2
YO3
YO4
YO5
YO6
YO7
OUTBUF
PAD
RESETCNTA
ENCNTA
CNTALD
INBUF
CNTCLR
CNTEN
CNTLD

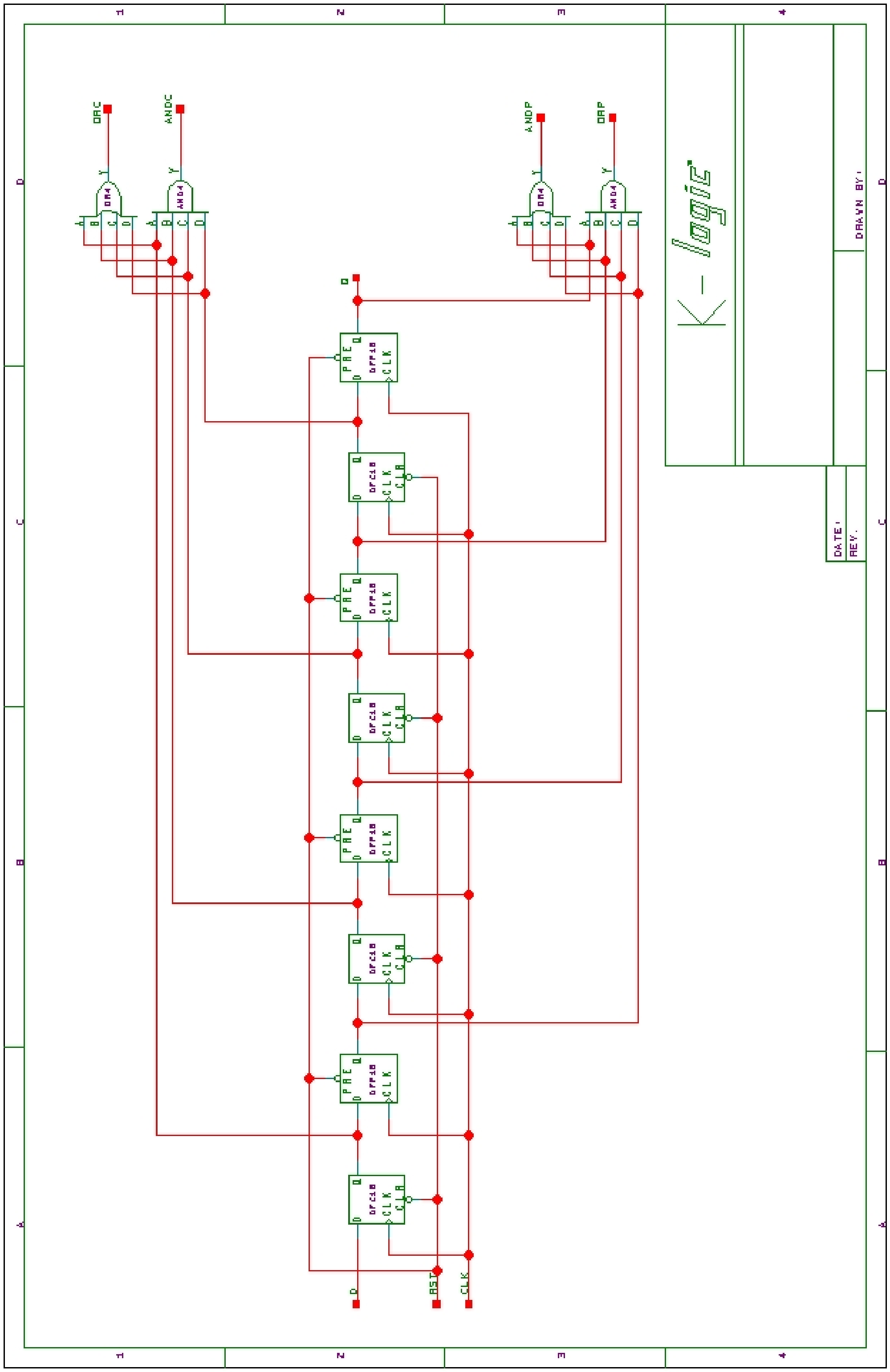

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

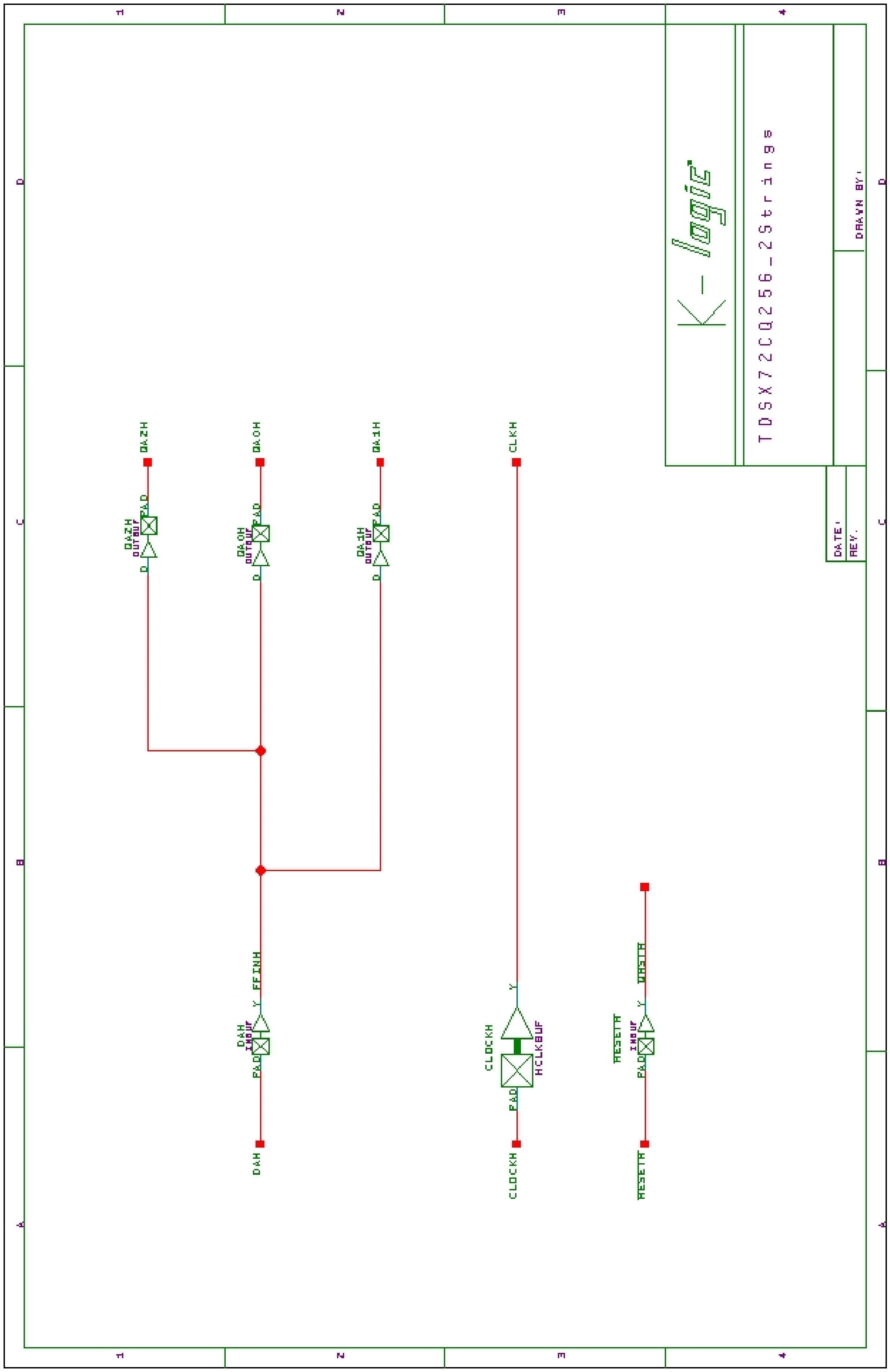

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr128
RST
D
CLK
DRAWN BY:
DATE:
REV:

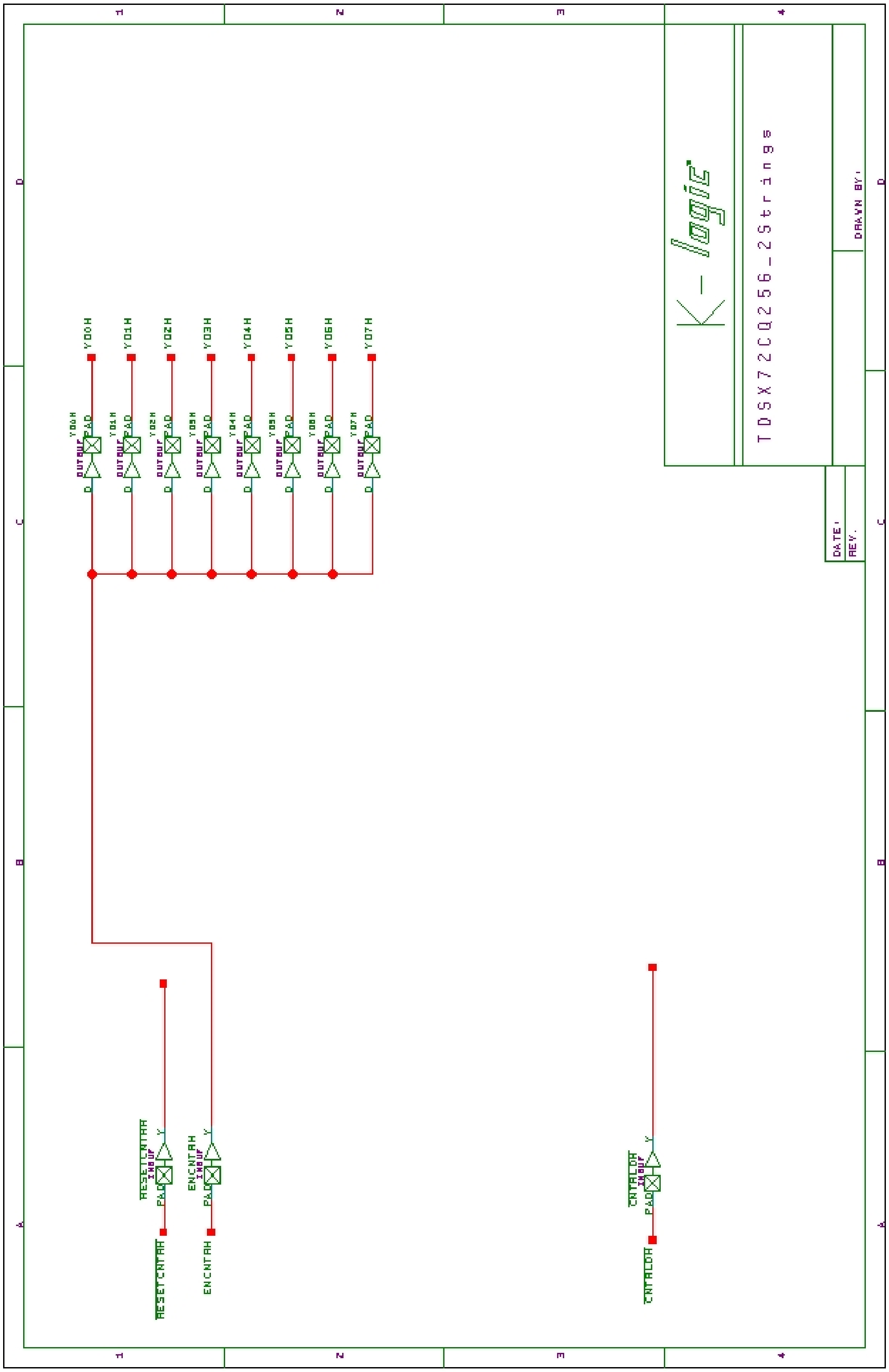

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr32
RST
D
CLK
DATE:
REV.
DRAWN BY:
K-logic


ORC
ANDC
ANDP
ORP
RST
D
CLK
DATE:
REV.
DRAWN BY:

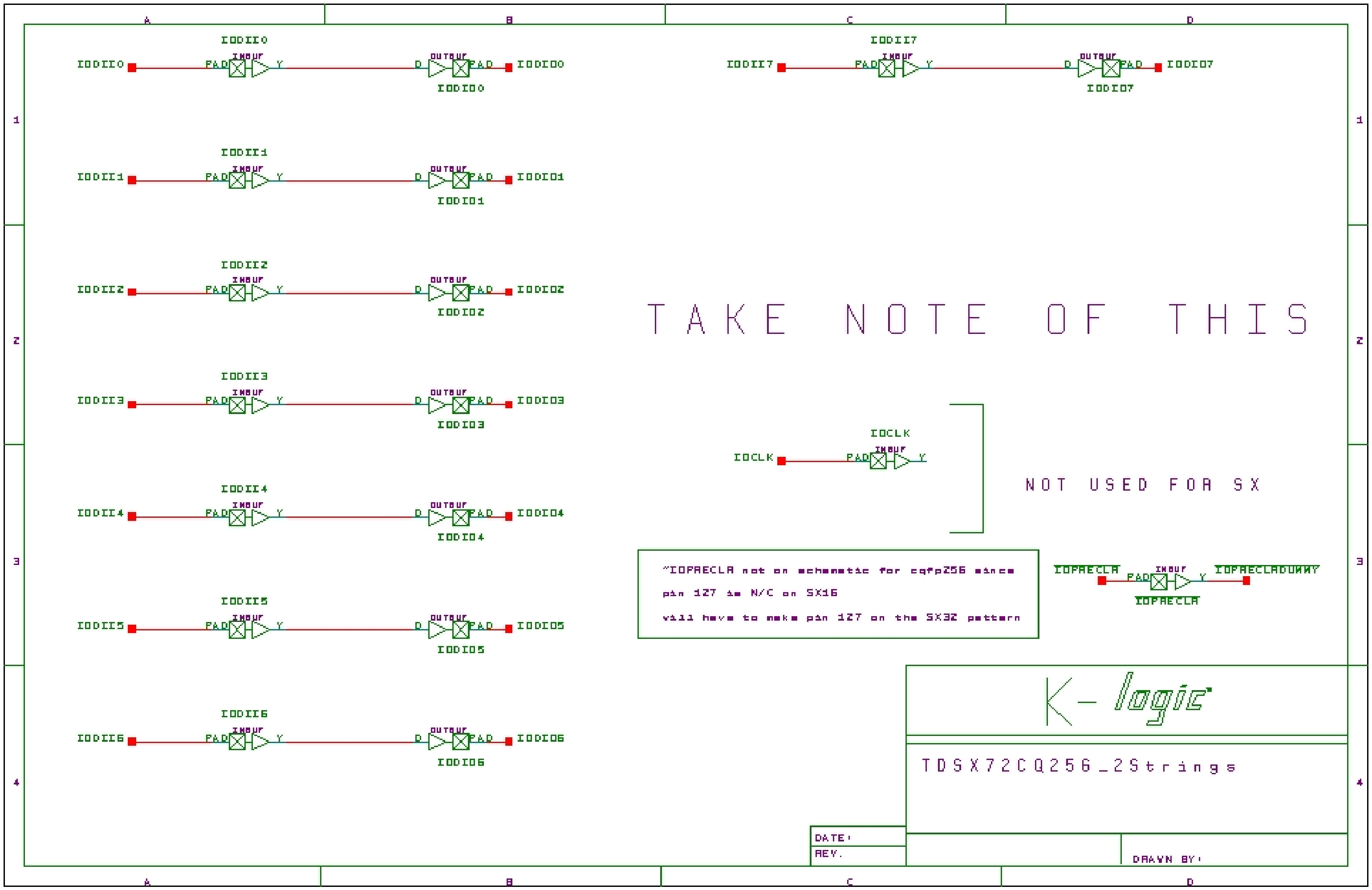

ORC
ANDC
ANDP
ORP
D
RST
CLK
K-logic
DATE:
REV.
DRAWN BY:

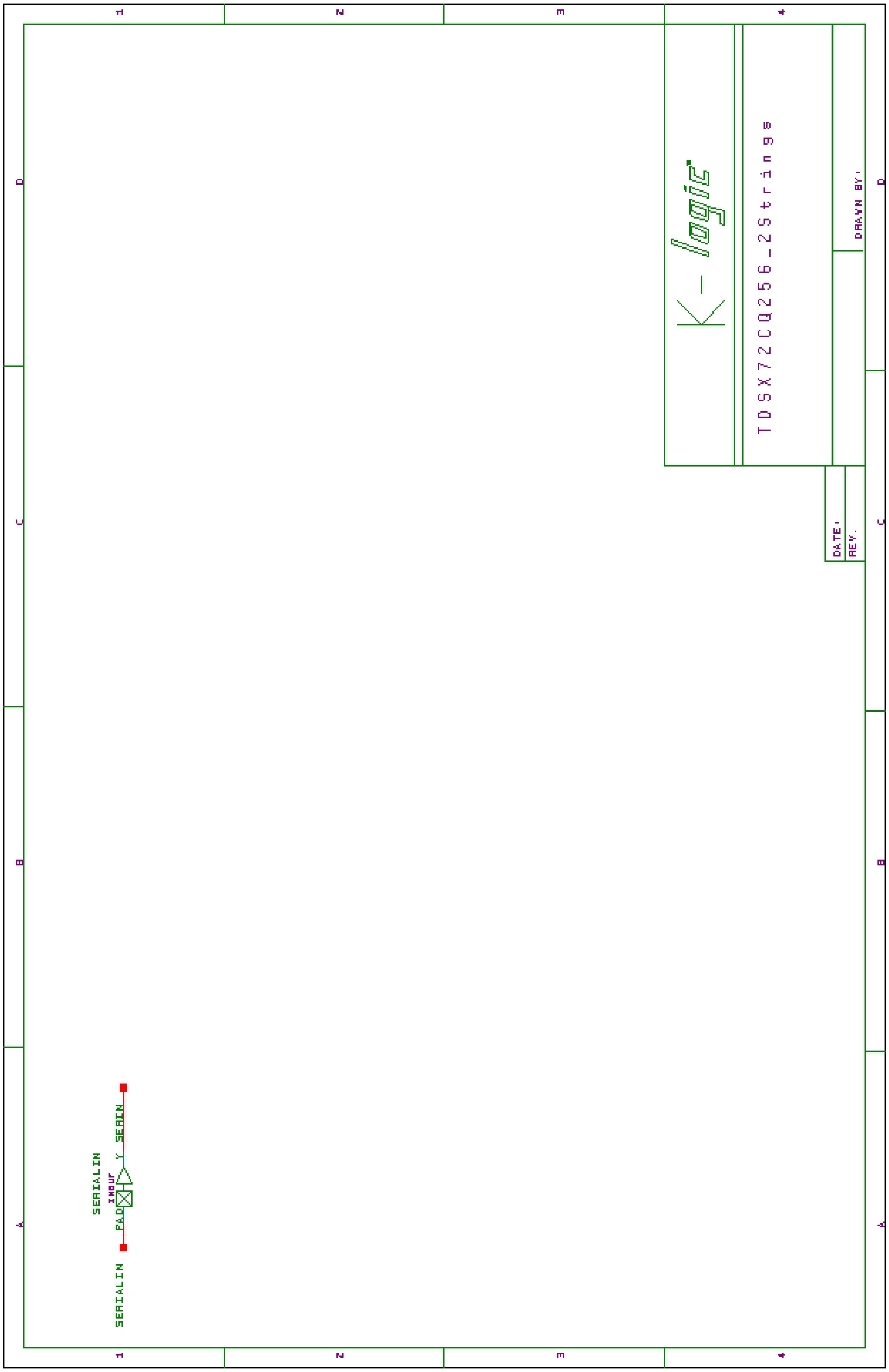


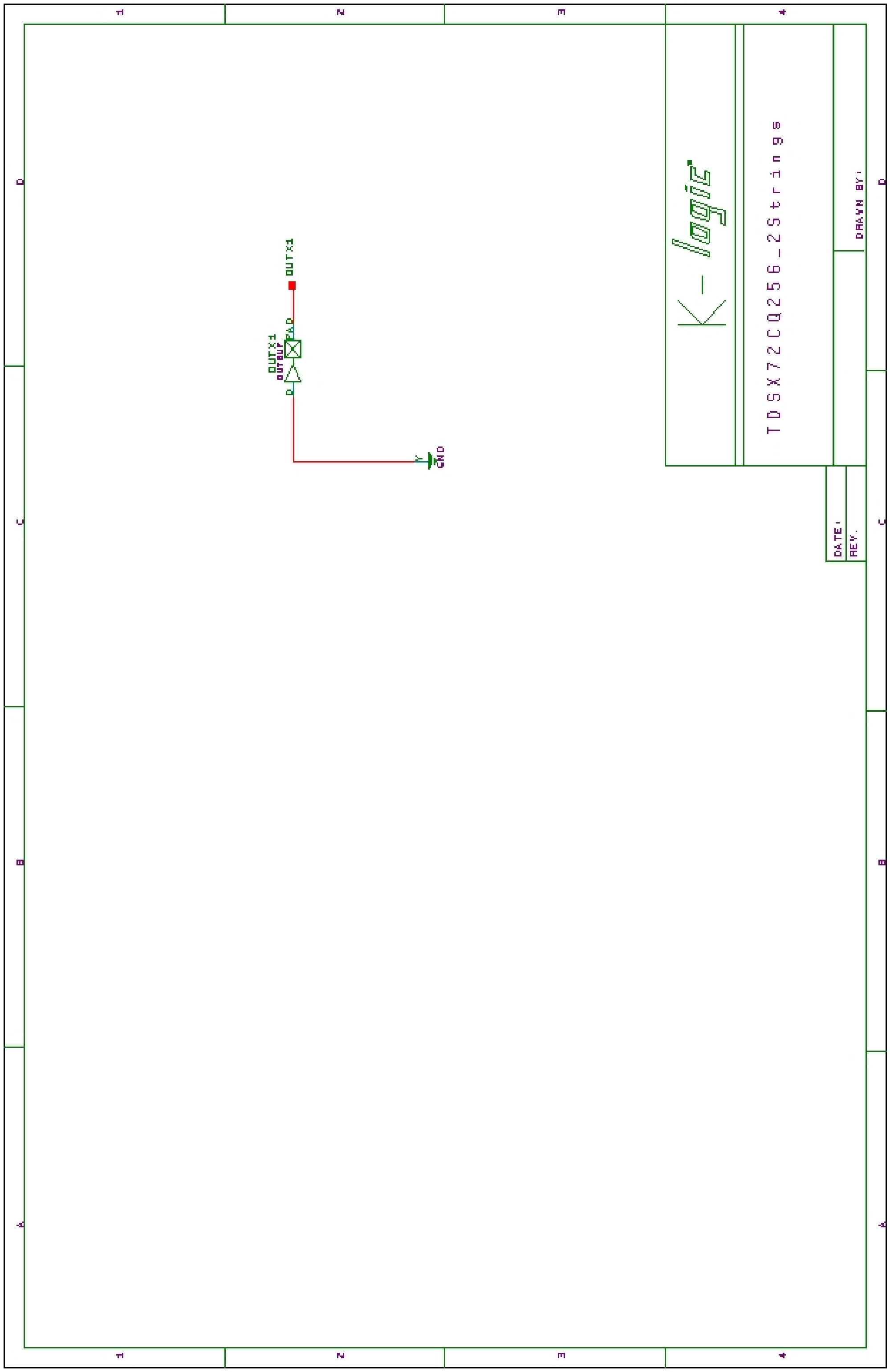
DA2H
DA0H
DA1H
CLKH
OUTBUF
PAD
D
DAH
INBUF
Y
FFINH
CLOCKH
HCLKBUF
RESETH
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.



TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
INBUF
RESETCNTAH
ENCNTAH
CNTALDH


TAKE NOTE OF THIS
NOT USED FOR SX
IOCLK
INBUF
PAD
Y
D
OUTBUF
IODII0
IODIO0
IODII1
IODIO1
IODII2
IODIO2
IODII3
IODIO3
IODII4
IODIO4
IODII5
IODIO5
IODII6
IODIO6
IODII7
IODIO7
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
K-logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


SERIALIN
SERIALIN
PAD
INBUF
Y
SERIN
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
OUTBUF
PAD
GND