TOTAL IONIZING DOSE TEST REPORT

No. 10T-RTSX72SU-CQ256-D1SG01
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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 60 krad (Si) per 25-mA spec after 10-day room temperature annealing.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10%-degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1SG01
Quantity Tested	5
Serial Number	60 krad: 8352, 8420 100 krad: 8292, 8318, 8321
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	7.5 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

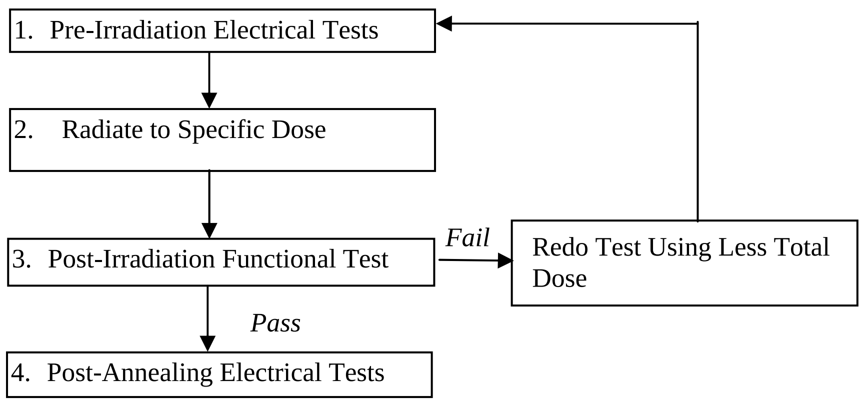


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in Actel products manufactured by sub-micron CMOS technology. To prove this point, test data with a high dose rate (1 krad (Si)/min) are compared to test data with a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. The results always show the low-dose-rate degradation less than the high-dose-rate degradation; thus indicating that the elevated rebound annealing would artificially reduce the radiation effects. Therefore, only room temperature annealing is performed in this report. Every DUT is annealed for approximately 10 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design, TDSX72CQ256_2Strings_r1, to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each tested electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and on the output pins (O_OR4 and O_NAND4) of a shift register with 1536 flip-flops. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{IL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on combinational nets listed in Row 3 and 4 of Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is measured as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Table 3 shows the pre-irradiation, post-irradiation, and post-annealing I_{CCA} and I_{CCI}. It indicates that the post-annealing I_{CC} (I_{CCA} + I_{CCI}) for 60 krad(SiO_2)-irradiated DUTs, DUT 8352 and 8420, pass the spec of 25 mA.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-rad	Post-rad	Post-ann	Pre-rad	Post-rad	Post-ann
8292	100 krad	1.6	220	161	5.7	180	61
8318	100 krad	1.6	270	168	5.7	210	66
8321	100 krad	1.6	320	171	5.7	240	75
8352	60 krad	1.6	30	11	5.7	30	12
8420	60 krad	1.6	20	10	5.7	28	11

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic thresholds. All data are within the spec limits; for each measurement, the post-annealing value is within ±10% of pre-irradiated value.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA/QA0				DAH/QA0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.58	1.64	1.30	1.29	1.46	1.55	1.37	1.50
8318	100 krad	1.57	1.63	1.32	1.38	1.48	1.57	1.36	1.45
8321	100 krad	1.55	1.54	1.29	1.34	1.47	1.55	1.37	1.30
8352	60 krad	1.56	1.60	1.30	1.27	1.48	1.55	1.37	1.31
8420	60 krad	1.56	1.55	1.33	1.30	1.46	1.53	1.36	1.31

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTRH/YO0H				IDII0/IDIO0			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.45	1.50	1.35	1.38	1.54	1.63	1.33	1.25
8318	100 krad	1.46	1.53	1.35	1.42	1.56	1.63	1.30	1.40
8321	100 krad	1.46	1.55	1.36	1.29	1.59	1.60	1.27	1.26
8352	60 krad	1.46	1.58	1.36	1.30	1.58	1.59	1.27	1.32
8420	60 krad	1.46	1.53	1.34	1.31	1.60	1.62	1.28	1.25

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII1/IDIO1			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.48	1.58	1.32	1.35
8318	100 krad	1.49	1.56	1.30	1.39
8321	100 krad	1.48	1.55	1.24	1.27
8352	60 krad	1.47	1.56	1.28	1.26
8420	60 krad	1.49	1.57	1.27	1.25

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2/IDIO2				IDII3/IDIO3			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.58	1.56	1.30	1.33	1.57	1.57	1.25	1.28
8318	100 krad	1.55	1.58	1.31	1.41	1.56	1.57	1.29	1.30
8321	100 krad	1.60	1.56	1.27	1.28	1.60	1.58	1.27	1.28
8352	60 krad	1.61	1.56	1.25	1.27	1.60	1.57	1.25	1.27
8420	60 krad	1.60	1.57	1.27	1.27	1.58	1.55	1.25	1.26

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4/IDIO4				IDII5/IDIO5			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.44	1.47	1.29	1.36	1.45	1.50	1.35	1.34
8318	100 krad	1.47	1.50	1.30	1.30	1.45	1.51	1.35	1.33
8321	100 krad	1.48	1.50	1.30	1.31	1.45	1.44	1.35	1.32
8352	60 krad	1.45	1.49	1.30	1.31	1.46	1.48	1.37	1.33
8420	60 krad	1.49	1.49	1.30	1.30	1.45	1.50	1.35	1.30

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6/IDIO6				IDII7/IDIO7			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
8292	100 krad	1.55	1.58	1.30	1.31	1.45	1.50	1.33	1.38
8318	100 krad	1.47	1.60	1.31	1.35	1.45	1.40	1.26	1.40
8321	100 krad	1.48	1.56	1.26	1.27	1.46	1.45	1.32	1.41
8352	60 krad	1.53	1.55	1.26	1.28	1.45	1.46	1.35	1.35
8420	60 krad	1.55	1.55	1.25	1.26	1.44	1.44	1.35	1.36

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies insignificantly.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
8292	100 krad	0.0108	0.0201	0.105	0.107	0.176	0.183	0.440	0.470	0.960	0.978
8318	100 krad	0.0107	0.0115	0.106	0.108	0.190	0.240	0.466	0.550	1.100	1.222
8321	100 krad	0.0107	0.0121	0.106	0.108	0.176	0.190	0.447	0.469	0.920	0.930
8352	60 krad	0.0107	0.0111	0.107	0.135	0.178	0.179	0.444	0.445	0.915	0.915
8420	60 krad	0.0107	0.0122	0.106	0.106	0.177	0.178	0.445	0.446	0.914	0.917

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
8292	100 krad	4.988	4.986	4.865	4.864	4.649	4.640	4.063	4.038	2.722	2.678
8318	100 krad	4.988	4.984	4.865	4.863	4.647	4.644	4.061	4.025	2.739	2.721
8321	100 krad	4.988	4.986	4.865	4.863	4.648	4.643	4.062	4.045	2.699	2.601
8352	60 krad	4.988	4.988	4.866	4.864	4.647	4.644	4.056	4.058	2.743	2.753
8420	60 krad	4.988	4.989	4.865	4.864	4.649	4.648	4.059	4.058	2.715	2.722

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. All DUTs pass the 10%-degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (µs)	Post-Annealing (µs)	Degradation (%)
8292	100 krad	1.2903	1.3109	1.22%
8318	100 krad	1.2855	1.3275	3.27%
8321	100 krad	1.3076	1.3500	3.29%
8352	60 krad	1.2745	1.2638	-0.84%
8420	60 krad	1.3210	1.3000	-1.59%

F. Transition Time

Figures 2 to 11 show pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

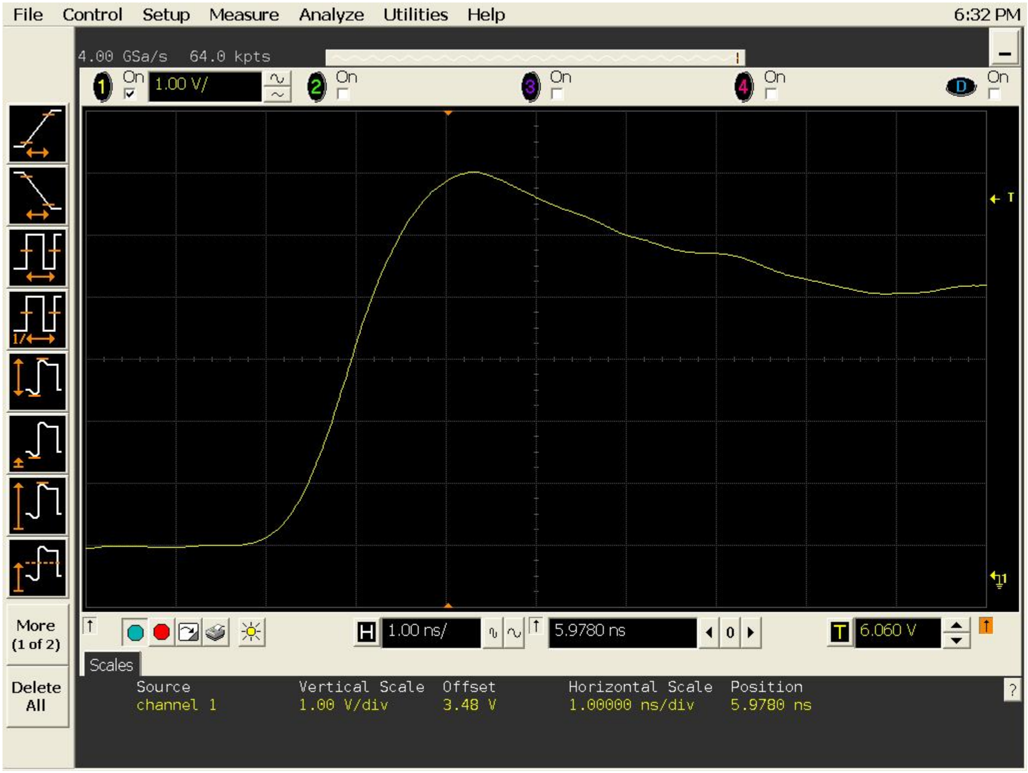


Figure 2(a) DUT 8292 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

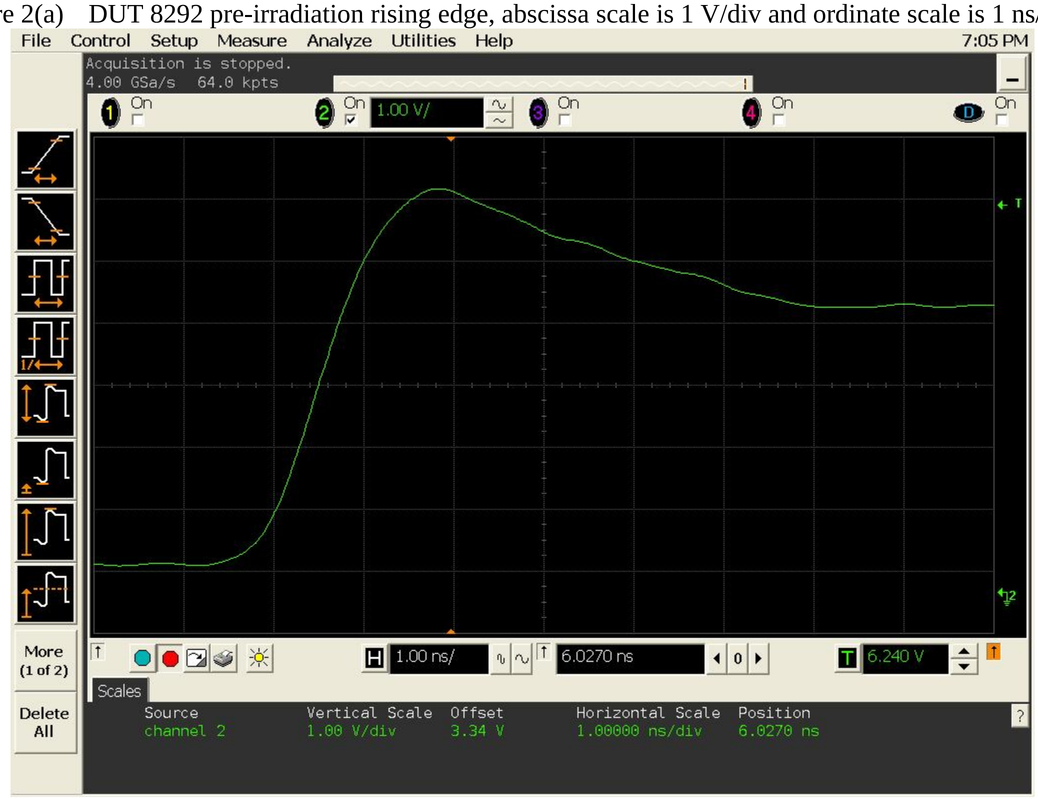


Figure 2(b) DUT 8292 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

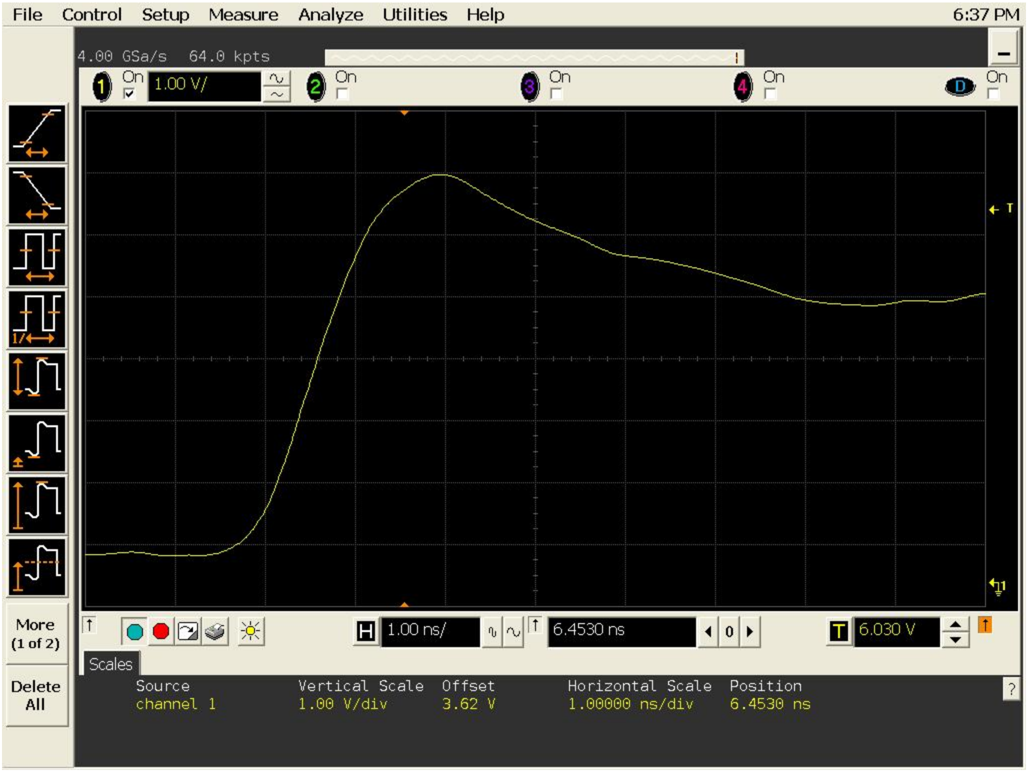


Figure 3(a) DUT 8318 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

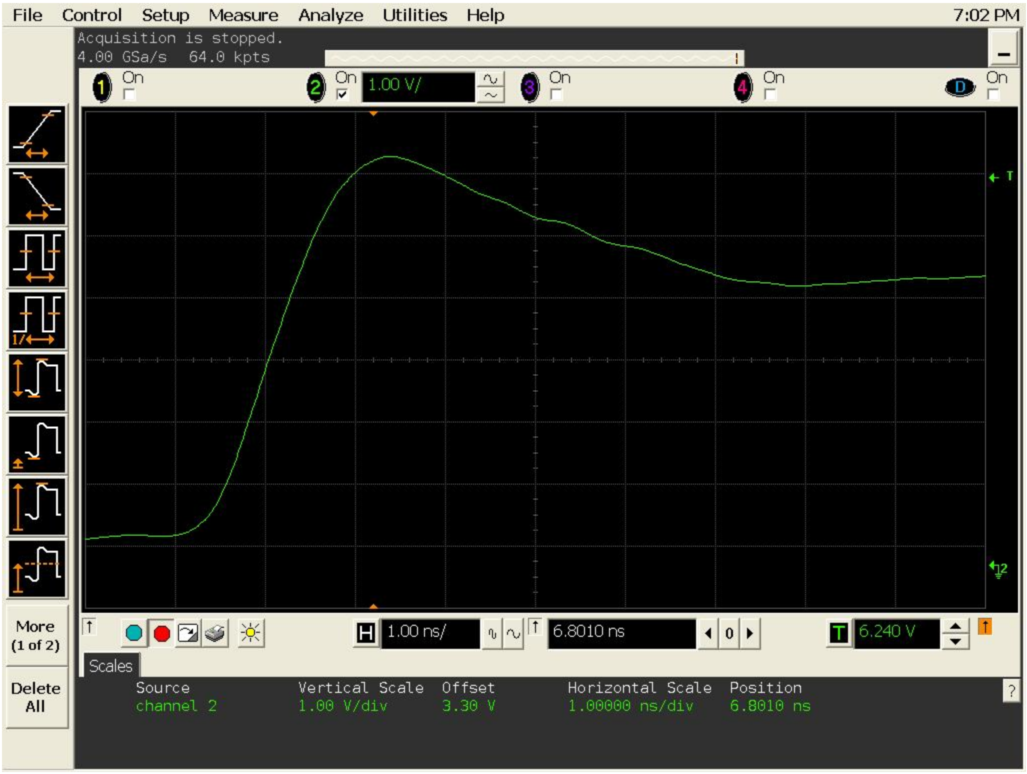


Figure 3(b) DUT 8318 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

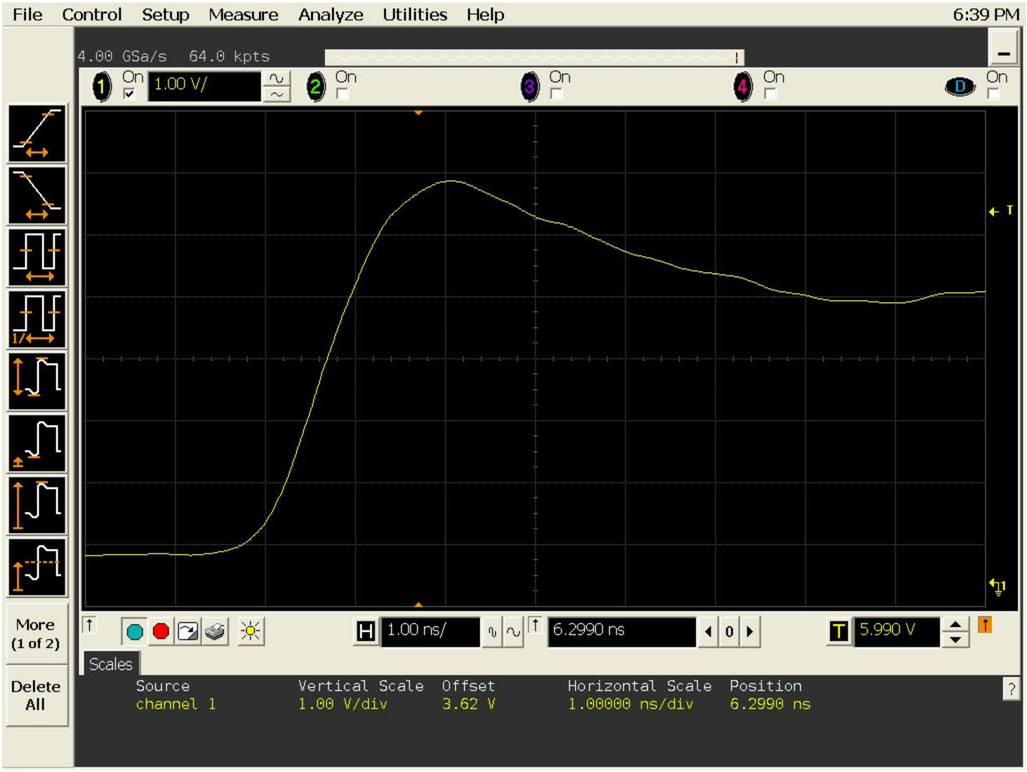


Figure 4(a) DUT 8321 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

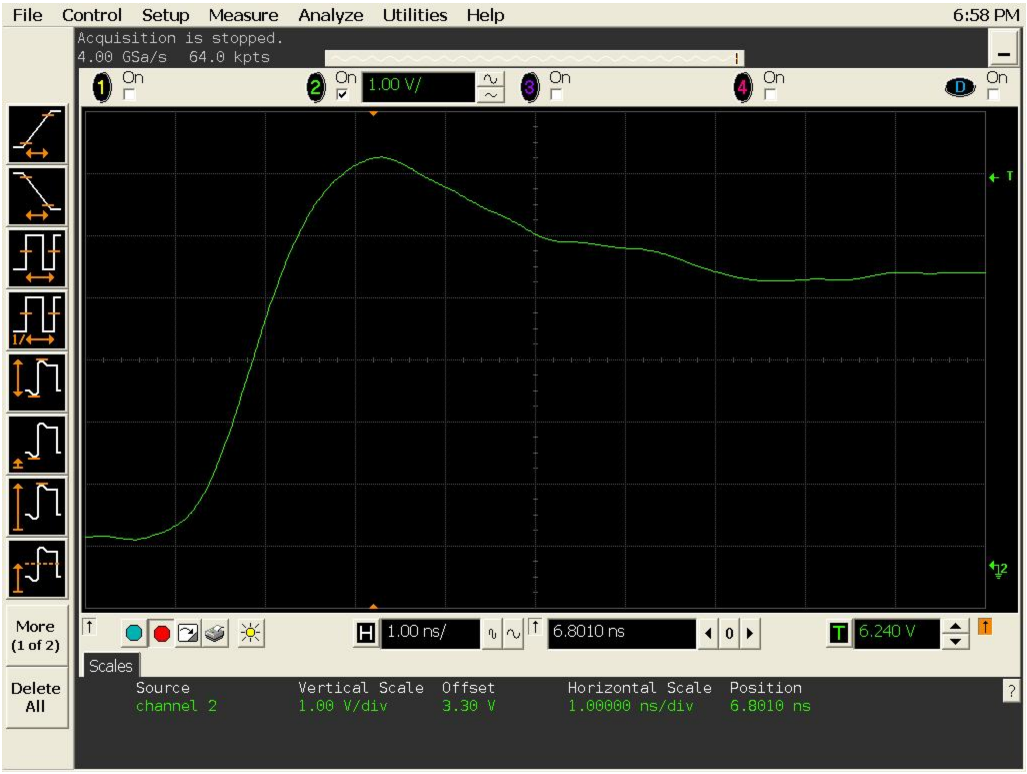


Figure 4(b) DUT 8321 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

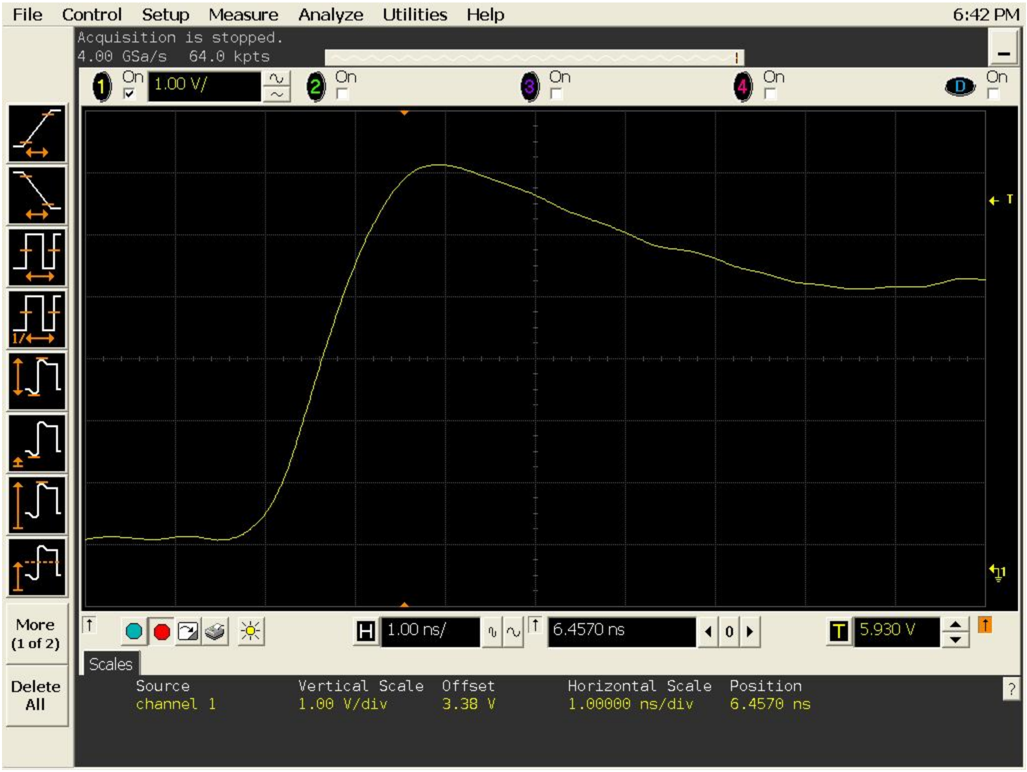


Figure 5(a) DUT 8352 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

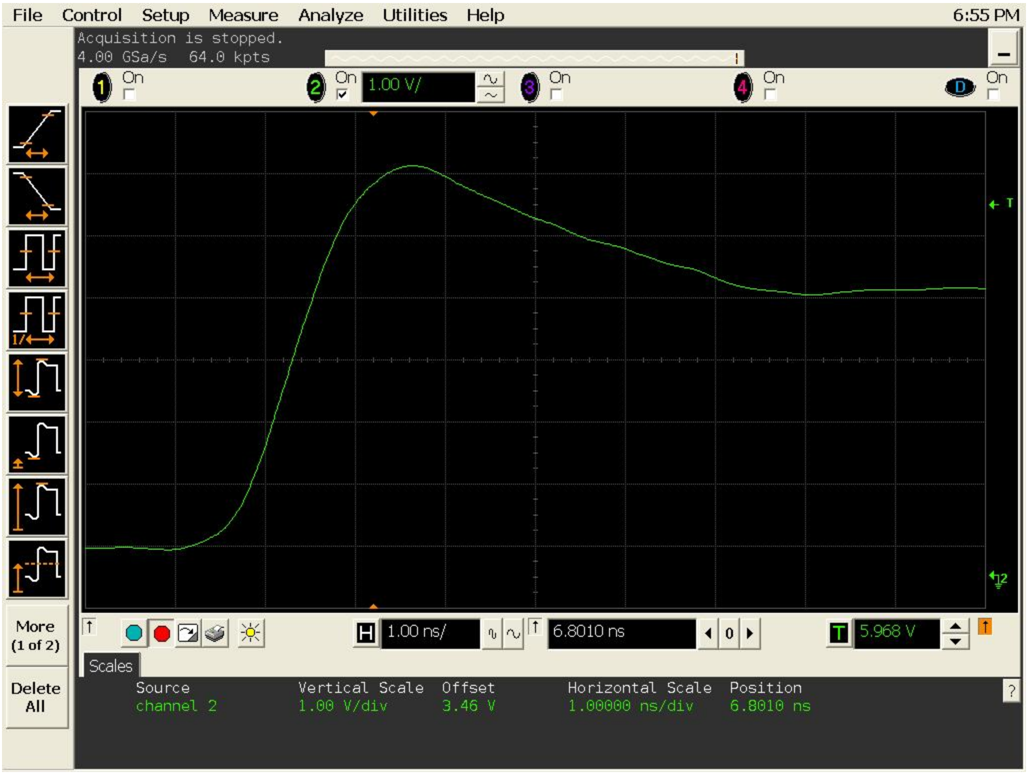


Figure 5(b) DUT 8352 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

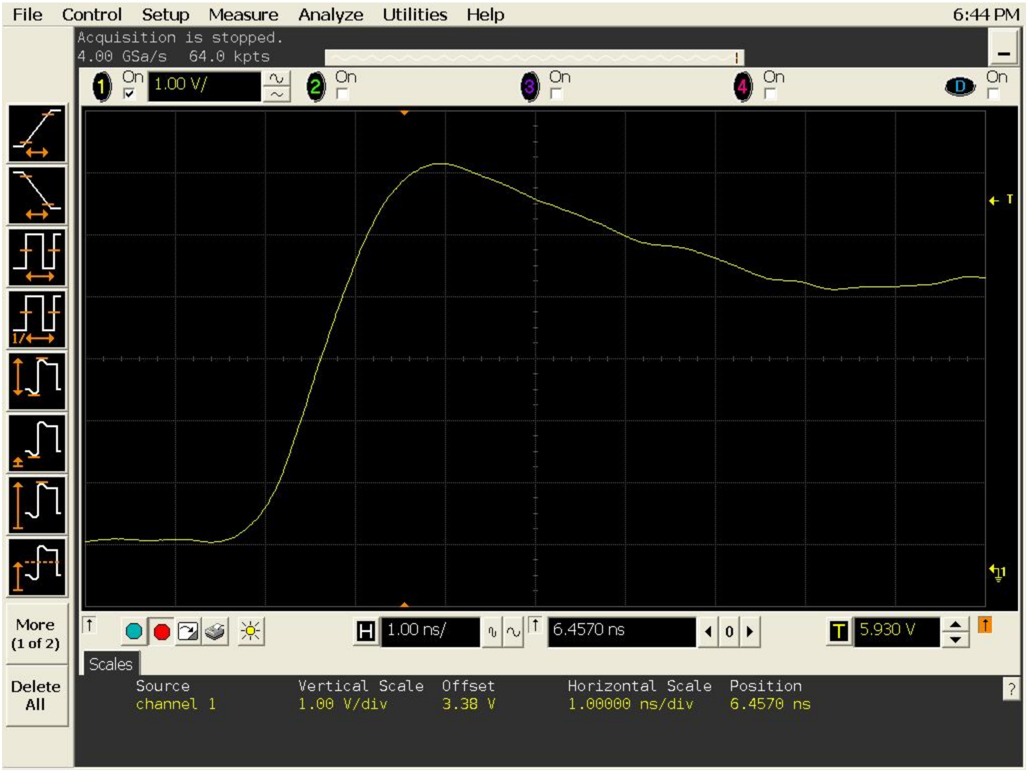


Figure 6(a) DUT 8420 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

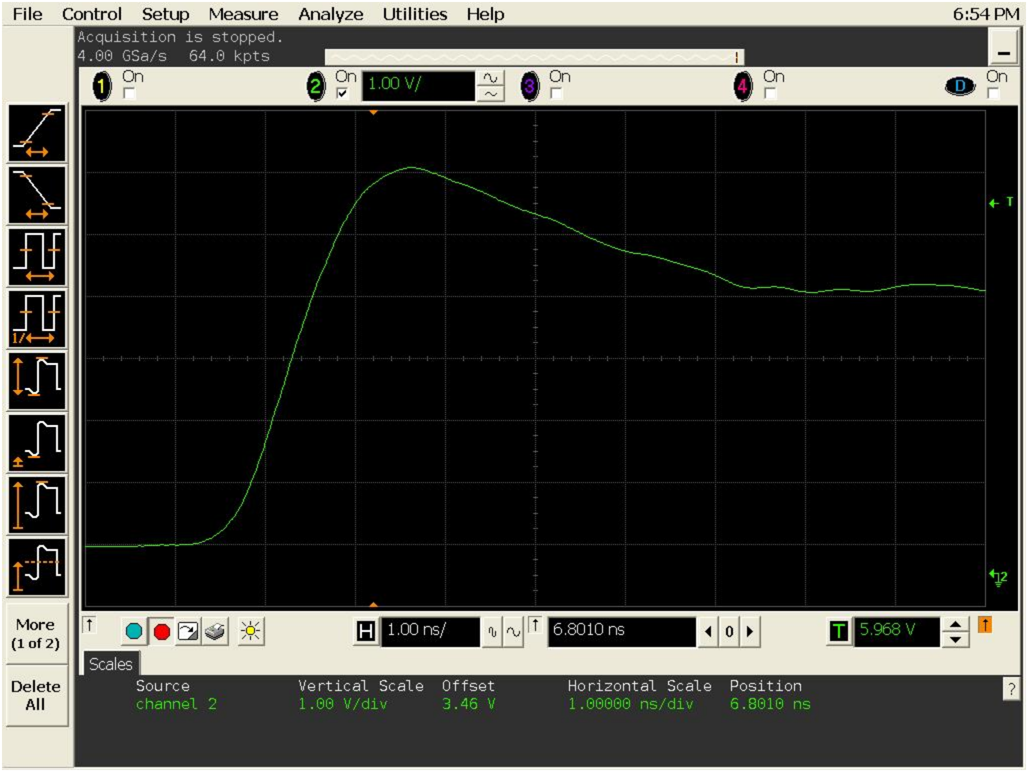


Figure 6(b) DUT 8420 post-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

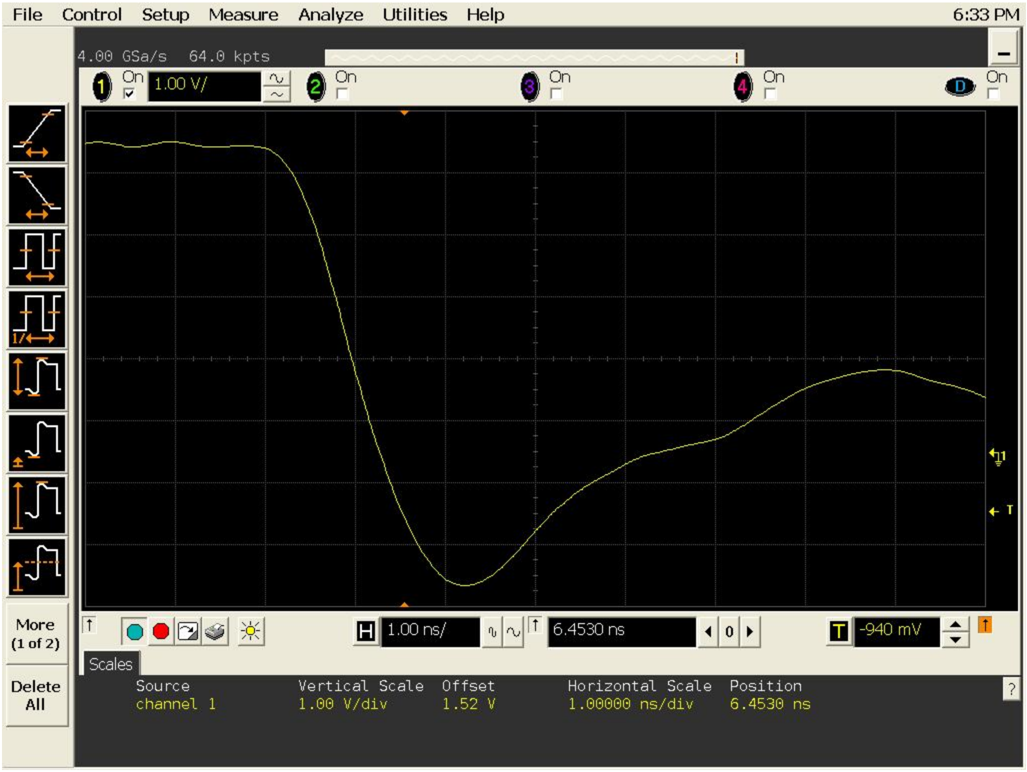


Figure 7(a) DUT 8292 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

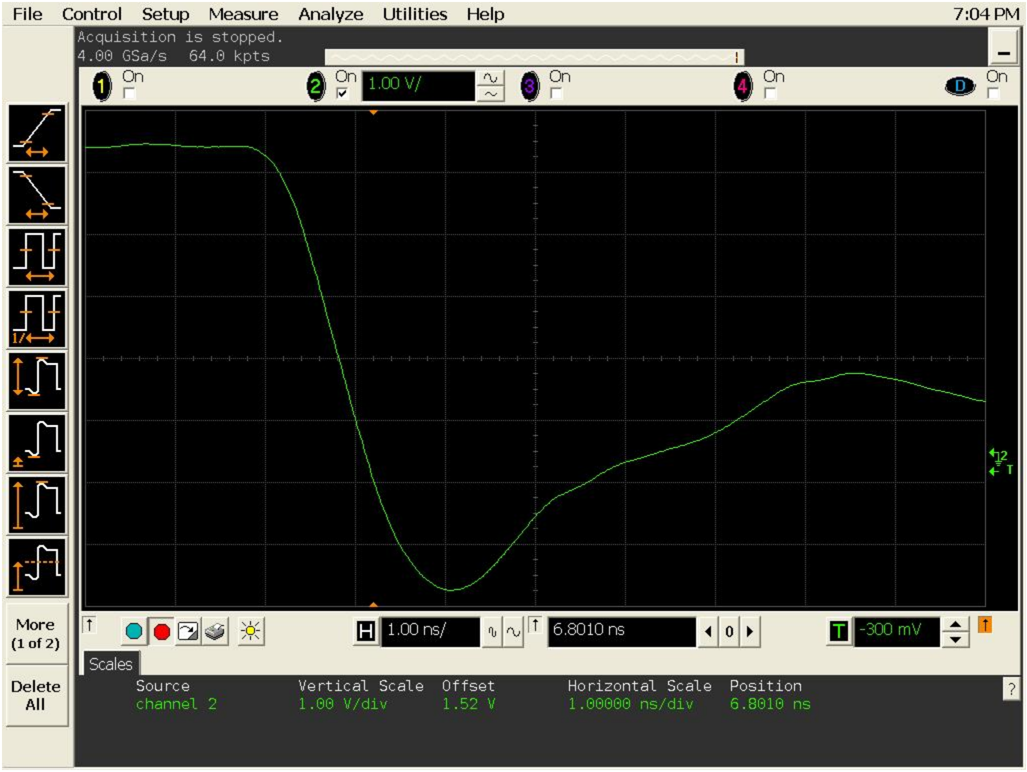


Figure 7(b) DUT 8292 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

Figure 8(a) DUT 8318 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

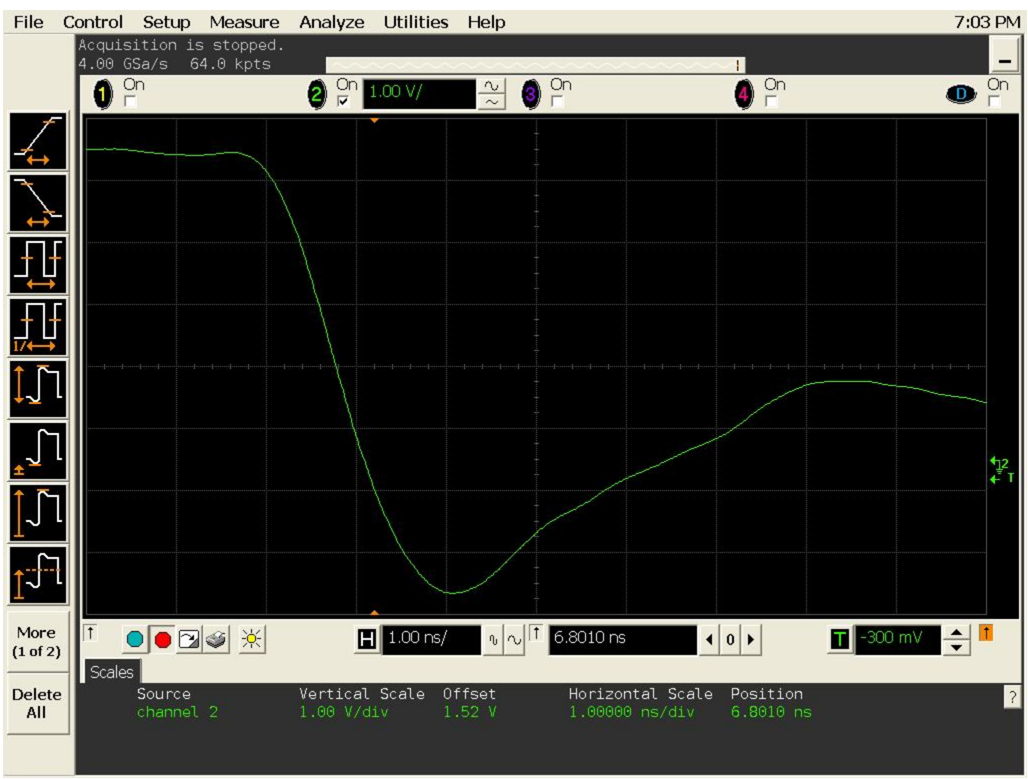


Figure 8(b) DUT 8318 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

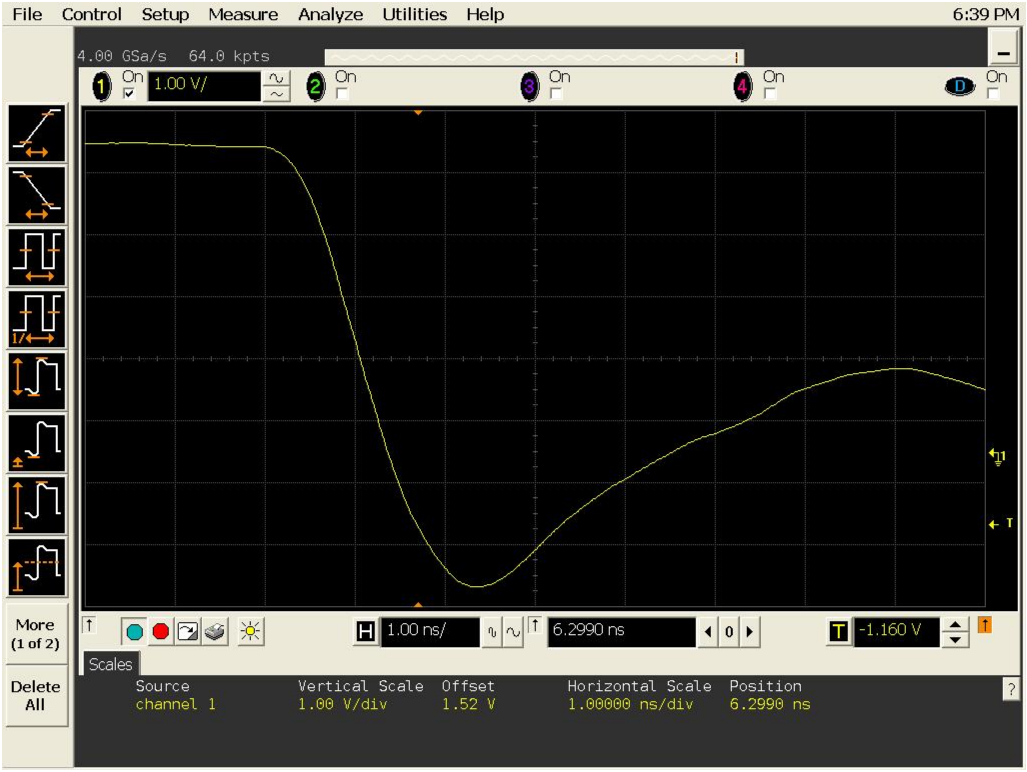


Figure 9(a) DUT 8321 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

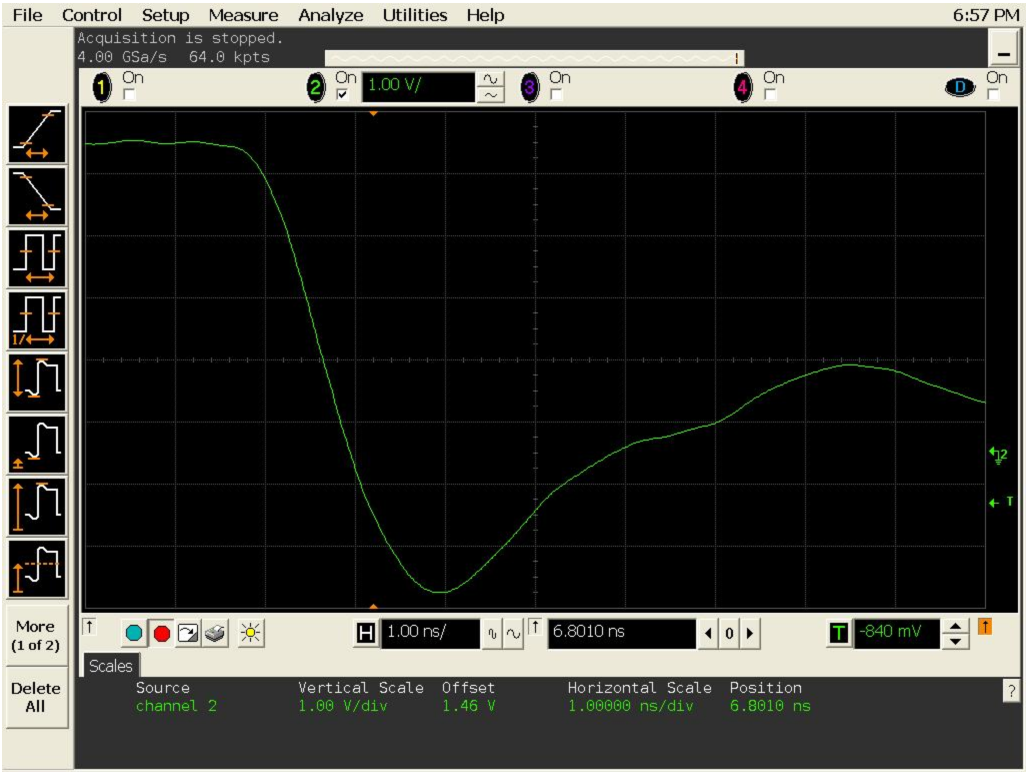


Figure 9(b) DUT 8321 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

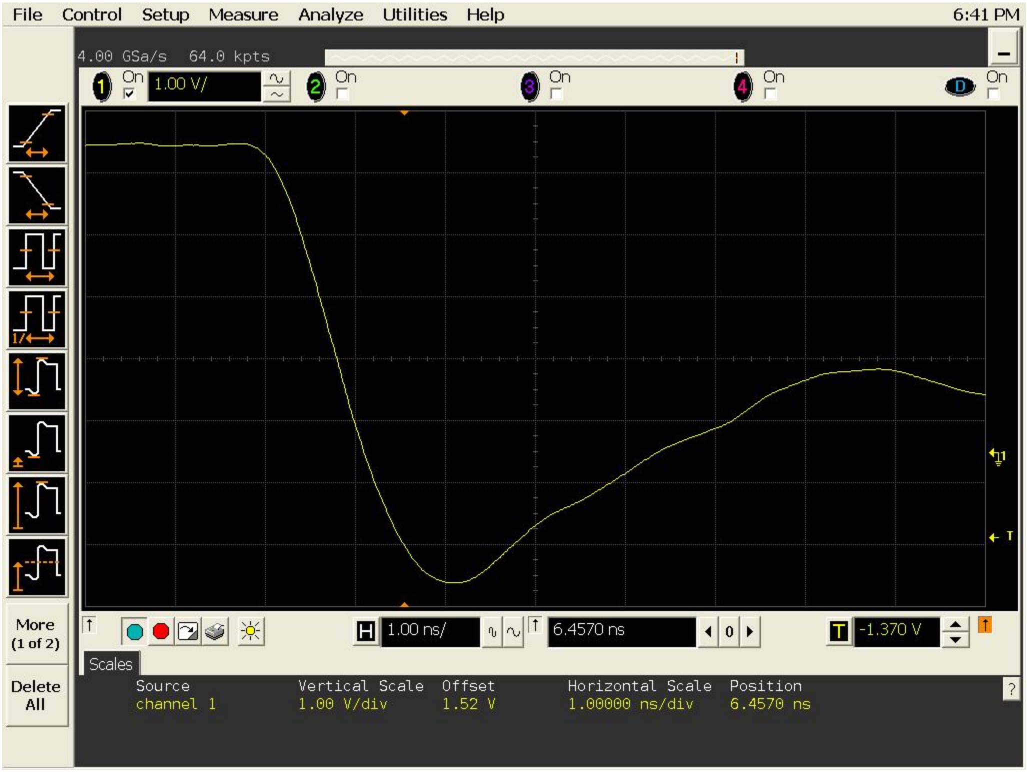


Figure 10(a) DUT 8352 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

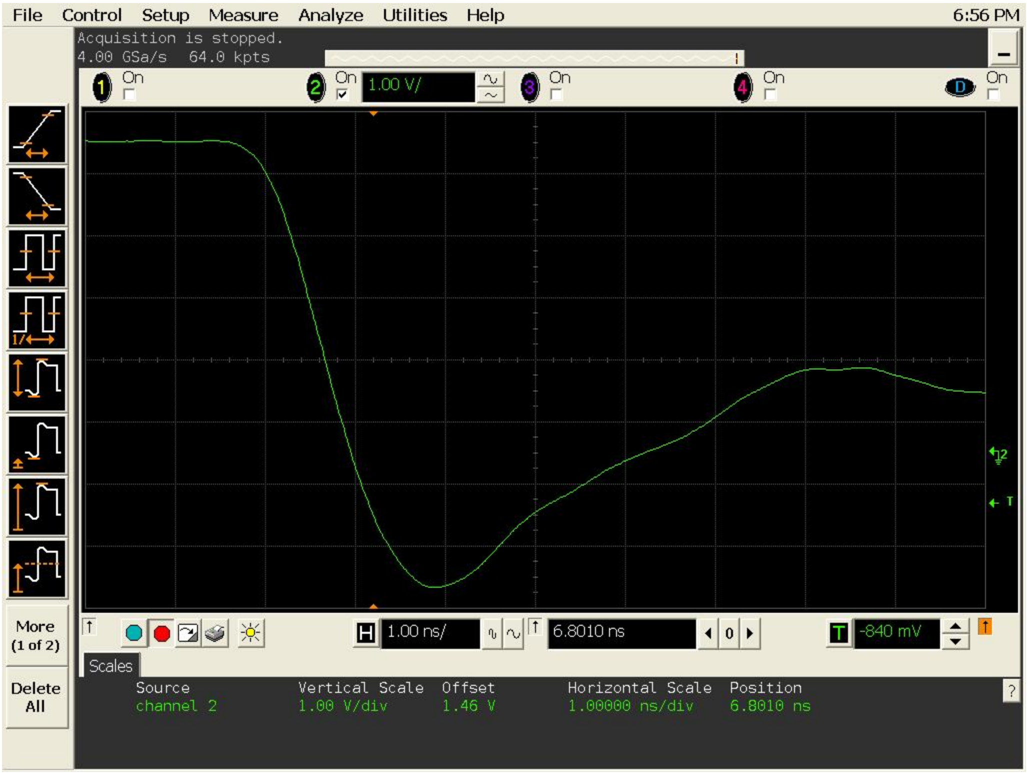


Figure 10(b) DUT 8352 post-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

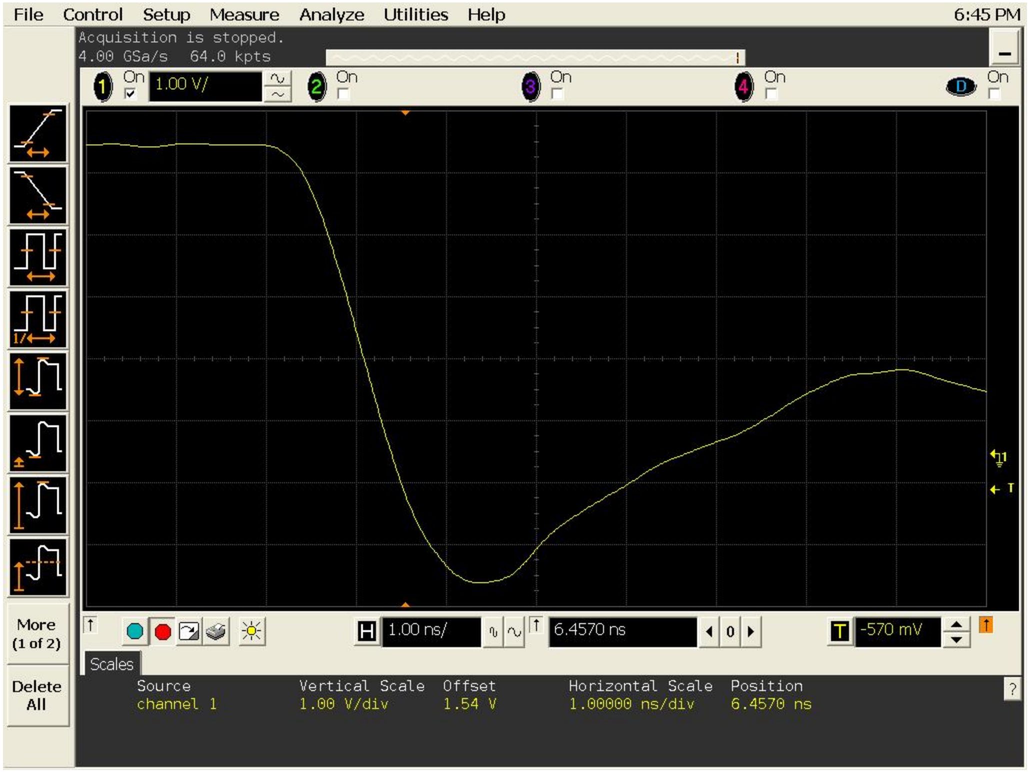


Figure 11(a) DUT 8420 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

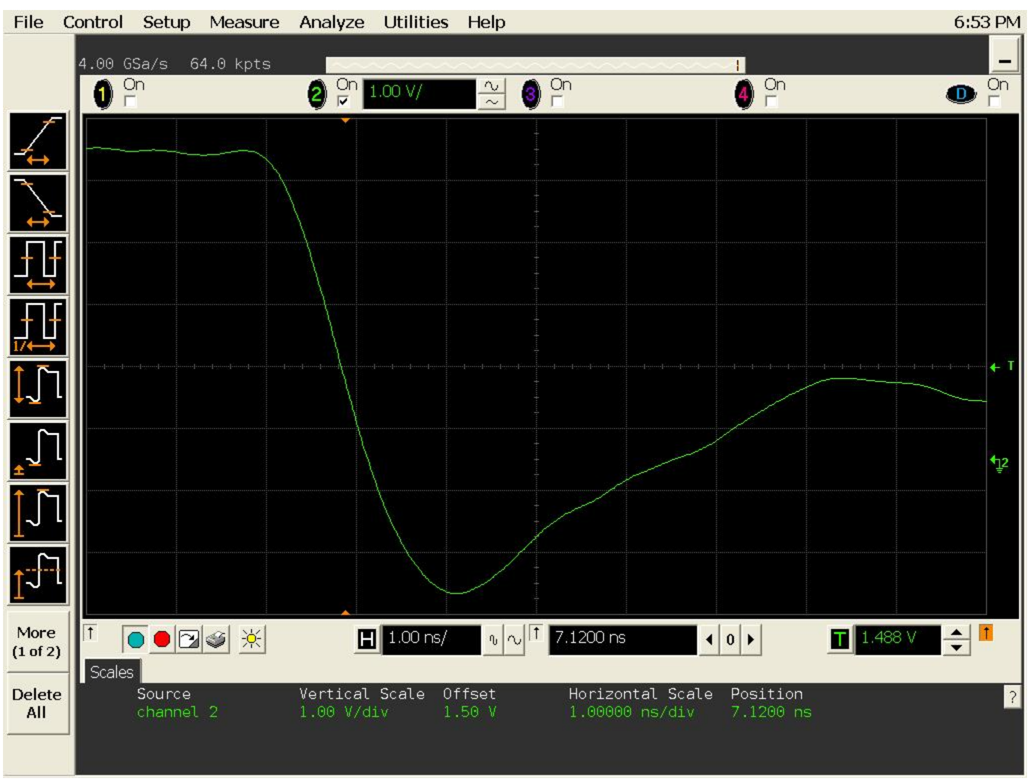
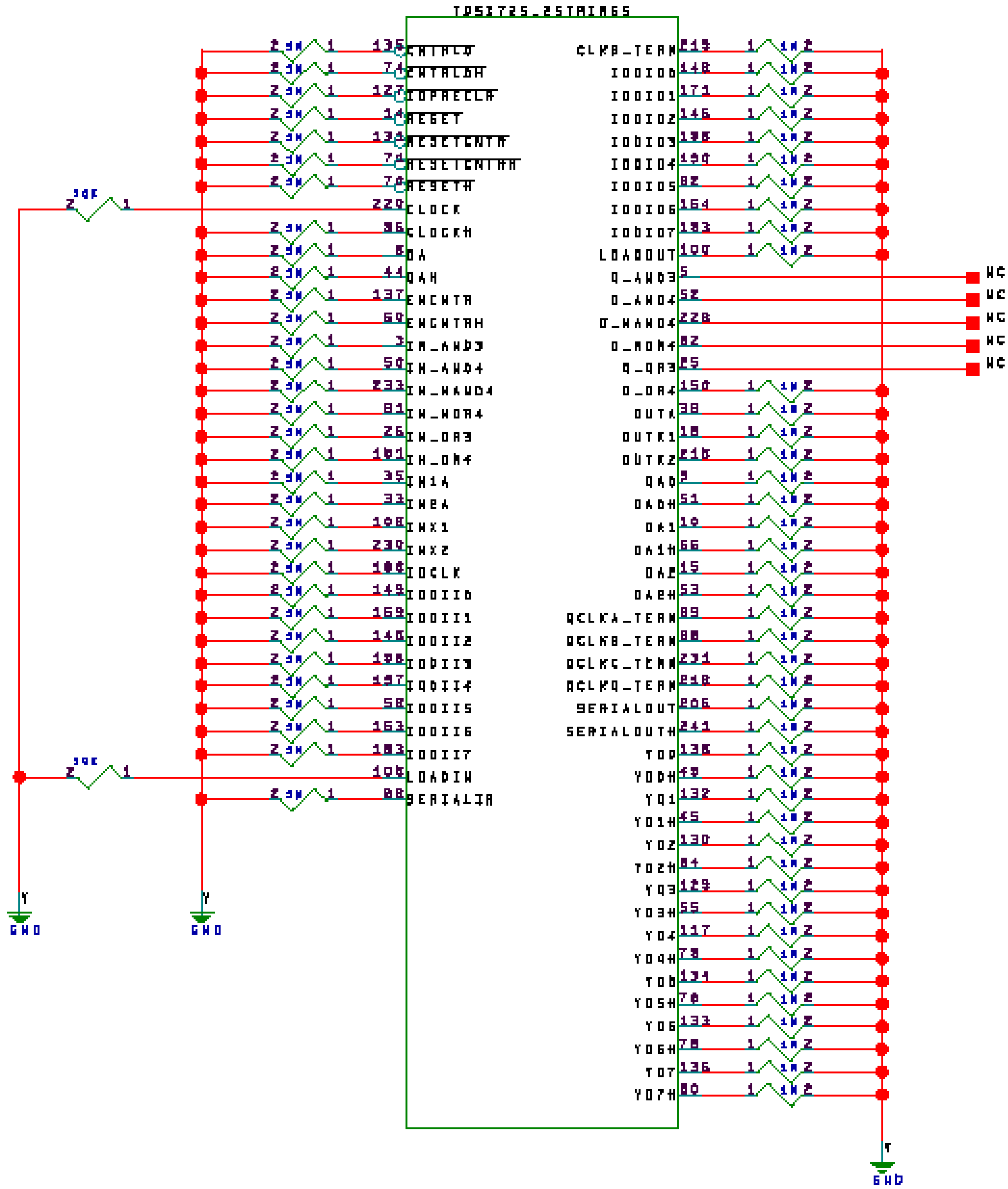
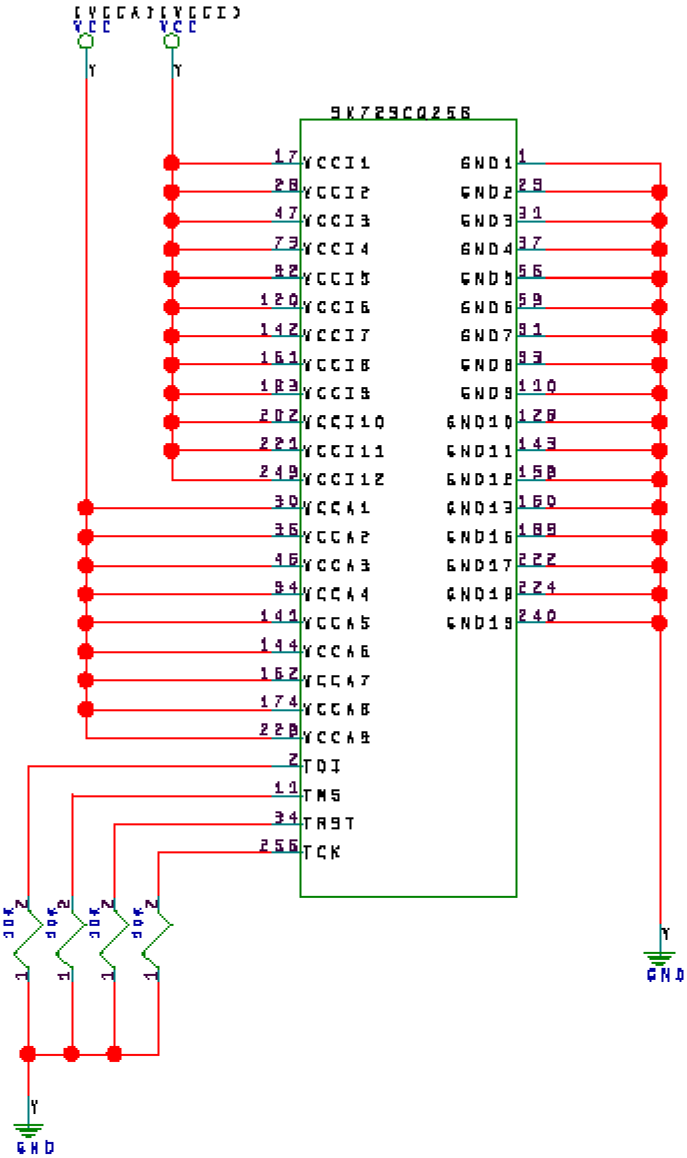


Figure 11(b) DUT 8420 post-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

Appendix A DUT Bias

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VCCI12
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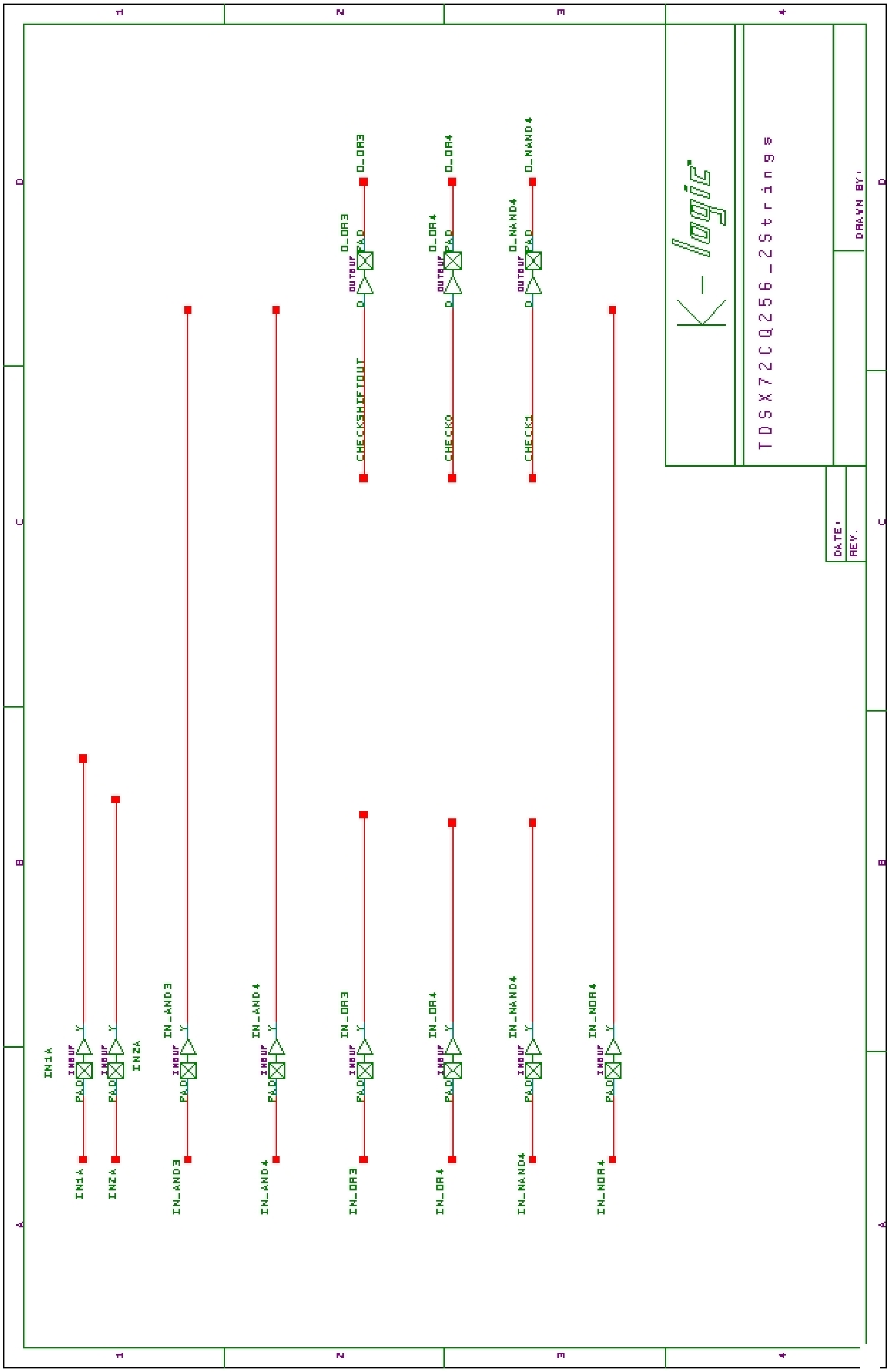
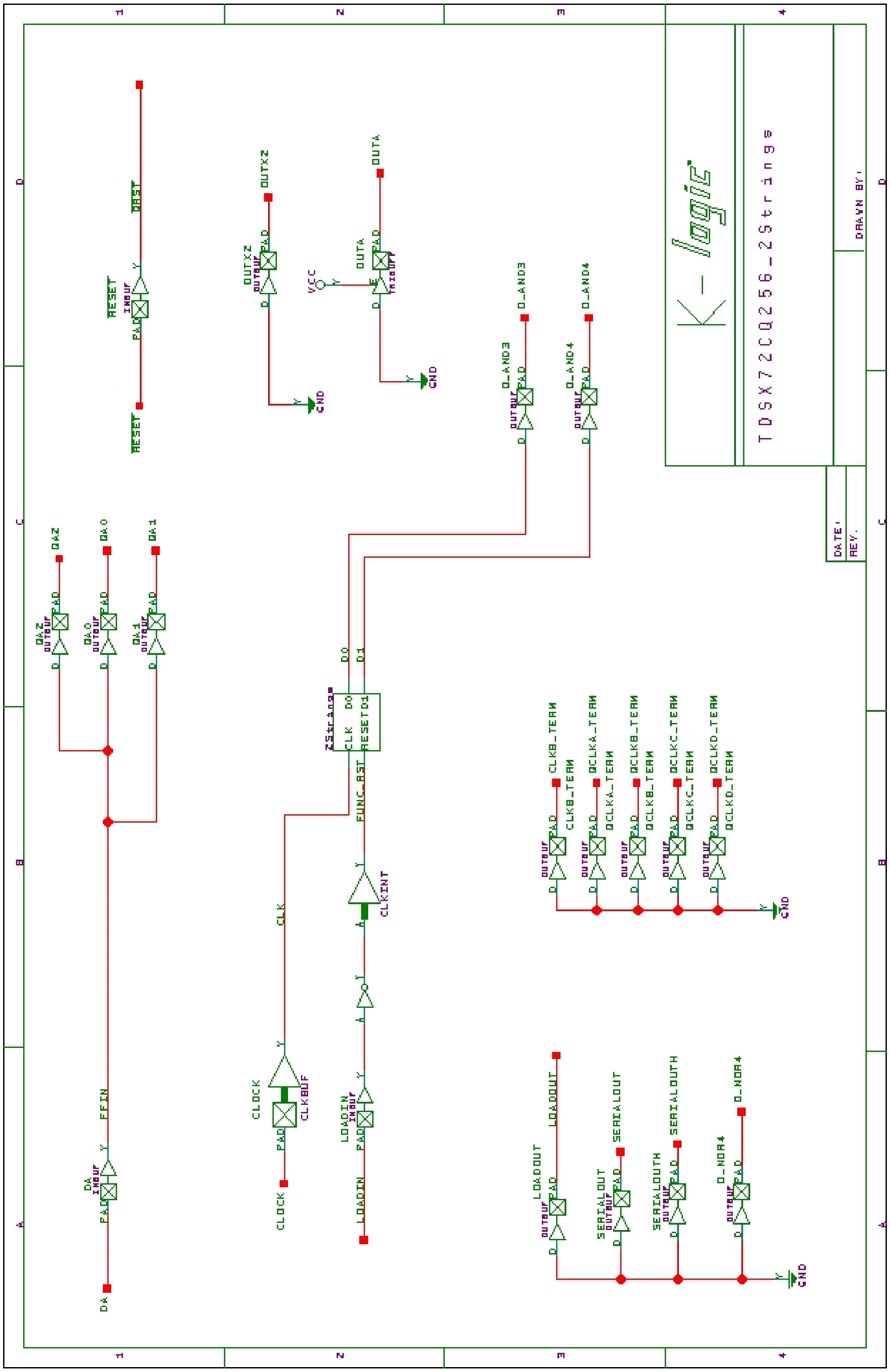
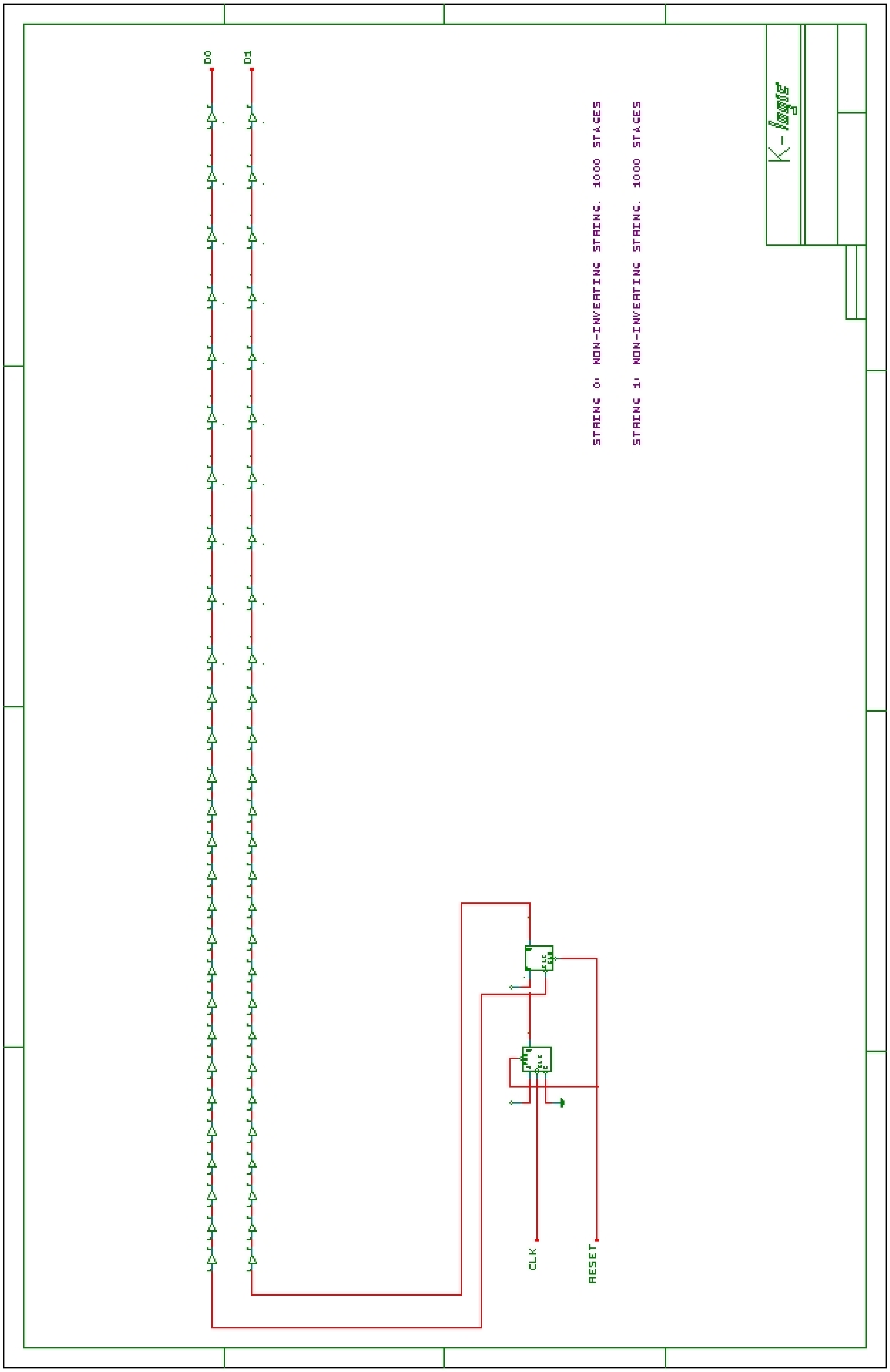
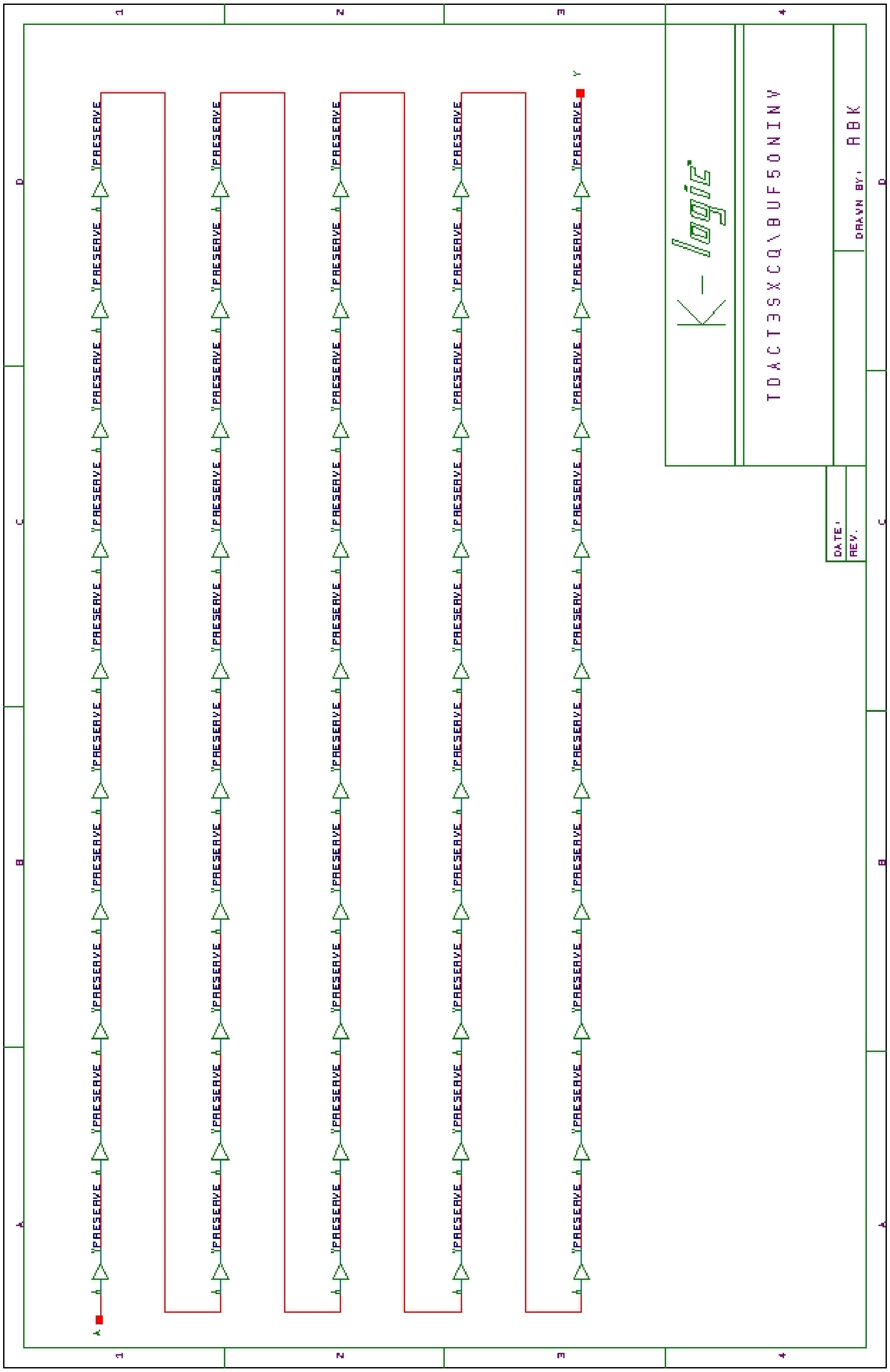
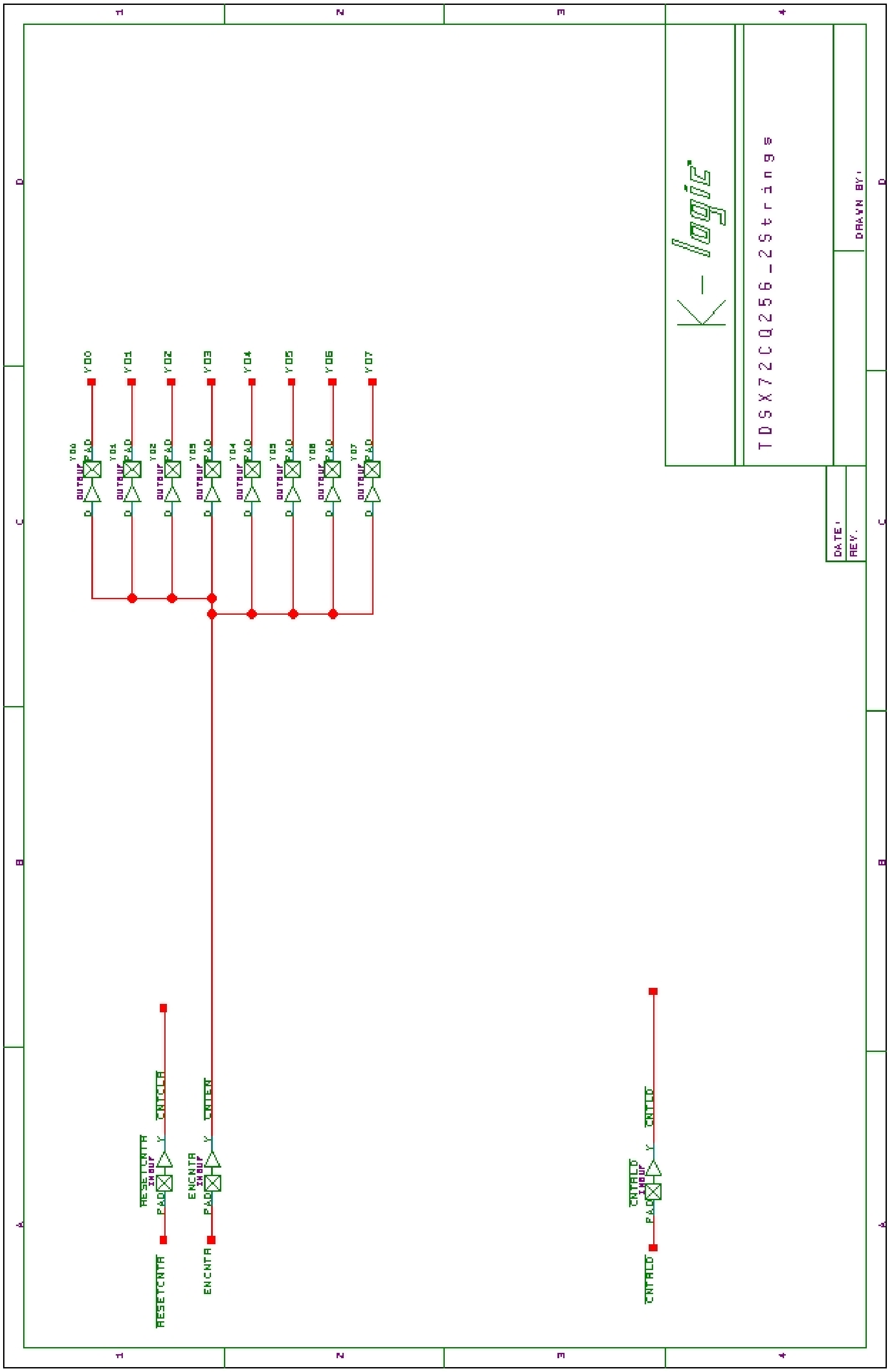
APPENDIX B DUT DESIGN SCHEMATICS

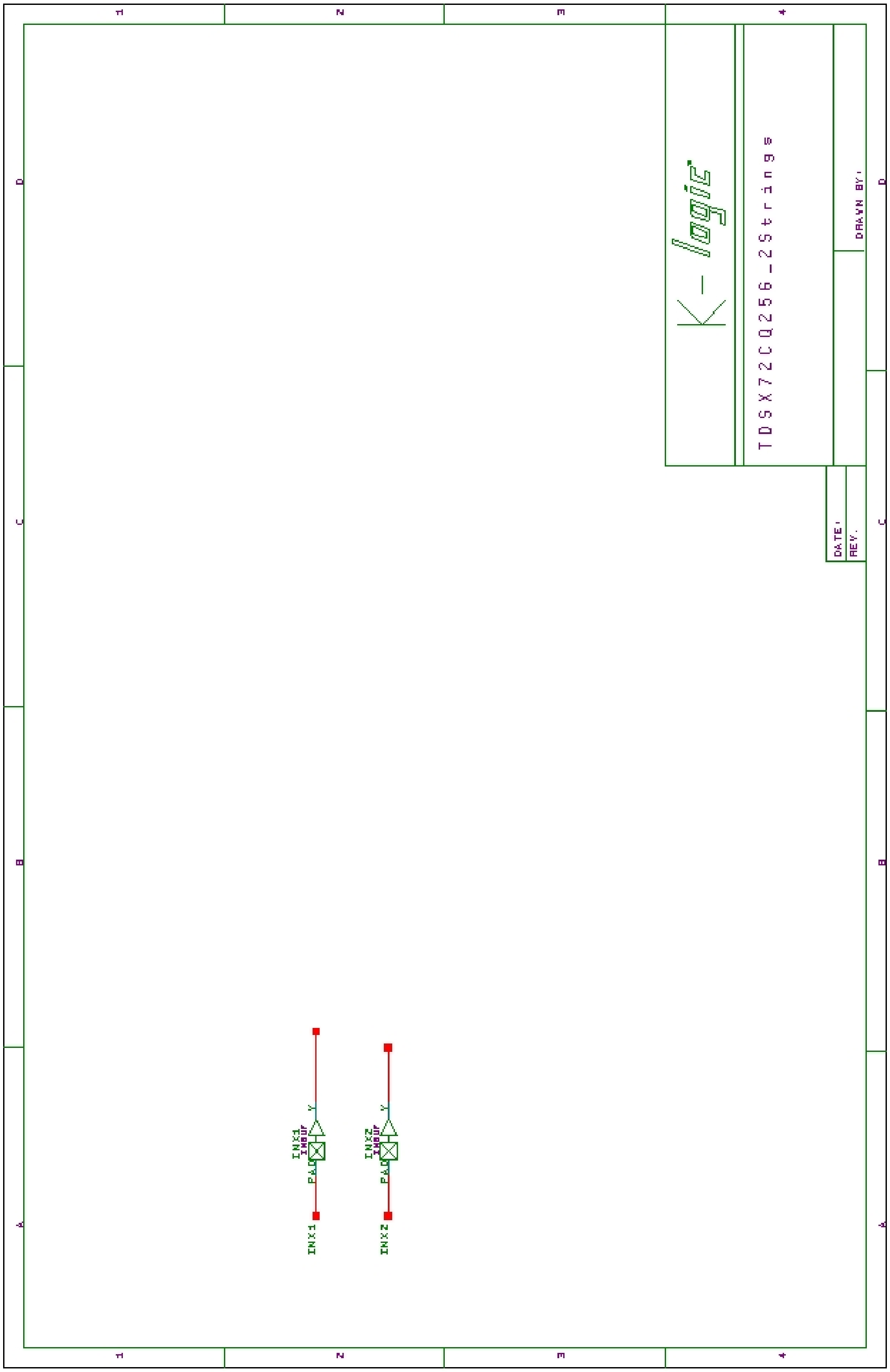


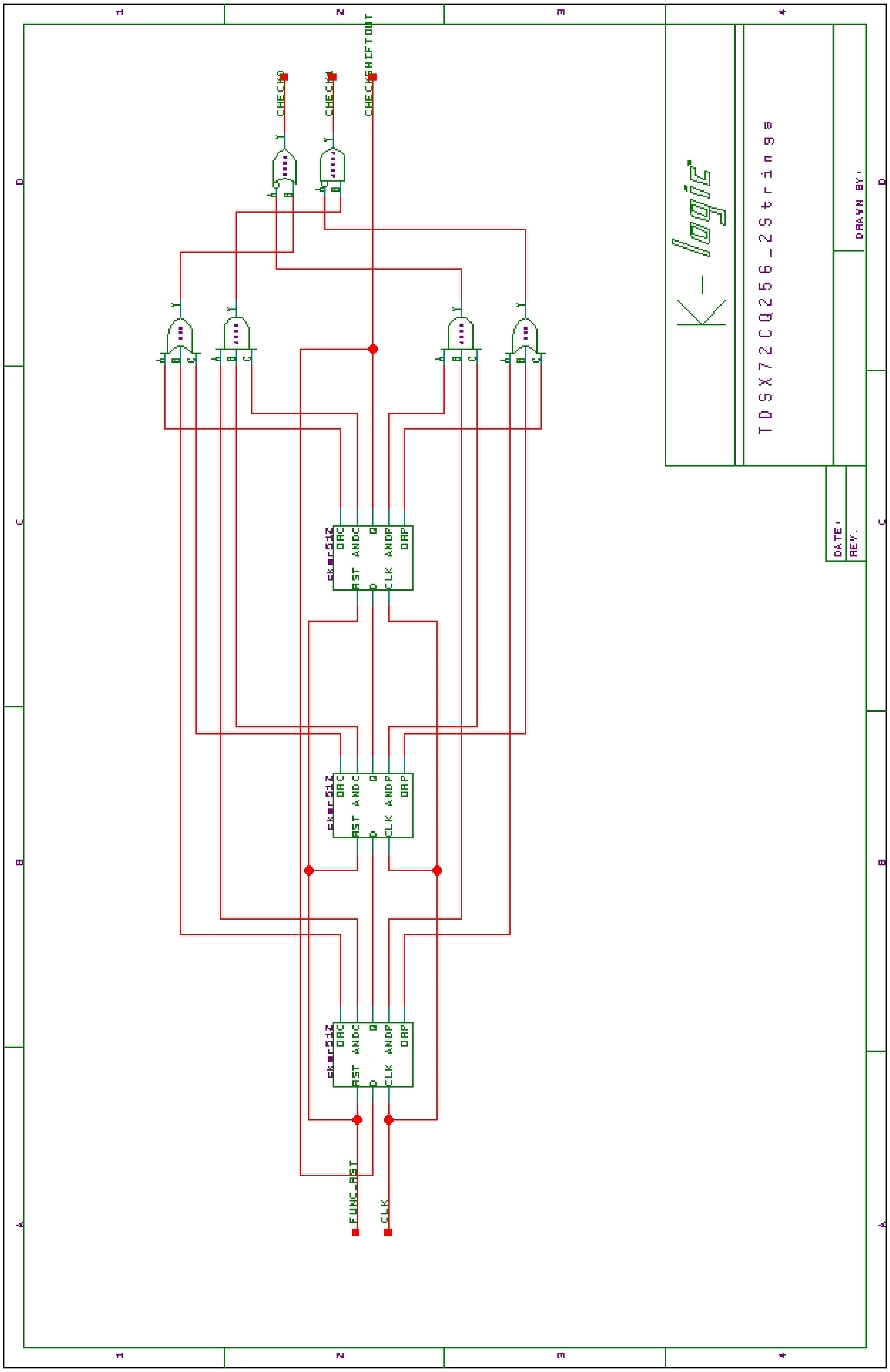

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
QRST
INBUF
PAD
OUTX2
OUTBUF
OUTA
TRIBUFF
VCC
GND
D_AND3
D_AND4
QAZ
QA0
QA1
2Strings
CLK
D0
D1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
DA
FFIN
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM

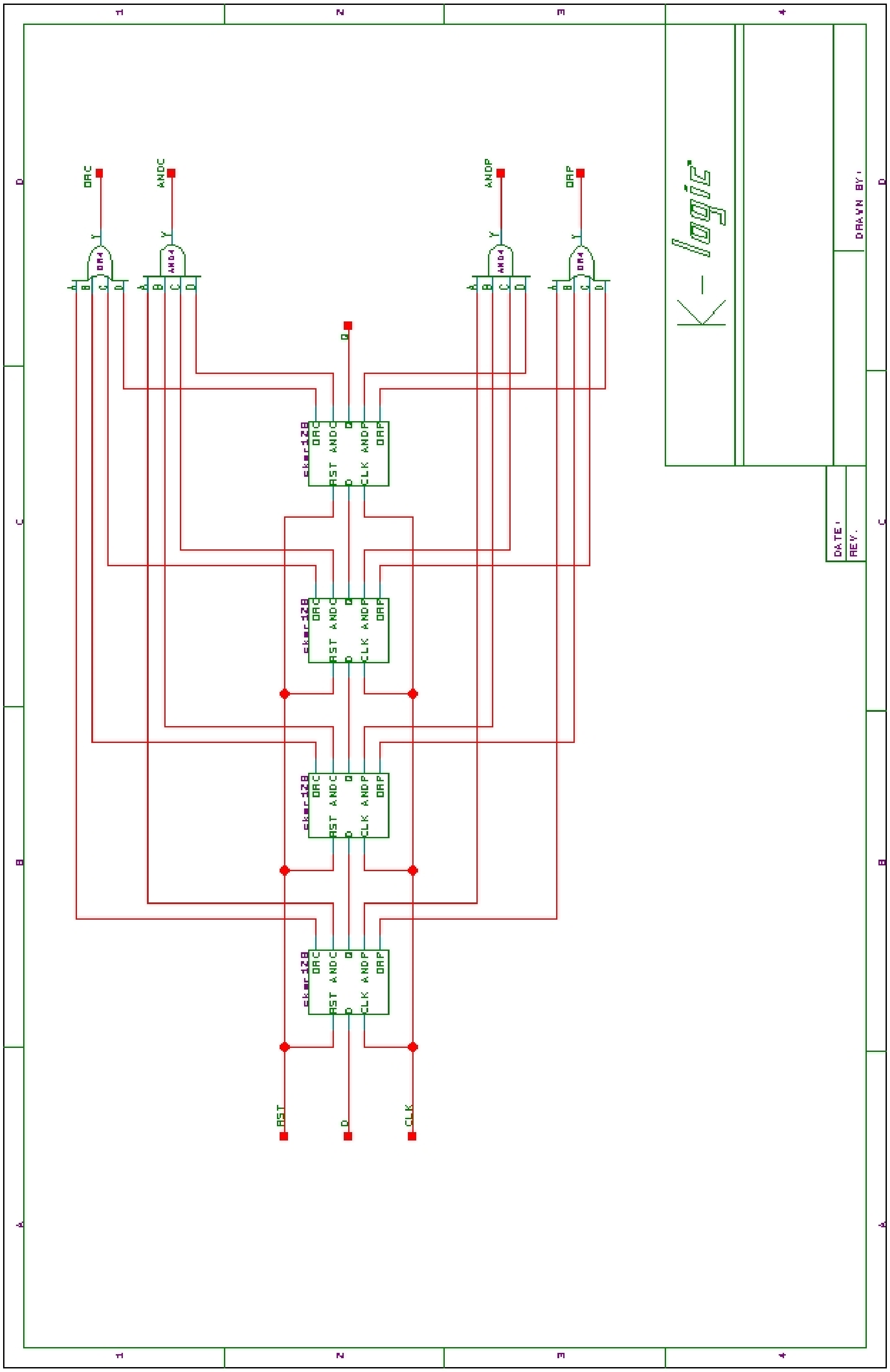

D0
D1
STRING 0: NON-INVERTING STRING. 1000 STAGES
STRING 1: NON-INVERTING STRING. 1000 STAGES
CLK
RESET


TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE
A
Y

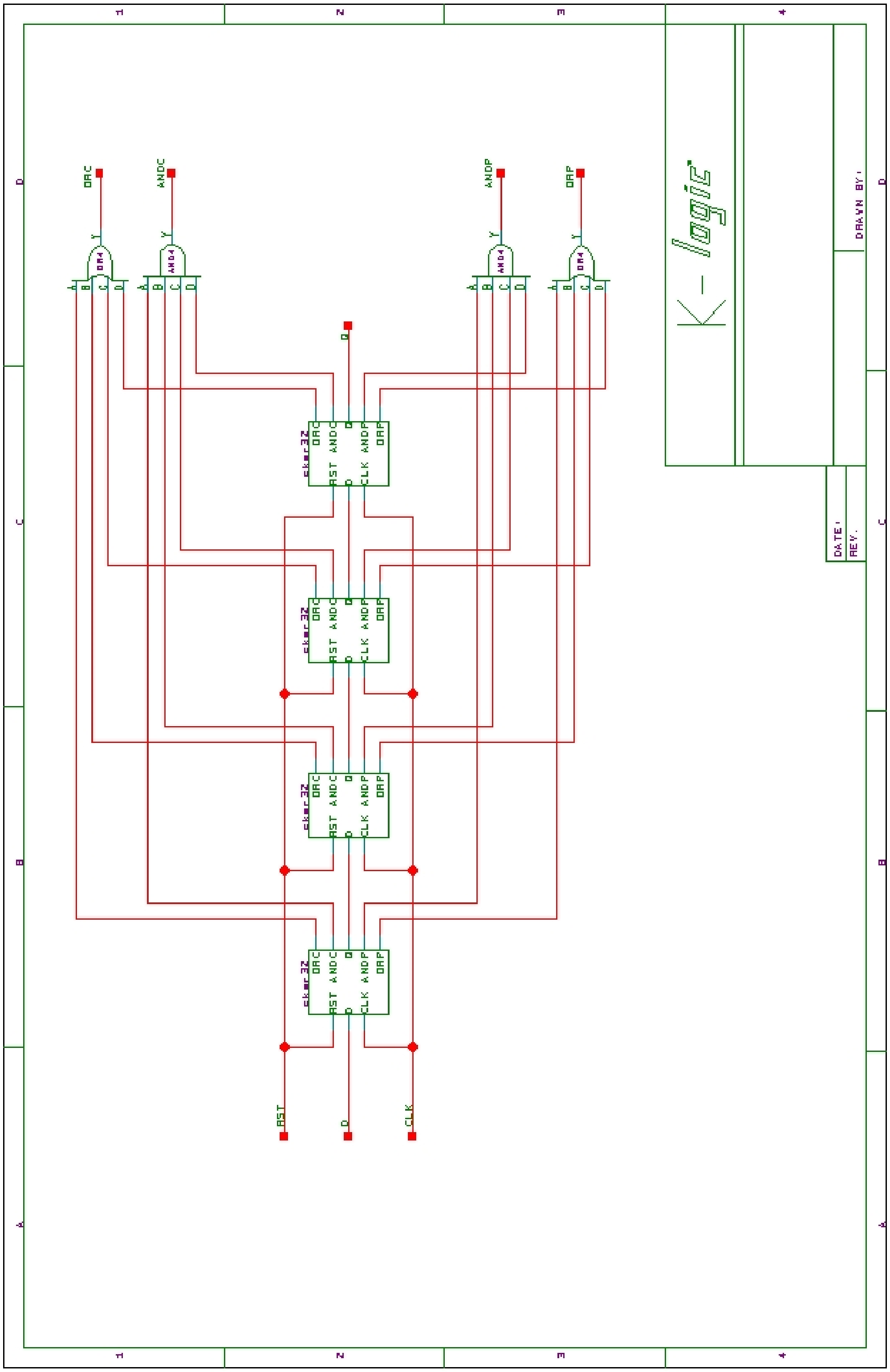

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
INBUF
RESETCNTA
CNTCLR
ENCNTA
CNTEN
CNTALD
CNTLD

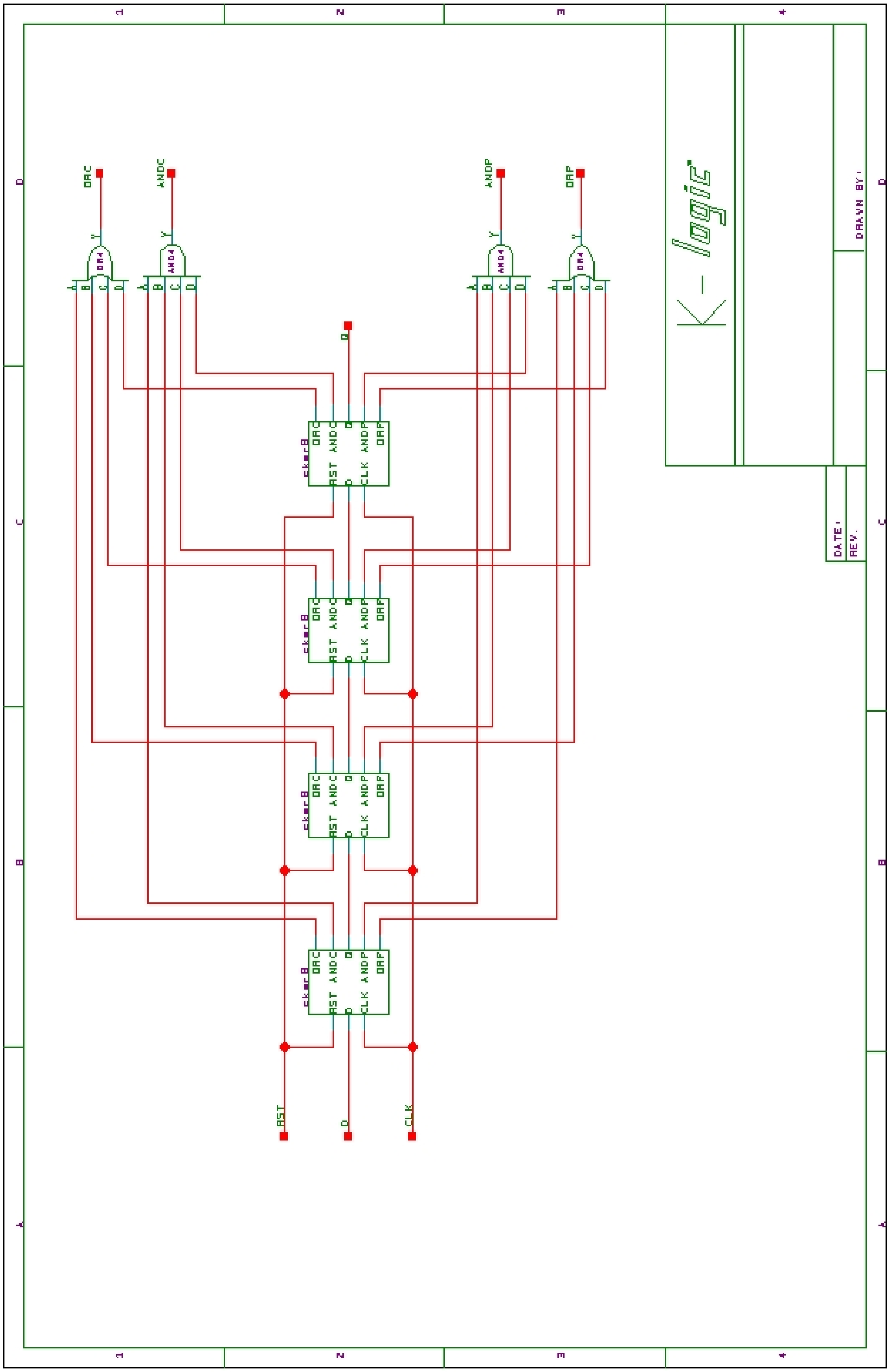

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INBUF
PAD
Y
INX1
INX2
INBUF
PAD
Y
INX2

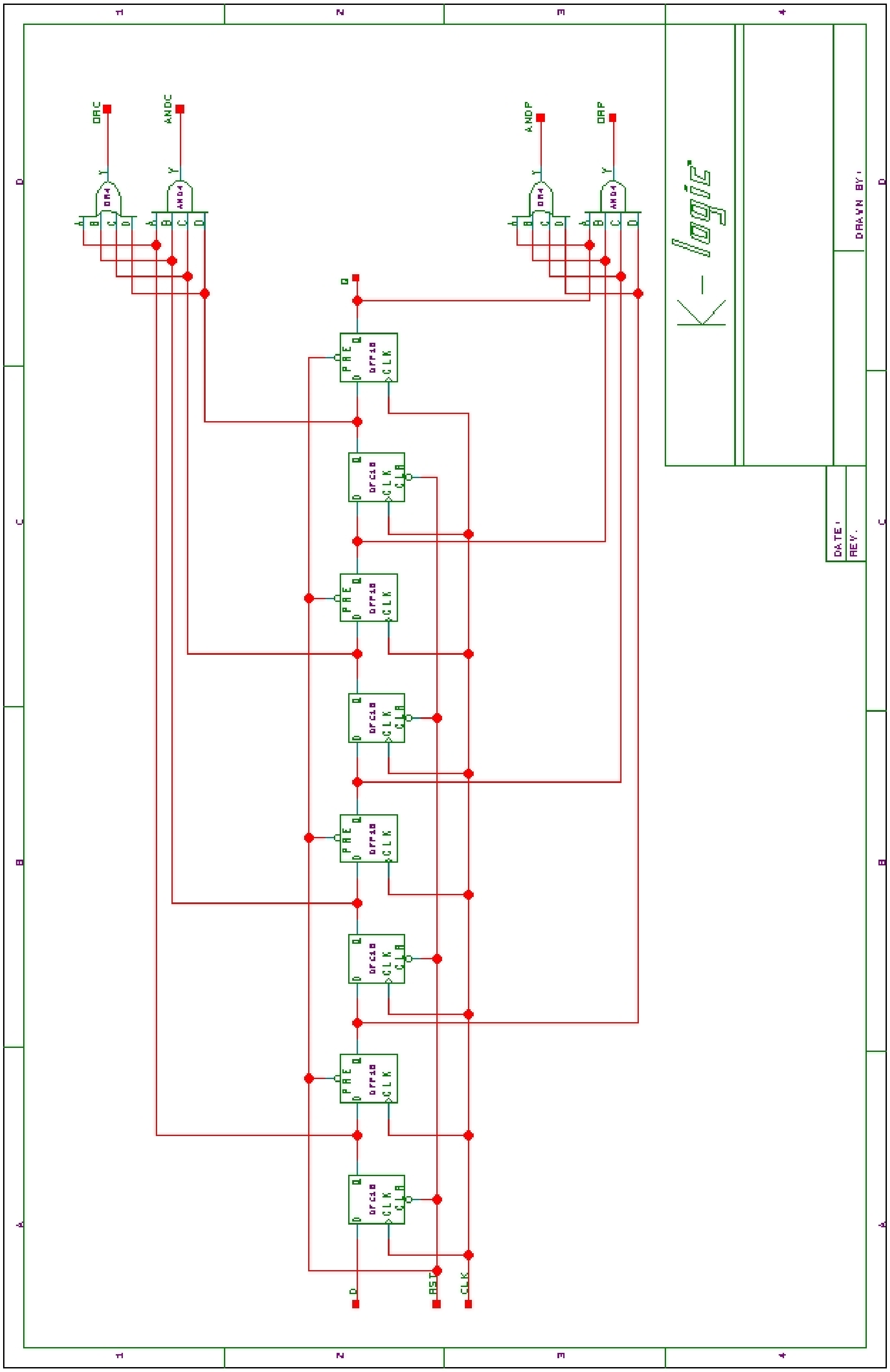

CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK
ckmr51Z
ORC
ANDC
RST
D
Q
ANDP
CLK
ORP
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

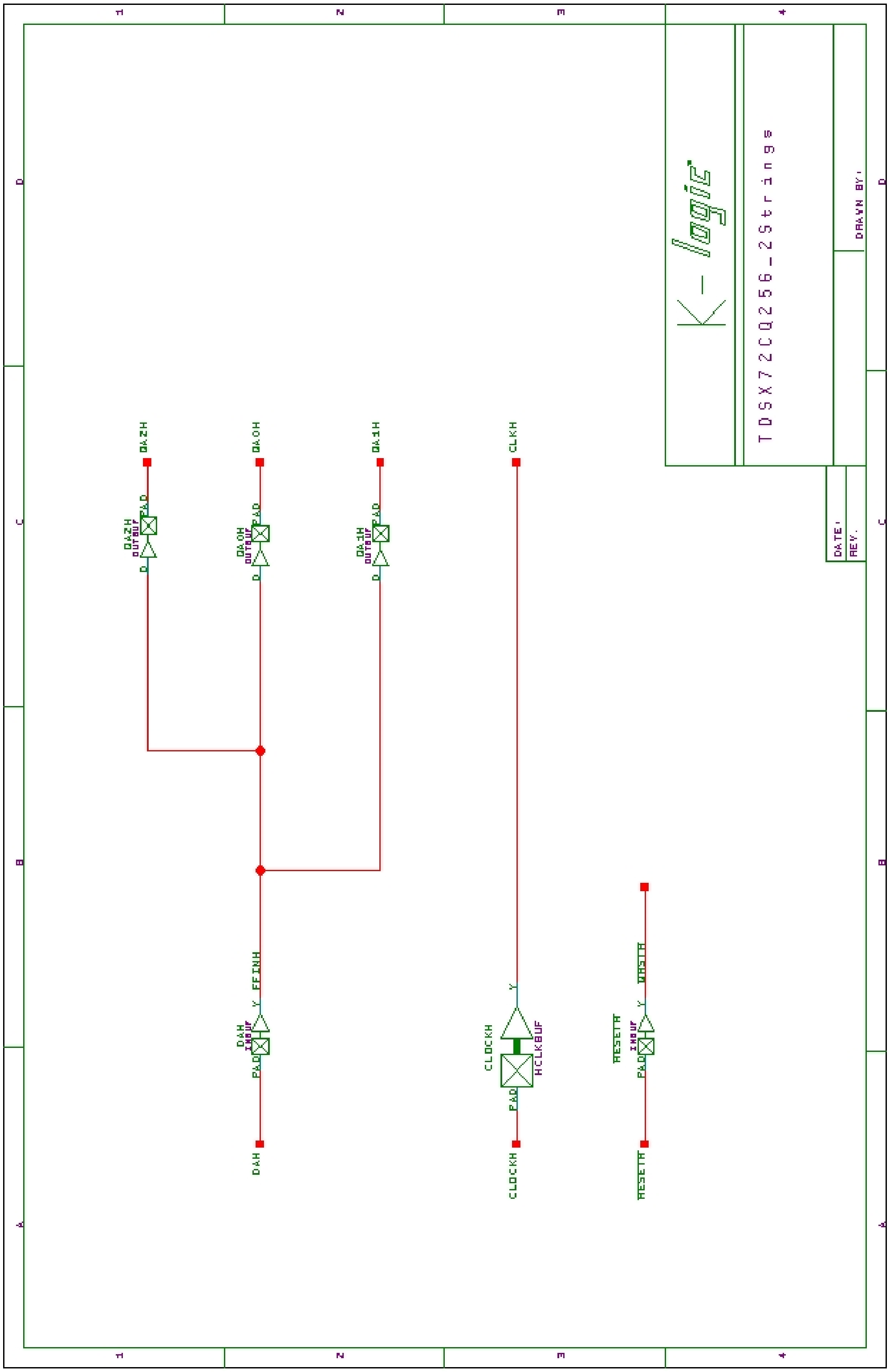


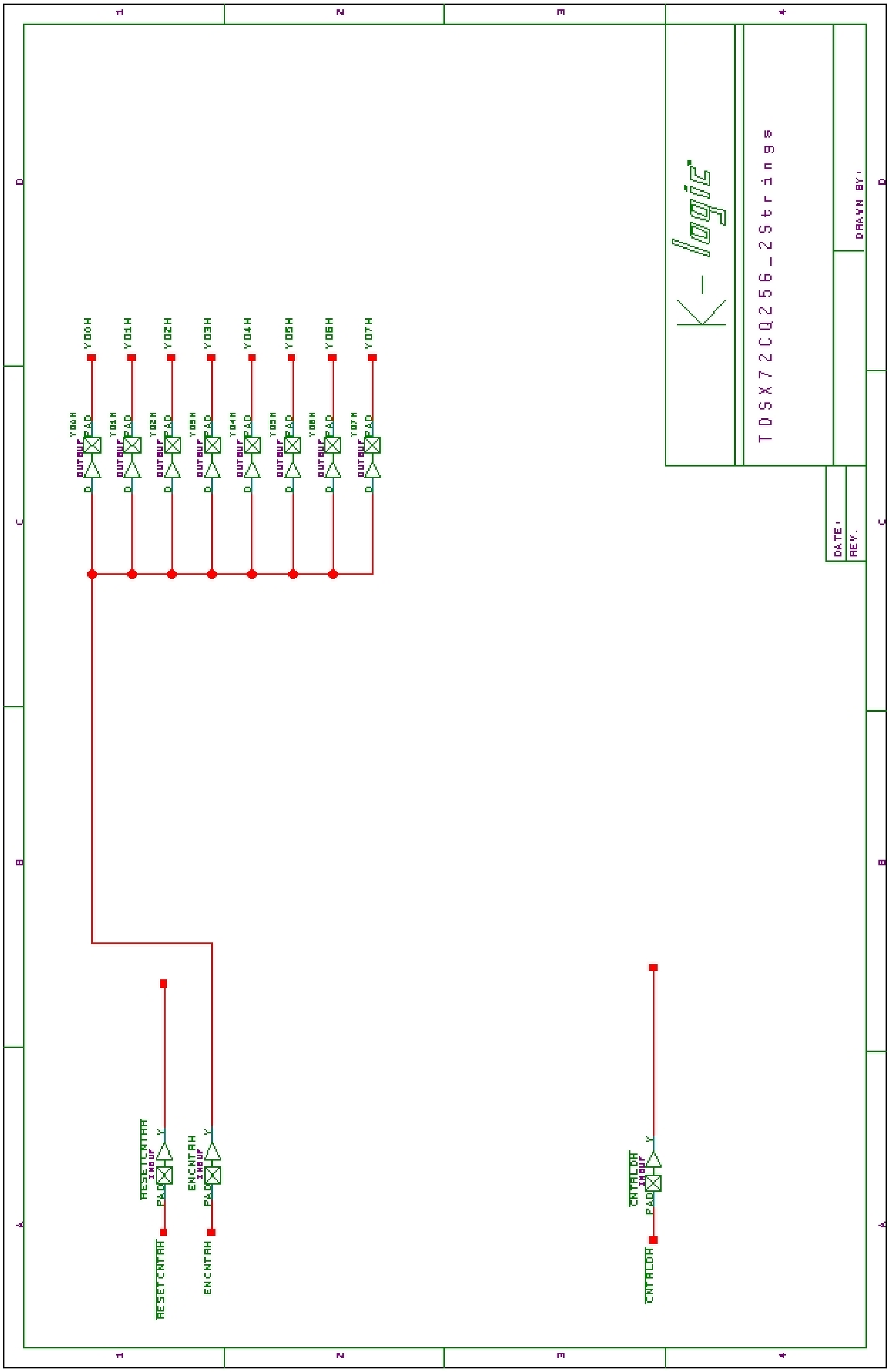
ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr128
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

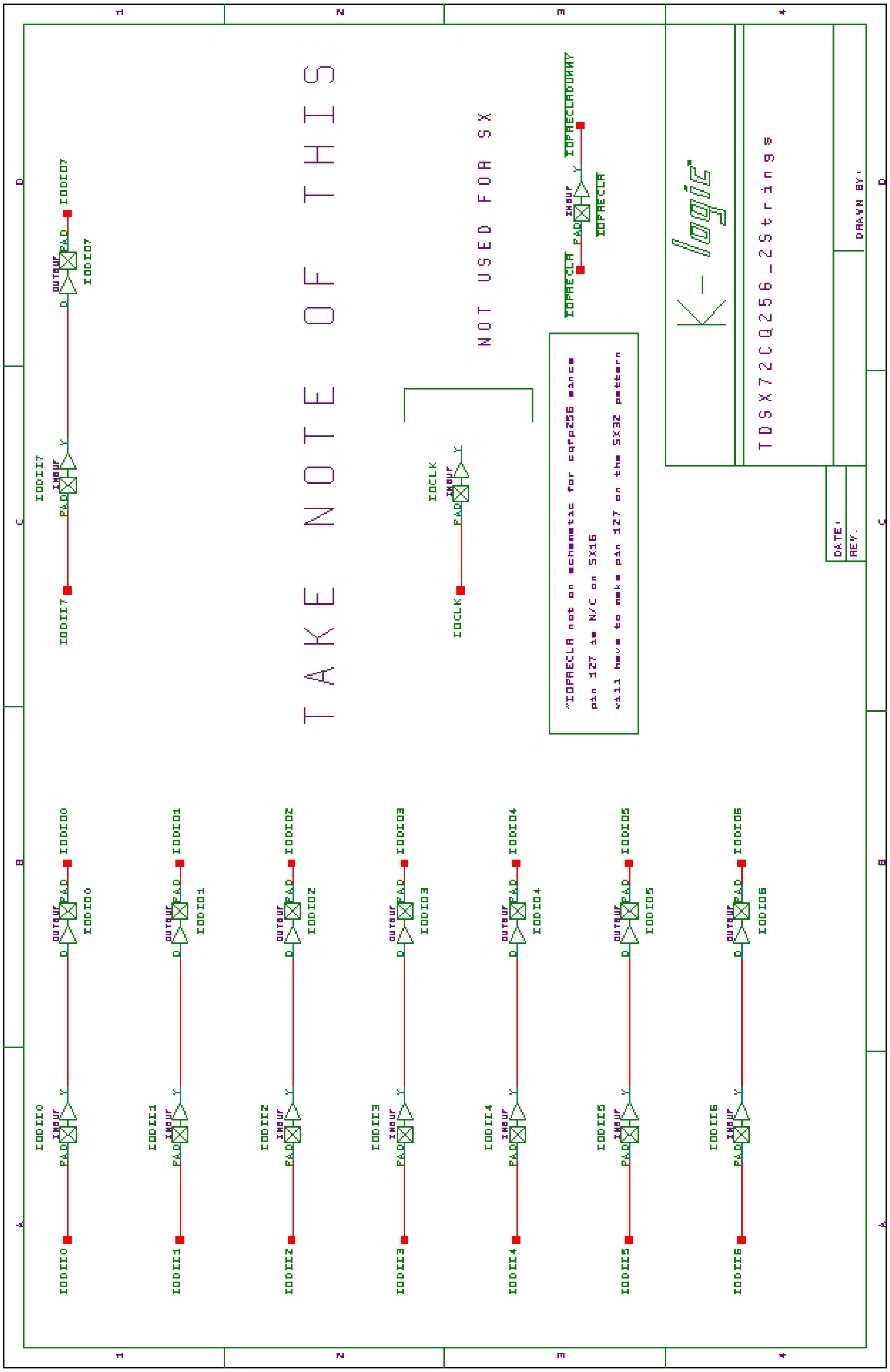

ORC
ANDC
ANDP
ORP
OR4
AND4
Q
ckmr32
RST
D
CLK
DRAWN BY:
DATE:
REV.

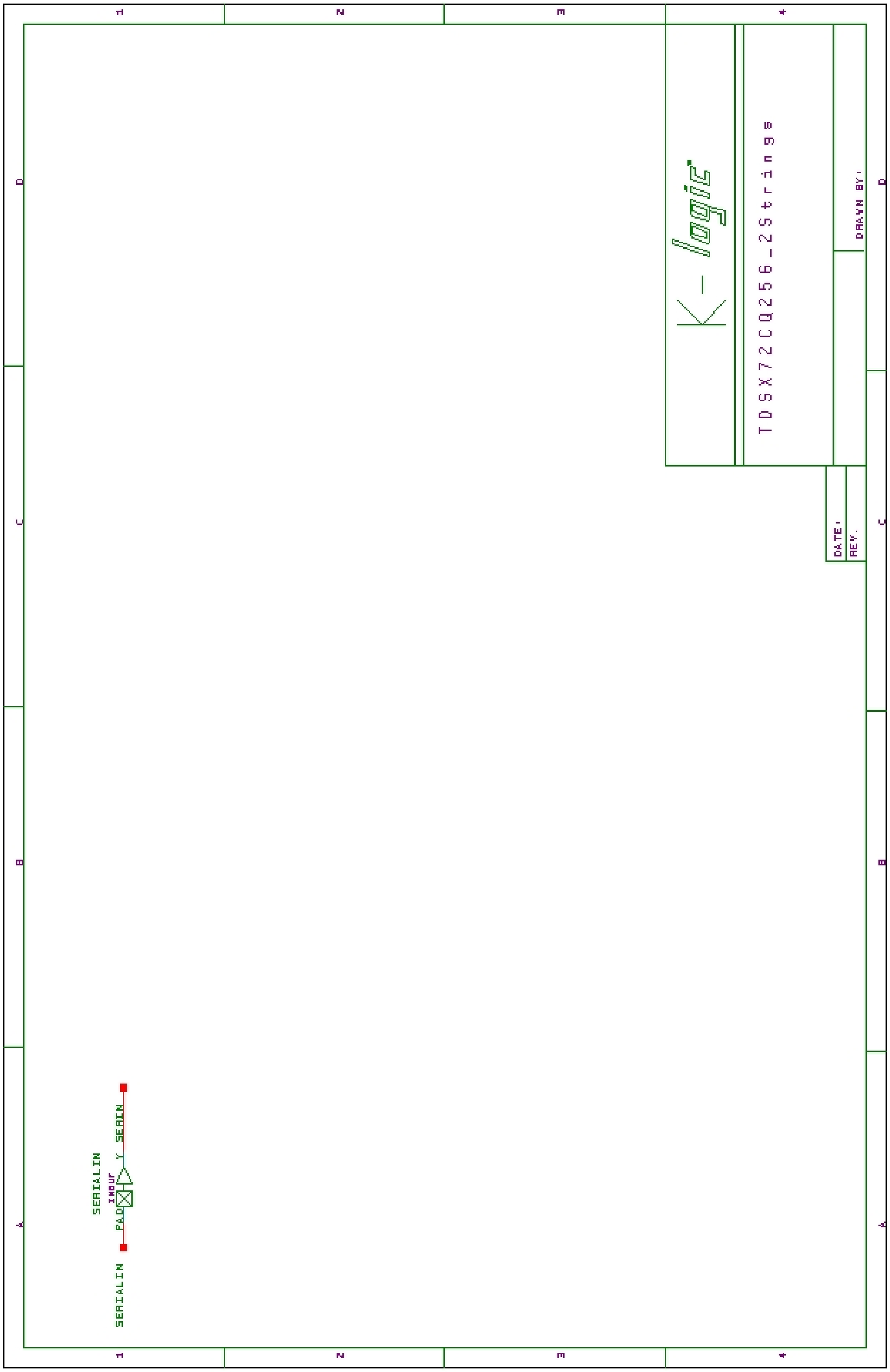

ORC
ANDC
ANDP
ORP
Q
OR4
AND4
ckmr8
RST
D
CLK
K-logic
DRAWN BY:
DATE:
REV.

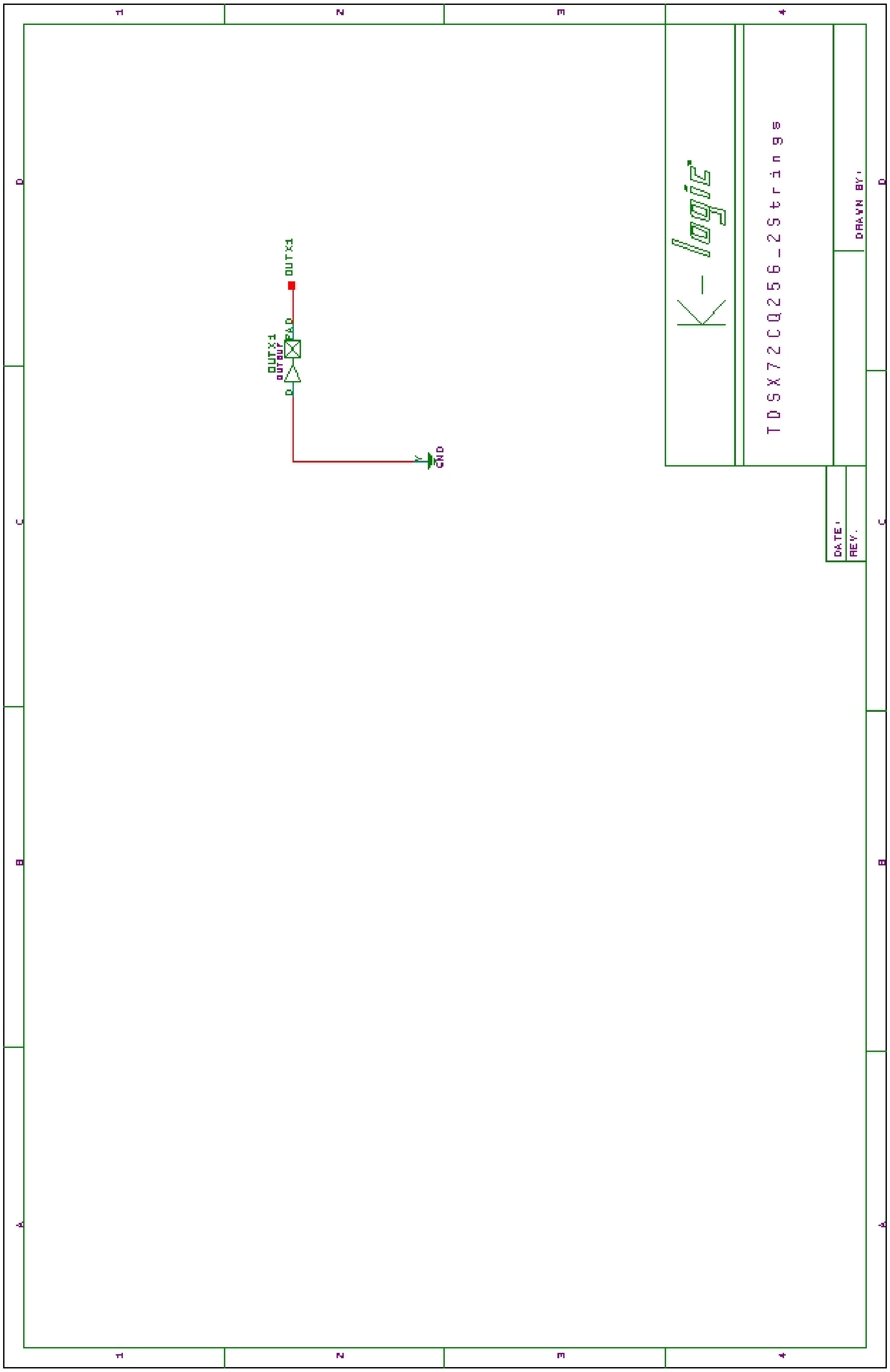

ORC
ANDC
ANDP
ORP
Q
D
RST
CLK
DFF1B
DFC1B
PRE
CLR
K-logic
DATE:
REV:
DRAWN BY:


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
OUTBUF
INBUF
HCLKBUF
DAH
CLOCKH
RESETH
FFINH


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
INBUF
RESETCNTRH
ENCNTRH
CNTRLDH


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since pin 127 is N/C on SX16 will have to make pin 127 on the SX32 pattern
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV:
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN


OUTX1
PAD
OUTBUF
D
GND
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.