Actel

TOTAL IONIZING DOSE TEST REPORT

No. 07T-RTAX2000S-D2S8N5
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I. Summary Table

Parameter	Tolerance
1. Functionality	Passed 300 krad(SiO_2)
2. Standby Power Supply Current (I_{CCA}/I_{CCI})	Passed 200 krad(SiO_2)
3. Input Threshold (V_{TIL}/V_{IH})	Passed 300 krad(SiO_2)
4. Output Threshold (V_{OL}/V_{OH})	Passed 300 krad(SiO_2)
5. Propagation Delay	Passed 300 krad(SiO_2) for ±10% degradation criterion
6. Transition Characteristic	Passed 300 krad(SiO_2)

II. Total Ionizing Dose (TID) Testing

The design of the following testing is based on an extensive, published database accumulated from the TID testing of many generations of antifuse-based FPGAs; the link of the database is in below.

http://www.actel.com/products/milaero/hireldata.aspx#tid

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. Each input is grounded during irradiation and annealing.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000S
Package	CG624
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	rtax2000_CG624_Top
Die Lot Number	D2S8N5
Quantity Tested	4
Serial Number	300 krad(SiO_2): 3853, 3859 200 krad(SiO_2): 3916, 3931
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Annealing Bias V_{CCI}/V_{CCA}	Static at 3.3 V/1.5 V
IO Configuration	Single ended: LVTTL Differential pair: LVPECL

B. Test Method

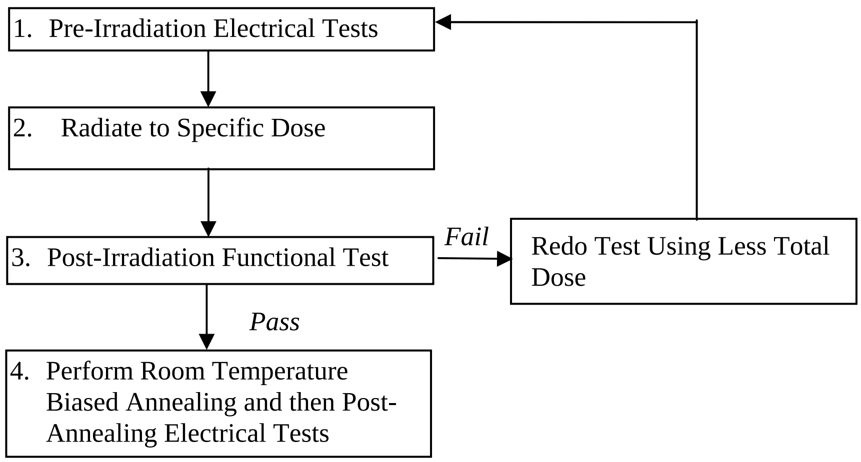

Figure 1 Parametric test flow chart

The test method basically is in compliance with the military standard TM1019.6. Figure 1 is the flow chart of the testing sequence. The accelerated annealing test in section 3.12 is not performed lot-to-lot. This is because for a deep-submicron CMOS technology used by the RTAXS product, the adverse effects due to interface state at the gate SiO_2/Si interface are negligible. The function of commercial non-irradiated transistors would be unreliable if the degradation of interface plays an important role. In other words, the SiO_2/Si interface in deep submicron CMOS transistors has to be radiation hard for even commercial applications. Thus the dominant annealing effect in RTAXS device is the reduction of trapped holes in the SiO_2; this basically alleviates the radiation effects on the DUT. Separate report on the accelerated annealing test will be provided to justify the omission of it in the lot testing; the justification testing will follow section 3.12.1.b.5.

Section 3.11 extended room temperature anneal test is also applied; room temperature annealing for 5 days was done on each device before the final parameter measurements.

C. Logic Design and Electrical Parameter Measurements

The DUT uses a high utilization generic design, rtax2000_CG624_Top, for testing total dose effects. These logic designs are described in the following subsections. Figure 2 shows the block diagram and the Verilog file (rtax2000_CG624_Top.v) is in the link:

http://www.actel.com/products/milaero/hireldata.aspx#tid

Generally, the functional test is performed on every design; most inputs are tested for threshold voltage and leakage current, including global clocks; the standby I_{CC} includes I_{CCI} and I_{CCA}. Except propagation delay and the transition characteristic, which is measured on the output O_BS, all other parameter measurements are done on a tester. Also note that, due to logistics limitation, the post-irradiation but pre-room-temperature-annealing functional test is performed on bench; the tested designs are shift registers and long buffer string, which are design 5 and 6 described in the following.

1. Embedded SRAM

This design is to test the function of the embedded SRAM. It uses all the RAM blocks available in the DUT. This design enables an automatic testing sequence that every bit is written and then read. Any error will be reported as a signal in the output.

2. Unidirectional LVTTL Input and Output

This is for testing radiation effects on unidirectional input and output threshold, leakage, and buffer fan-out. There are 3 sub-designs: a) a logic-core buffer with 8 fan-outs; b) a logic-core buffer with 3 fan-outs; c) 6 channels of input buffer directly connected to output buffer without core logic. LVTTL is used because it is the worst case among all the single-ended standards.

3. Bidirectional LVTTL IO

This design is for testing the radiation effects on the input/output characteristic of the bidirectional IO. There are 7 channels of bidirectional IO for radiation effects testing.

4. LVPECL Input

This design is for testing the radiation effects on the LVPECL differential inputs. 3.3V-LVPECL is considered the worst case differential input standard in the DUT. There are 7 channels.

5. Shift Registers

This design is to test the radiation effects on the function of flip-flops, which are configured R-Cells. There are 4 shift registers and each using a different global clock; one has 3,584 bits and the other three each has 2,048 bits.

6. Long Buffer String

This design is to measure the radiation effects on the propagation delay. The input of the design using a clock feeding a toggle flip-flop to generate a checkerboard signal; this signal is then fed into a buffer string with 10,000 stages. The time delay between the input clock edge at CLOCK_IN and the output switching due to this clock edge at O_BS is defined as propagation delay high to low (T_{pdhl}) or low to high (T_{pdlh}); the percentage change of the average of T_{pdhl} and T_{pdlh} is used to determine the radiation effects. A more than 10% of propagation change is considered as failure.

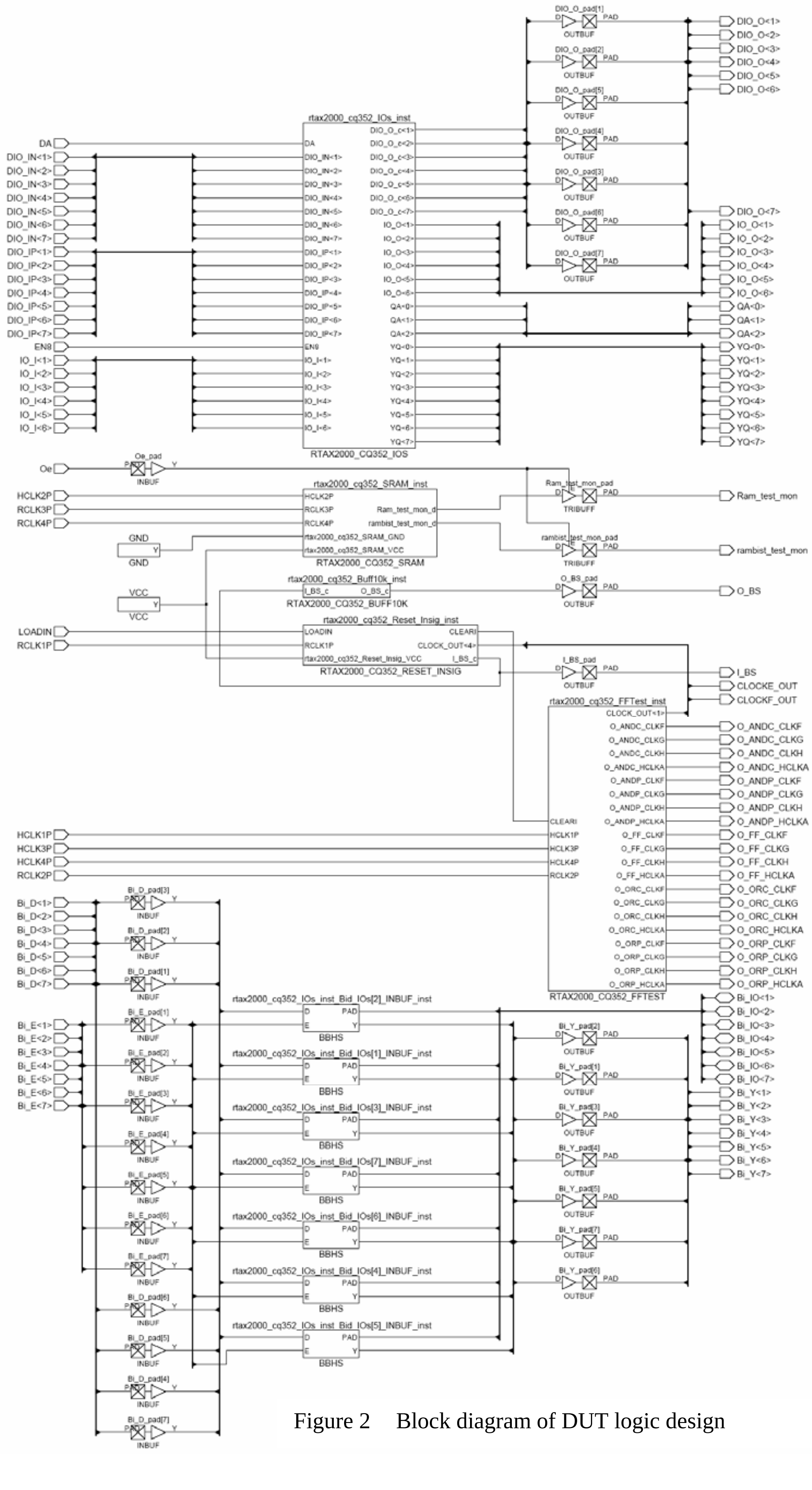

Figure 2 Block diagram of DUT logic design

III. Test Results

A. Functional Test

Every DUT passed the pre-irradiation and post-annealing functional tests on the tester; it also passed post-irradiation test on-bench.

B. Standby Power Supply Current (I_{CCA} and I_{CCI})

Figure 3-8 show the in-flux standby I_{CCA} and I_{CCI} versus total dose of every DUT.

In compliance with TM1019.6 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing I_{CC} in this test is defined as the addition of highest I_{CCI}, I_{CCDA} and $I_{CCDIFFA}$ values in Table 2-4 of the RTAXS spec sheet:

http://www.actel.com/documents/RTAXS_DS.pdf

Thus for I_{CCA}, the PIPL is 500 mA; the PIPL of I_{CCI} equals to 35+10+3.13×7 = 66.91(mA). Note that there are 7 pairs of differential LVPECL inputs in each DUT.

Table 2 summarizes the pre-irradiation, post-irradiation and post-annealing I_{CC} data: the post-annealing I_{CCA} of every DUT pass the PIPL easily; the post-annealing I_{CCI} of DUTs irradiated to 200 krad(SiO_2) all pass the PIPL, while the I_{CCI} of DUTs irradiated to 300 krad(SiO_2) all exceed the PIPL.

Table 2 Pre-irradiation, Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose krad (SiO_2)	I_{CCA} (mA)			I_{CCI} (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
3853	300	4.38	30	5.1	25.5	255	144
3859	300	4.6	28	3.6	25.6	256	148
3916	200	4.0	3.59	3.6	25.2	89	43.2
3931	200	4.5	3.5	4.4	24.4	99	46.5

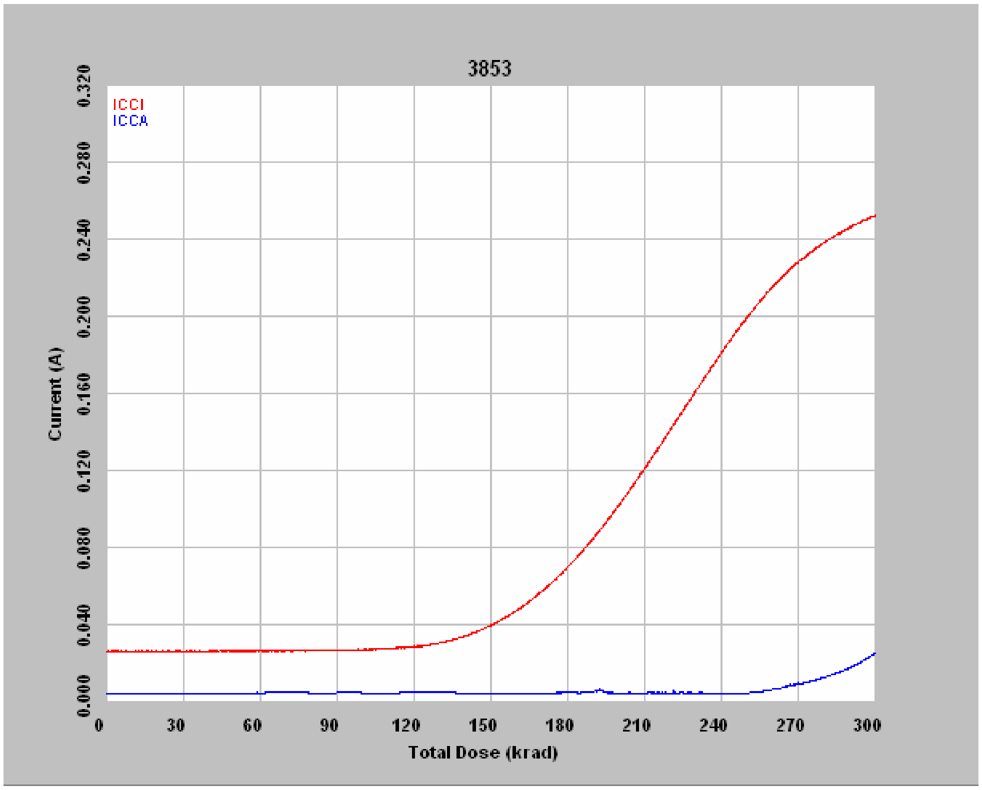

Figure 3 DUT 3853 in-flux I_{CCA} and I_{CCI}. The spikes are due to bad contacts.

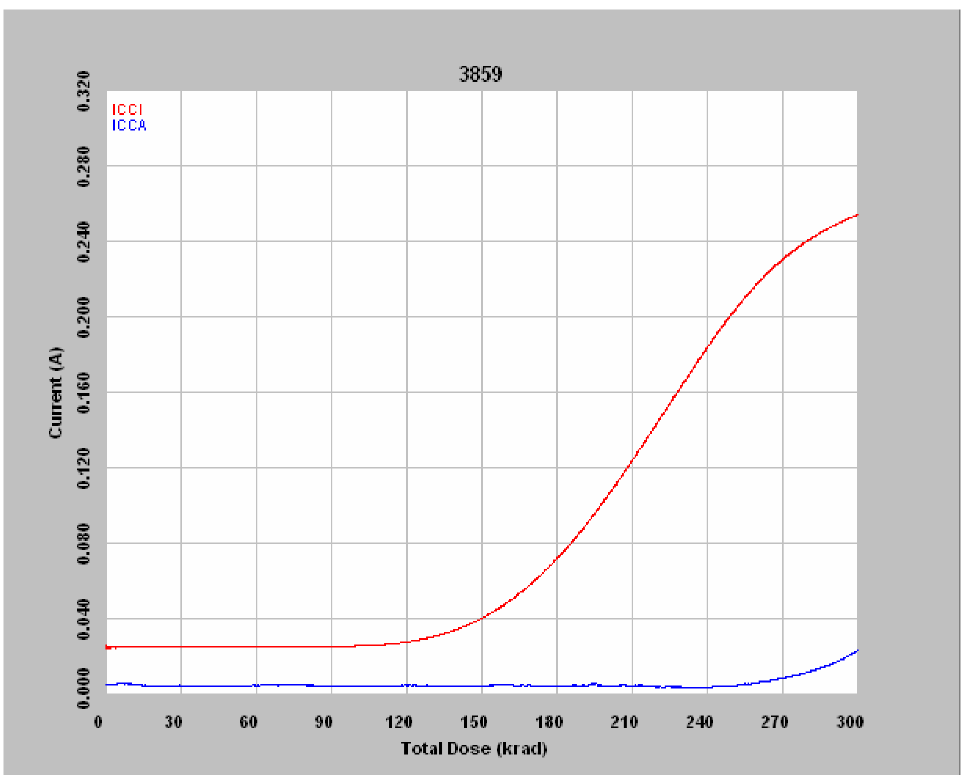

Figure 4 DUT 3859 in-flux I_{CCA} and I_{CCI}

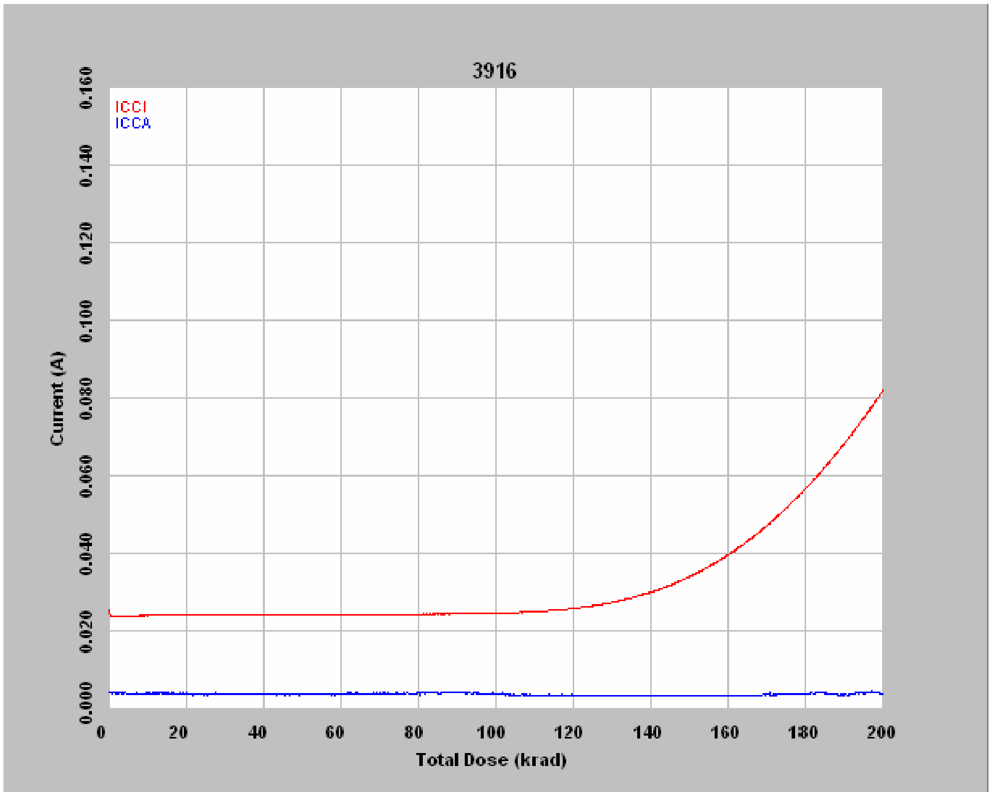

Figure 5 DUT 3916 in-flux I_{CCA} and I_{CCI}

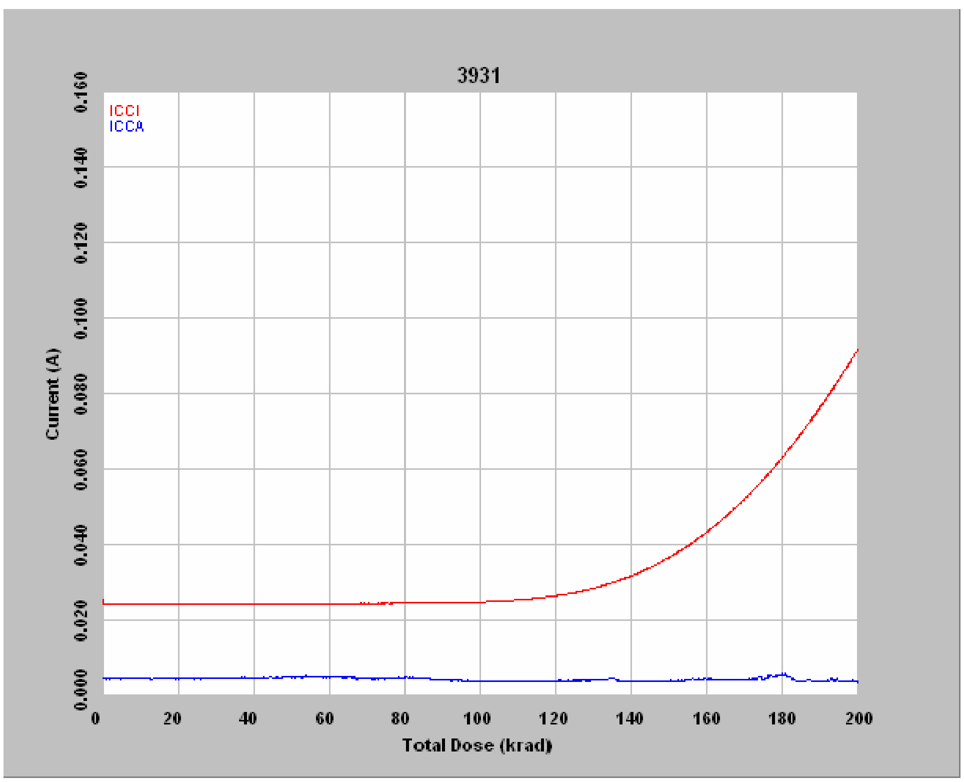

Figure 6 DUT 3931 in-flux I_{CCA} and I_{CCI}

C. Single-Ended V_{IL}/V_{IH} and I_{IL}/I_{IH}

Table 3 displays the pre-irradiation and post-annealing single-ended V_{IL}; every data in this table passes the spec. Table 4 displays the pre-irradiation and post-annealing single-ended V_{IH}; every data in this table passes the spec.

Table 5 displays the pre-irradiation and post-annealing single-ended I_{IL}; every data in the table passes the spec. Table 6 displays the pre-irradiation and post-annealing single-ended I_{IH}; every data in the table passes the spec. The PIPL for both I_{IL} and I_{IH} is 5 μA.

Table 3a

DUT		**3853**		**3859**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.385	1.375	1.385	1.38
bi_levels_vil	Bi_D_6	1.375	1.365	1.375	1.365
bi_levels_vil	Bi_D_5	1.38	1.37	1.375	1.365
bi_levels_vil	Bi_D_4	1.385	1.375	1.38	1.37
bi_levels_vil	Bi_D_3	1.38	1.37	1.385	1.375
bi_levels_vil	Bi_D_2	1.375	1.365	1.375	1.365
bi_levels_vil	Bi_D_1	1.375	1.365	1.375	1.365
bi_levels_vil	DA	1.38	1.385	1.385	1.385
bi_levels_vil	EN8	1.355	1.355	1.36	1.355
bi_levels_vil	IO_I_6	1.365	1.36	1.365	1.36
bi_levels_vil	IO_I_5	1.355	1.36	1.355	1.36
bi_levels_vil	IO_I_4	1.405	1.395	1.4	1.4
bi_levels_vil	IO_I_3	1.4	1.4	1.4	1.395
bi_levels_vil	IO_I_2	1.405	1.4	1.41	1.4
bi_levels_vil	IO_I_1	1.4	1.39	1.4	1.4
bi_levels_vil	RCLK1P	1.44	1.435	1.44	1.43
bi_levels_vil	RCLK2P	1.44	1.43	1.44	1.435

Table 3b

DUT		**3916**		**3931**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	Bi_D_7	1.395	1.385	1.385	1.38
bi_levels_vil	Bi_D_6	1.38	1.37	1.375	1.365
bi_levels_vil	Bi_D_5	1.385	1.375	1.38	1.37
bi_levels_vil	Bi_D_4	1.385	1.38	1.385	1.375
bi_levels_vil	Bi_D_3	1.385	1.38	1.38	1.375
bi_levels_vil	Bi_D_2	1.38	1.375	1.375	1.365
bi_levels_vil	Bi_D_1	1.38	1.375	1.38	1.37
bi_levels_vil	DA	1.39	1.385	1.385	1.385
bi_levels_vil	EN8	1.355	1.355	1.355	1.355
bi_levels_vil	IO_I_6	1.37	1.365	1.37	1.365
bi_levels_vil	IO_I_5	1.36	1.365	1.355	1.365
bi_levels_vil	IO_I_4	1.41	1.405	1.41	1.405
bi_levels_vil	IO_I_3	1.39	1.4	1.4	1.385
bi_levels_vil	IO_I_2	1.41	1.405	1.41	1.405
bi_levels_vil	IO_I_1	1.405	1.395	1.4	1.4
bi_levels_vil	RCLK1P	1.44	1.435	1.435	1.43
bi_levels_vil	RCLK2P	1.445	1.435	1.435	1.43

Table 4a

DUT		3853		3859	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.385	1.375	1.385	1.375
bi_levels_vih	Bi_D_6	1.39	1.385	1.39	1.38
bi_levels_vih	Bi_D_5	1.39	1.38	1.385	1.375
bi_levels_vih	Bi_D_4	1.385	1.375	1.38	1.37
bi_levels_vih	Bi_D_3	1.395	1.385	1.39	1.385
bi_levels_vih	Bi_D_2	1.39	1.38	1.39	1.385
bi_levels_vih	Bi_D_1	1.39	1.375	1.385	1.375
bi_levels_vih	DA	1.4	1.395	1.405	1.4
bi_levels_vih	EN8	1.42	1.415	1.415	1.41
bi_levels_vih	IO_I_6	1.425	1.415	1.425	1.42
bi_levels_vih	IO_I_5	1.44	1.435	1.42	1.44
bi_levels_vih	IO_I_4	1.4	1.395	1.4	1.395
bi_levels_vih	IO_I_3	1.41	1.405	1.41	1.4
bi_levels_vih	IO_I_2	1.4	1.39	1.4	1.395
bi_levels_vih	IO_I_1	1.405	1.4	1.405	1.4
bi_levels_vih	RCLK1P	1.435	1.425	1.43	1.425
bi_levels_vih	RCLK2P	1.44	1.425	1.44	1.43

Table 4b

DUT		3916		3931	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	Bi_D_7	1.39	1.385	1.385	1.38
bi_levels_vih	Bi_D_6	1.395	1.39	1.39	1.385
bi_levels_vih	Bi_D_5	1.395	1.385	1.39	1.375
bi_levels_vih	Bi_D_4	1.385	1.38	1.385	1.375
bi_levels_vih	Bi_D_3	1.4	1.395	1.395	1.39
bi_levels_vih	Bi_D_2	1.395	1.39	1.39	1.385
bi_levels_vih	Bi_D_1	1.39	1.385	1.39	1.385
bi_levels_vih	DA	1.405	1.405	1.4	1.405
bi_levels_vih	EN8	1.44	1.44	1.415	1.41
bi_levels_vih	IO_I_6	1.43	1.43	1.43	1.415
bi_levels_vih	IO_I_5	1.445	1.425	1.42	1.44
bi_levels_vih	IO_I_4	1.405	1.4	1.405	1.4
bi_levels_vih	IO_I_3	1.415	1.41	1.415	1.405
bi_levels_vih	IO_I_2	1.405	1.4	1.405	1.4
bi_levels_vih	IO_I_1	1.41	1.405	1.41	1.405
bi_levels_vih	RCLK1P	1.435	1.425	1.43	1.42
bi_levels_vih	RCLK2P	1.44	1.43	1.435	1.43

Table 5a

DUT		3853				3859			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIL_Inputs_Max_	Bi_D_1	121.6455	pA	-1.5525	nA	-296.886	pA	-3.8544	nA
IIL_Inputs_Max_	Bi_D_2	3.8884	nA	1.168	nA	2.4236	nA	330.9113	pA
IIL_Inputs_Max_	Bi_D_3	1.5865	nA	540.1771	pA	1.168	nA	2.005	nA
IIL_Inputs_Max_	Bi_D_4	-3.6357	nA	-4.2637	nA	-3.4264	nA	-3.6357	nA
IIL_Inputs_Max_	Bi_D_5	-914.6662	pA	-1.3333	nA	-1.3333	nA	-1.7519	nA
IIL_Inputs_Max_	Bi_D_6	-1.3	nA	-3.3927	nA	-4.0205	nA	-5.6947	nA
IIL_Inputs_Max_	Bi_D_7	-3.4485	nA	-6.1713	nA	-3.0296	nA	-6.1713	nA
IIL_Inputs_Max_	Bi_E_1	-3.2391	nA	-1.773	nA	-1.9824	nA	-1.5636	nA
IIL_Inputs_Max_	Bi_E_2	-1.9824	nA	-3.2391	nA	-2.4013	nA	-1.1447	nA
IIL_Inputs_Max_	Bi_E_3	-1.773	nA	-725.793	pA	-2.4013	nA	-1.1447	nA
IIL_Inputs_Max_	Bi_E_4	-3.2391	nA	-725.793	pA	-2.6108	nA	-2.4013	nA
IIL_Inputs_Max_	Bi_E_5	-3.2391	nA	-1.773	nA	1.3686	nA	-2.8202	nA
IIL_Inputs_Max_	Bi_E_6	-2.4013	nA	-1.3541	nA	-1.5636	nA	-306.911	pA
IIL_Inputs_Max_	Bi_E_7	-306.9113	pA	-1.9824	nA	-2.4013	nA	-2.4013	nA
IIL_Inputs_Max_	DA	-3.3153	nA	-6.0377	nA	-4.1529	nA	-4.9906	nA
IIL_Inputs_Max_	DIO_IN_1	-1.0907	nA	-3.1834	nA	-44.3349	pA	374.2134	pA
IIL_Inputs_Max_	DIO_IN_2	-1.2211	nA	-3.1058	nA	-3.1058	nA	-4.1529	nA
IIL_Inputs_Max_	DIO_IN_3	-3.3153	nA	-3.5247	nA	-2.4776	nA	-3.5247	nA
IIL_Inputs_Max_	DIO_IN_4	583.4875	pA	-1.5093	nA	-881.432	pA	-2.3464	nA
IIL_Inputs_Max_	DIO_IN_5	-2.687	nA	-3.1058	nA	-3.7341	nA	-592.809	pA
IIL_Inputs_Max_	DIO_IN_6	-3.7341	nA	-4.9906	nA	-3.5247	nA	-3.1058	nA
IIL_Inputs_Max_	DIO_IN_7	-3.3153	nA	-3.3153	nA	-1.0116	nA	-1.4305	nA
IIL_Inputs_Max_	DIO_IP_1	2.0484	nA	-1.9278	nA	1.2113	nA	-1.5093	nA
IIL_Inputs_Max_	DIO_IP_2	-2.687	nA	-3.9435	nA	-1.4305	nA	-1.6399	nA
IIL_Inputs_Max_	DIO_IP_3	-462.8832	pA	-672.1573	pA	374.2134	pA	1.002	nA
IIL_Inputs_Max_	DIO_IP_4	-4.1529	nA	-3.7341	nA	-2.4776	nA	-2.687	nA
IIL_Inputs_Max_	DIO_IP_5	-2.8964	nA	-2.2682	nA	-1.2211	nA	-2.0587	nA
IIL_Inputs_Max_	DIO_IP_6	-2.8964	nA	-1.4305	nA	-2.8964	nA	-2.8964	nA
IIL_Inputs_Max_	DIO_IP_7	-1.8493	nA	-1.4305	nA	-1.0116	nA	-2.687	nA
IIL_Inputs_Max_	EN8	-2.2682	nA	-1.2211	nA	-1.4305	nA	-1.8493	nA
IIL_Inputs_Max_	HCLK1P	-516.3522	pA	-3.4485	nA	-2.4013	nA	-2.4013	nA
IIL_Inputs_Max_	HCLK2P	1.2113	nA	583.4875	pA	1.002	nA	374.2134	pA
IIL_Inputs_Max_	HCLK3P	4.9348	nA	3.4699	nA	2.005	nA	1.5865	nA
IIL_Inputs_Max_	HCLK4P	-914.6662	pA	-914.6662	pA	-1.3333	nA	-1.9612	nA
IIL_Inputs_Max_	IO_I_1	164.9393	pA	-1.9278	nA	-672.157	pA	2.0484	nA
IIL_Inputs_Max_	IO_I_2	2.8421	nA	2.4236	nA	1.3772	nA	958.7088	pA
IIL_Inputs_Max_	IO_I_3	164.9393	pA	-672.1573	pA	-881.432	pA	-1.7185	nA
IIL_Inputs_Max_	IO_I_4	2.6328	nA	3.4699	nA	2.2143	nA	1.7958	nA
IIL_Inputs_Max_	IO_I_5	374.2134	pA	-44.3349	pA	164.9393	pA	164.9393	pA
IIL_Inputs_Max_	IO_I_6	-3.5247	nA	-592.8091	pA	-5.6189	nA	-802.229	pA
IIL_Inputs_Max_	LOADIN	-4.2481	nA	-5.7152	nA	-5.5056	nA	-6.5535	nA

IIL_Inputs_Max_	RCLK1P	374.2134	pA	-44.3349	pA	164.9393	pA	583.4875	pA
IIL_Inputs_Max_	RCLK2P	-77.4112	pA	1.3878	nA	-496.039	pA	-2.5892	nA
IIL_Inputs_Max_	RCLK3P	1.3772	nA	2.005	nA	4.9348	nA	4.307	nA
IIL_Inputs_Max_	RCLK4P	-3.4485	nA	-2.1919	nA	-1.773	nA	-1.773	nA

Table 5b

DUT		3916				3931			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIL_Inputs_Max_	Bi_D_1	-1.5525	nA	-506.152	pA	-2.8081	nA	-1.5525	nA
IIL_Inputs_Max_	Bi_D_2	540.1771	pA	1.7958	nA	2.005	nA	-87.6203	pA
IIL_Inputs_Max_	Bi_D_3	1.3772	nA	1.7958	nA	1.5865	nA	1.5865	nA
IIL_Inputs_Max_	Bi_D_4	-5.7289	nA	-4.8916	nA	-5.3103	nA	-4.8916	nA
IIL_Inputs_Max_	Bi_D_5	-2.7985	nA	-3.4264	nA	-2.1705	nA	-4.0544	nA
IIL_Inputs_Max_	Bi_D_6	-4.2298	nA	-4.8576	nA	-4.0205	nA	-5.2762	nA
IIL_Inputs_Max_	Bi_D_7	-3.658	nA	-6.3807	nA	-5.5429	nA	-2.6108	nA
IIL_Inputs_Max_	Bi_E_1	-3.2391	nA	-2.6108	nA	-3.2391	nA	-3.2391	nA
IIL_Inputs_Max_	Bi_E_2	-1.3541	nA	-2.8202	nA	-2.4013	nA	-3.4485	nA
IIL_Inputs_Max_	Bi_E_3	-3.2391	nA	-2.8202	nA	-2.8202	nA	-1.773	nA
IIL_Inputs_Max_	Bi_E_4	-1.9824	nA	-1.773	nA	-2.4013	nA	-1.3541	nA
IIL_Inputs_Max_	Bi_E_5	-1.1447	nA	-306.911	pA	-1.9824	nA	-1.9824	nA
IIL_Inputs_Max_	Bi_E_6	-2.1919	nA	-2.1919	nA	-3.8674	nA	-3.2391	nA
IIL_Inputs_Max_	Bi_E_7	-2.4013	nA	-3.2391	nA	-725.793	pA	-1.5636	nA
IIL_Inputs_Max_	DA	-4.7812	nA	-3.5247	nA	-4.3624	nA	-5.2	nA
IIL_Inputs_Max_	DIO_IN_1	-1.9278	nA	-3.602	nA	-44.3349	pA	-2.7649	nA
IIL_Inputs_Max_	DIO_IN_2	-2.687	nA	-3.7341	nA	-2.4776	nA	-3.1058	nA
IIL_Inputs_Max_	DIO_IN_3	-2.687	nA	-3.7341	nA	-3.7341	nA	-4.5718	nA
IIL_Inputs_Max_	DIO_IN_4	374.2134	pA	-3.1834	nA	-4.0205	nA	-462.883	pA
IIL_Inputs_Max_	DIO_IN_5	-2.0587	nA	-2.2682	nA	-2.2682	nA	-2.2682	nA
IIL_Inputs_Max_	DIO_IN_6	-802.229	pA	-2.0587	nA	-2.8964	nA	-3.3153	nA
IIL_Inputs_Max_	DIO_IN_7	-3.1058	nA	-2.0587	nA	-2.8964	nA	-2.687	nA
IIL_Inputs_Max_	DIO_IP_1	-253.609	pA	-1.0907	nA	-2.3464	nA	-3.8113	nA
IIL_Inputs_Max_	DIO_IP_2	-2.2682	nA	-2.0587	nA	-1.2211	nA	-3.5247	nA
IIL_Inputs_Max_	DIO_IP_3	-2.9742	nA	-672.157	pA	-44.3349	pA	-2.9742	nA
IIL_Inputs_Max_	DIO_IP_4	-2.4776	nA	-2.2682	nA	-3.9435	nA	-2.4776	nA
IIL_Inputs_Max_	DIO_IP_5	-3.3153	nA	-1.6399	nA	-2.0587	nA	-3.5247	nA
IIL_Inputs_Max_	DIO_IP_6	-2.8964	nA	-2.687	nA	-3.9435	nA	-3.1058	nA
IIL_Inputs_Max_	DIO_IP_7	-1.2211	nA	-1.0116	nA	-1.6399	nA	-592.809	pA
IIL_Inputs_Max_	EN8	-383.389	pA	-1.4305	nA	-802.229	pA	-3.1058	nA
IIL_Inputs_Max_	HCLK1P	-1.3541	nA	-1.3541	nA	-1.773	nA	-3.658	nA
IIL_Inputs_Max_	HCLK2P	-2.3464	nA	-1.3	nA	583.4875	pA	-1.0907	nA
IIL_Inputs_Max_	HCLK3P	3.6792	nA	2.8421	nA	4.7255	nA	4.5162	nA
IIL_Inputs_Max_	HCLK4P	-2.5892	nA	-3.8451	nA	-1.124	nA	-2.3799	nA
IIL_Inputs_Max_	IO_I_1	-2.1371	nA	792.7617	pA	1.4206	nA	-1.7185	nA
IIL_Inputs_Max_	IO_I_2	2.6328	nA	2.6328	nA	1.7958	nA	2.005	nA
IIL_Inputs_Max_	IO_I_3	-881.432	pA	-881.432	pA	164.9393	pA	-2.9742	nA
IIL_Inputs_Max_	IO_I_4	2.6328	nA	1.168	nA	2.8421	nA	1.5865	nA
IIL_Inputs_Max_	IO_I_5	1.2113	nA	164.9393	pA	374.2134	pA	583.4875	pA
IIL_Inputs_Max_	IO_I_6	-2.2682	nA	-173.969	pA	-2.8964	nA	-592.809	pA
IIL_Inputs_Max_	LOADIN	-6.763	nA	-5.0864	nA	-6.3439	nA	-6.763	nA

IIL_Inputs_Max_	RCLK1P	-672.157	pA	-1.7185	nA	-881.432	pA	-1.5093	nA
IIL_Inputs_Max_	RCLK2P	-1.124	nA	-2.3799	nA	-1.3333	nA	-2.7985	nA
IIL_Inputs_Max_	RCLK3P	2.005	nA	-87.6203	pA	749.443	pA	1.7958	nA
IIL_Inputs_Max_	RCLK4P	-1.9824	nA	-725.793	pA	-1.773	nA	-2.1919	nA

Table 5c

DUT		**3853**				**3859**			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIL_BiOuts_Max_	Bi_IO_1	-4.4391	nA	-5.0669	nA	-2.1371	nA	-4.2298	nA
IIL_BiOuts_Max_	Bi_IO_2	-5.5196	nA	-5.1009	nA	-3.8451	nA	-5.9382	nA
IIL_BiOuts_Max_	Bi_IO_3	-705.3524	pA	-1.9612	nA	-1.3333	nA	-1.9612	nA
IIL_BiOuts_Max_	Bi_IO_4	-1.0907	nA	-2.1371	nA	-881.432	pA	-672.157	pA
IIL_BiOuts_Max_	Bi_IO_5	-3.4264	nA	-2.3799	nA	-2.1705	nA	-3.2171	nA
IIL_BiOuts_Max_	Bi_IO_6	-4.0385	nA	-3.6194	nA	-2.5715	nA	-5.0864	nA
IIL_BiOuts_Max_	Bi_IO_7	-2.1523	nA	-4.2481	nA	-3.4098	nA	-3.829	nA

Table 5d

DUT		**3916**				**3931**			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIL_BiOuts_Max_	Bi_IO_1	-4.0205	nA	-5.0669	nA	-1.3	nA	-3.1834	nA
IIL_BiOuts_Max_	Bi_IO_2	-1.9612	nA	-4.473	nA	-1.7519	nA	-5.1009	nA
IIL_BiOuts_Max_	Bi_IO_3	759.8438	pA	-3.0078	nA	-1.7519	nA	-4.473	nA
IIL_BiOuts_Max_	Bi_IO_4	-3.1834	nA	-4.4391	nA	-1.3	nA	-1.3	nA
IIL_BiOuts_Max_	Bi_IO_5	-1.5426	nA	-4.473	nA	131.9025	pA	-2.3799	nA
IIL_BiOuts_Max_	Bi_IO_6	-5.0864	nA	-2.9906	nA	-3.6194	nA	-2.5715	nA
IIL_BiOuts_Max_	Bi_IO_7	-1.9427	nA	-6.3439	nA	-2.5715	nA	-4.8768	nA

Table 6a

DUT		3853				3859			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIH_Inputs_Max_	Bi_D_1	7.0274	nA	8.283	nA	7.6552	nA	8.0737	nA
IIH_Inputs_Max_	Bi_D_2	5.144	nA	6.8182	nA	5.3533	nA	6.1904	nA
IIH_Inputs_Max_	Bi_D_3	3.6792	nA	4.307	nA	4.307	nA	4.307	nA
IIH_Inputs_Max_	Bi_D_4	2.4344	nA	1.3878	nA	2.225	nA	1.8064	nA
IIH_Inputs_Max_	Bi_D_5	550.53	pA	550.53	pA	1.1785	nA	-286.725	pA
IIH_Inputs_Max_	Bi_D_6	4.9782	nA	3.7226	nA	6.6524	nA	5.1875	nA
IIH_Inputs_Max_	Bi_D_7	2.2064	nA	2.8347	nA	3.463	nA	2.6253	nA
IIH_Inputs_Max_	Bi_E_1	740.2928	pA	1.5781	nA	-516.352	pA	1.5781	nA
IIH_Inputs_Max_	Bi_E_2	2.4158	nA	530.852	pA	1.3686	nA	-1.1447	nA
IIH_Inputs_Max_	Bi_E_3	4.0913	nA	1.5781	nA	530.852	pA	321.4112	pA
IIH_Inputs_Max_	Bi_E_4	2.6253	nA	-516.3522	pA	-1.3541	nA	-516.352	pA
IIH_Inputs_Max_	Bi_E_5	-725.793	pA	1.1592	nA	740.2928	pA	-1.773	nA
IIH_Inputs_Max_	Bi_E_6	-306.9113	pA	949.7336	pA	-1.773	nA	1.5781	nA
IIH_Inputs_Max_	Bi_E_7	2.4158	nA	530.852	pA	-516.352	pA	530.852	pA
IIH_Inputs_Max_	DA	1.5014	nA	1.0826	nA	2.5485	nA	2.3391	nA
IIH_Inputs_Max_	DIO_IN_1	1.8391	nA	3.9319	nA	3.5133	nA	3.5133	nA
IIH_Inputs_Max_	DIO_IN_2	-802.2291	pA	2.3391	nA	-1.2211	nA	2.5485	nA
IIH_Inputs_Max_	DIO_IN_3	873.1309	pA	-1.6399	nA	-173.969	pA	1.7108	nA
IIH_Inputs_Max_	DIO_IN_4	3.9319	nA	-1.0907	nA	2.8855	nA	583.4875	pA
IIH_Inputs_Max_	DIO_IN_5	1.292	nA	1.292	nA	-592.809	pA	-1.0116	nA
IIH_Inputs_Max_	DIO_IN_6	1.5014	nA	1.292	nA	1.292	nA	663.7109	pA
IIH_Inputs_Max_	DIO_IN_7	1.0826	nA	244.8709	pA	663.7109	pA	1.0826	nA
IIH_Inputs_Max_	DIO_IP_1	1.4206	nA	-44.3349	pA	1.4206	nA	3.7226	nA
IIH_Inputs_Max_	DIO_IP_2	663.7109	pA	-592.8091	pA	-1.0116	nA	663.7109	pA
IIH_Inputs_Max_	DIO_IP_3	2.8855	nA	1.6299	nA	1.6299	nA	2.467	nA
IIH_Inputs_Max_	DIO_IP_4	1.0826	nA	-592.8091	pA	-592.809	pA	-802.229	pA
IIH_Inputs_Max_	DIO_IP_5	454.2909	pA	-1.2211	nA	2.1297	nA	663.7109	pA
IIH_Inputs_Max_	DIO_IP_6	-173.9691	pA	35.4509	pA	1.5014	nA	35.4509	pA
IIH_Inputs_Max_	DIO_IP_7	1.5014	nA	-1.0116	nA	454.2909	pA	663.7109	pA
IIH_Inputs_Max_	EN8	1.9202	nA	454.2909	pA	1.292	nA	873.1309	pA
IIH_Inputs_Max_	HCLK1P	-1.5636	nA	-306.9113	pA	-516.352	pA	-935.234	pA
IIH_Inputs_Max_	HCLK2P	2.6762	nA	1.8391	nA	1.2113	nA	2.2577	nA
IIH_Inputs_Max_	HCLK3P	4.0977	nA	3.4699	nA	5.5626	nA	3.4699	nA
IIH_Inputs_Max_	HCLK4P	1.1785	nA	-2.3799	nA	131.9025	pA	-1.9612	nA
IIH_Inputs_Max_	IO_I_1	3.5133	nA	2.6762	nA	3.9319	nA	1.4206	nA
IIH_Inputs_Max_	IO_I_2	4.307	nA	4.5162	nA	3.8884	nA	3.6792	nA
IIH_Inputs_Max_	IO_I_3	3.3041	nA	2.467	nA	1.6299	nA	1.2113	nA
IIH_Inputs_Max_	IO_I_4	5.5626	nA	5.7718	nA	5.144	nA	5.7718	nA

IIH_Inputs_Max_	IO_I_5	2.6762	nA	792.7617	pA	583.4875	pA	4.1411	nA
IIH_Inputs_Max_	IO_I_6	244.8709	pA	-802.2291	pA	-802.229	pA	663.7109	pA
IIH_Inputs_Max_	LOADIN	1.6201	nA	991.3508	pA	2.668	nA	2.668	nA
IIH_Inputs_Max_	RCLK1P	2.467	nA	792.7617	pA	792.7617	pA	2.2577	nA
IIH_Inputs_Max_	RCLK2P	341.2162	pA	-3.0078	nA	2.6437	nA	-3.6357	nA
IIH_Inputs_Max_	RCLK3P	4.5162	nA	7.4459	nA	3.4699	nA	4.5162	nA
IIH_Inputs_Max_	RCLK4P	1.7875	nA	-306.9113	pA	-306.911	pA	-516.352	pA

Table 6b

DUT		3916				3931			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIH_Inputs_Max_	Bi_D_1	9.7479	nA	8.4923	nA	7.8645	nA	8.283	nA
IIH_Inputs_Max_	Bi_D_2	6.8182	nA	7.4459	nA	4.7255	nA	6.1904	nA
IIH_Inputs_Max_	Bi_D_3	2.6328	nA	7.4459	nA	3.0514	nA	4.0977	nA
IIH_Inputs_Max_	Bi_D_4	969.1575	pA	1.3878	nA	2.6437	nA	1.5971	nA
IIH_Inputs_Max_	Bi_D_5	969.1575	pA	-496.039	pA	-286.725	pA	1.1785	nA
IIH_Inputs_Max_	Bi_D_6	4.3504	nA	4.3504	nA	5.6061	nA	6.4432	nA
IIH_Inputs_Max_	Bi_D_7	3.463	nA	2.6253	nA	2.4158	nA	2.4158	nA
IIH_Inputs_Max_	Bi_E_1	949.7336	pA	1.1592	nA	1.1592	nA	1.3686	nA
IIH_Inputs_Max_	Bi_E_2	2.8347	nA	-935.234	pA	949.7336	pA	1.5781	nA
IIH_Inputs_Max_	Bi_E_3	-306.911	pA	1.7875	nA	1.1592	nA	-97.4705	pA
IIH_Inputs_Max_	Bi_E_4	740.2928	pA	111.9703	pA	1.3686	nA	530.852	pA
IIH_Inputs_Max_	Bi_E_5	1.5781	nA	1.7875	nA	530.852	pA	-97.4705	pA
IIH_Inputs_Max_	Bi_E_6	-935.234	pA	949.7336	pA	111.9703	pA	740.2928	pA
IIH_Inputs_Max_	Bi_E_7	-516.352	pA	321.4112	pA	1.5781	nA	321.4112	pA
IIH_Inputs_Max_	DA	3.805	nA	663.7109	pA	3.1768	nA	2.3391	nA
IIH_Inputs_Max_	DIO_IN_1	2.0484	nA	2.6762	nA	3.0948	nA	2.467	nA
IIH_Inputs_Max_	DIO_IN_2	244.8709	pA	454.2909	pA	-1.0116	nA	244.8709	pA
IIH_Inputs_Max_	DIO_IN_3	244.8709	pA	-2.687	nA	1.0826	nA	663.7109	pA
IIH_Inputs_Max_	DIO_IN_4	1.6299	nA	2.0484	nA	4.3504	nA	2.8855	nA
IIH_Inputs_Max_	DIO_IN_5	-1.4305	nA	-383.389	pA	873.1309	pA	1.0826	nA
IIH_Inputs_Max_	DIO_IN_6	-802.229	pA	1.0826	nA	663.7109	pA	35.4509	pA
IIH_Inputs_Max_	DIO_IN_7	1.0826	nA	1.9202	nA	-1.0116	nA	2.3391	nA
IIH_Inputs_Max_	DIO_IP_1	1.002	nA	2.0484	nA	2.8855	nA	2.6762	nA
IIH_Inputs_Max_	DIO_IP_2	244.8709	pA	-173.969	pA	1.7108	nA	1.292	nA
IIH_Inputs_Max_	DIO_IP_3	3.5133	nA	1.8391	nA	1.8391	nA	1.6299	nA
IIH_Inputs_Max_	DIO_IP_4	-1.0116	nA	-592.809	pA	663.7109	pA	-173.969	pA
IIH_Inputs_Max_	DIO_IP_5	873.1309	pA	1.0826	nA	873.1309	pA	1.0826	nA
IIH_Inputs_Max_	DIO_IP_6	-802.229	pA	454.2909	pA	-383.389	pA	-1.0116	nA
IIH_Inputs_Max_	DIO_IP_7	873.1309	pA	244.8709	pA	35.4509	pA	1.7108	nA
IIH_Inputs_Max_	EN8	-2.0587	nA	2.7579	nA	4.0144	nA	663.7109	pA
IIH_Inputs_Max_	HCLK1P	-306.911	pA	111.9703	pA	2.2064	nA	111.9703	pA

IIH_Inputs_Max_	HCLK2P	3.5133	nA	3.3041	nA	2.6762	nA	792.7617	pA
IIH_Inputs_Max_	HCLK3P	4.307	nA	4.5162	nA	5.144	nA	4.0977	nA
IIH_Inputs_Max_	HCLK4P	-914.666	pA	-2.1705	nA	-1.7519	nA	-1.124	nA
IIH_Inputs_Max_	IO_I_1	1.6299	nA	1.2113	nA	792.7617	pA	2.0484	nA
IIH_Inputs_Max_	IO_I_2	3.4699	nA	5.9811	nA	5.144	nA	4.5162	nA
IIH_Inputs_Max_	IO_I_3	2.8855	nA	1.2113	nA	1.6299	nA	164.9393	pA
IIH_Inputs_Max_	IO_I_4	5.144	nA	4.5162	nA	3.0514	nA	5.3533	nA
IIH_Inputs_Max_	IO_I_5	3.5133	nA	1.8391	nA	583.4875	pA	1.6299	nA
IIH_Inputs_Max_	IO_I_6	-2.0587	nA	2.9673	nA	1.292	nA	454.2909	pA
IIH_Inputs_Max_	LOADIN	2.0392	nA	1.2009	nA	3.2967	nA	2.0392	nA
IIH_Inputs_Max_	RCLK1P	583.4875	pA	1.2113	nA	792.7617	pA	2.467	nA
IIH_Inputs_Max_	RCLK2P	2.0157	nA	-1.9612	nA	-2.1705	nA	-914.666	pA
IIH_Inputs_Max_	RCLK3P	5.144	nA	5.9811	nA	5.5626	nA	4.5162	nA
IIH_Inputs_Max_	RCLK4P	-2.4013	nA	-935.234	pA	-1.3541	nA	-306.911	pA

Table 6c

DUT		**3853**				**3859**			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIH_BiOuts_Max_	Bi_IO_1	3.3041	nA	164.9393	pA	1.2113	nA	374.2134	pA
IIH_BiOuts_Max_	Bi_IO_2	-1.124	nA	131.9025	pA	-1.3333	nA	-1.7519	nA
IIH_BiOuts_Max_	Bi_IO_3	-286.725	pA	-914.6662	pA	-3.0078	nA	-1.5426	nA
IIH_BiOuts_Max_	Bi_IO_4	1.8391	nA	-672.1573	pA	2.8855	nA	2.2577	nA
IIH_BiOuts_Max_	Bi_IO_5	-496.0387	pA	-2.7985	nA	-1.5426	nA	-705.352	pA
IIH_BiOuts_Max_	Bi_IO_6	-475.6976	pA	-475.6976	pA	-2.3619	nA	-1.5236	nA
IIH_BiOuts_Max_	Bi_IO_7	-1.5236	nA	572.1941	pA	-894.854	pA	-1.1044	nA

Table 6d

DUT		**3916**				**3931**			
Parameter	Design	Pre-Irrad		Post-Ann		Pre-Irrad		Post-Ann	
IIH_BiOuts_Max_	Bi_IO_1	792.7617	pA	-253.609	pA	583.4875	pA	374.2134	pA
IIH_BiOuts_Max_	Bi_IO_2	-77.4112	pA	550.53	pA	-1.3333	nA	-2.5892	nA
IIH_BiOuts_Max_	Bi_IO_3	-1.7519	nA	-3.2171	nA	-1.3333	nA	-705.352	pA
IIH_BiOuts_Max_	Bi_IO_4	-1.3	nA	-2.1371	nA	374.2134	pA	1.4206	nA
IIH_BiOuts_Max_	Bi_IO_5	-1.5426	nA	-1.3333	nA	-1.7519	nA	341.2162	pA

IIH_BiOuts_Max_	Bi_IO_6	153.0374	pA	-1.314	nA	-1.5236	nA	-1.314	nA
IIH_BiOuts_Max_	Bi_IO_7	-2.3619	nA	-1.5236	nA	-1.7332	nA	-894.854	pA

D. Differential Input (LVPECL) Threshold Voltage (V_{IL}/V_{IH})

Table 7 and 8 show the pre-irradiation and post-annealing threshold-voltages of the LVPECL input. Every data passes the spec.

Table 7a

DUT		**3853**		**3859**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	110	85	105	75
bi_levels_vil	DIO_IP_6	110	85	105	80
bi_levels_vil	DIO_IP_5	115	90	105	80
bi_levels_vil	DIO_IP_4	100	75	85	60
bi_levels_vil	DIO_IP_3	90	70	90	70
bi_levels_vil	DIO_IP_2	100	75	90	65
bi_levels_vil	DIO_IP_1	75	55	80	60

Table7b

DUT		**3916**		**3931**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vil	DIO_IP_7	100	95	110	105
bi_levels_vil	DIO_IP_6	110	100	110	100
bi_levels_vil	DIO_IP_5	115	105	110	100
bi_levels_vil	DIO_IP_4	80	75	95	85
bi_levels_vil	DIO_IP_3	85	75	85	75
bi_levels_vil	DIO_IP_2	85	75	85	80
bi_levels_vil	DIO_IP_1	90	80	80	75

Table 8a

DUT		3853		3859	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	105	85	100	75
bi_levels_vih	DIO_IP_6	105	85	100	80
bi_levels_vih	DIO_IP_5	110	90	100	75
bi_levels_vih	DIO_IP_4	100	75	80	60
bi_levels_vih	DIO_IP_3	90	65	90	70
bi_levels_vih	DIO_IP_2	95	70	85	60
bi_levels_vih	DIO_IP_1	80	55	85	60

Table 8b

DUT		3916		3931	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vih	DIO_IP_7	100	95	110	100
bi_levels_vih	DIO_IP_6	105	100	105	100
bi_levels_vih	DIO_IP_5	110	100	110	100
bi_levels_vih	DIO_IP_4	80	75	90	85
bi_levels_vih	DIO_IP_3	80	75	85	75
bi_levels_vih	DIO_IP_2	80	75	85	80
bi_levels_vih	DIO_IP_1	90	85	85	75

E. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 9 and 10. Every post-annealing data passes the spec.

Table 9a

DUT		**3853**		**3859**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35
bi_levels_vol	Bi_IO_6	30	35	35	35
bi_levels_vol	Bi_IO_5	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35
bi_levels_vol	Bi_IO_2	35	30	35	35
bi_levels_vol	Bi_IO_1	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25
bi_levels_vol	Bi_Y_3	30	25	30	30
bi_levels_vol	Bi_Y_2	25	25	25	25
bi_levels_vol	Bi_Y_1	30	30	30	30
bi_levels_vol	CLOCKE_OUT	25	20	20	20
bi_levels_vol	CLOCKF_OUT	20	25	25	25
bi_levels_vol	QA_2	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20
bi_levels_vol	QA_0	20	20	20	20

Table 9b

DUT		**3916**		**3931**	
Parameter (mV)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_vol	Bi_IO_7	35	35	35	35
bi_levels_vol	Bi_IO_6	30	35	30	30
bi_levels_vol	Bi_IO_5	35	35	35	35
bi_levels_vol	Bi_IO_4	35	35	35	35
bi_levels_vol	Bi_IO_3	35	35	35	35
bi_levels_vol	Bi_IO_2	35	35	30	30
bi_levels_vol	Bi_IO_1	35	35	35	35
bi_levels_vol	Bi_Y_7	25	25	25	25
bi_levels_vol	Bi_Y_6	25	25	25	25
bi_levels_vol	Bi_Y_5	25	25	25	25
bi_levels_vol	Bi_Y_4	25	25	25	25
bi_levels_vol	Bi_Y_3	30	25	30	25
bi_levels_vol	Bi_Y_2	25	25	25	25
bi_levels_vol	Bi_Y_1	30	25	30	25
bi_levels_vol	CLOCKE_OUT	20	20	20	20
bi_levels_vol	CLOCKF_OUT	25	20	25	25
bi_levels_vol	QA_2	20	20	20	20
bi_levels_vol	QA_1	20	20	20	20
bi_levels_vol	QA_0	20	20	20	20

Table 10a

DUT		**3853**		**3859**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.965	2.97	2.965	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_6	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.975	2.97	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.965	2.97	2.965
bi_levels_voh	QA_1	2.97	2.965	2.97	2.965
bi_levels_voh	QA_0	2.97	2.97	2.97	2.97

Table 10b

DUT		**3916**		**3931**	
Parameter (V)	Design	Pre-Irrad	Post-Ann	Pre-Irrad	Post-Ann
bi_levels_voh	Bi_IO_7	2.97	2.97	2.97	2.97
bi_levels_voh	Bi_IO_6	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_5	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_4	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_3	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_2	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_IO_1	2.965	2.965	2.965	2.965
bi_levels_voh	Bi_Y_7	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_6	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_5	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_4	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_3	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_2	2.98	2.98	2.98	2.98
bi_levels_voh	Bi_Y_1	2.98	2.98	2.98	2.98
bi_levels_voh	CLOCKE_OUT	2.975	2.97	2.975	2.97
bi_levels_voh	CLOCKF_OUT	2.975	2.97	2.975	2.97
bi_levels_voh	QA_2	2.97	2.97	2.97	2.97
bi_levels_voh	QA_1	2.97	2.97	2.97	2.97
bi_levels_voh	QA_0	2.97	2.97	2.97	2.97

F. Propagation Delay

Table 11 lists the pre-irradiation and post-annealing propagation delays. The results show small radiation effects; in any case the percentage change is well below ±10%.

Table 11 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose krad(SiO_2)	Pre-Irradiation (µs)	Post-Annealing (µs)	Degradation
3853	300	7.618	7.599	-0.24%
3859	300	7.501	7.485	-0.21%
3916	200	7.572	7.485	-1.14%
3931	200	7.334	7.239	-1.30%

G. Transition Characteristic

Figures 7 to 14 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not observable.

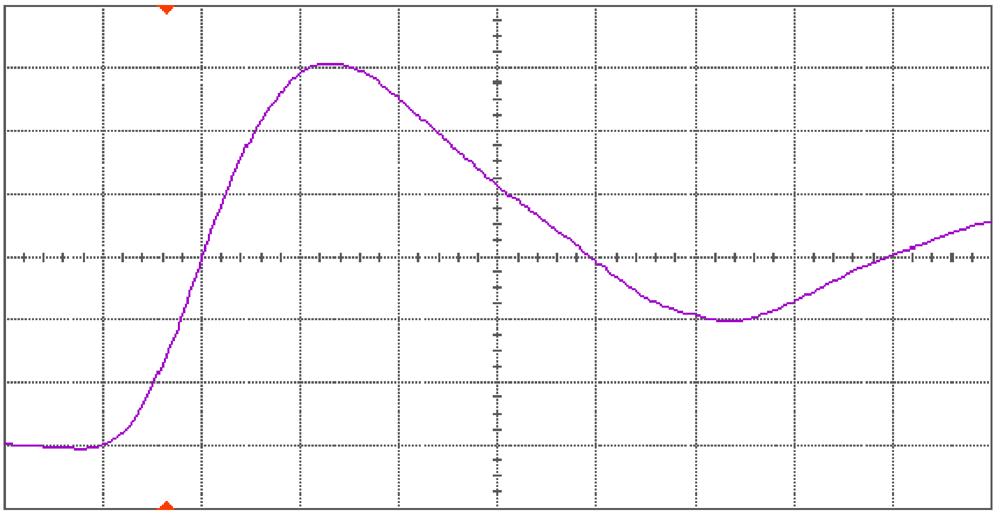

Figure 7(a) DUT 3853 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div .

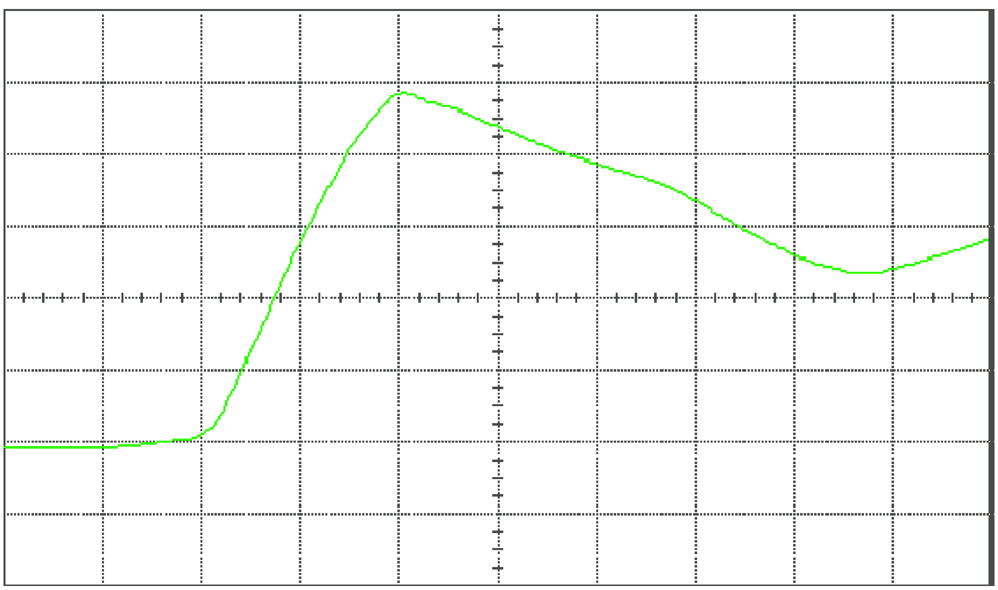

Figure 7(b) DUT 3853 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

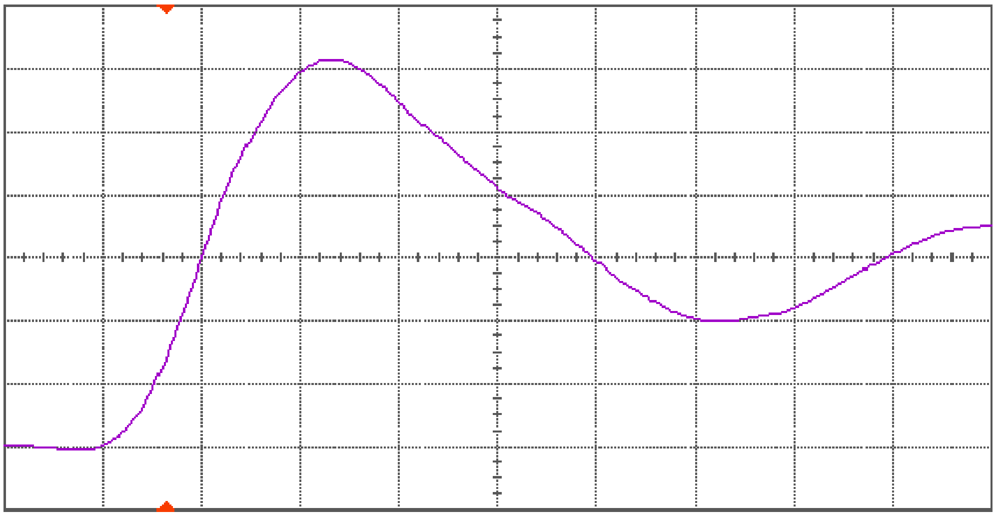

Figure 8(a) DUT 3859 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div .

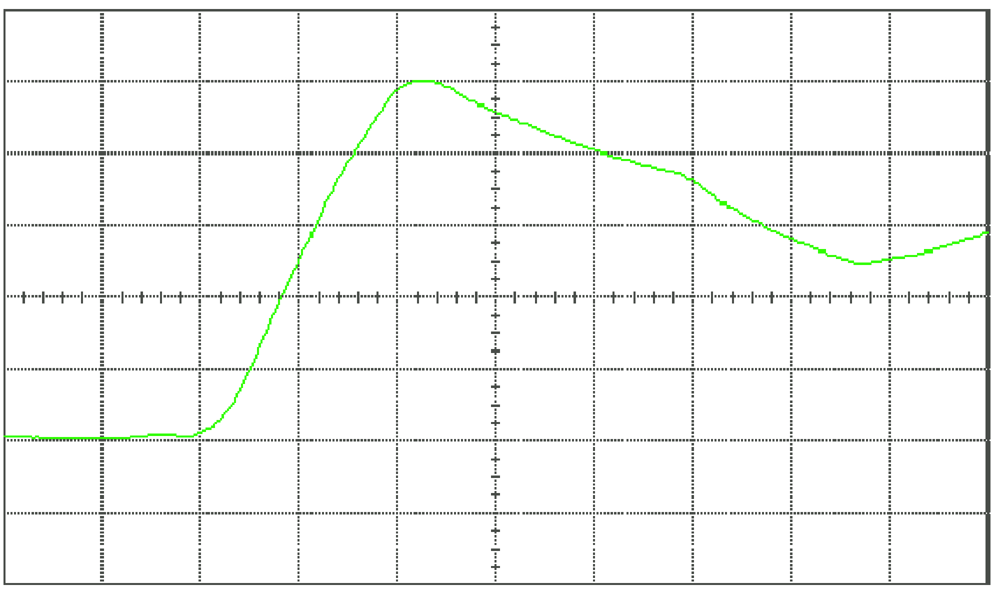

Figure 8(b) DUT 3859 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

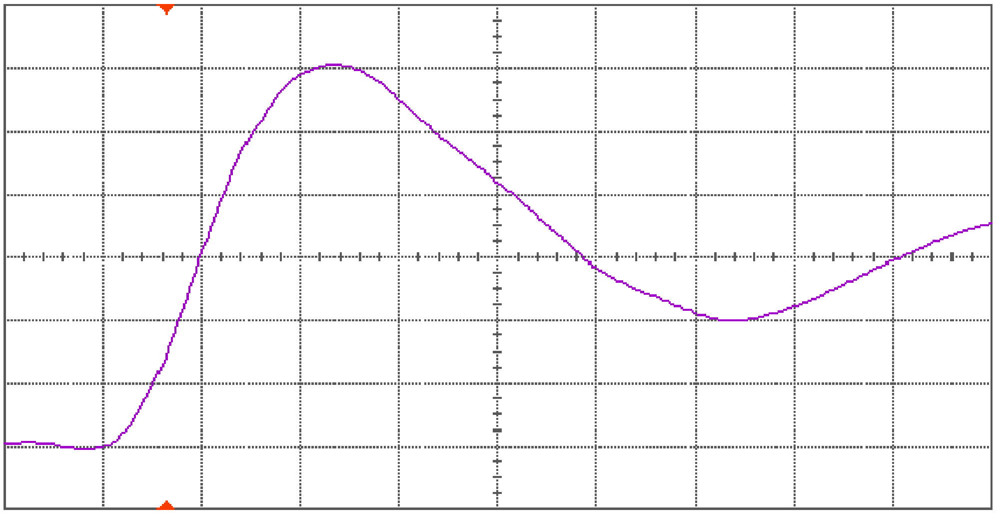

Figure 9(a) DUT 3916 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div .

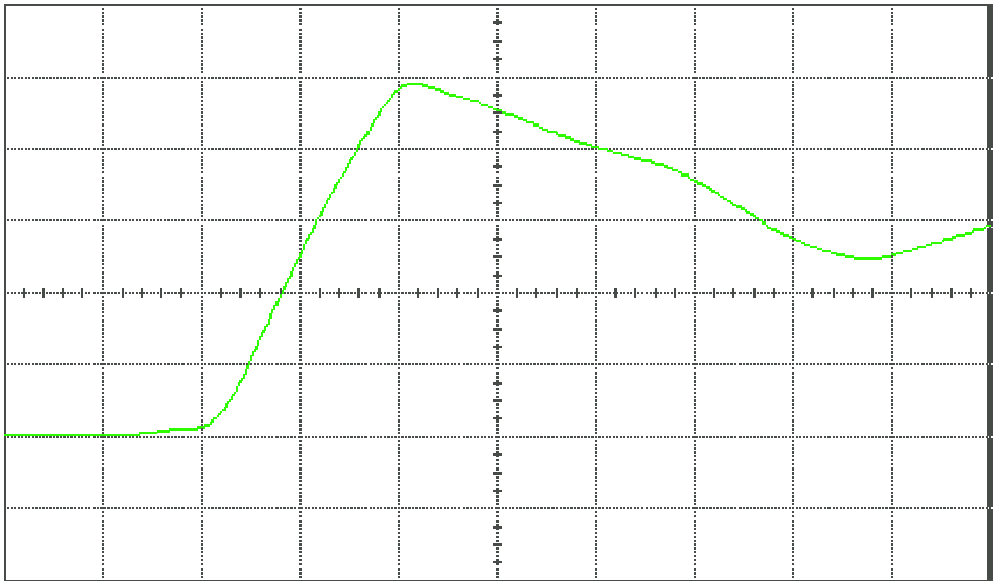

Figure 9(b) DUT 3916 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div

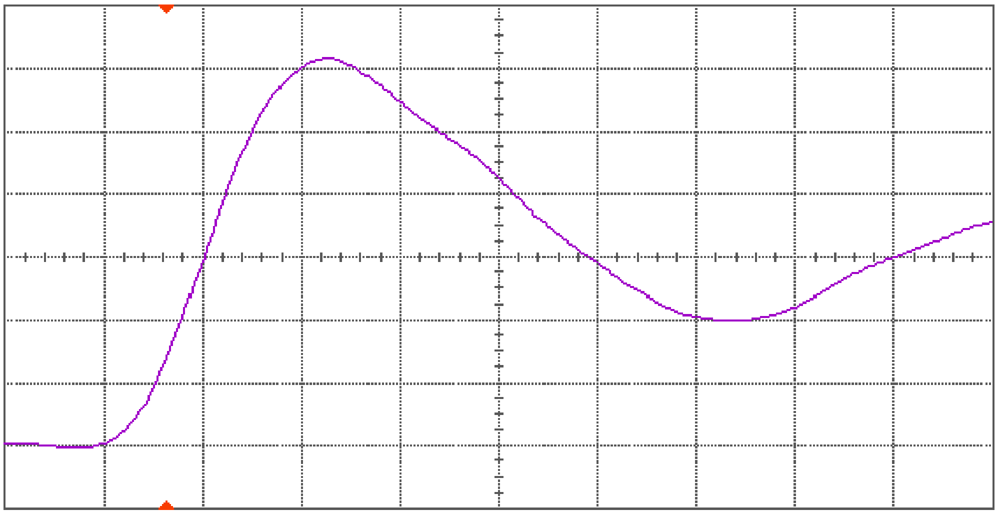

Figure 10(a) DUT 3931 pre-irradiation rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div .

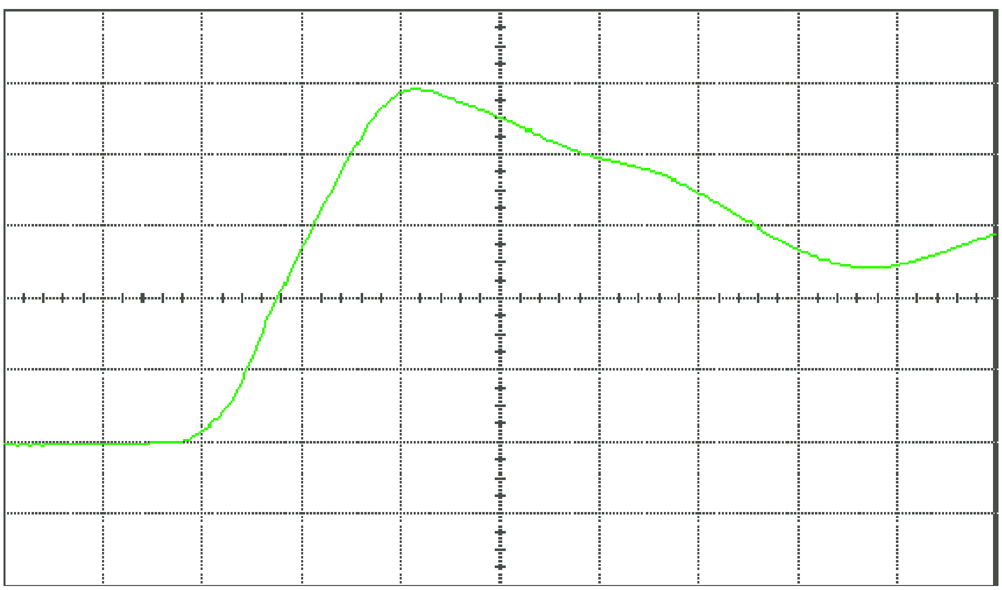

Figure 10(b) DUT 3931 post-annealing rising edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

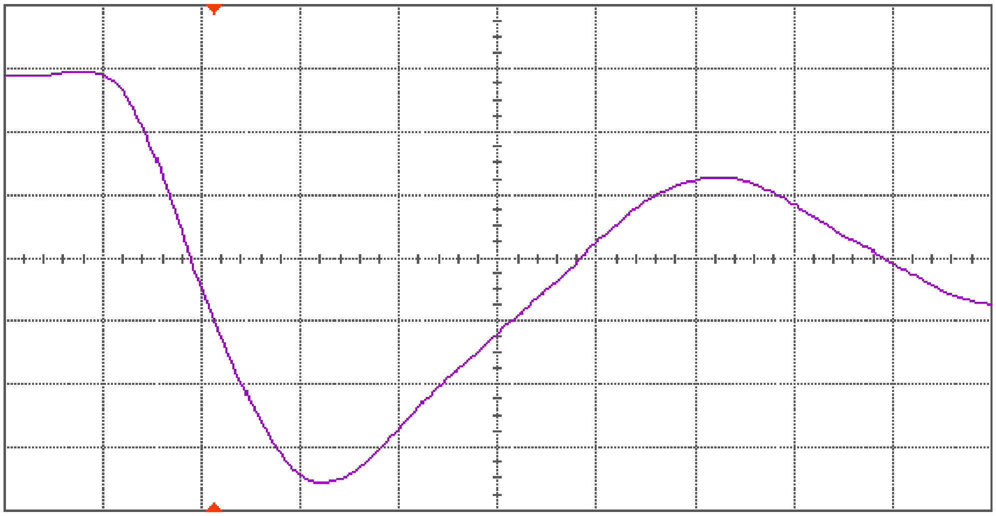

Figure 11(a) DUT 3853 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

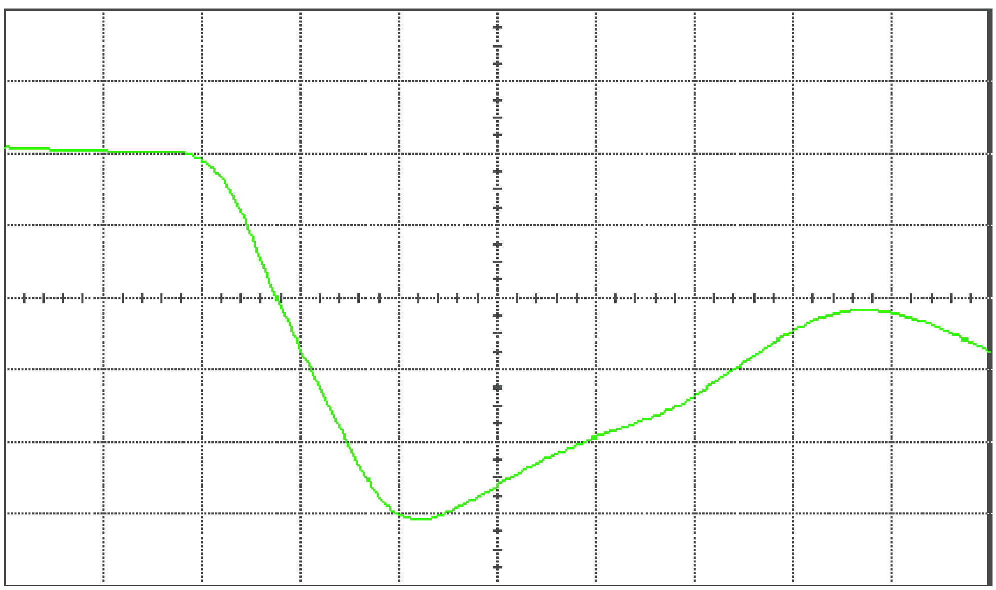

Figure 11(b) DUT 3853 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

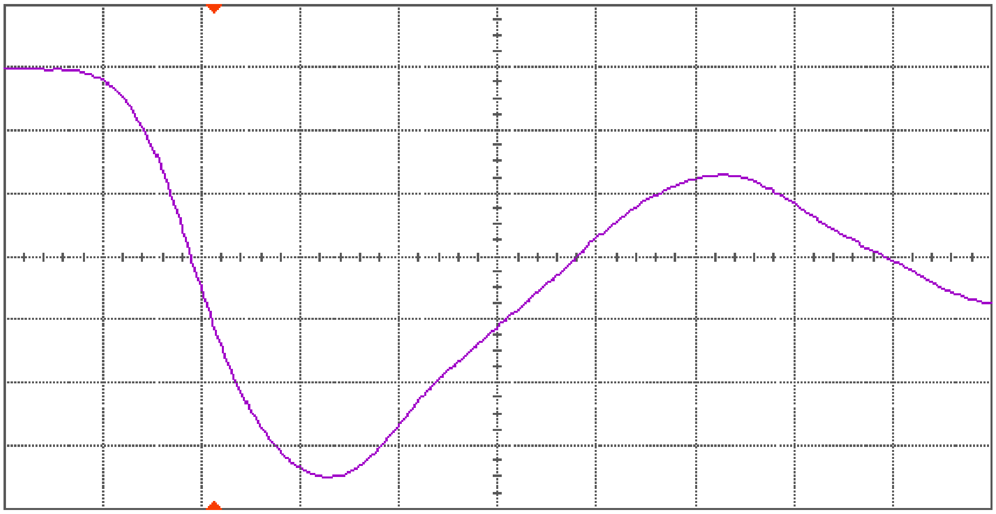

Figure 12(a) DUT 3859 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

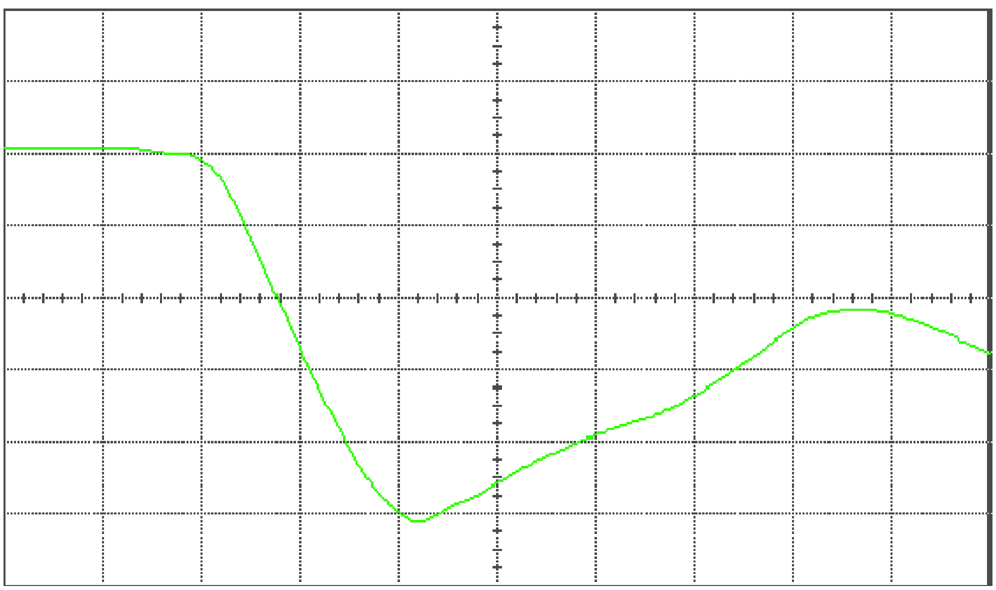

Figure 12(b) DUT 3859 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

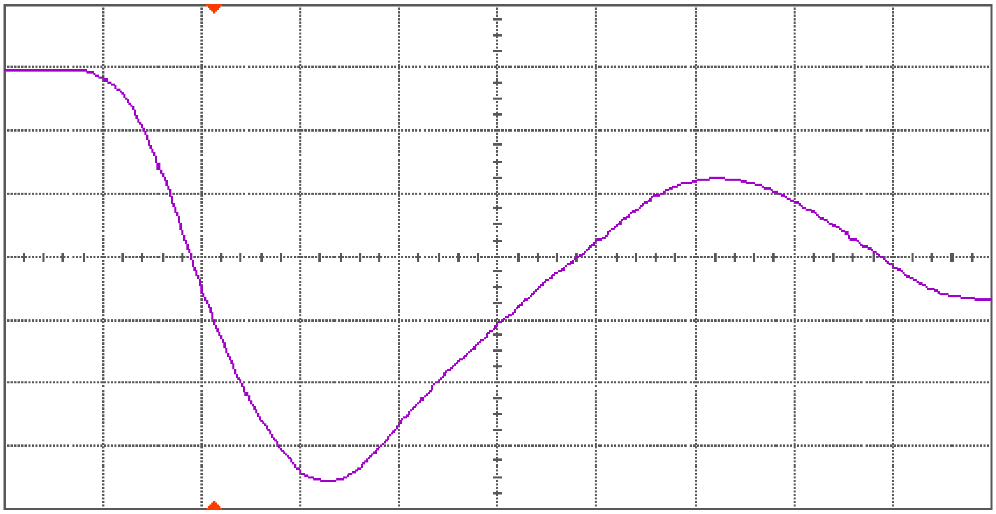

Figure 13(a) DUT 3916 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

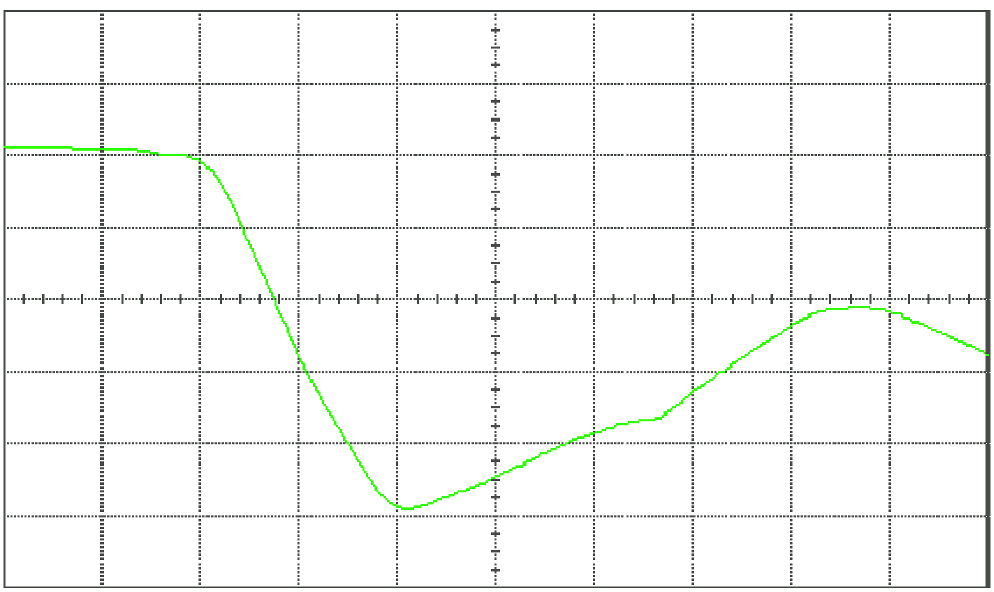

Figure 13(b) DUT 3916 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

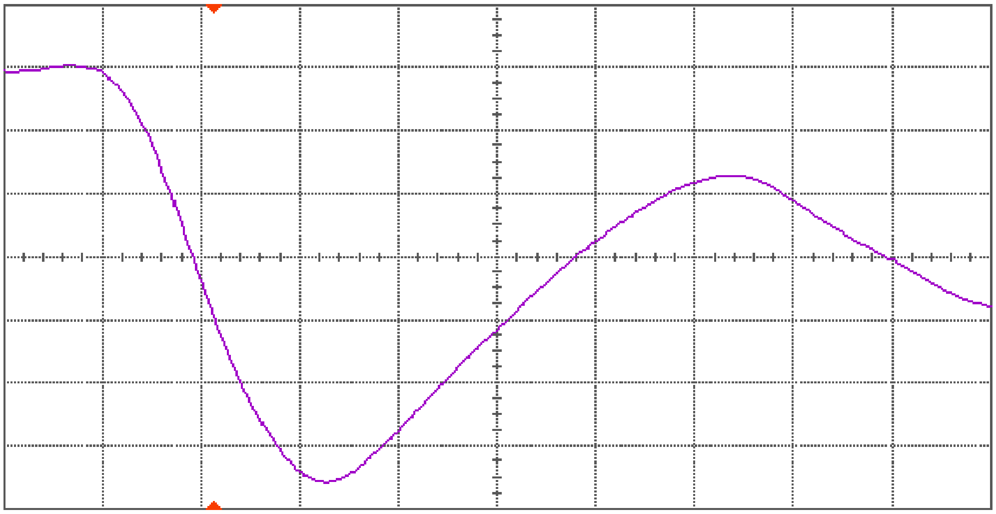

Figure 14(a) DUT 3931 pre-irradiation falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.

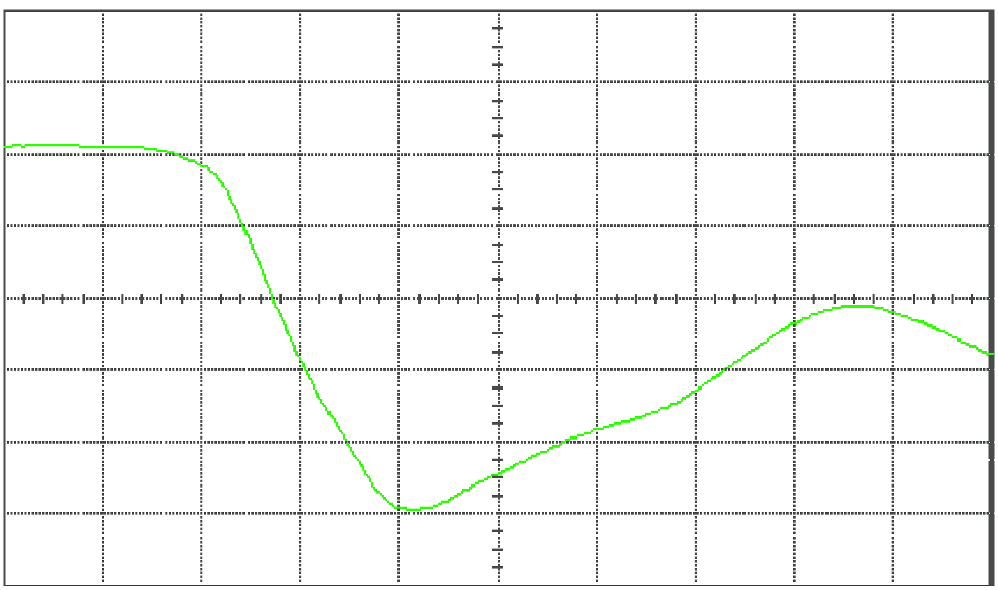

Figure 14(b) DUT 3931 post-annealing falling edge, abscissa scale is 1 V/div and ordinate scale is 1 ns/div.