TOTAL IONIZING DOSE TEST REPORT

No. 06T-RTSX72SU-D1N2W1
April 28, 2006
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 90 krad (Si) per 25-mA spec after room temperature annealing. Post 100 krad (Si) and after 15 days room temperature annealing: average I_{CCA} = 96.7 mA; average I_{CCI} = 59.7 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10%-degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings_r1
Die Lot Number	D1N2W1
Quantity Tested	6
Serial Number	60 krad: 84539, 84543 90 krad: 84531 100 krad: 84588, 84601, 84604
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

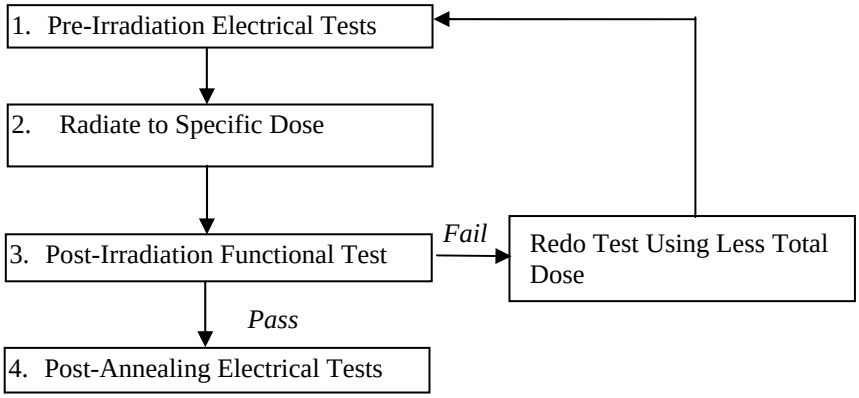


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. Both 60 krad-irradiated and 100 krad-irradiated group are annealed for approximately 15 days.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings_r1) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on combinational nets listed in Row 3 and 4 in Table 2. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffers (DA/QA0, DAH/QA0H, ENCNTRH/YO0H, IDII0/IDIO0, IDII1/IDIO1, IDII2/IDIO2, IDII3/IDIO3, IDII4/IDIO4, IDII5/IDIO5, IDII6/IDIO6, IDII7/IDIO7)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (DA/QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. Functionality

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. Power Supply Current (I_{CCA} and I_{CCI})

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 7 basically show the radiation-induced leakage current. The room temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3 Post Irradiation and Post-Annealing I_{CC}

DUT	Total Dose	I_{CCA} (mA)		I_{CCI} (mA)	
		Post-rad	Post-ann	Post-rad	Post-ann
84531	90 krad	33	22	45	NA
84539	60 krad	30	24	45	NA
84543	60 krad	31	19	45	23
84588	100 krad	374	105	260	65
84601	100 krad	285	97	215	58
84604	100 krad	263	88	204	56

A semi-log empirical equation is used to extrapolate the room temperature annealing for 10 years. Using the worst case, DUT 84588, the tolerance is extracted as 92 krad for a 10 year mission.

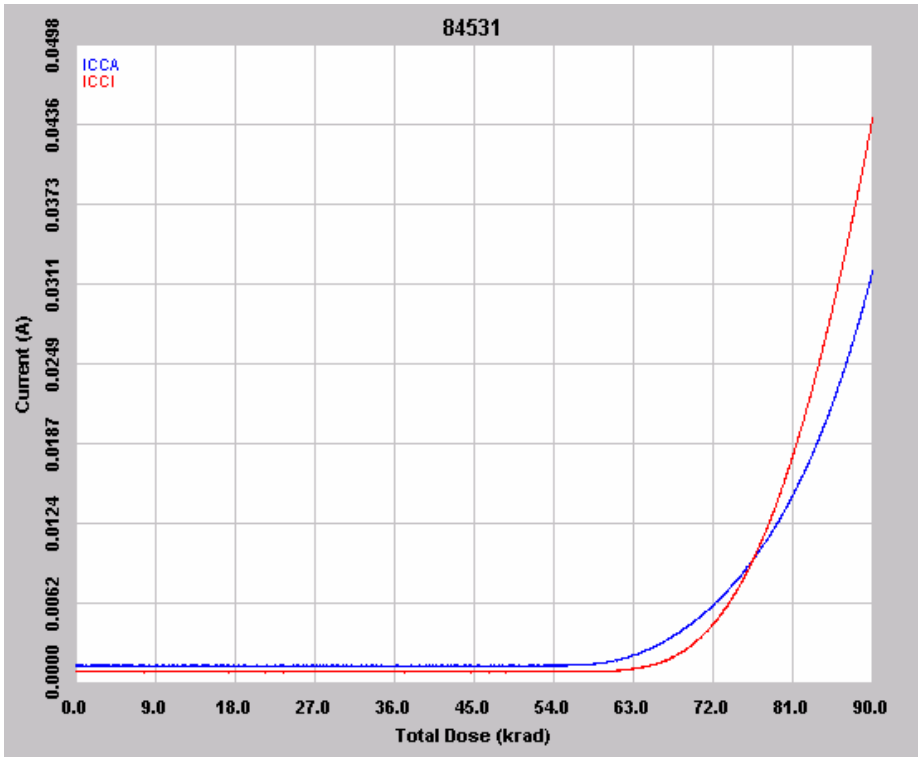


Figure 2 DUT 84531 in-flux I_{CCA} and I_{CCI}

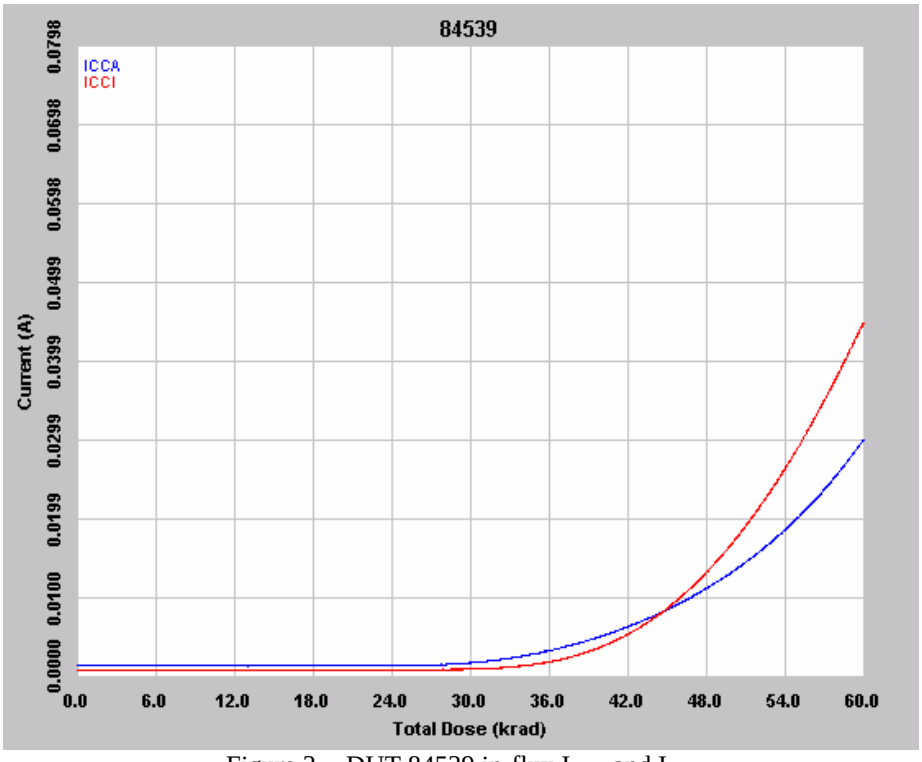


Figure 3 DUT 84539 in-flux I_{CCA} and I_{CCI}

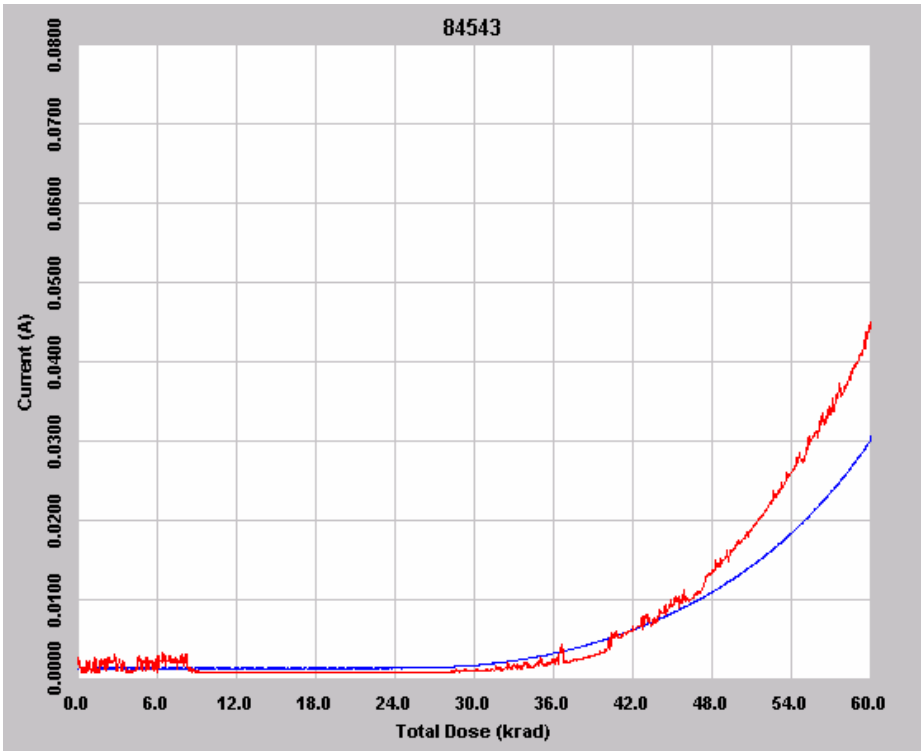


Figure 4 DUT 84543 in-flux I_{CCA} and I_{CCI}

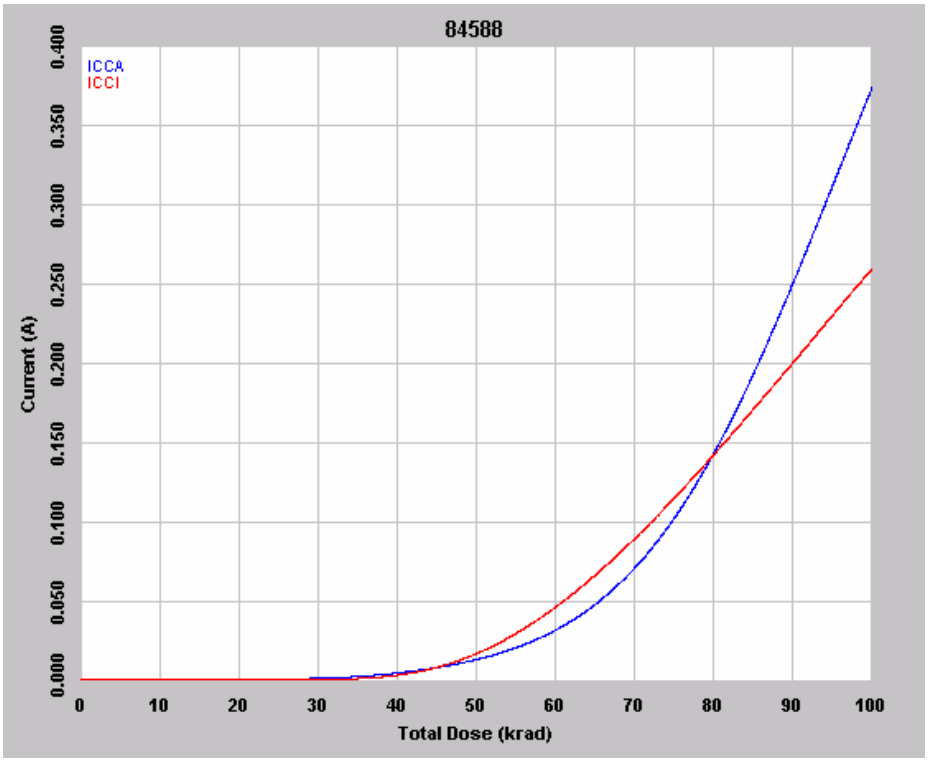


Figure 5 DUT 84588 in-flux I_{CCA} and I_{CCI}

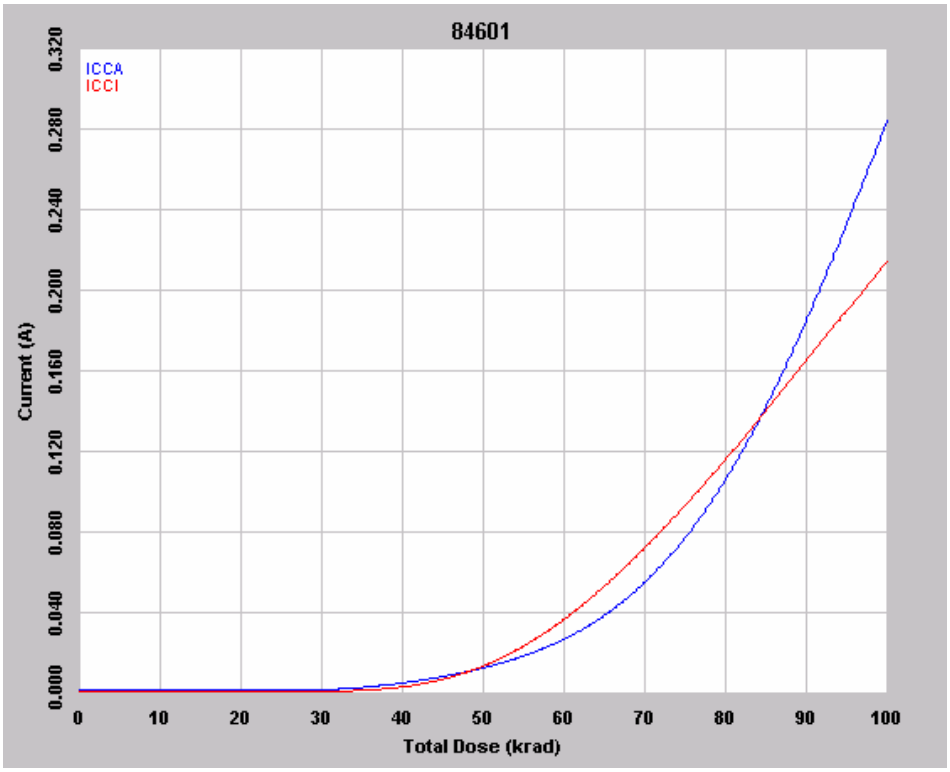


Figure 6 DUT 84601 in-flux I_{CCA} and I_{CCI}

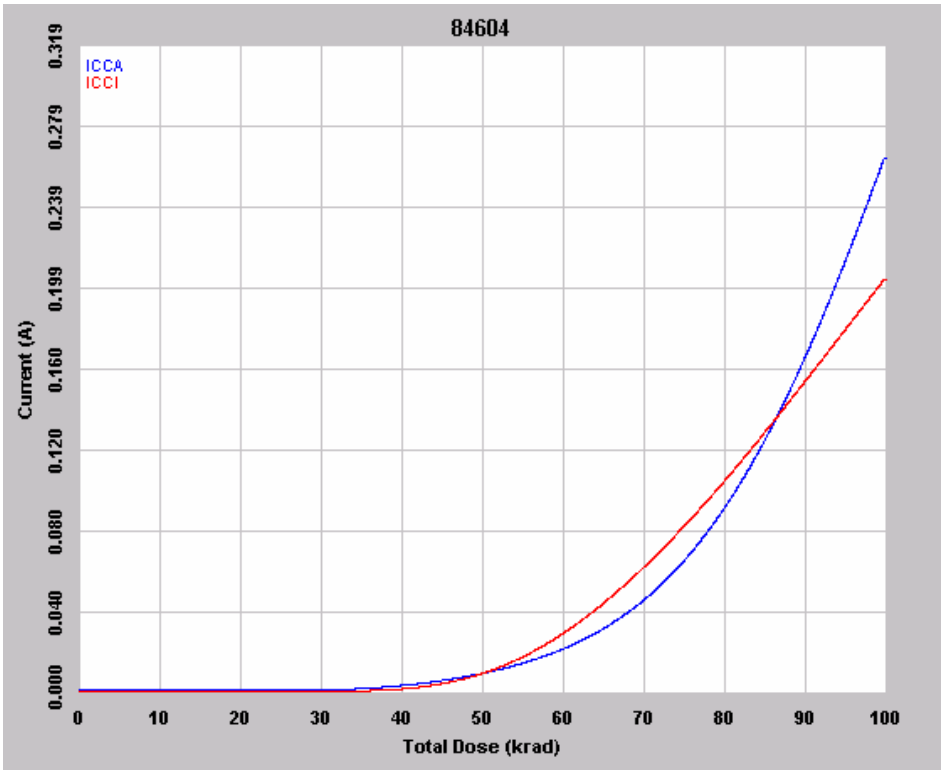


Figure 7 DUT 84604 in-flux I_{CCA} and I_{CCI}

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4a Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		DA / QA0				DAH / QA0H			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.46	1.41	1.41	1.36	1.47	1.42	1.40	1.35
84539	60 krad	1.48	1.42	1.43	1.37	1.46	1.43	1.41	1.36
84543	60 krad	1.48	1.41	1.42	1.36	1.46	1.42	1.40	1.35
84588	100 krad	1.46	1.38	1.41	1.32	1.47	1.41	1.41	1.33
84601	100 krad	1.46	1.38	1.41	1.31	1.46	1.39	1.40	1.32
84604	100 krad	1.46	1.38	1.41	1.33	1.48	1.41	1.41	1.33

Table 4b Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		ENCNTRH / YO0H				IDII0 / IDIO0			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.46	1.40	1.40	1.34	1.45	1.47	1.43	1.42
84539	60 krad	1.48	1.42	1.43	1.36	1.47	1.47	1.42	1.42
84543	60 krad	1.46	1.41	1.41	1.35	1.46	1.44	1.41	1.41
84588	100 krad	1.47	1.37	1.41	1.31	1.44	1.44	1.41	1.41
84601	100 krad	1.46	1.36	1.41	1.31	1.46	1.45	1.41	1.41
84604	100 krad	1.47	1.37	1.42	1.33	1.45	1.47	1.42	1.42

Table 4c Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII1/ IDIO1			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.46	1.46	1.41	1.40
84539	60 krad	1.46	1.46	1.41	1.41
84543	60 krad	1.46	1.46	1.41	1.41
84588	100 krad	1.46	1.46	1.40	1.40
84601	100 krad	1.46	1.46	1.41	1.41
84604	100 krad	1.47	1.48	1.41	1.41

Table 4d Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII2 / IDIO2				IDII3 / IDIO3			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.46	1.44	1.42	1.41	1.47	1.46	1.41	1.41
84539	60 krad	1.45	1.44	1.41	1.41	1.47	1.47	1.41	1.41
84543	60 krad	1.45	1.44	1.41	1.43	1.46	1.46	1.41	1.41
84588	100 krad	1.45	1.44	1.41	1.41	1.46	1.46	1.41	1.41
84601	100 krad	1.45	1.44	1.41	1.39	1.46	1.46	1.41	1.41
84604	100 krad	1.39	1.39	1.42	1.43	1.48	1.48	1.42	1.42

Table 4e Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII4 / IDIO4				IDII5 / IDIO5			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.45	1.39	1.40	1.40	1.46	1.44	1.42	1.46
84539	60 krad	1.37	1.37	1.40	1.41	1.39	1.45	1.47	1.48
84543	60 krad	1.37	1.42	1.39	1.39	1.44	1.43	1.46	1.45
84588	100 krad	1.35	1.32	1.40	1.44	1.44	1.39	1.46	1.39
84601	100 krad	1.42	1.43	1.40	1.39	1.46	1.45	1.42	1.45
84604	100 krad	1.45	1.39	1.42	1.44	1.43	1.41	1.48	1.45

Table 4f Pre-Irradiation and Post-Annealing Input Thresholds

In/Out Pin:		IDII6 / IDIO6				IDII7 / IDIO7			
DUT	Total Dose	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann	Pre-rad	Post-Ann
		V_{IL} (V)		V_{IH} (V)		V_{IL} (V)		V_{IH} (V)	
84531	90 krad	1.45	1.44	1.39	1.39	1.44	1.44	1.42	1.42
84539	60 krad	1.45	1.45	1.40	1.40	1.44	1.44	1.42	1.41
84543	60 krad	1.44	1.43	1.39	1.39	1.31	1.43	1.42	1.41
84588	100 krad	1.44	1.43	1.39	1.38	1.43	1.42	1.42	1.40
84601	100 krad	1.45	1.44	1.39	1.39	1.31	1.42	1.41	1.40
84604	100 krad	1.46	1.45	1.41	1.40	1.45	1.44	1.42	1.41

D. Output-Drive Voltage (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	Total Dose	1 mA		12 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
84531	90 krad	0.144	0.143	0.224	0.221	0.283	0.279	0.506	0.500	0.971	0.955
84539	60 krad	0.142	0.140	0.220	0.217	0.277	0.274	0.496	0.490	0.945	0.930
84543	60 krad	0.142	0.140	0.220	0.218	0.278	0.274	0.497	0.491	0.948	0.935
84588	100 krad	0.143	0.141	0.221	0.219	0.279	0.277	0.500	0.495	0.955	0.943
84601	100 krad	0.143	0.142	0.222	0.220	0.280	0.277	0.502	0.497	0.961	0.946
84604	100 krad	0.143	0.141	0.221	0.219	0.279	0.276	0.499	0.494	0.952	0.939

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	Total Dose	1 mA		8 mA		20 mA		50 mA		100 mA	
		Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
84531	90 krad	4.82	4.82	4.74	4.74	4.59	4.59	4.03	4.03	2.68	2.69
84539	60 krad	4.82	4.82	4.74	4.74	4.59	4.59	4.04	4.04	2.73	2.73
84543	60 krad	4.82	4.82	4.74	4.74	4.59	4.59	4.03	4.03	2.68	2.68
84588	100 krad	4.82	4.82	4.74	4.73	4.59	4.59	4.03	4.02	2.67	2.63
84601	100 krad	4.82	4.82	4.74	4.73	4.59	4.59	4.03	4.03	2.70	2.66
84604	100 krad	4.82	4.82	4.74	4.74	4.59	4.59	4.04	4.03	2.73	2.70

E. Propagation Delay

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. All DUTs pass the 10%-degradation criterion.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Total Dose	Pre-Irradiation (μs)	Post-Annealing	Degradation
84531	90 krad	1.10	1.10	0.45%
84539	60 krad	1.07	1.08	0.42%
84543	60 krad	1.10	1.10	-0.09%
84588	100 krad	1.10	1.12	2.00%
84601	100 krad	1.12	1.13	1.34%
84604	100 krad	1.08	1.09	1.67%

F. Transition Time

Figures 8 to 19 show the pre-irradiation and post-annealing transition edges. In each case, the radiation effect is not significant.

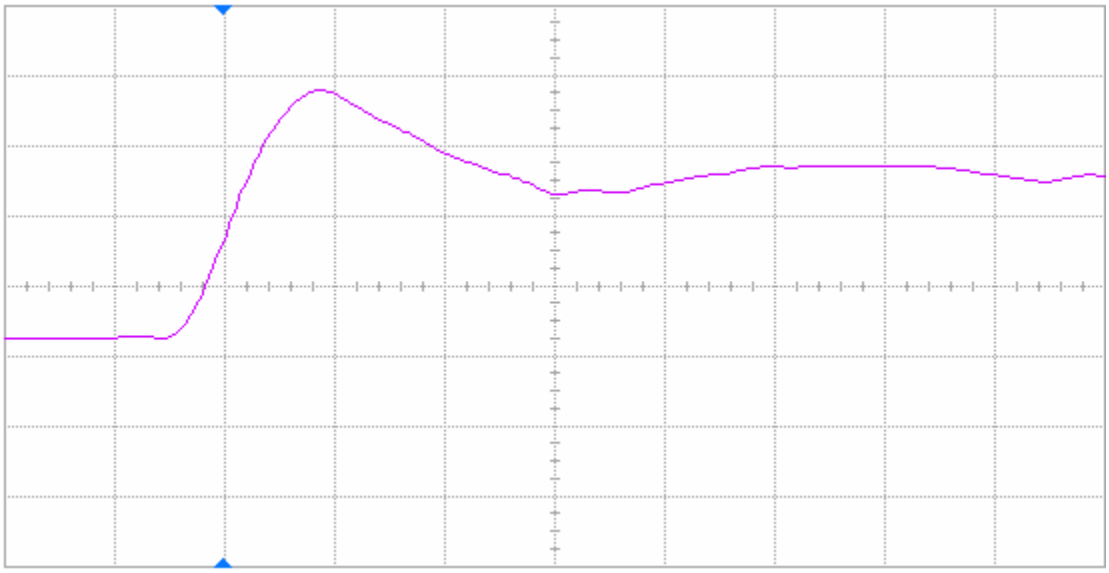


Figure 8(a) DUT 84531 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

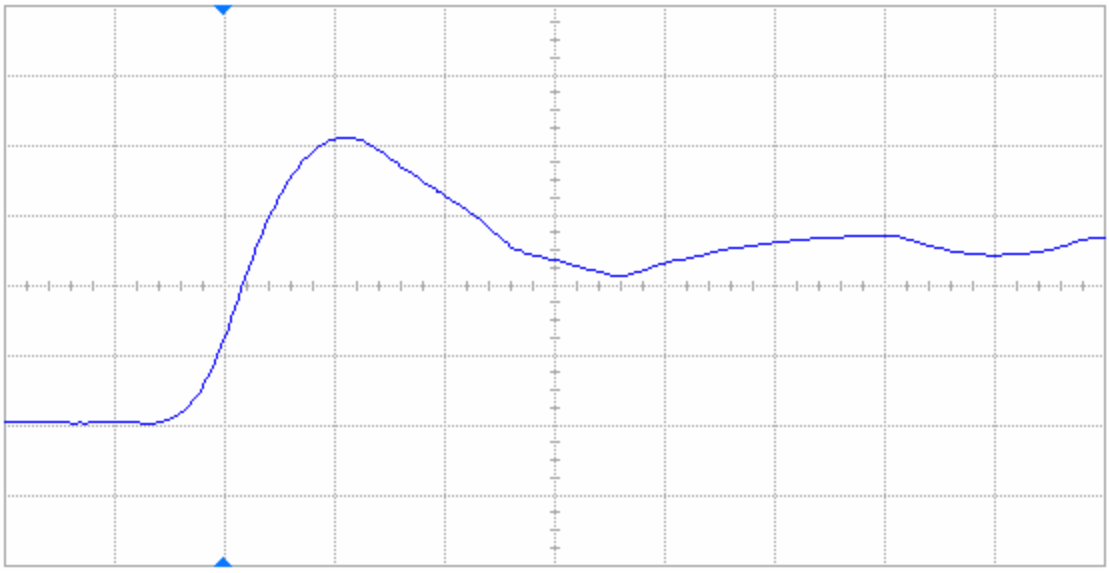


Figure 8(b) DUT 84531 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

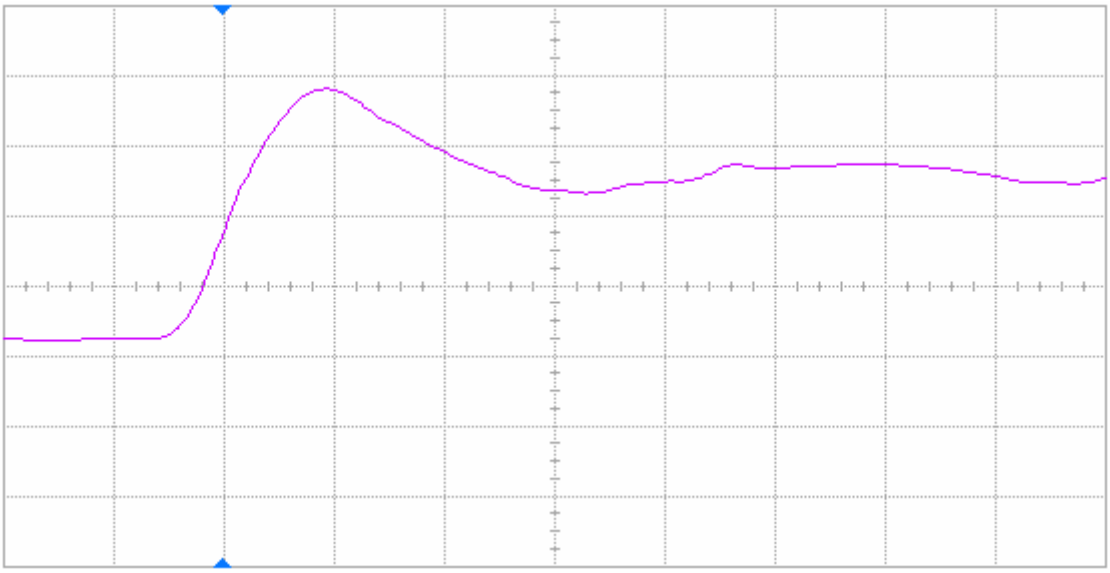


Figure 9(a) DUT 84539 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

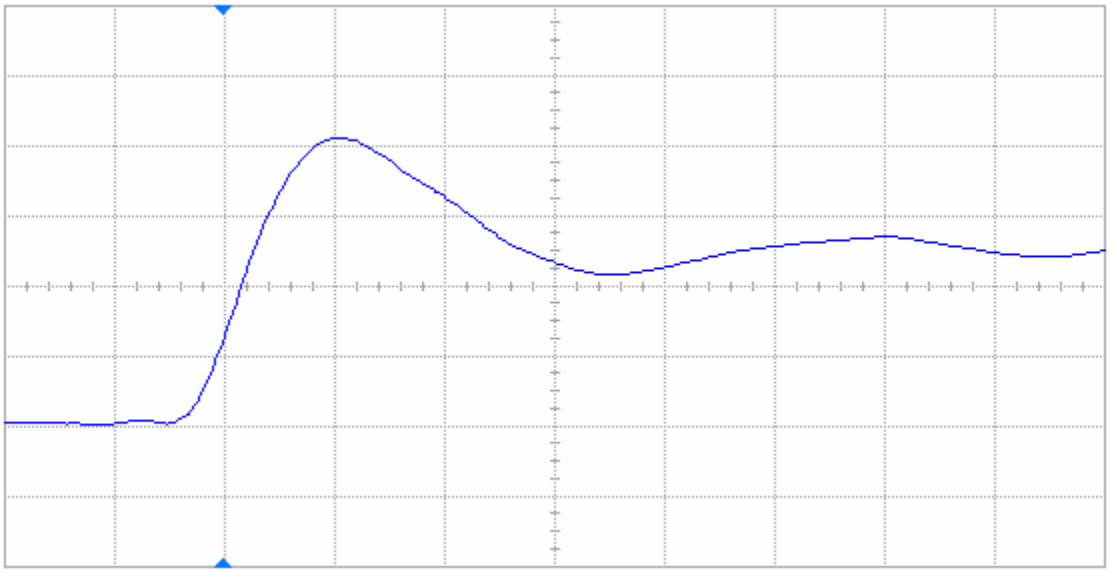


Figure 9(b) DUT 84539 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

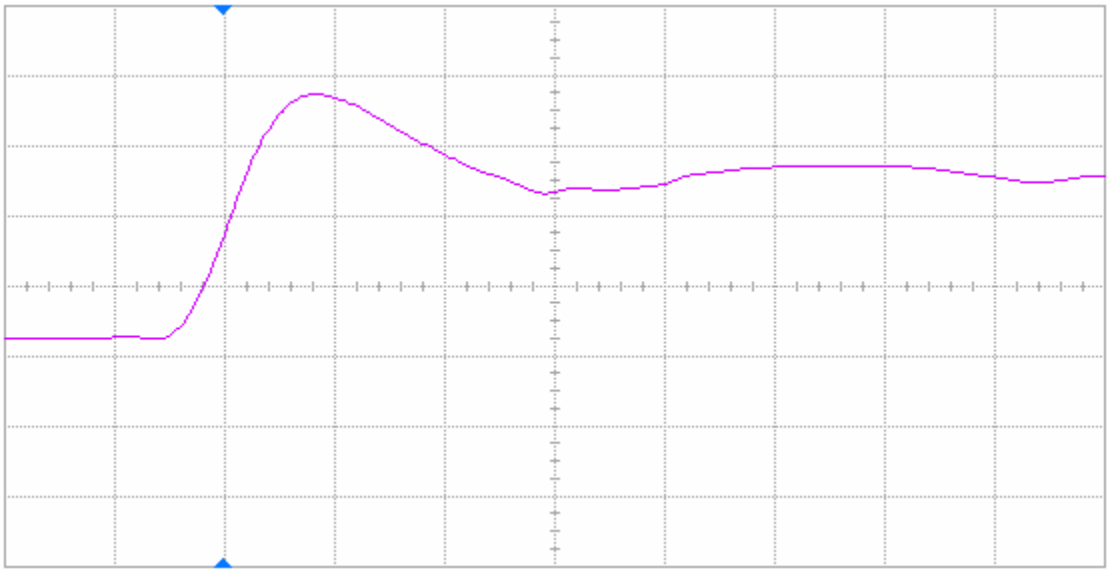


Figure 10(a) DUT 84543 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

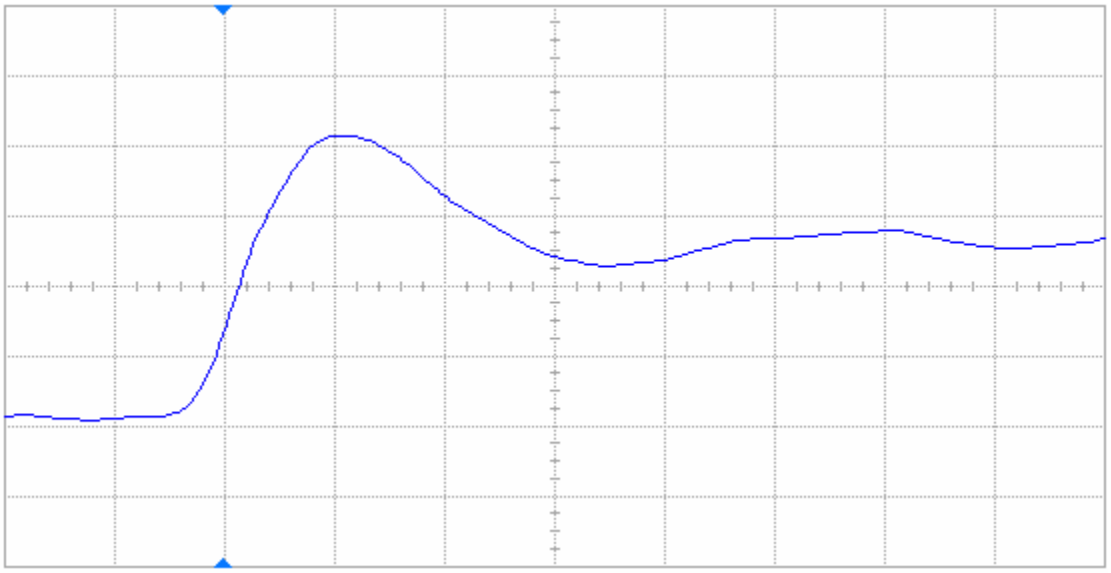


Figure 10(b) DUT 84543 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

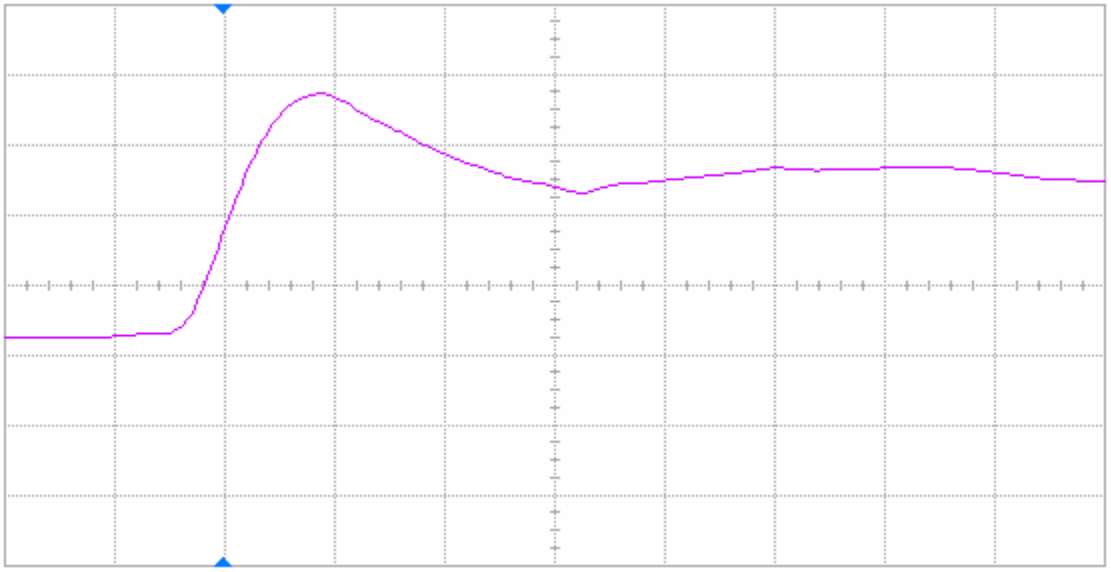


Figure 11(a) DUT 84588 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

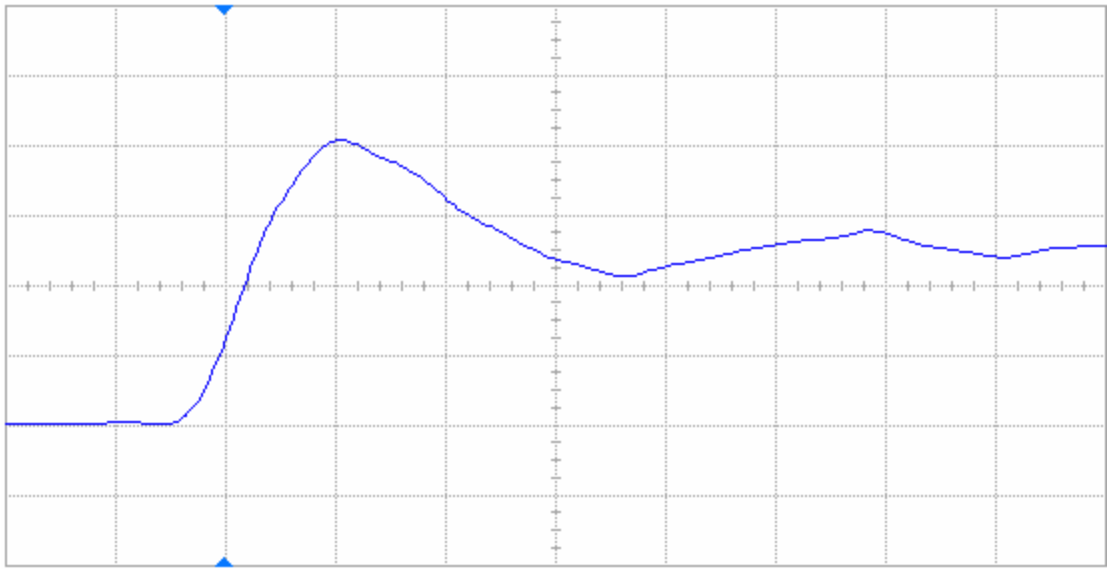


Figure 11(b) DUT 84588 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

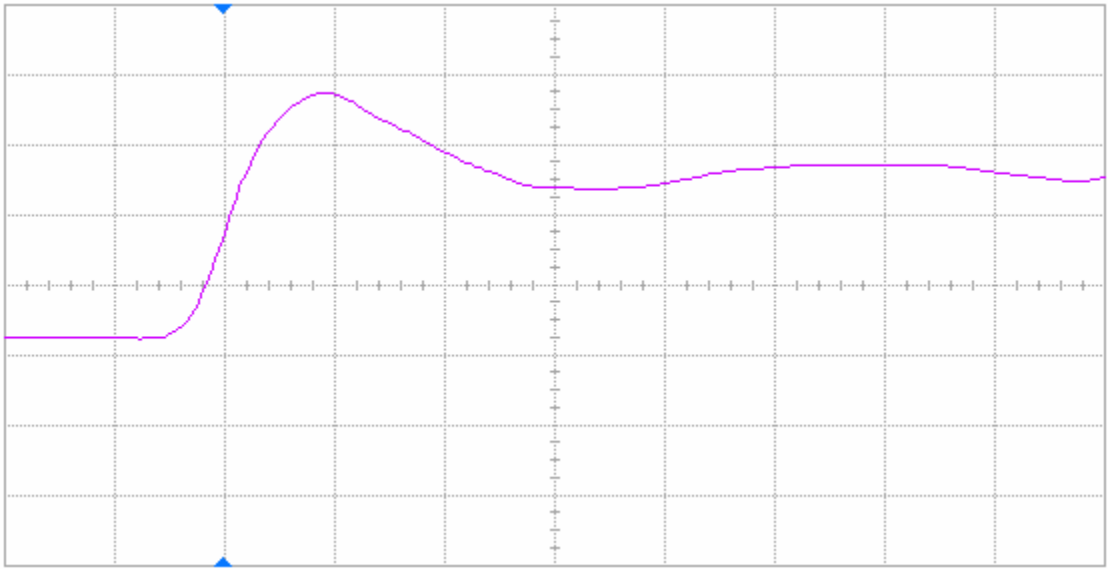


Figure 12(a) DUT 84601 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

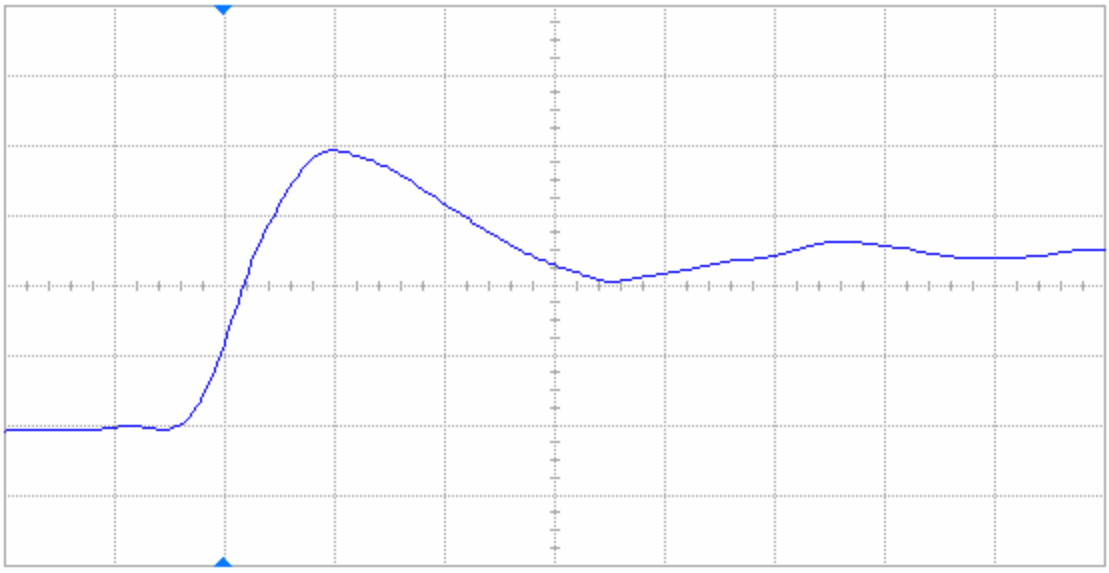


Figure 12(b) DUT 84601 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

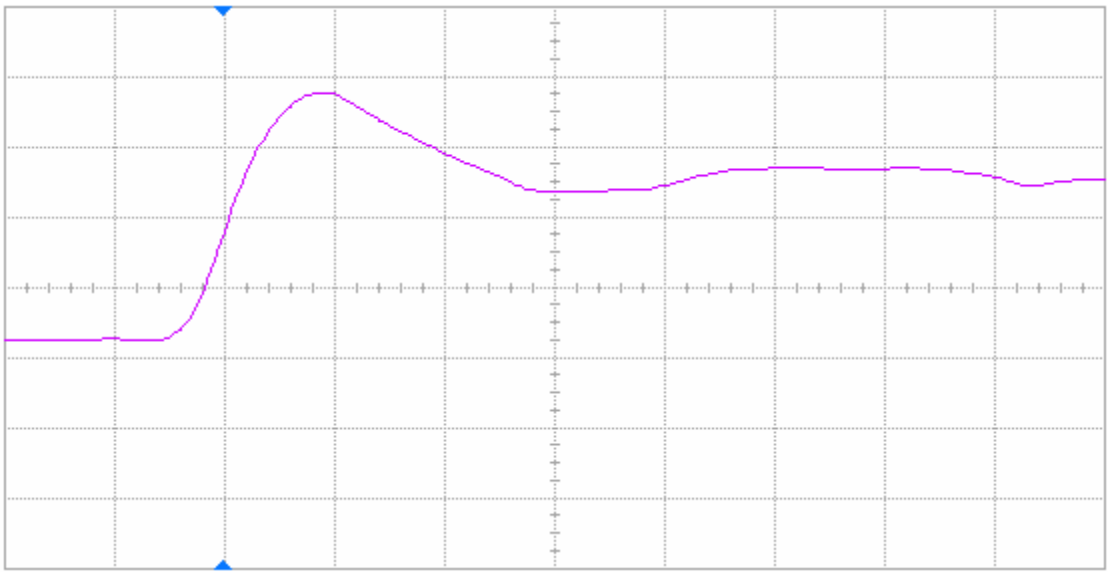


Figure 13(a) DUT 84604 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

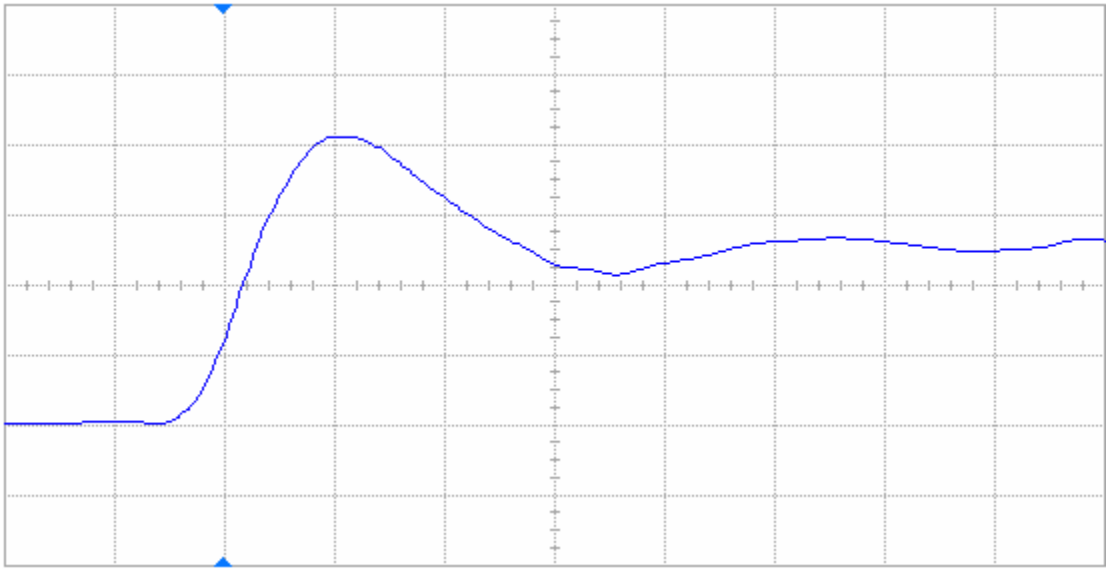


Figure 13(b) DUT 84604 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

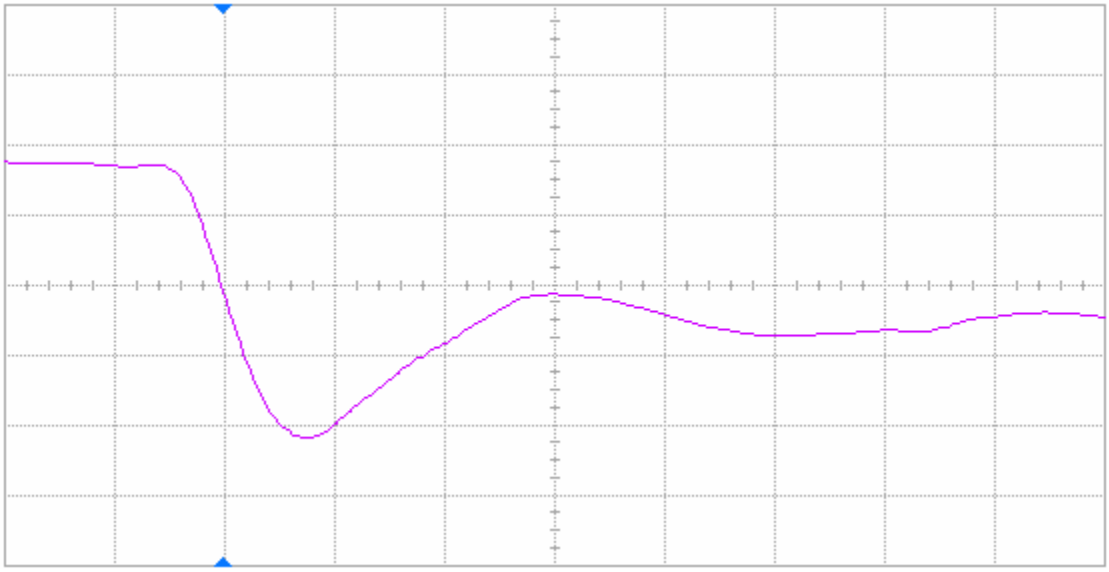


Figure 14(a) DUT 84531 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

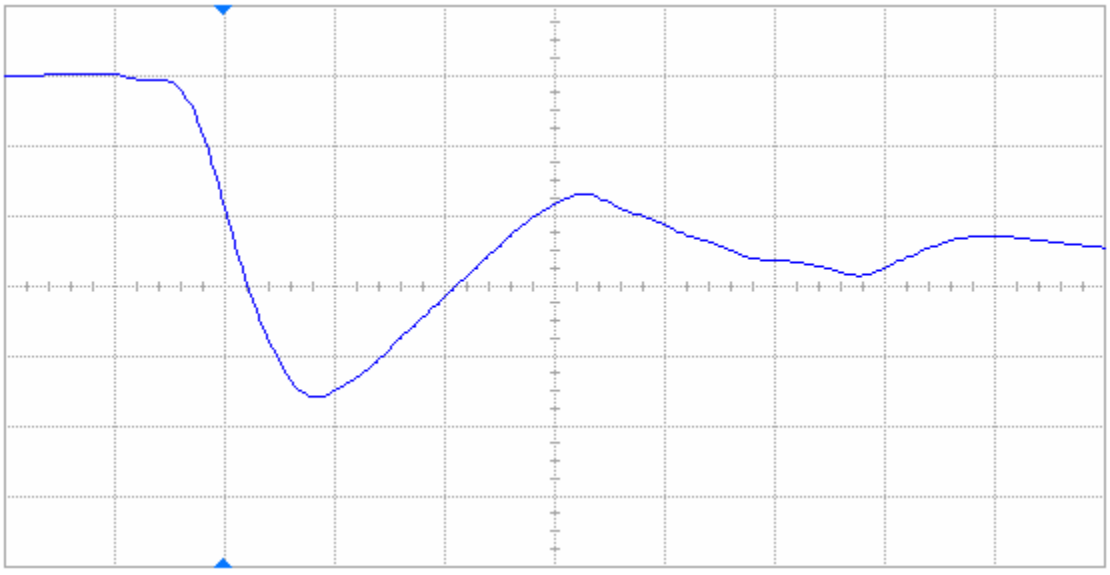


Figure 14(b) DUT 84531 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

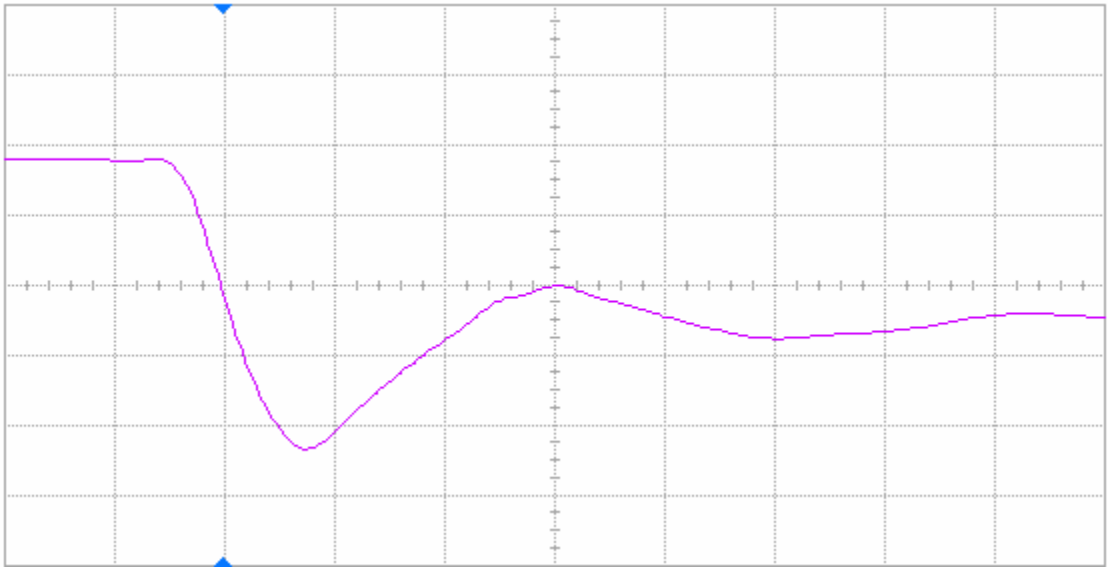


Figure 15(a) DUT 84539 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

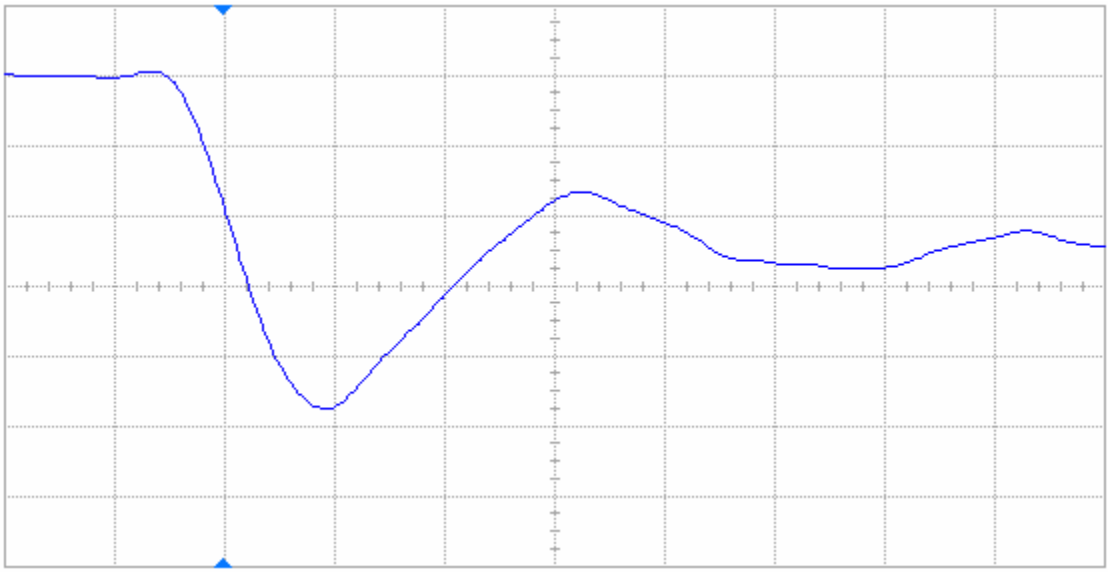


Figure 15(b) DUT 84539 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

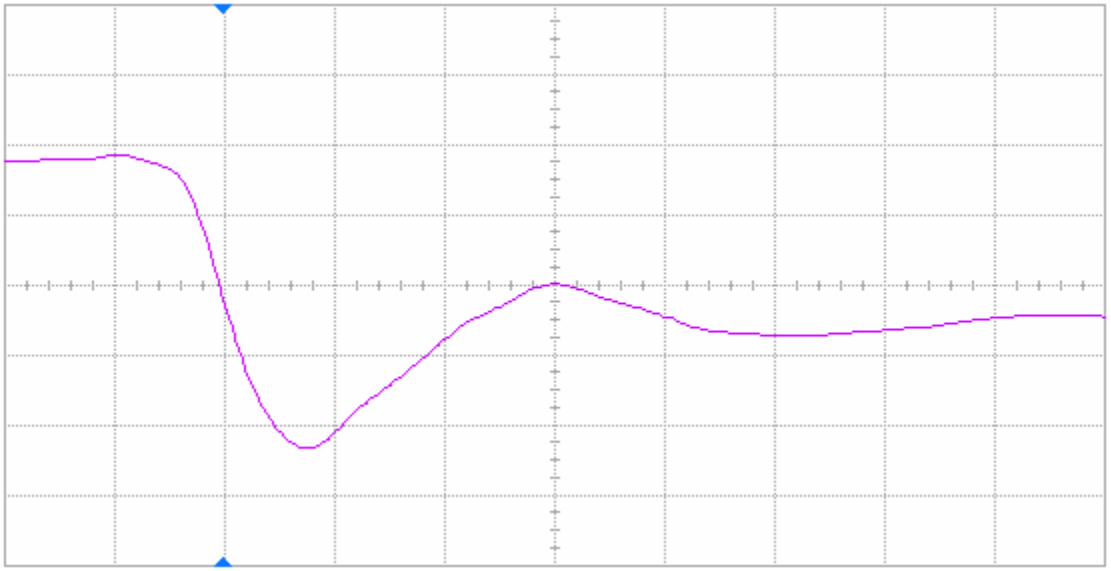


Figure 16(a) DUT 84543 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

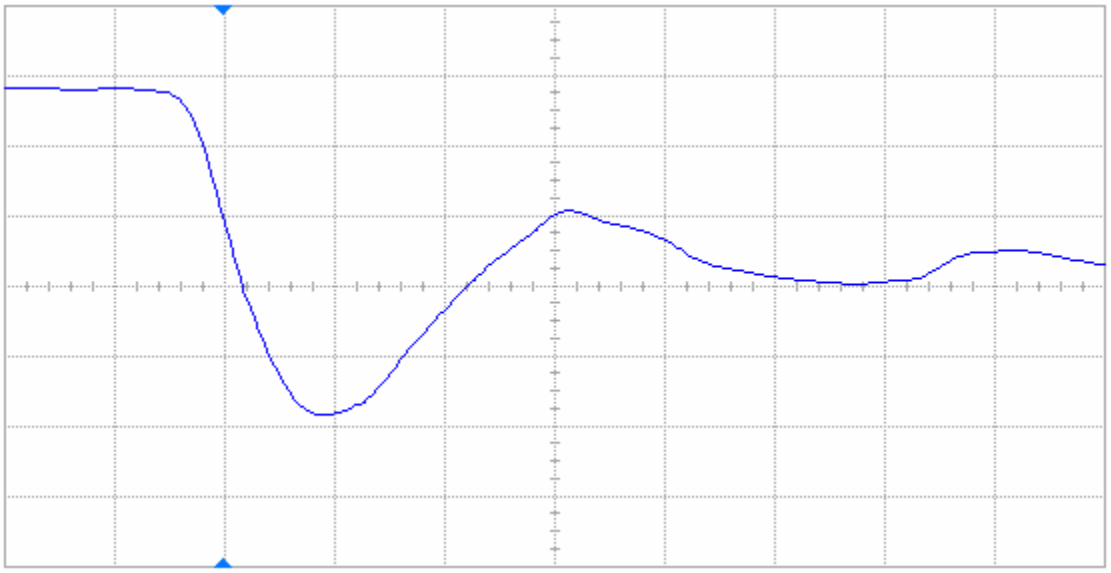


Figure 16(b) DUT 84543 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

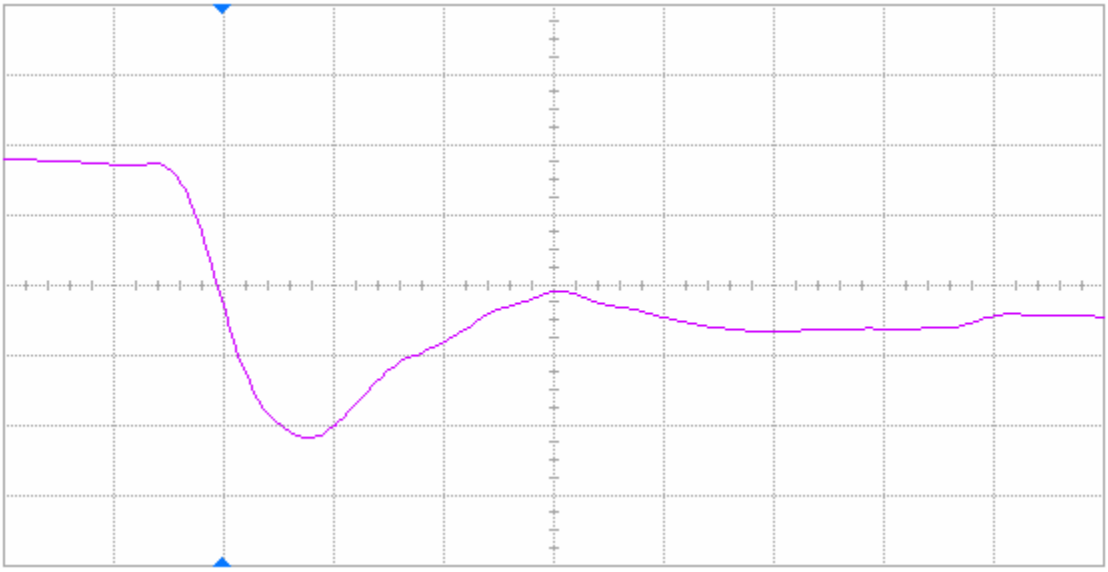


Figure 17(a) DUT 84588 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

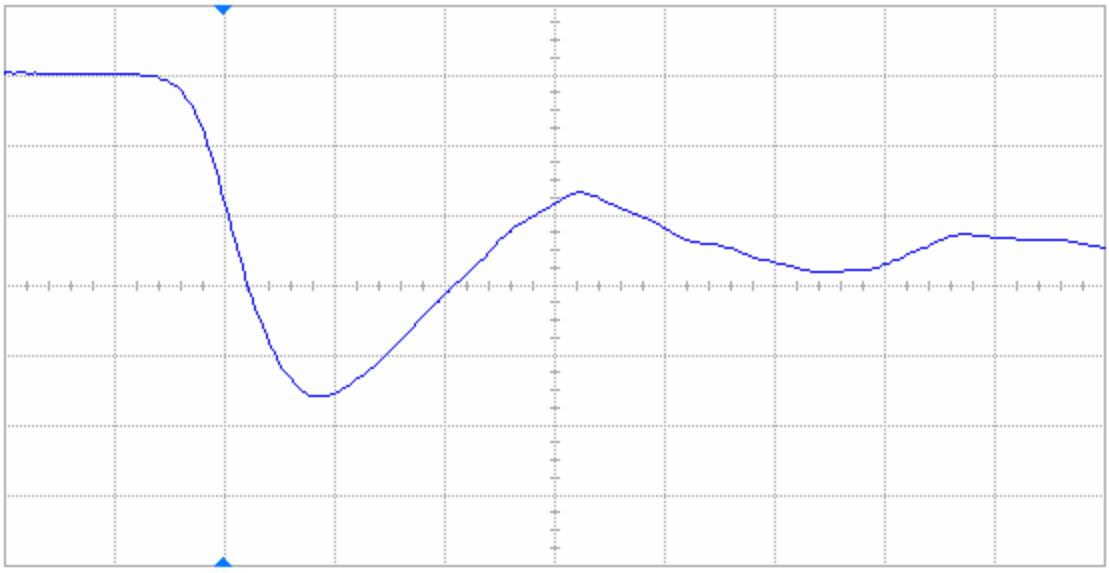


Figure 17(b) DUT 84588 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

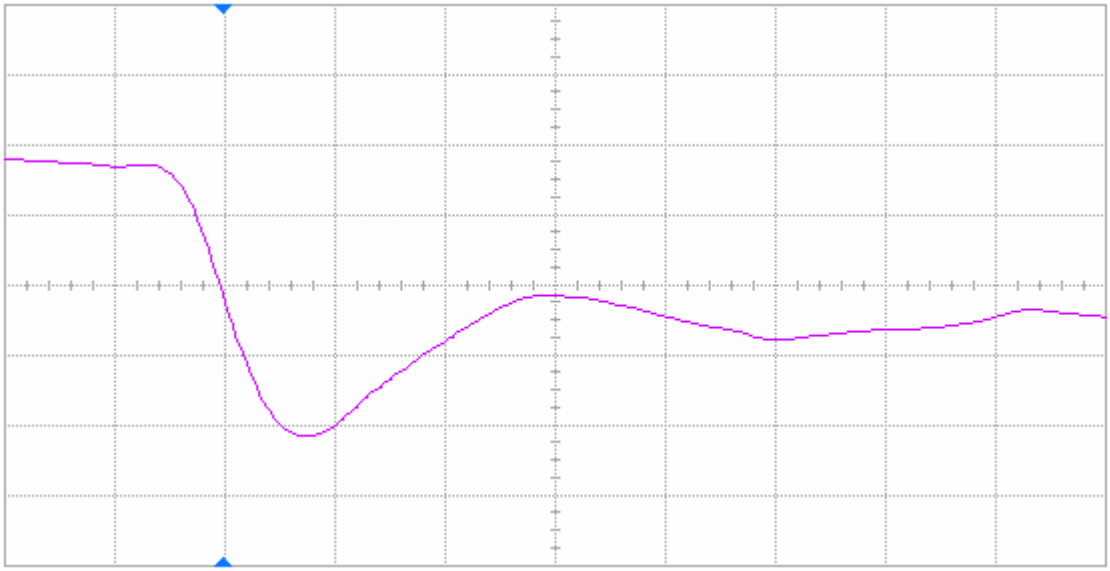


Figure 18(a) DUT 84601 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

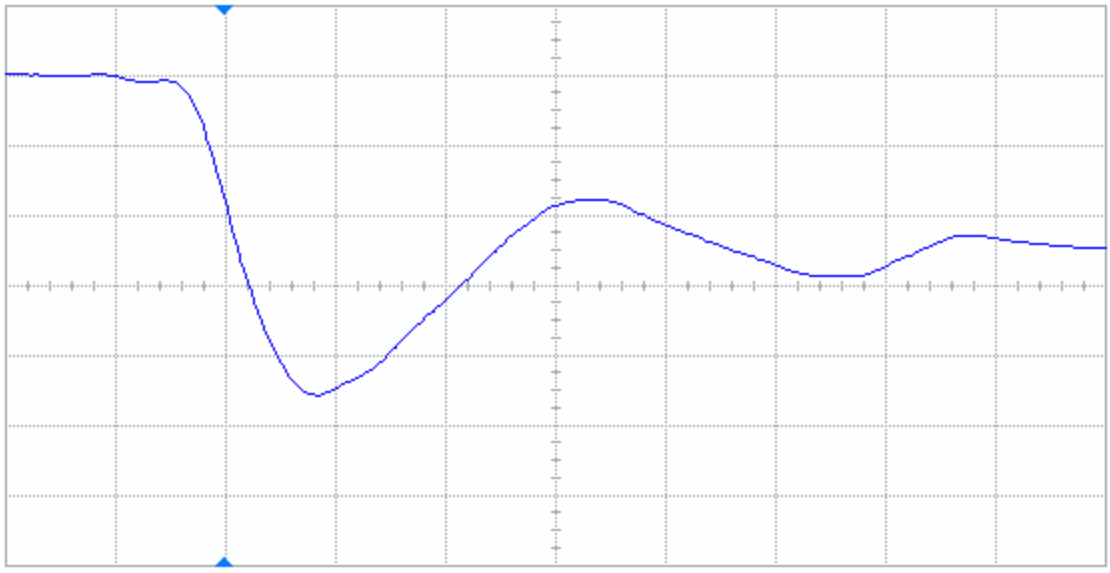


Figure 18(b) DUT 84601 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

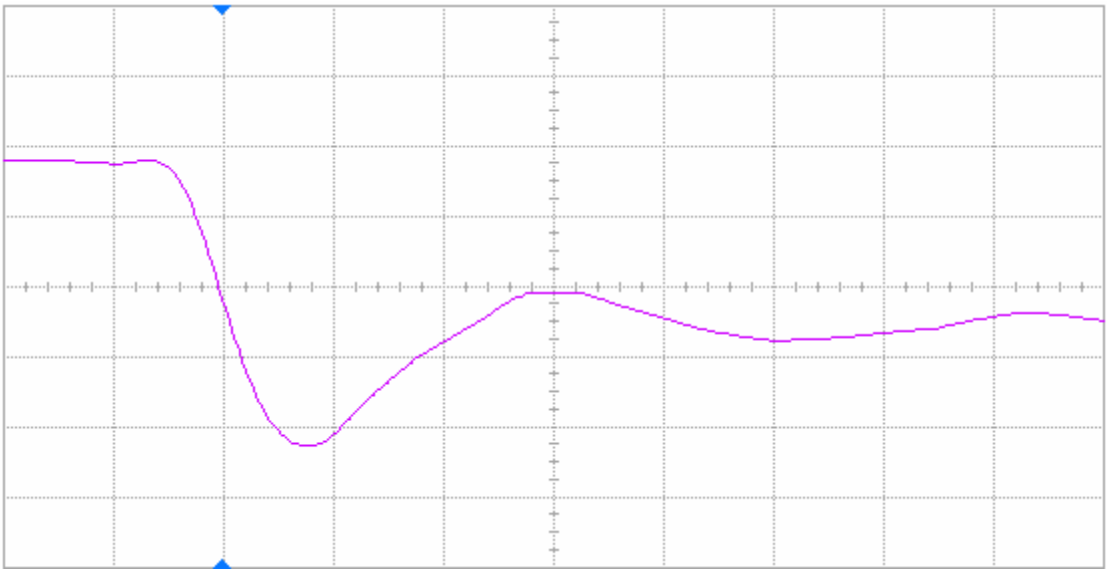


Figure 19(a) DUT 84604 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

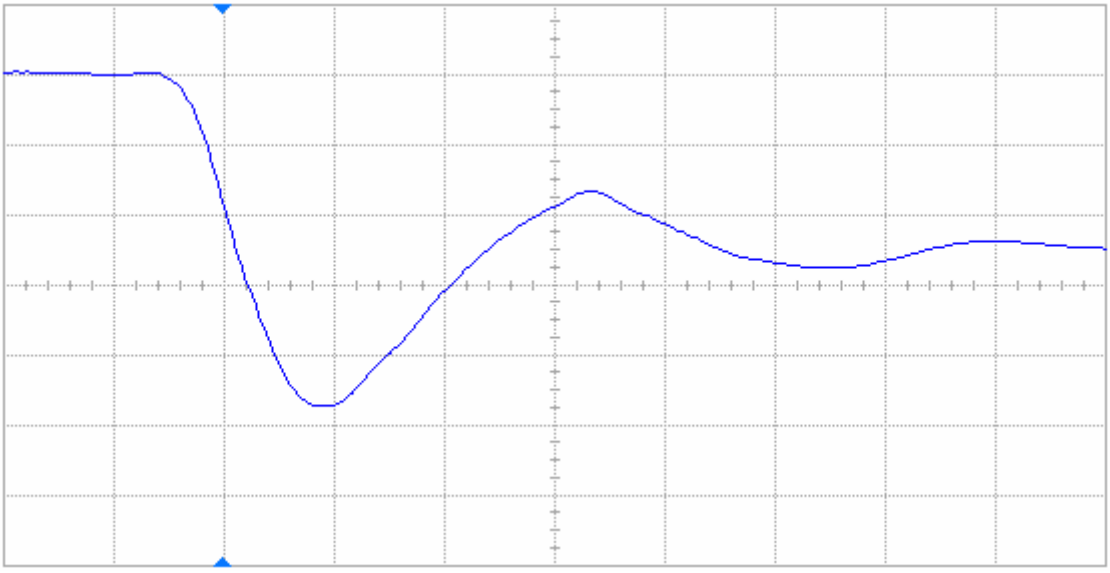
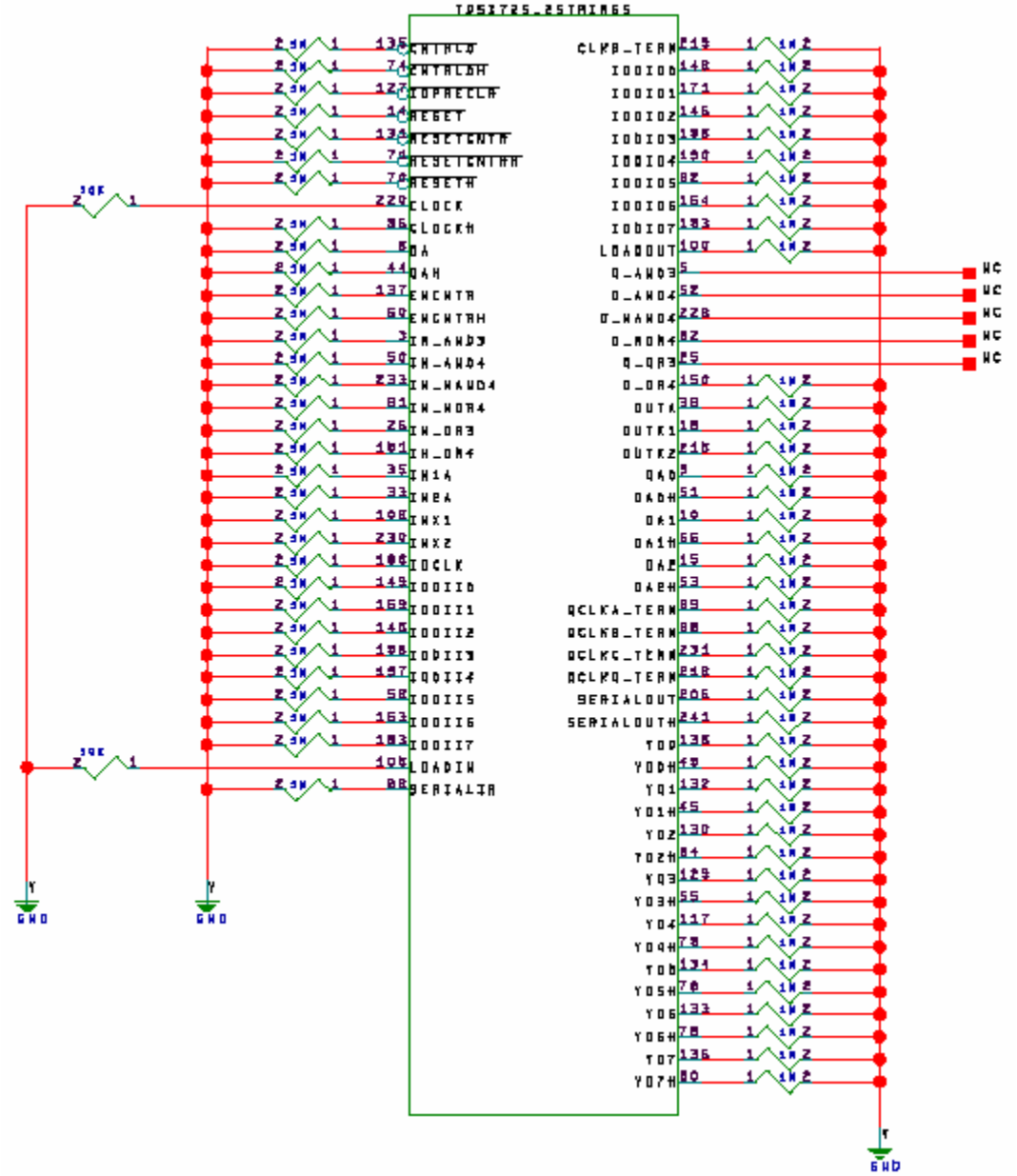
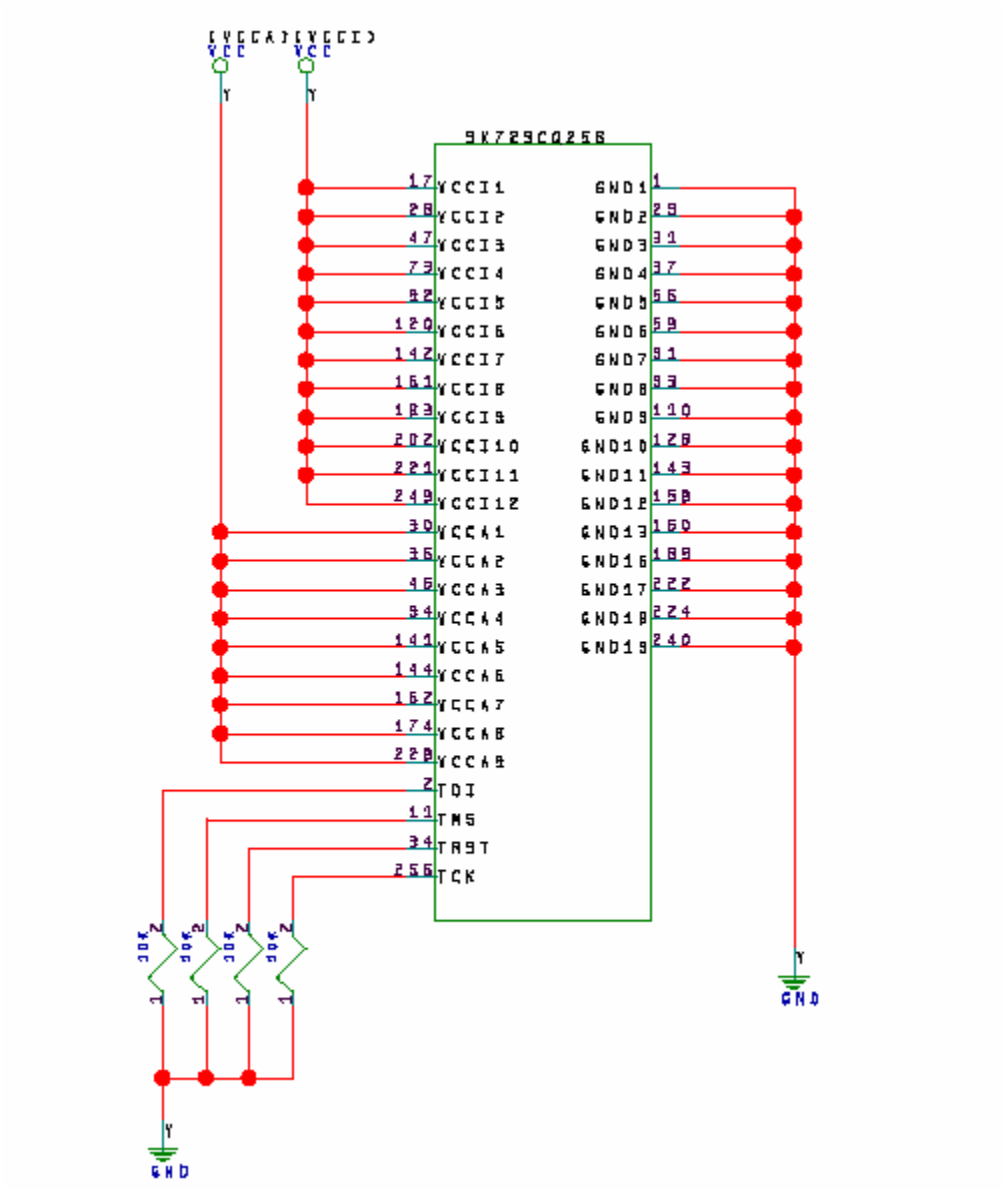


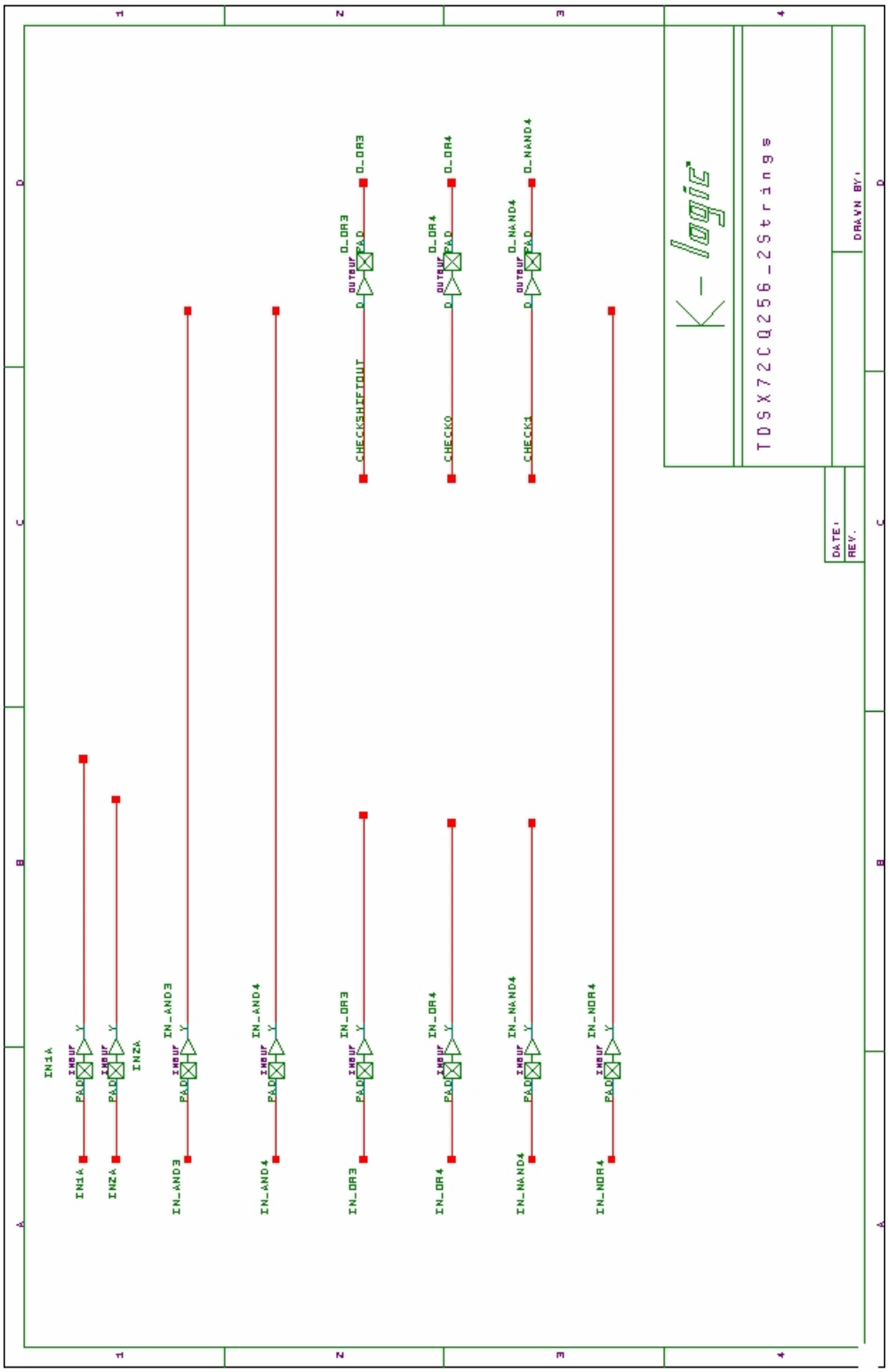
Figure 19(b) DUT 84604 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

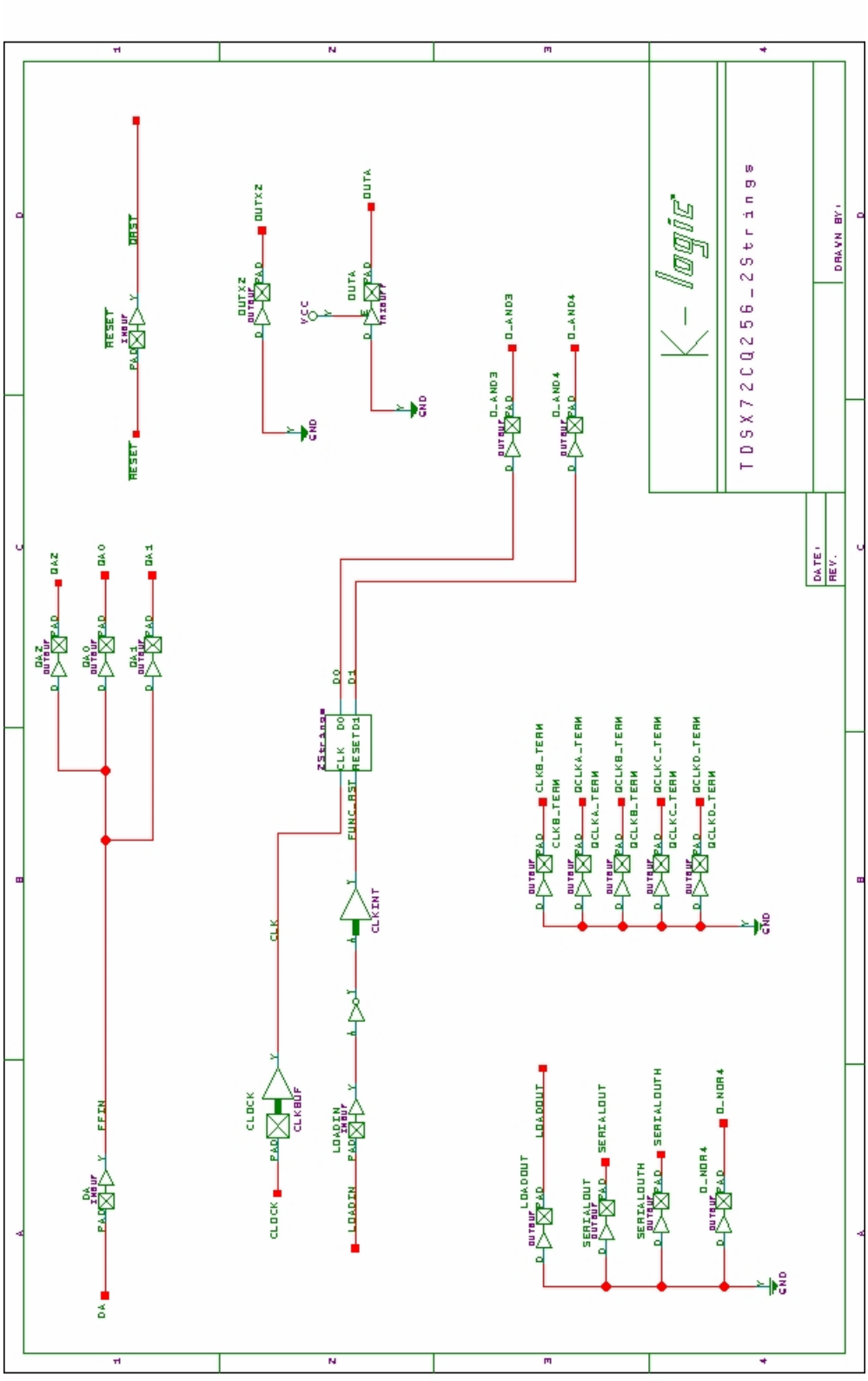
Appendix A DUT Bias

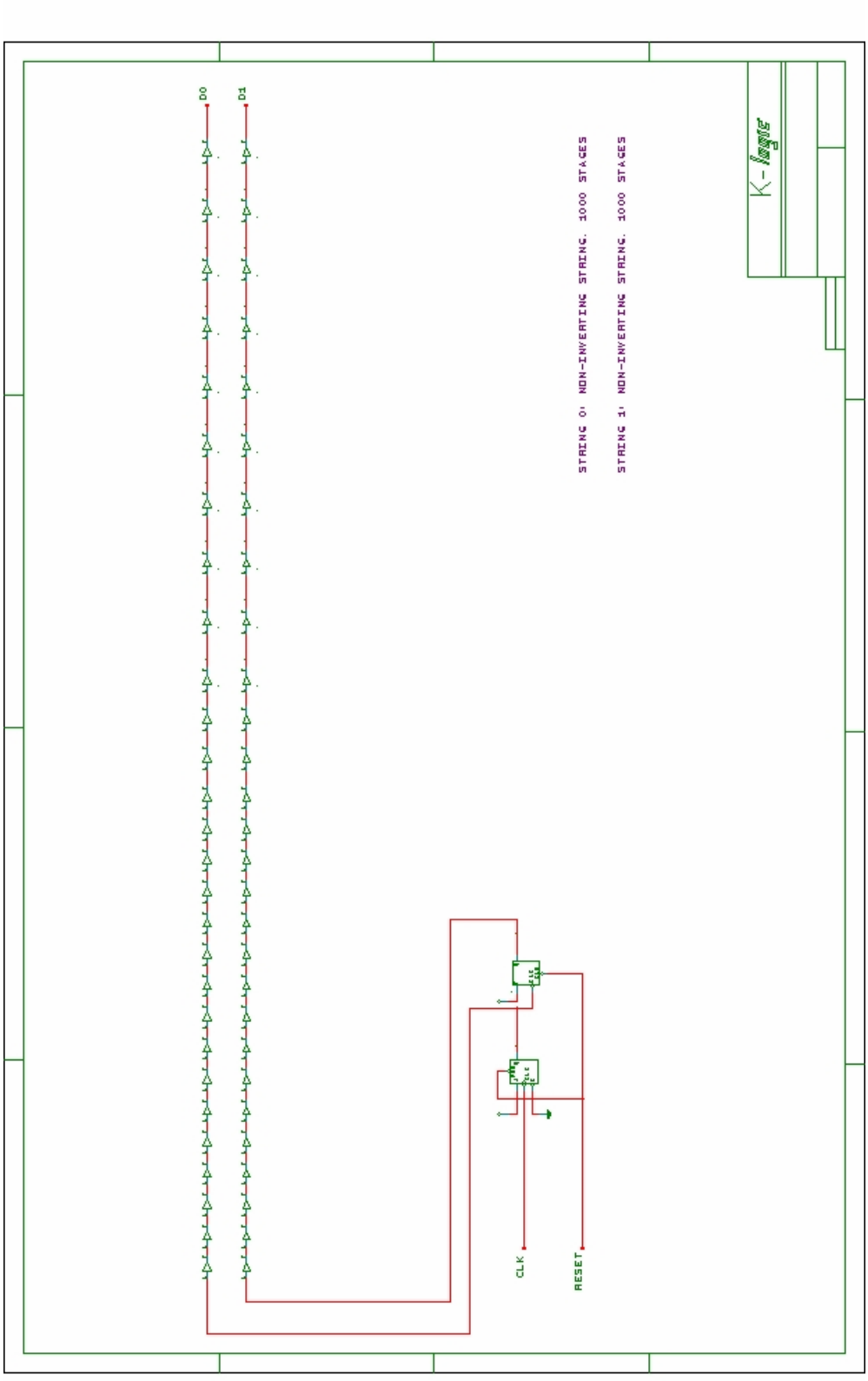


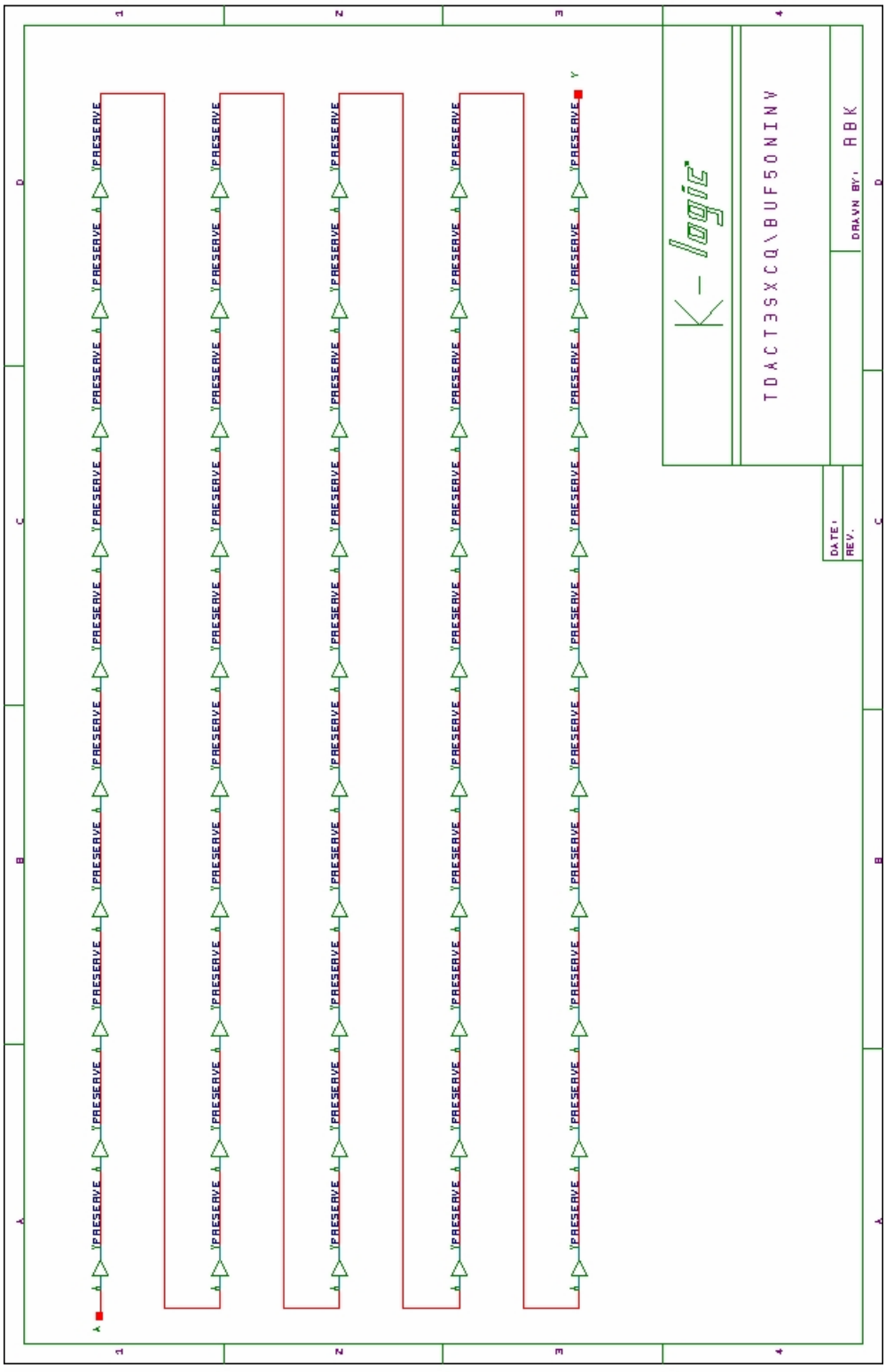

XC9572XL-VQ64
VCCINT
VCCIO
VCC
VCC
GND
GND
TDI
TMS
TRST
TCK
10K
10K
10K
10K

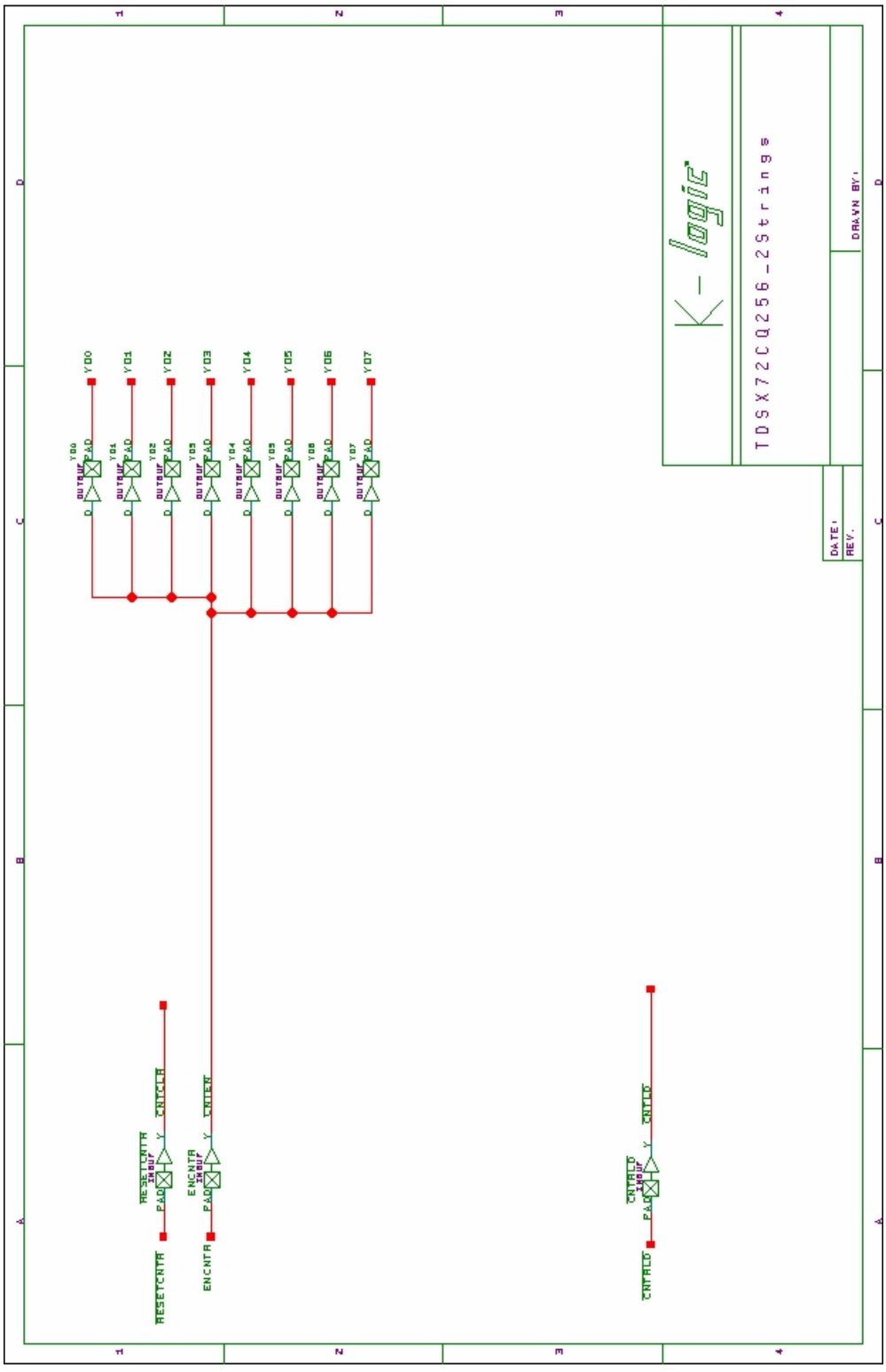
APPENDIX B DUT DESIGN SCHEMATICS

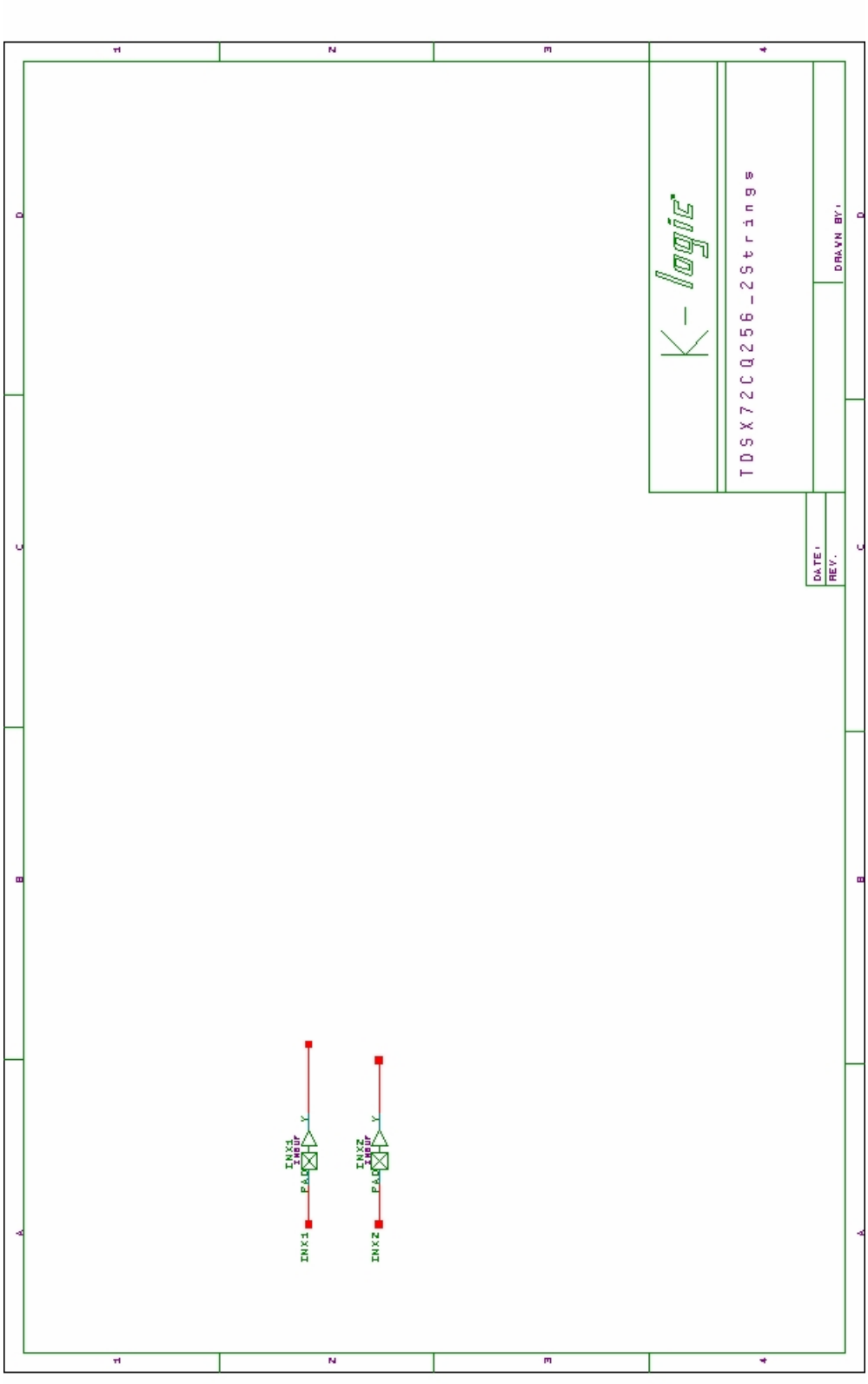


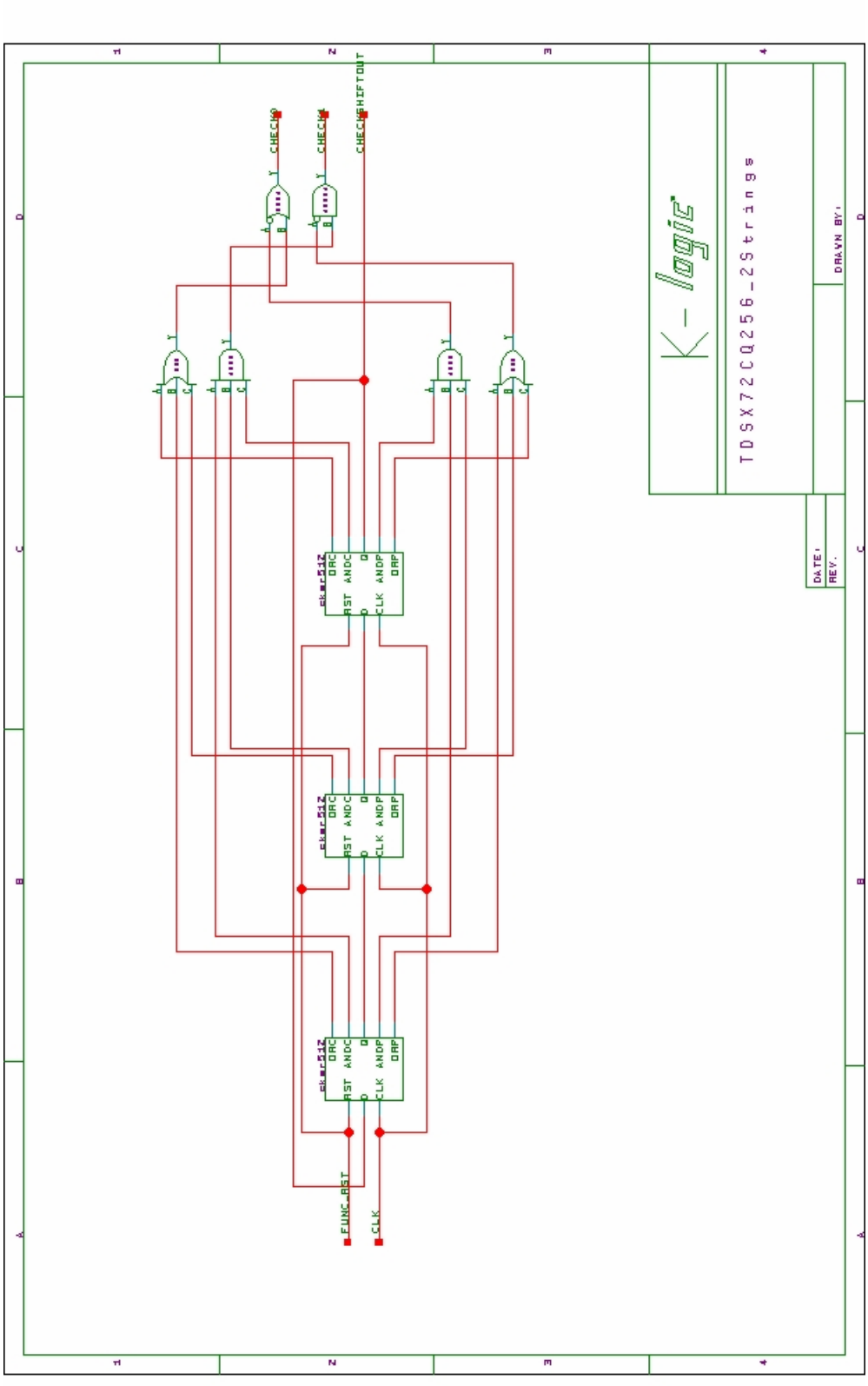

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
CLOCK
CLKBUF
CLK
CLKINT
LOADIN
2Strings
CLK D0 D1
RESET
FUNC_RST
CLKB_TERM
CLKA_TERM
CLKC_TERM
CLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

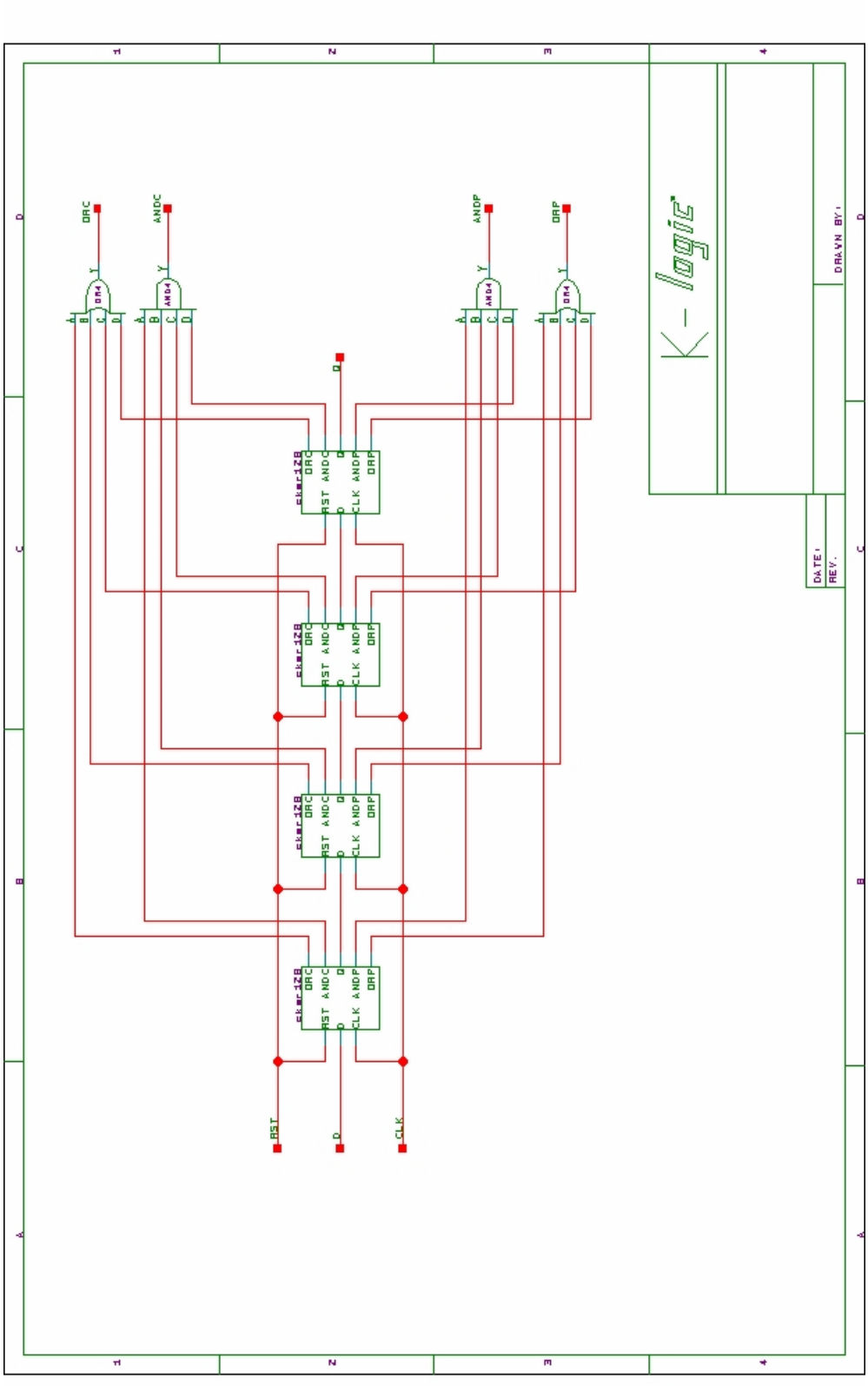

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-logic
CLK
RESET

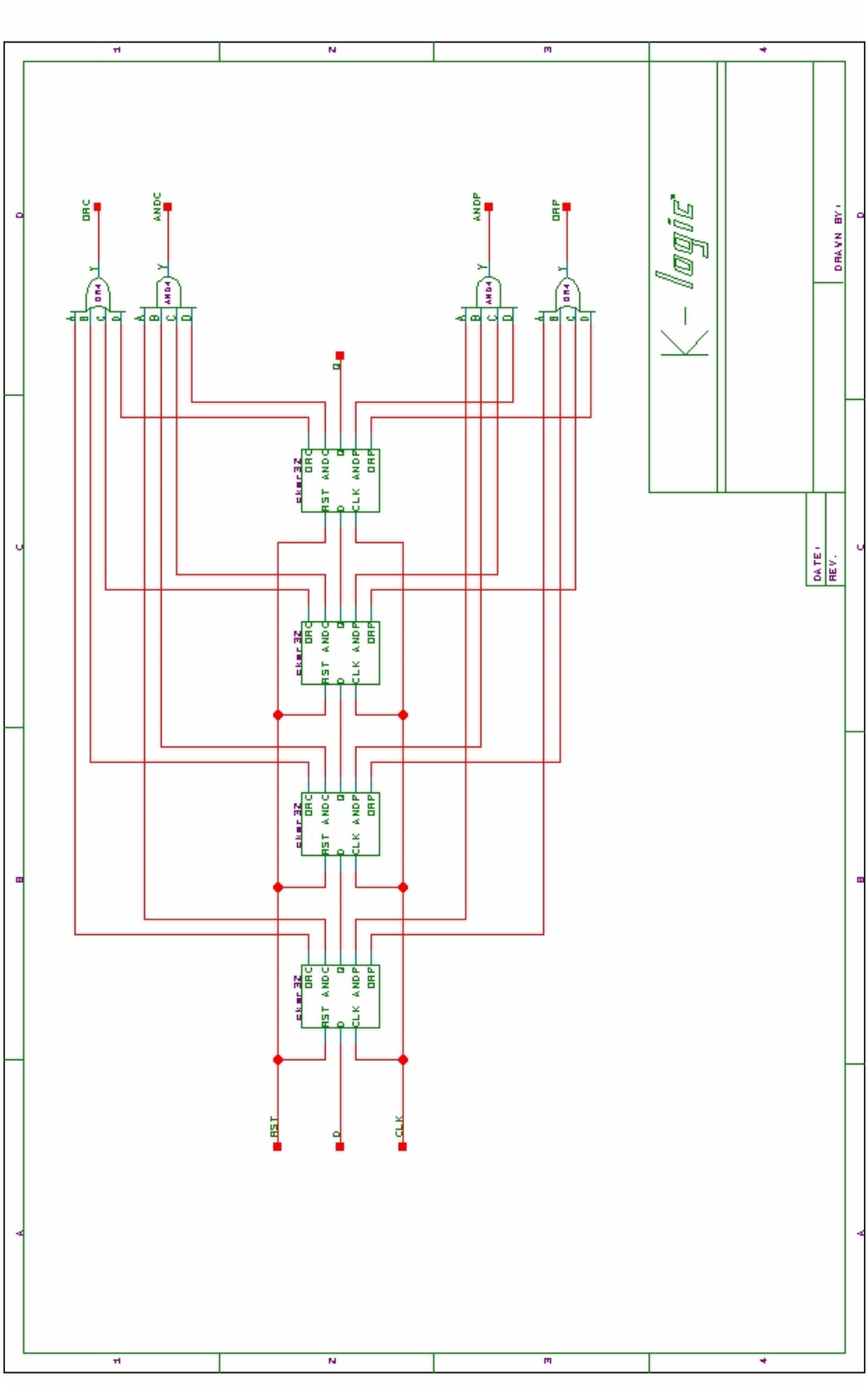

K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
PRESERVE

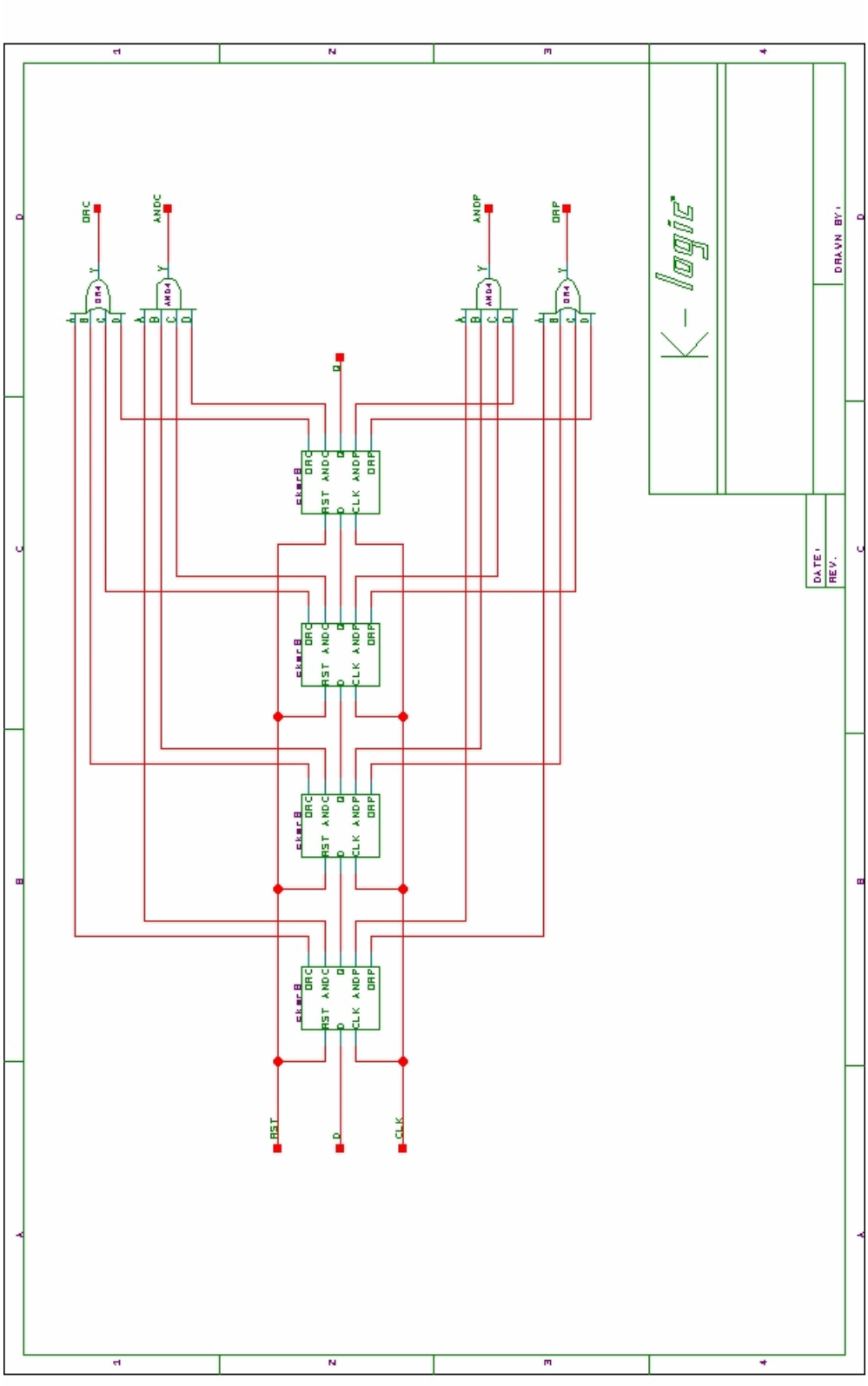

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0
YD1
YD2
YD3
YD4
YD5
YD6
YD7
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRLCR
CNTRLEN
CNTRLDO
CNTRLDO

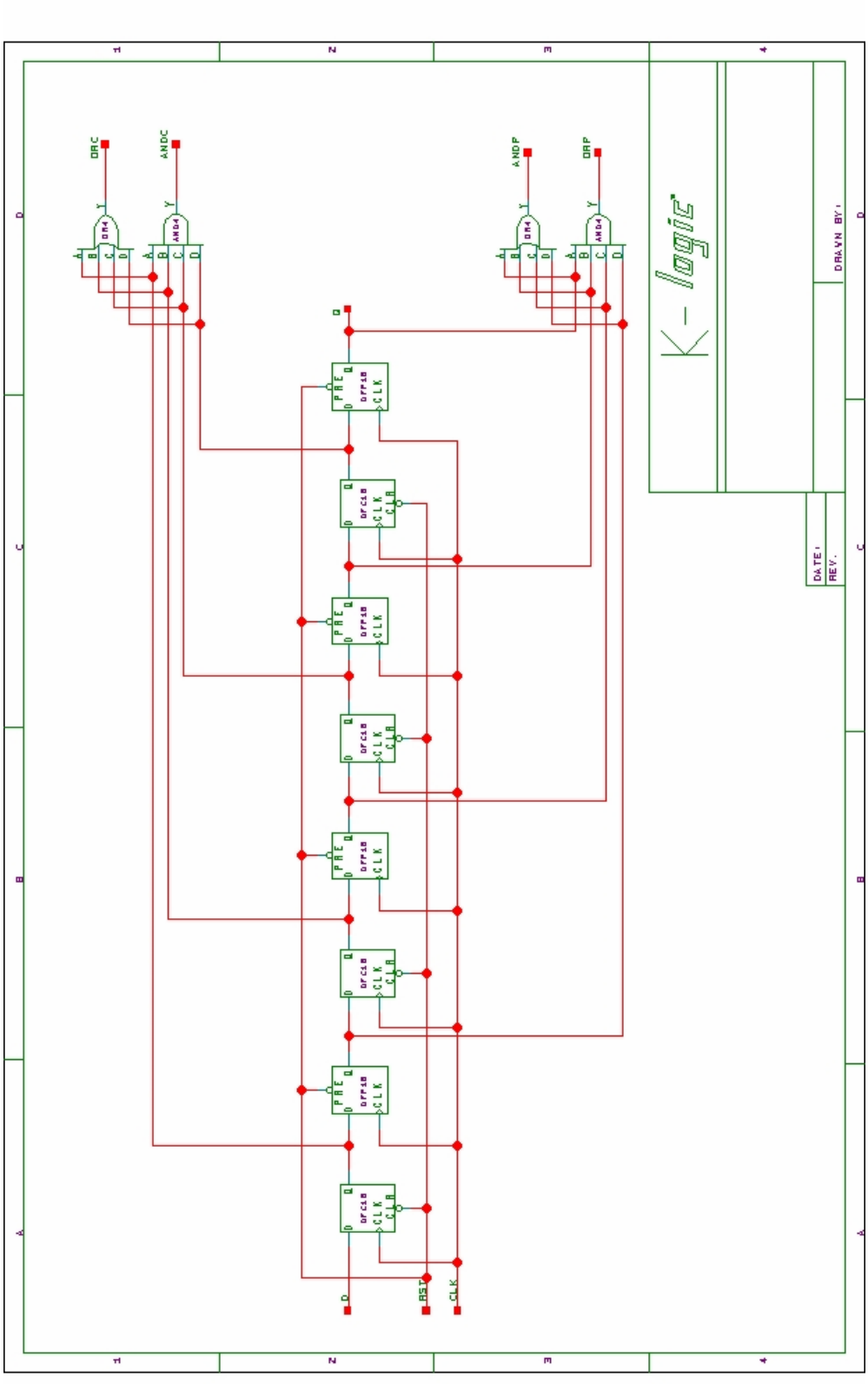

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

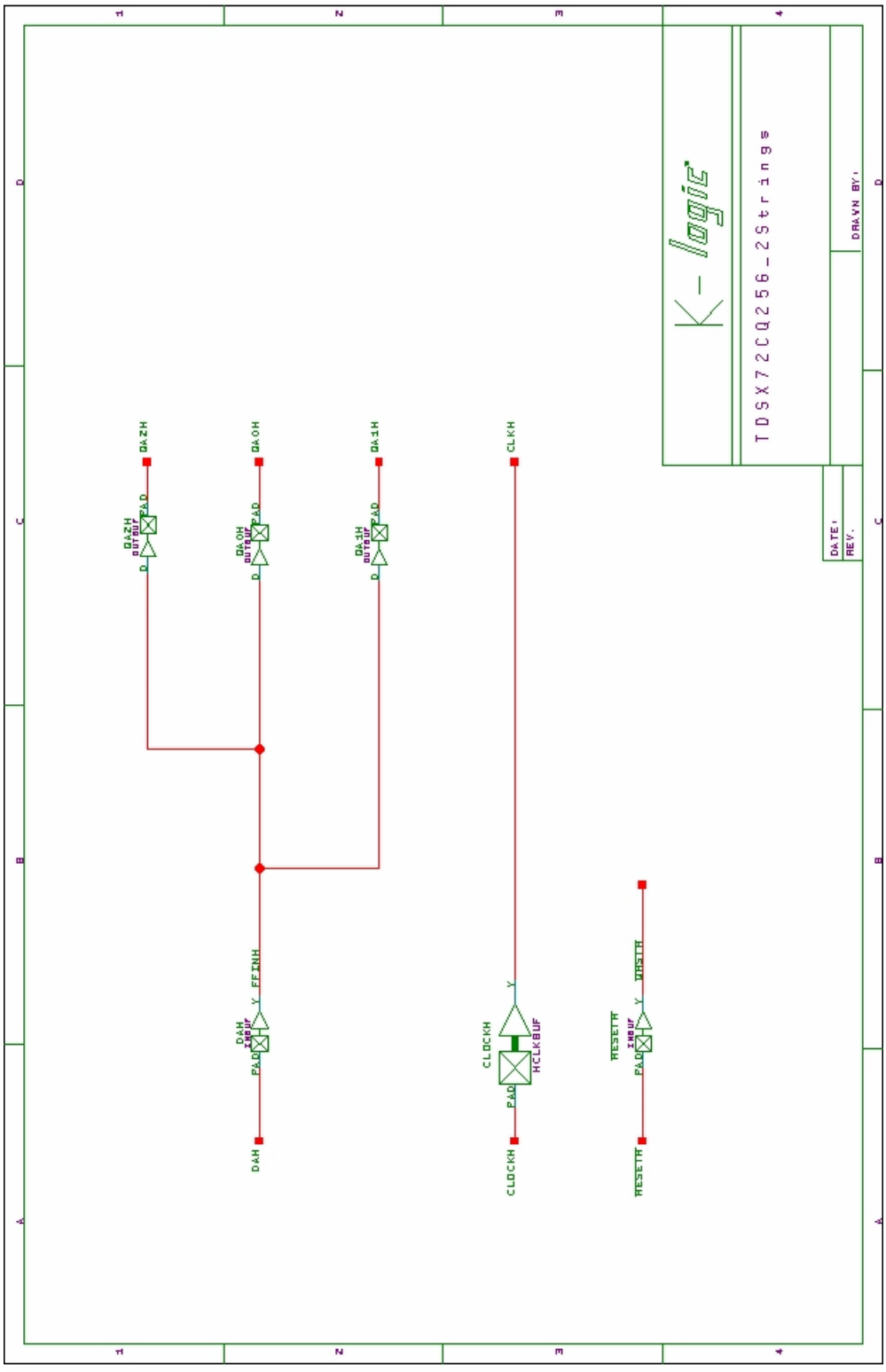

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECK0
CHECK1
CHECKSHIFTOUT
FUNC_RST
CLK

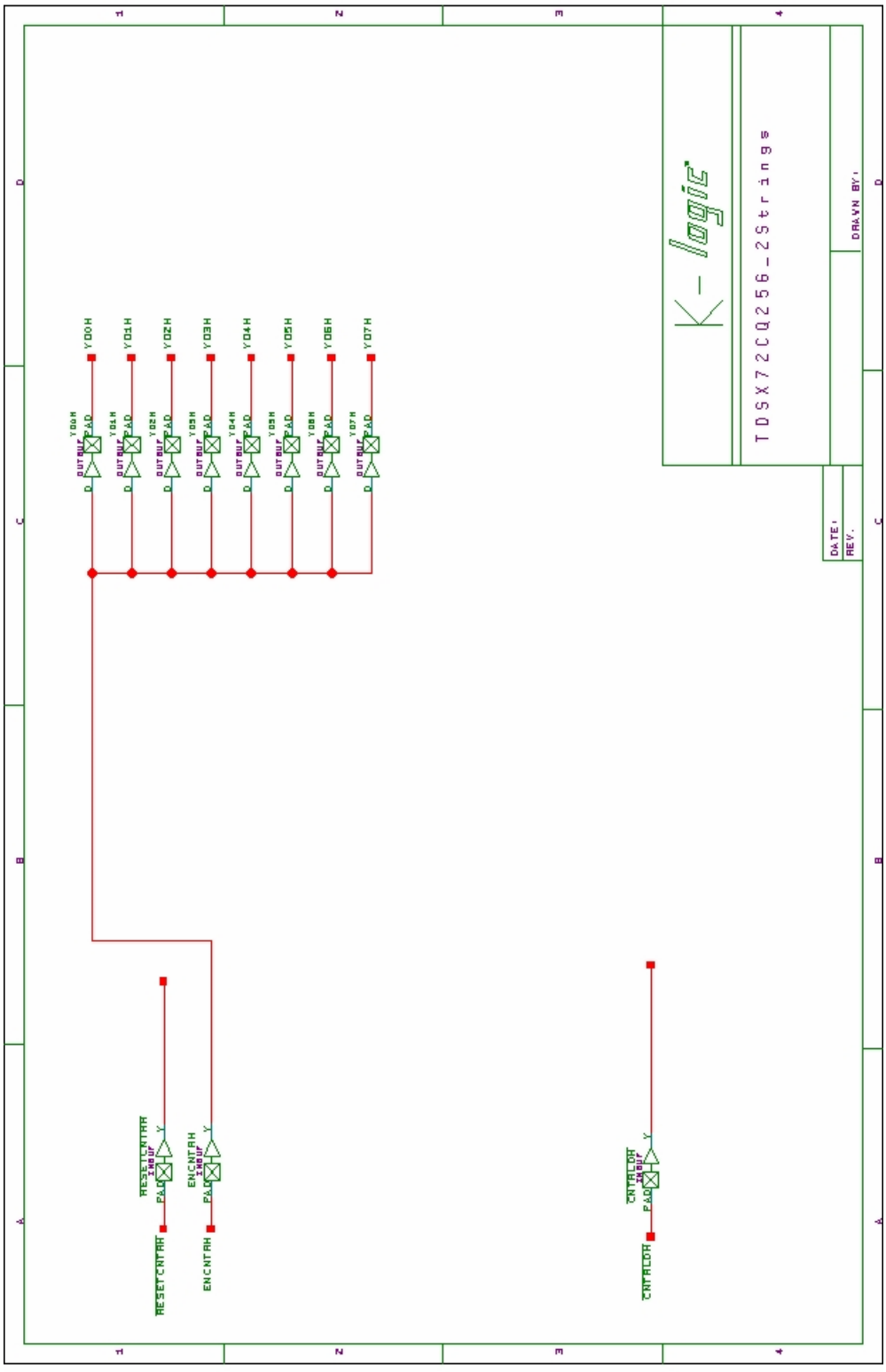

DRC
ANDC
ANDP
DRP
AND4
Y
A
B
C
D
fdrc4ce
RST
CLK
Q
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

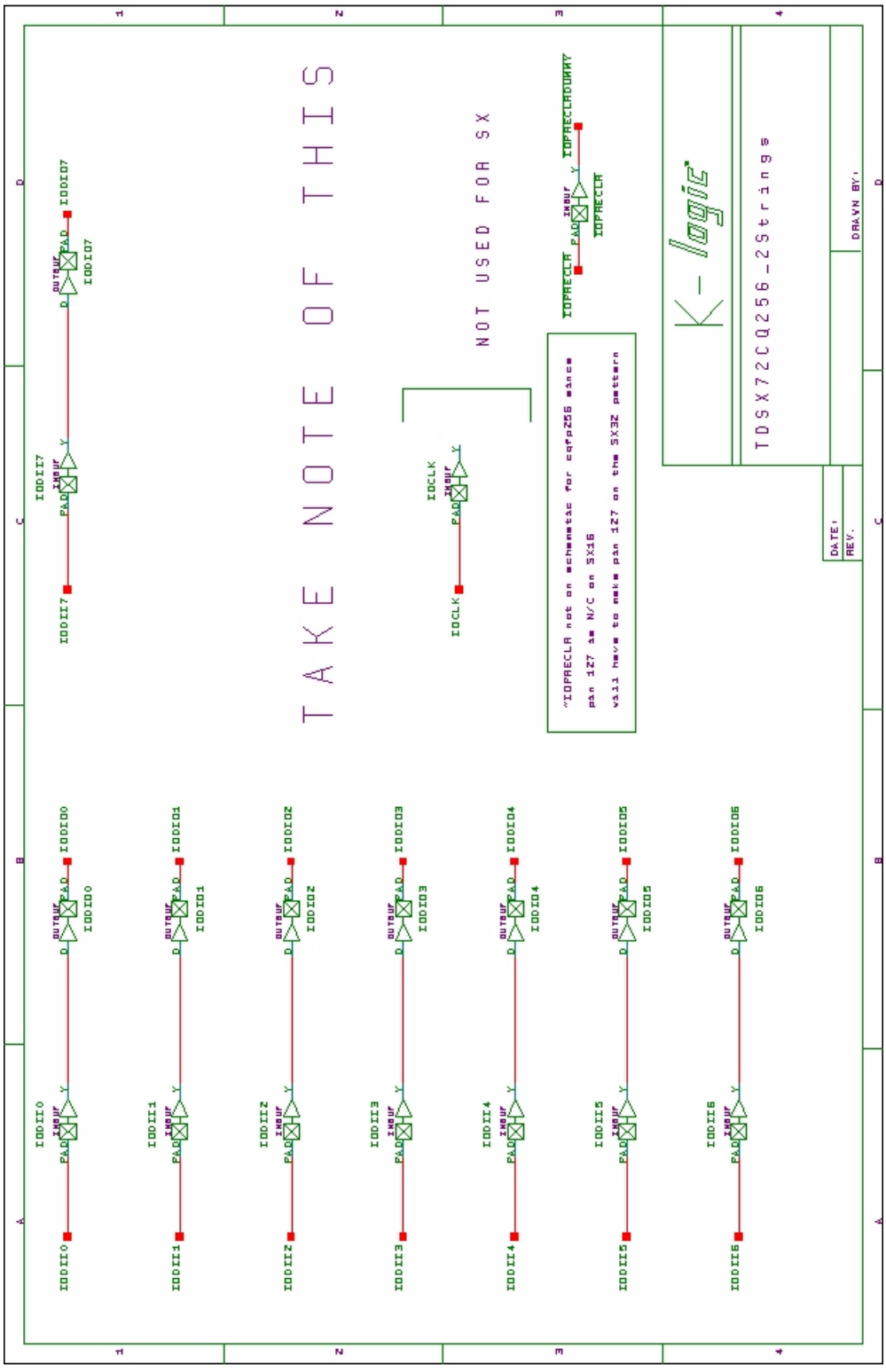

K - logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDP
DRP
AND4
OR4
fskr3Z
RST
CLK
D
Q

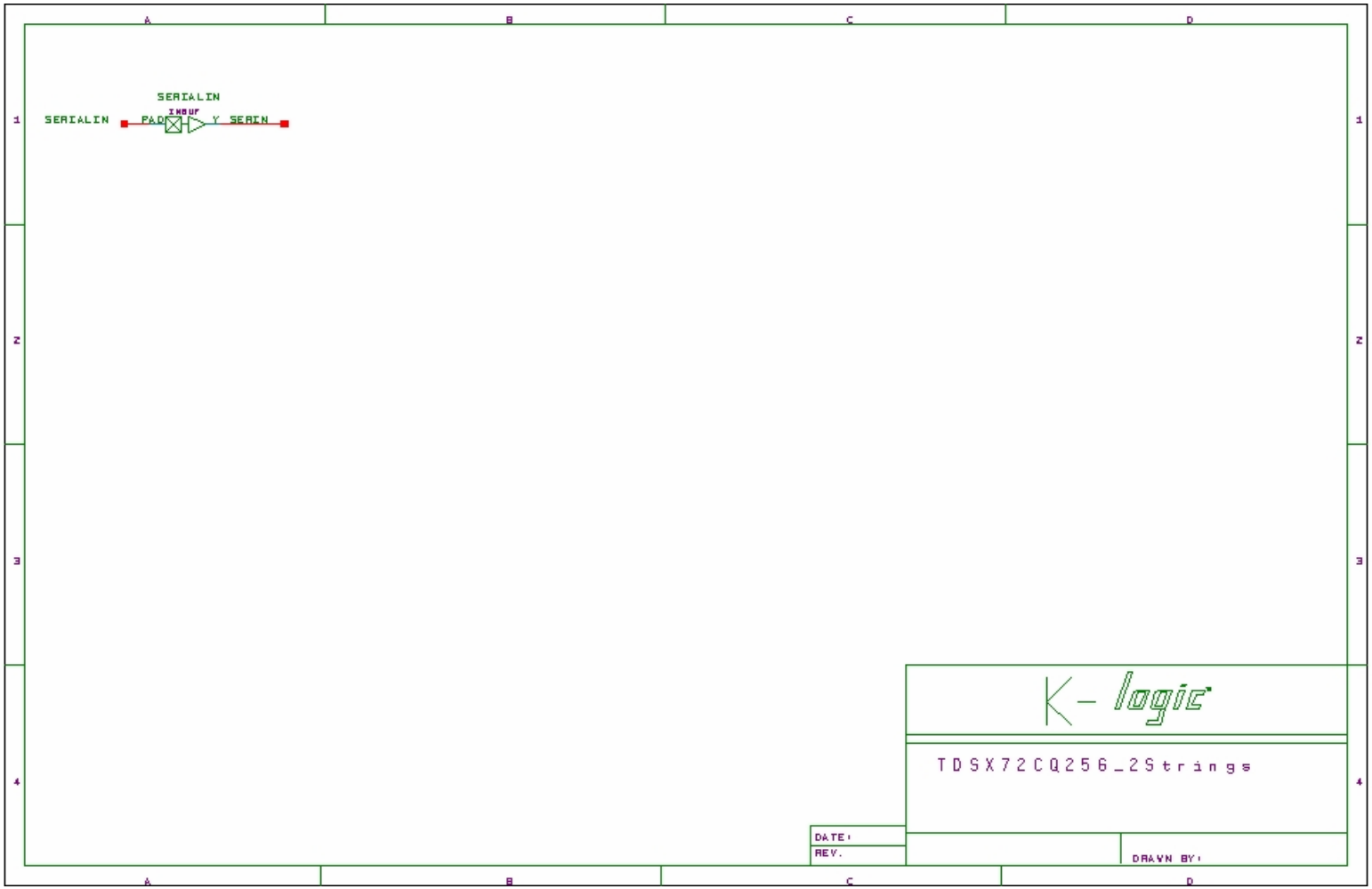

DRC
ANDC
ANDP
DRP
AND4
Y
A
B
C
D
Q
Ckmr8
DRC
ANDC
ANDP
DRP
RST
CLK
D
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

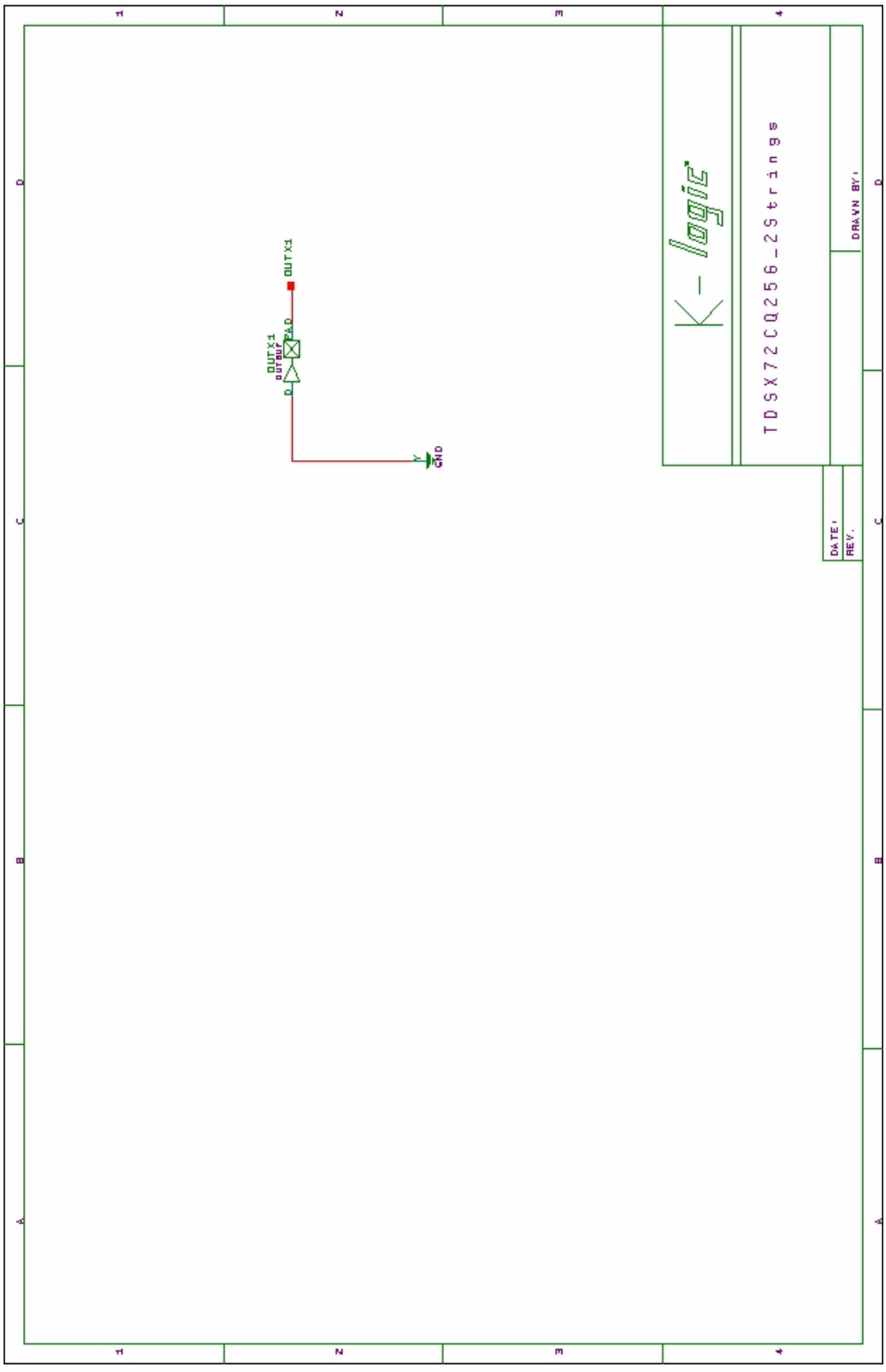

K- logic
DRAWN BY:
DATE:
REV.
ANDC
ANDF
ORC
ORF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF
DA0H OUTBUF
DA1H OUTBUF
PAD
D
DAH IMBUF
Y FFINH
DAH
CLOCKH
Y
HCLKBUF
RESETH
RESETH IMBUF
Y WRSTH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
RESETCNTAR
ENCNTAR
CNTALCOH


TAKE NOTE OF THIS
NOT USED FOR SX
IOPRECLR not on schematic for csfp256 mance
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.


A
B
C
D
1
2
3
4
SERIALIN
SERIALIN
IMBUF
PAD
Y
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
PAD
GND