TOTAL IONIZING DOSE TEST REPORT

No. 04T-RTSX72SU-D1AYH1
December 15, 2004
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad (Si)
2. Power Supply Current (I_{CCA}/I_{CCI})	Passed 67.2 krad (Si) per 25-mA spec. Post 100 krad (Si) and after 10 days room temperature annealing: average I_{CCA} = 71.6 mA; average I_{CCI} = 122.8 mA.
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad (Si)
4. Output Drive (V_{OL}/V_{OH})	Passed 100 krad (Si)
5. Propagation Delay	Passed 100 krad (Si) per 10% degradation criterion
6. Transition Time	Passed 100 krad (Si)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the base of an extensive database (see, for example, TID data of antifuse-based FPGA in http://www.actel.com/ and http://www.klabs.org/) accumulated from the TID testing of many generations of antifuse-based FPGAs. One distinctive quality about this testing is the bench measurement of electrical parameters. Compared to an automatic-tester measurement, the bench measurement provides lower noise, better accuracy and more flexibility. The bench measurement samples pins for some measurements (e.g. threshold voltage measurement). However, since the tolerance is determined by the most degraded parameter, which is I_{CC} or propagation delay, sampling the pins for measuring non-critical parameters is appropriate.

A. Device Under Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input or output is grounded through a 1-M ohm resistor; during annealing each input or output is grounded through a 1-k ohm resistor. Appendix A contains the schematics of the bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTSX72SU
Package	CQFP256
Foundry	United Microelectronics Corp.
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	D1AYH1
Quantity Tested	5
Serial Number	60456, 60574, 60578, 60580, 60588
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad (Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

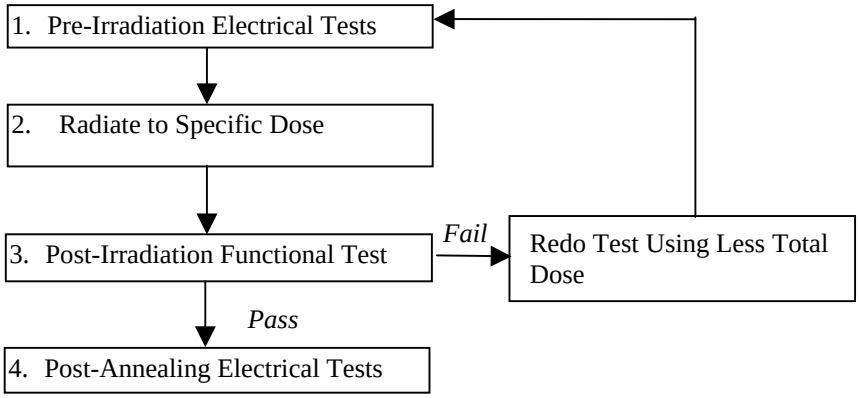


Figure 1 Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 is the flow chart showing the steps for parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019 is unnecessary because there is no adverse time dependent effect (TDE) in products manufactured by sub-micron CMOS technology. To prove this point, test data using a high dose rate (1 krad (Si)/min) are compared with test data using a low dose rate (1 krad (Si)/hr) for devices manufactured by several generations of sub-micron CMOS technologies. Since the results always show the low-dose-rate degradation less than the high-dose-rate degradation, the elevated rebound annealing would artificially improve the electrical parameters. Therefore, only room temperature annealing is performed in this report. DUTs are biased annealed at room temperature for 10 days after the 100-krad (Si) irradiations.

C. Design and Parametric Measurements

DUTs use a high utilization generic design (TDSX72CQ256_2Strings) to test total dose effects in typical space applications. Appendix B contains the schematics illustrating the logic design.

Table 2 lists each electrical parameter and the corresponding logic design. The functionality is measured on the output pins (O_AND3 and O_AND4) of two combinational buffer-strings with 1400 buffers each and output pins (O_OR4 and O_NAND4) of a shift register with 1536 bits. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively. The input logic thresholds (V_{TIL}/V_{IH}) and output-drive voltages (V_{OL}/V_{OH}) are measured on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured on the O_AND4 output of one buffer string. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the output O_AND4. Both the low-to-high and high-to-low output transitions are measured; the propagation delay is defined as the average of these two transitions. The transition characteristics, measured on the output O_AND4, are displayed as oscilloscope snapshots showing the rising and falling edge during logic transitions.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Characteristic	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passes the pre-irradiation, post-irradiation, and post-annealing functional tests.

B. *Power Supply Current (I_{CCA} and I_{CCI})*

Since the pre-irradiation I_{CCA} and I_{CCI} of every DUT are below 1 mA, the in-flux I_{CC}-plots of Figure 2 to Figure 6 basically show the radiation-induced leakage current. The room-temperature annealing effect on I_{CC} is shown by Table 3, where the post-annealing data compares with the post-irradiation data.

Table 3. Post Irradiation and Post-Annealing I_{CC}

DUT	I_{CCA} (mA)		I_{CCI} (mA)	
	Post-rad	Post-ann	Post-rad	Post-ann
60456	40.2	38	51.3	35
60574	215.3	75	172.1	132
60578	240.9	76	187.5	137
60580	262	86	202	150
60588	241.4	83	174.4	160

An empirical equation is used to extract the total dose tolerance per the 25 mA-I_{CC} specification. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux currents when total dose equals to γ. Using the-worst-case in-flux currents degradation, DUT 60580 (Figure 4), the tolerance ($\gamma_{critical}$) is obtained as approximately 67.2 krad (Si).

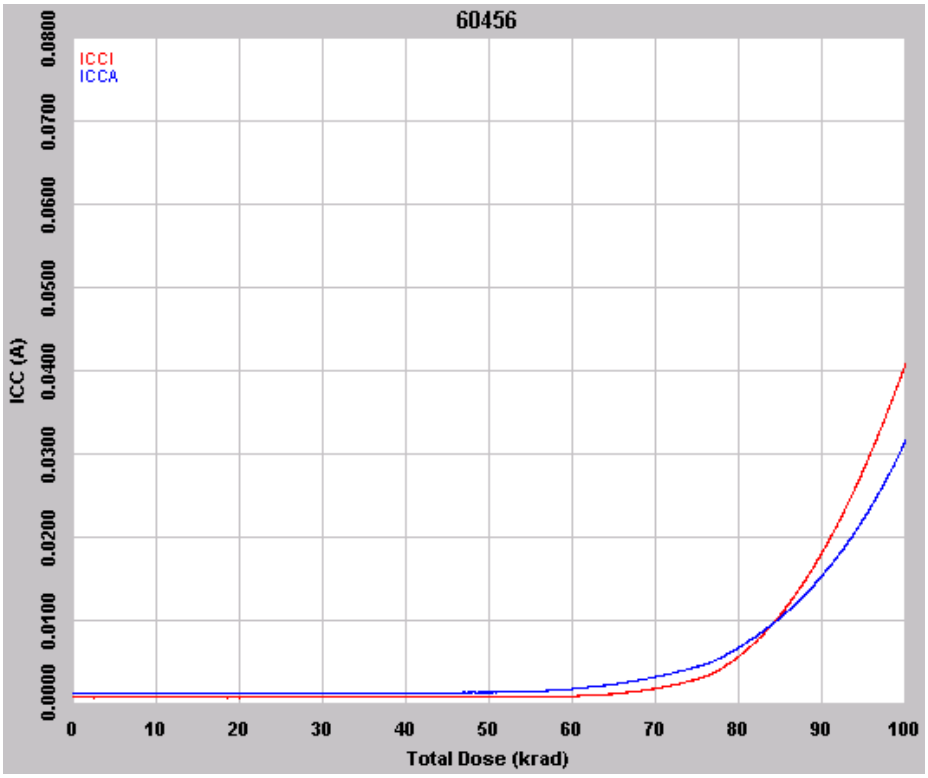


Figure 2 DUT 60456 in-flux I_{CCA} and I_{CCI}

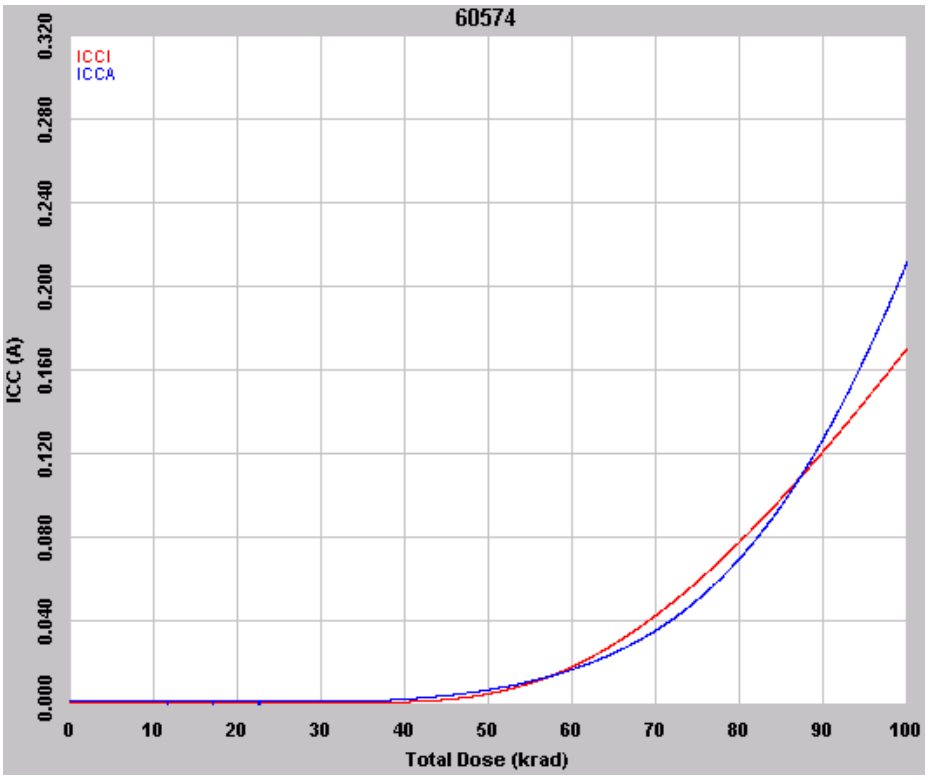


Figure 3 DUT 60574 in-flux I_{CCA} and I_{CCI}

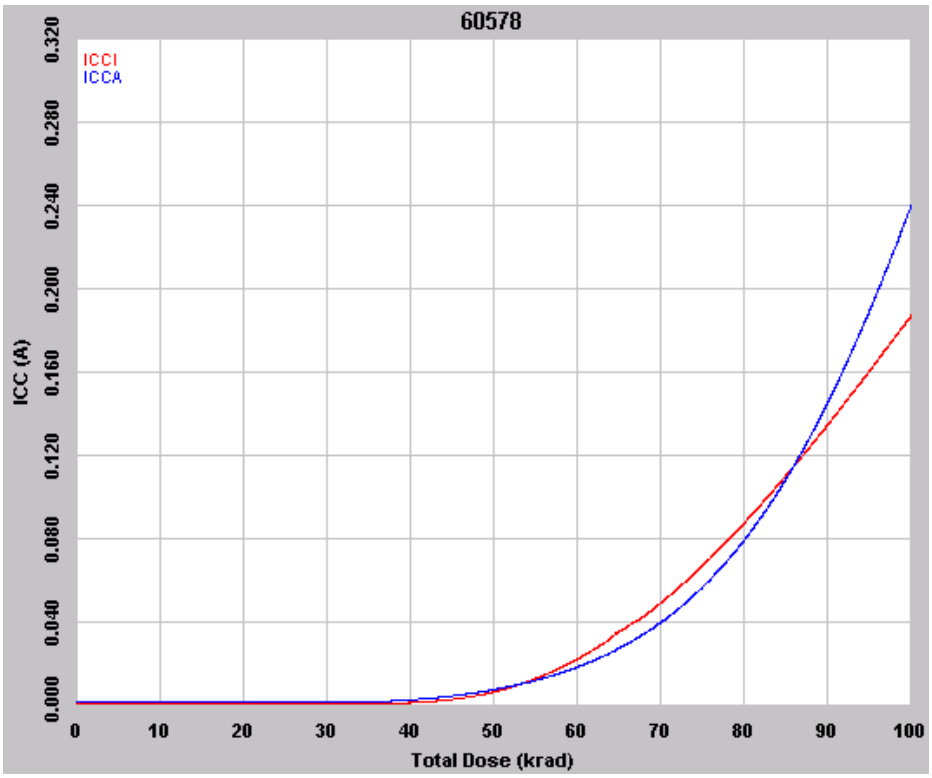


Figure 4 DUT 60578 in-flux I_{CCA} and I_{CCI}

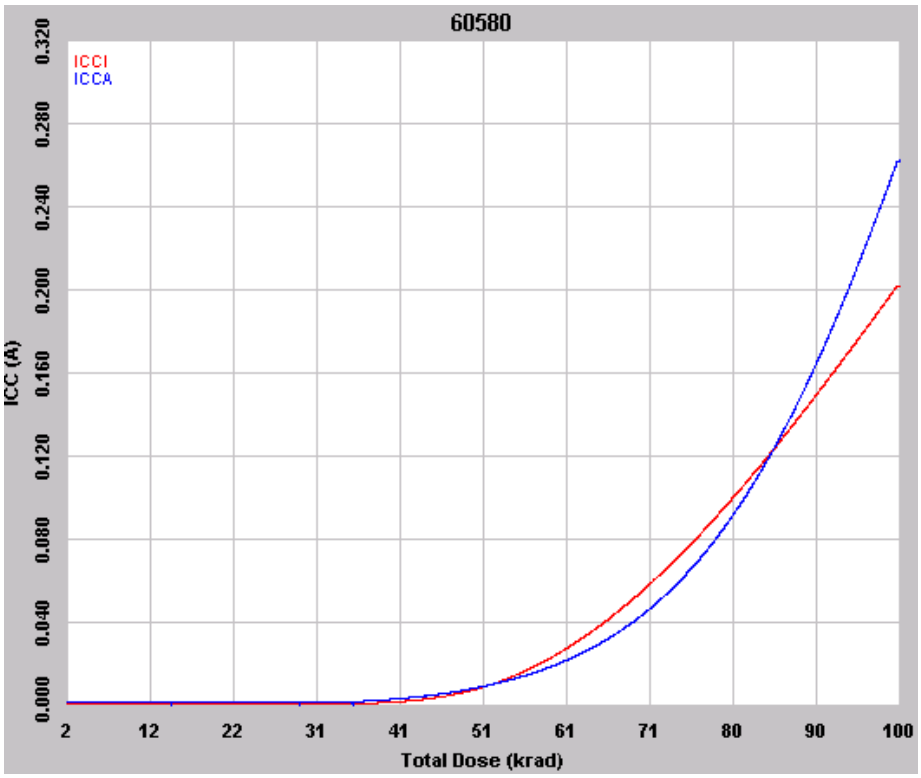


Figure 5 DUT 60580 in-flux I_{CCA} and I_{CCI}

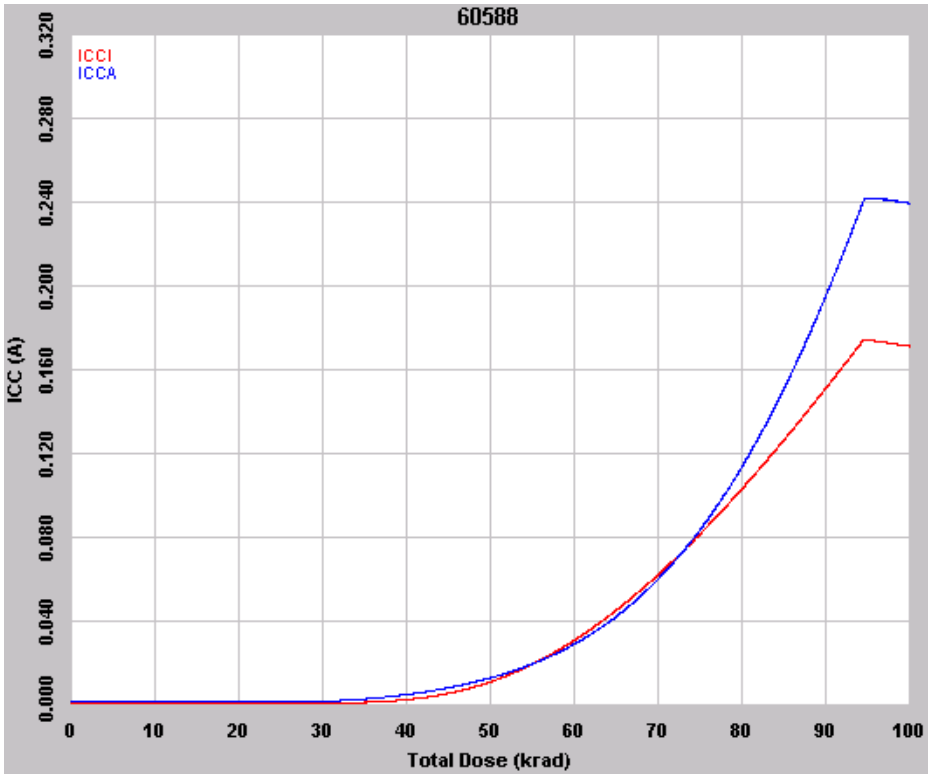


Figure 6 DUT 60588 in-flux I_{CCA} and I_{CCI}, note that the offset of peak currents from 100 krad is due to a recording error

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-Irradiation and Post-Annealing Input Thresholds

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL} (V)	V_{IH} (V)	V_{IL} (V)	V_{IH} (V)
60456	1.33	1.50	1.33	1.48
60574	1.31	1.47	1.37	1.52
60578	1.33	1.49	1.27	1.50
60580	1.32	1.48	1.34	1.51
60588	1.32	1.48	1.34	1.49

D. *Output-Drive Voltage (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in Tables 5 and 6. The post-annealing data are within the spec limits; in each case, the post-annealing data varies minutely with respect to the pre-irradiation data.

Table 5 Pre-Irradiation and Post-Annealing V_{OL} (V) at Various Sinking Current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
60456	0.008	0.009	0.100	0.102	0.167	0.169	0.421	0.425	0.865	0.872
60574	0.008	0.009	0.101	0.105	0.168	0.174	0.425	0.439	0.873	0.902
60578	0.009	0.009	0.101	0.103	0.169	0.172	0.427	0.432	0.878	0.888
60580	0.008	0.009	0.101	0.102	0.169	0.171	0.426	0.430	0.876	0.883
60588	0.009	0.009	0.102	0.103	0.170	0.171	0.429	0.432	0.882	0.887

Table 6 Pre-Irradiation and Post-Annealing V_{OH} (V) at Various Sourcing Current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
60456	4.98	4.98	4.86	4.86	4.64	4.63	4.05	4.01	2.65	2.53
60574	4.98	4.98	4.86	4.85	4.65	4.62	4.06	4.01	2.71	2.49
60578	4.99	4.98	4.86	4.86	4.65	4.64	4.06	4.01	2.72	2.55
60580	4.99	4.99	4.86	4.86	4.64	4.63	4.05	4.00	2.66	2.50
60588	4.99	4.98	4.86	4.87	4.64	4.64	4.05	4.01	2.70	2.54

E. *Propagation Delay*

Table 7 lists the pre-irradiation and post-annealing propagation delays, and also lists the radiation-induced degradations in percentage. DUT 60578 has the worst degradation of 3.68%.

Table 7 Radiation-Induced Propagation Delay Degradations

DUT	Pre-Irradiation (ns)	Post-Annealing (ns)	Degradation
60456	1290.4	1309.8	1.50%
60574	1274.7	1310.2	2.81%
60578	1268.0	1315.1	3.68%
60580	1294.6	1338.4	3.42%
60588	1274.5	1317.9	3.43%

F. Transition Time

Figures 7 to 16 show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is not significant.

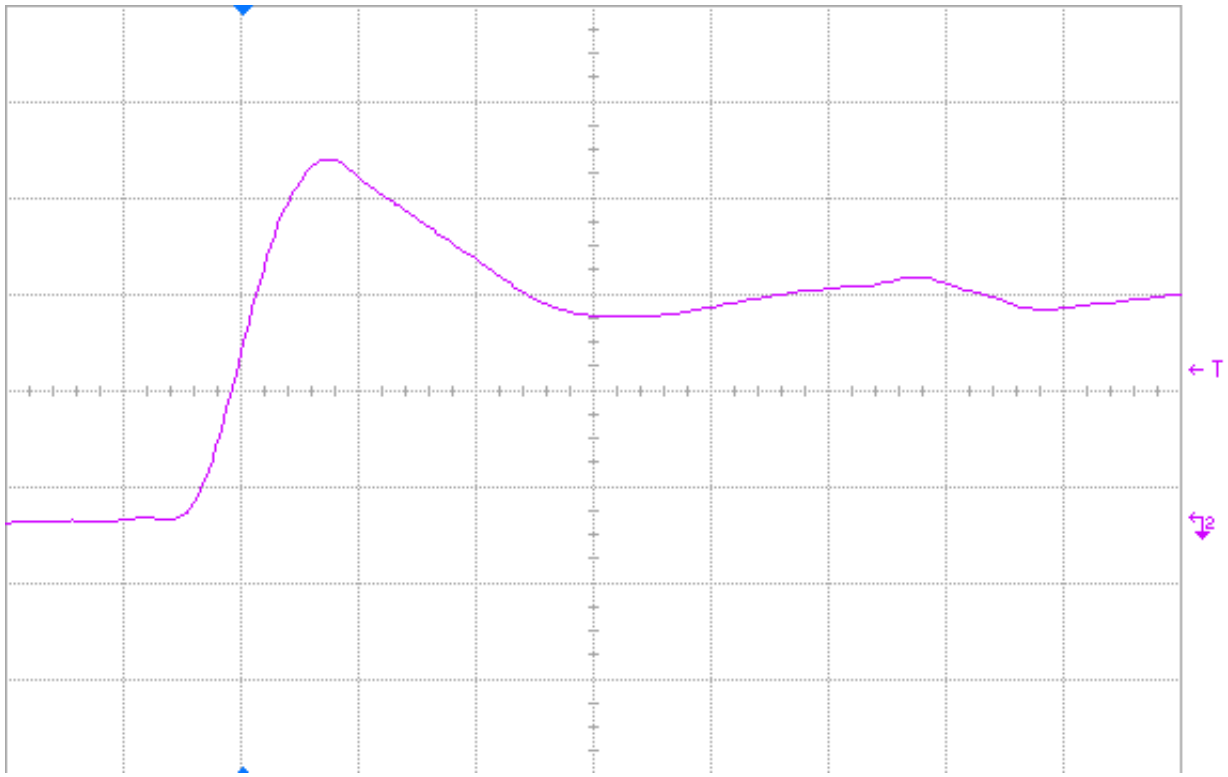


Figure 7(a) DUT 60456 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

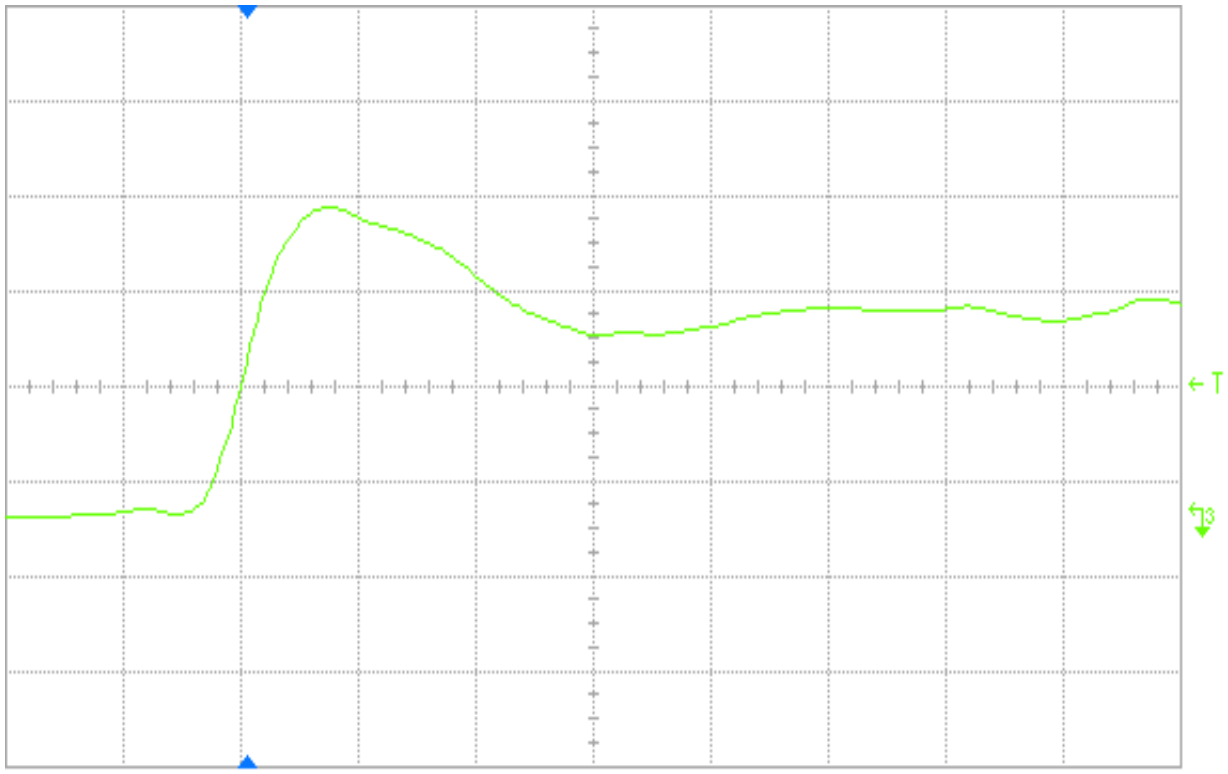


Figure 7(b) DUT 60456 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

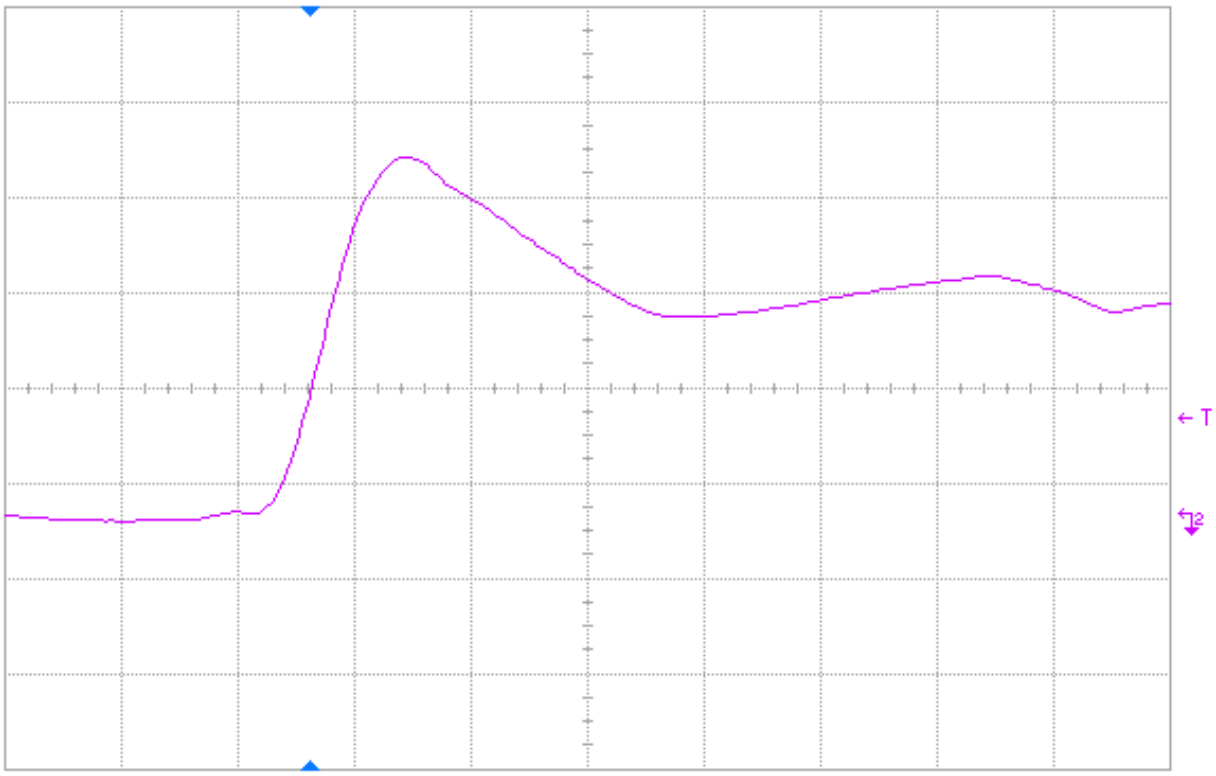


Figure 8(a) DUT 60574 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

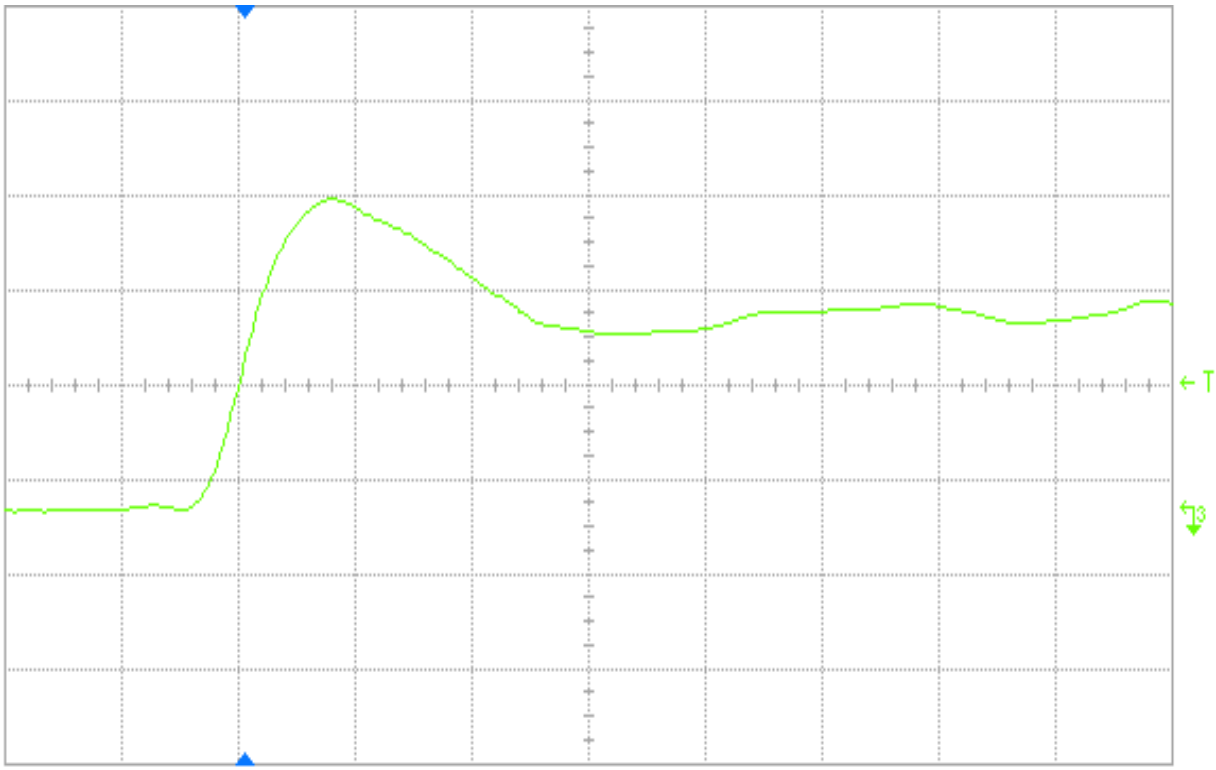


Figure 8(b) DUT 60574 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

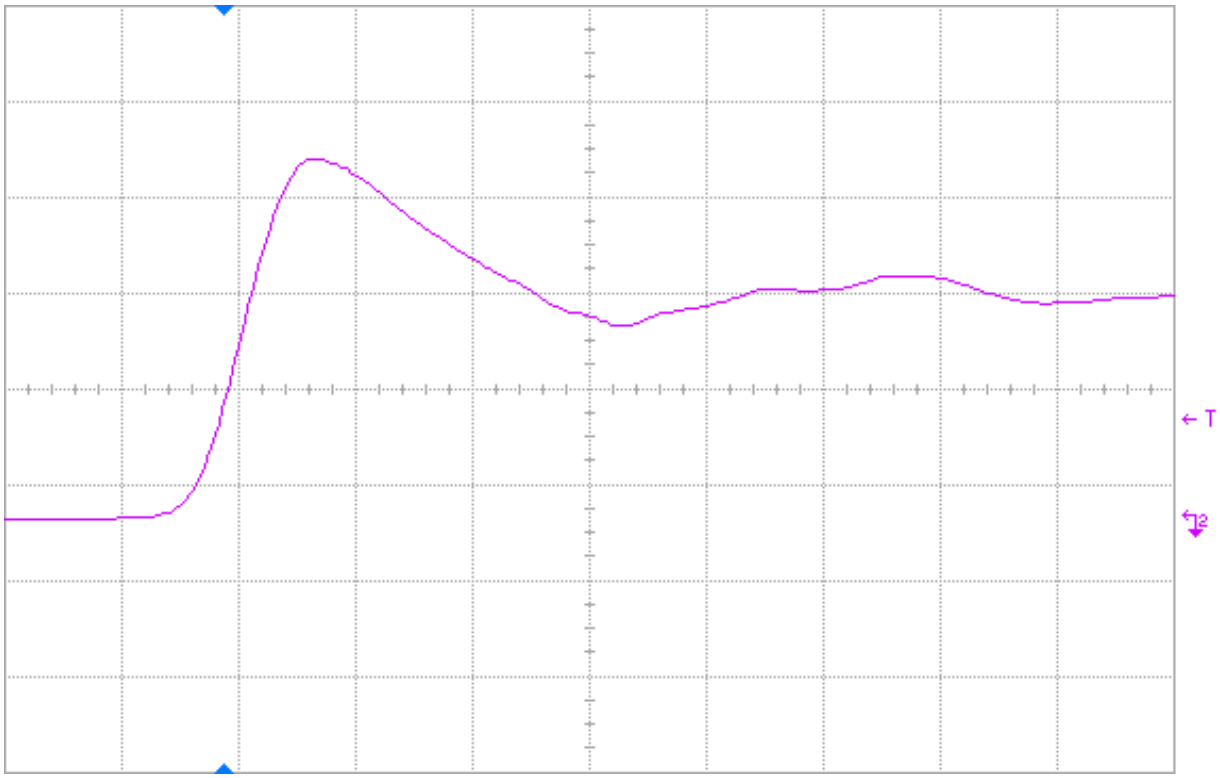


Figure 9(a) DUT 60578 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

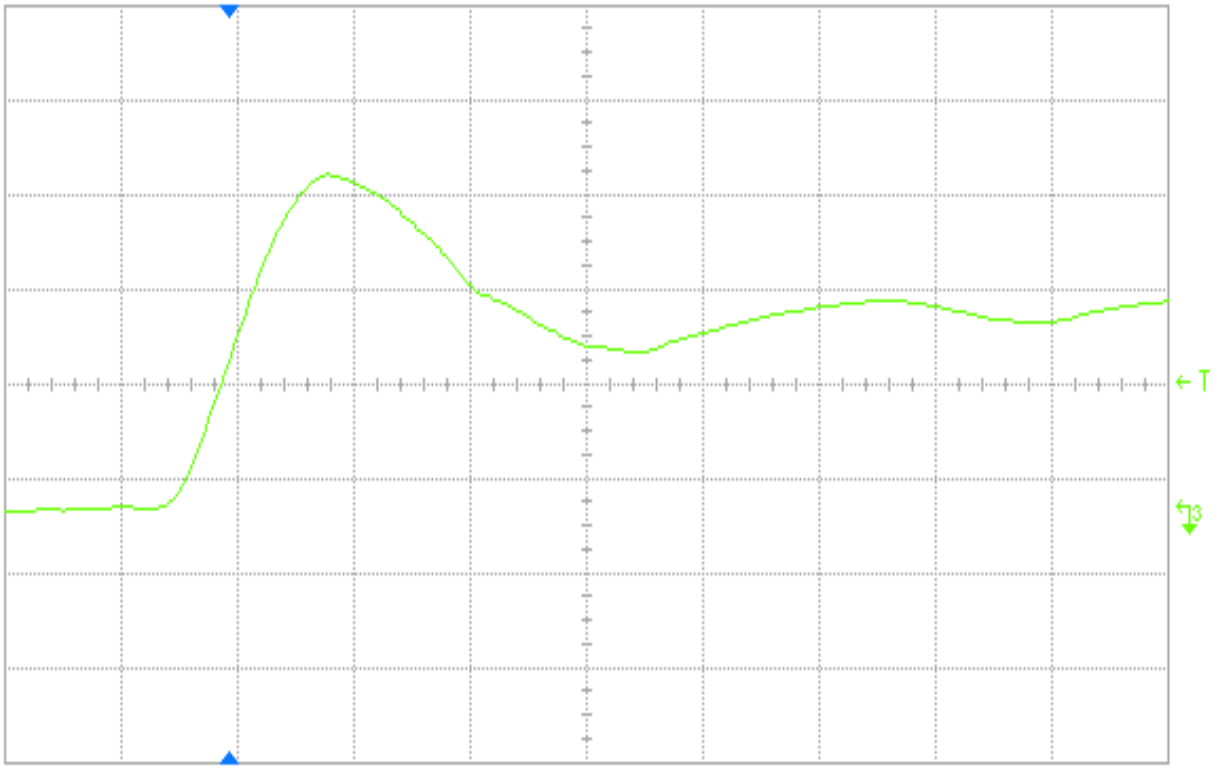


Figure 9(b) DUT 60578 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

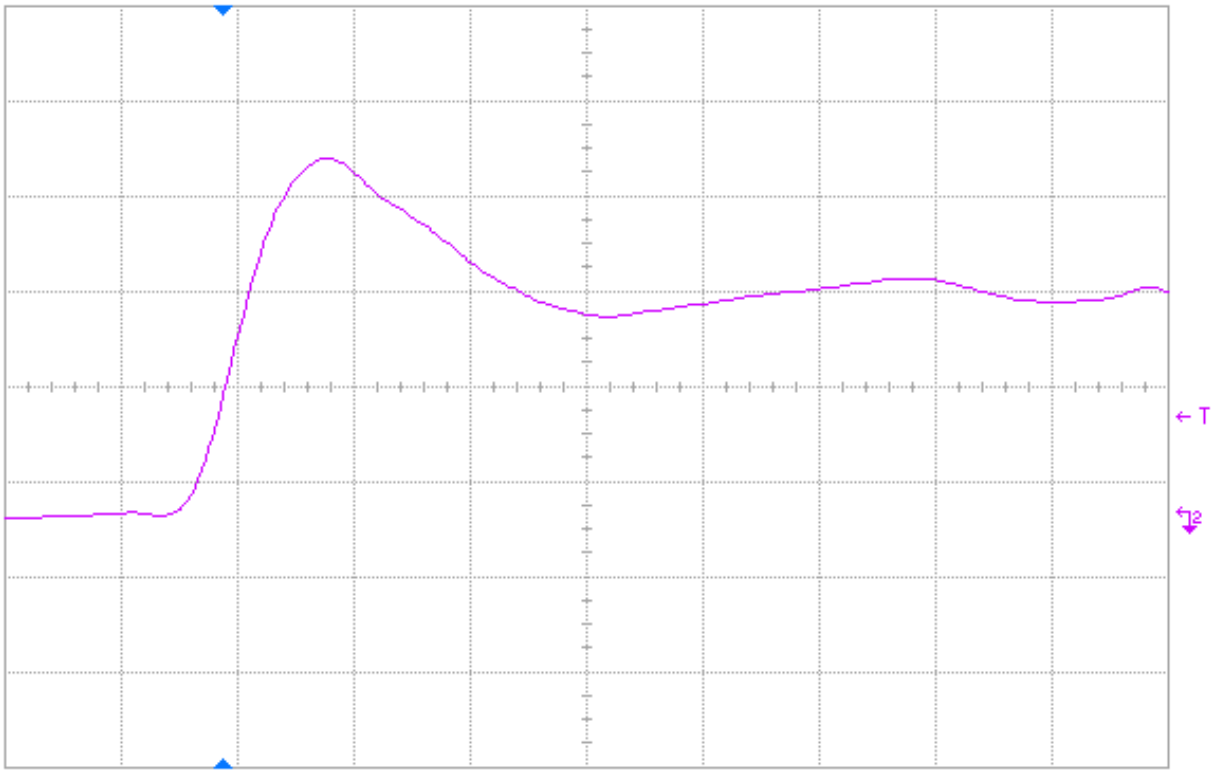


Figure 10(a) DUT 60580 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

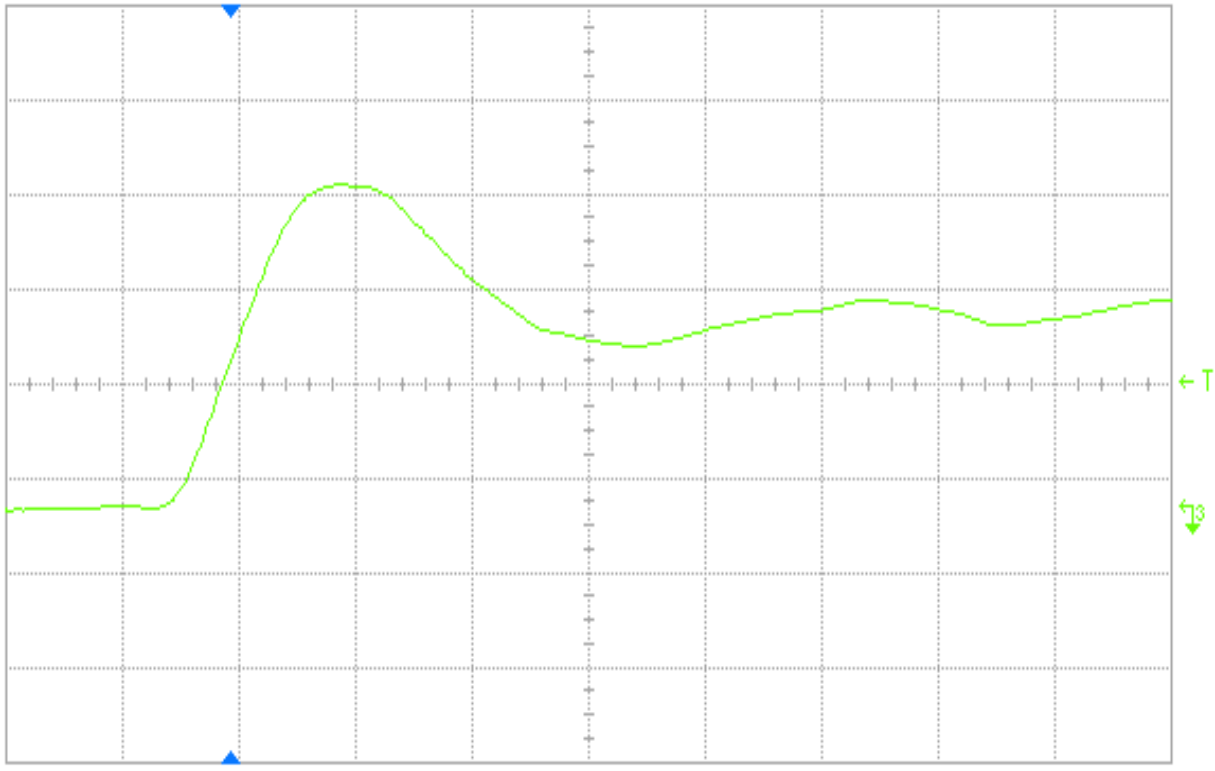


Figure 10(b) DUT 60580 post-annealing rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

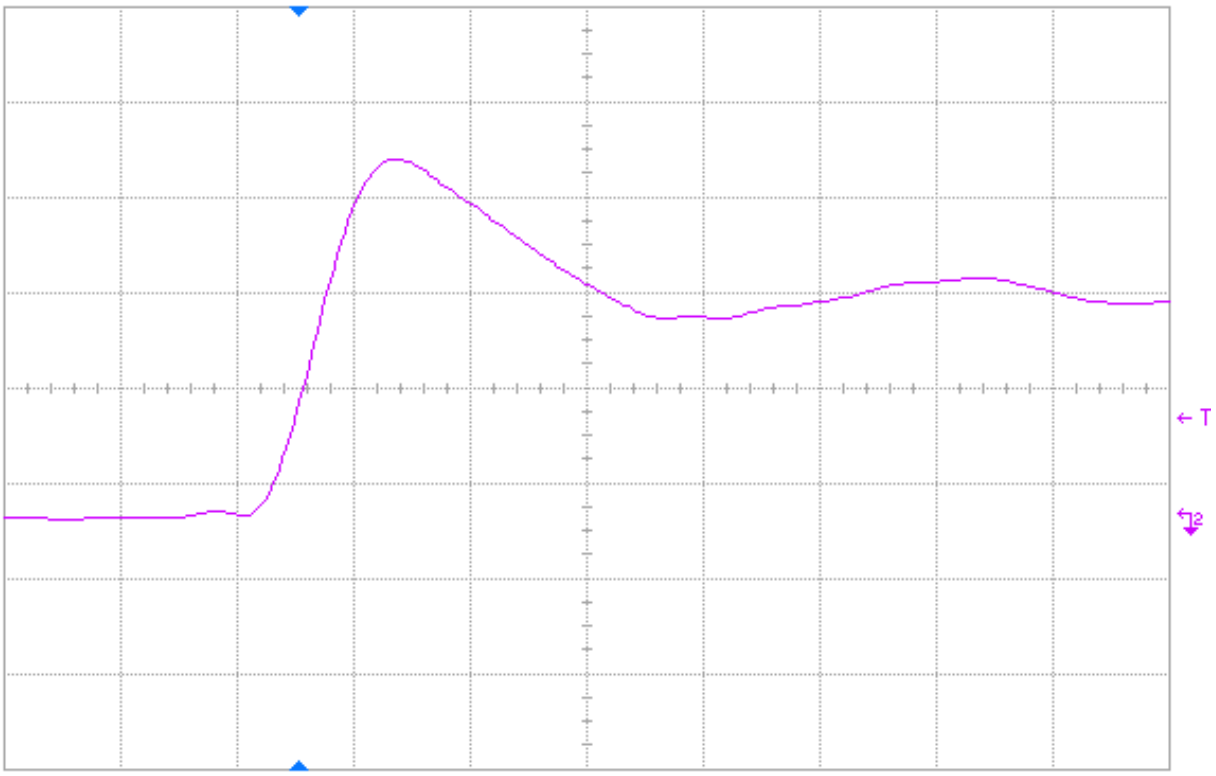


Figure 11(a) DUT 60588 pre-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

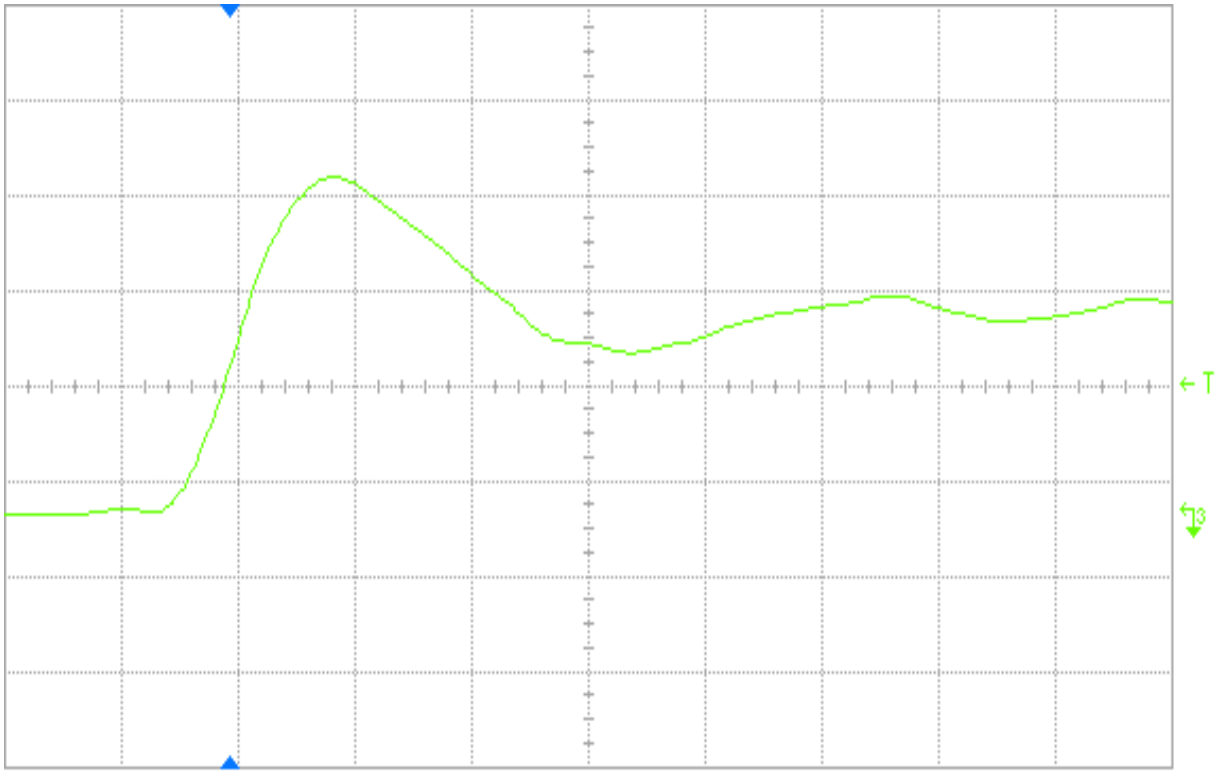


Figure 11(b) DUT 60588 post-irradiation rising edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

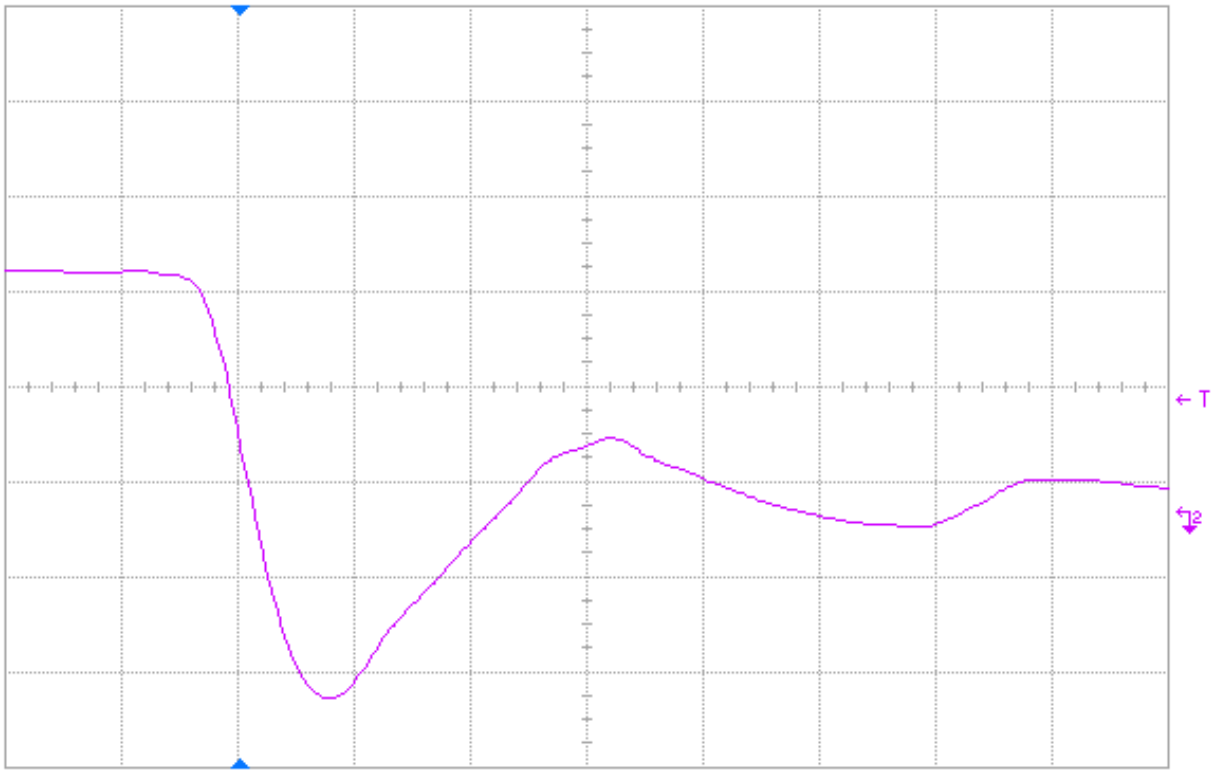


Figure 12(a) DUT 60456 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

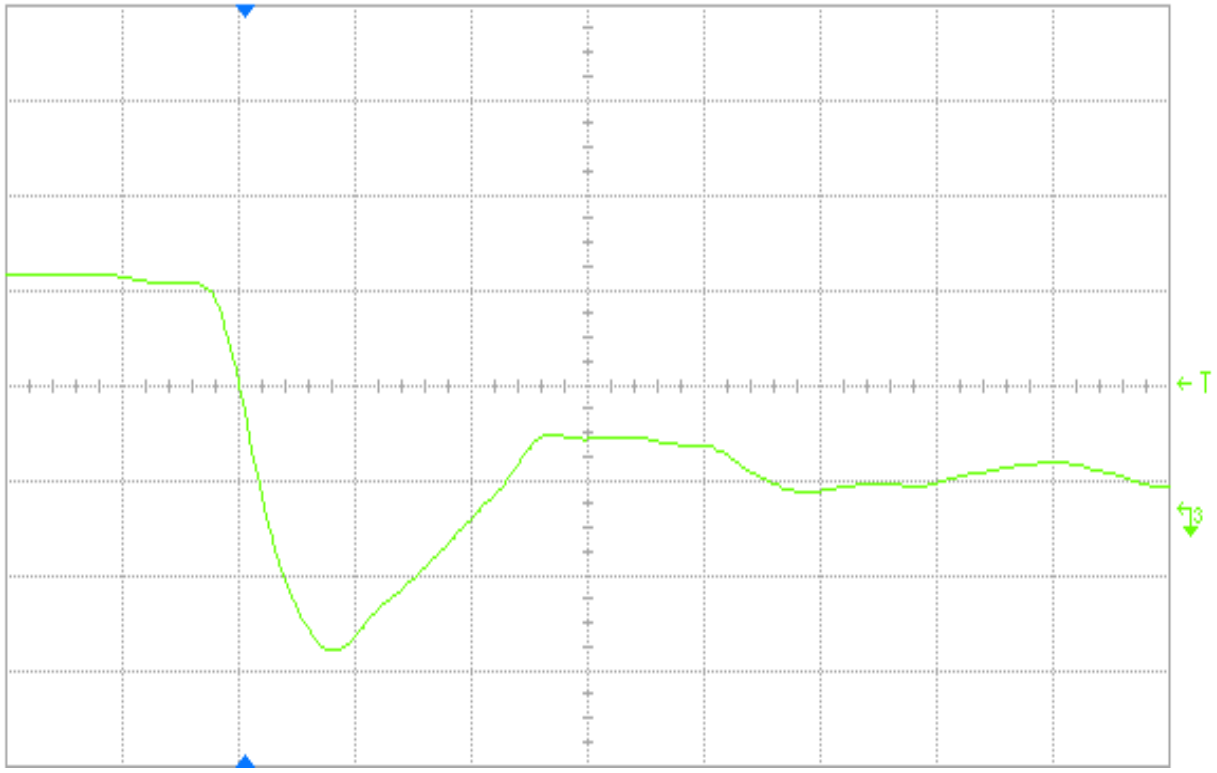


Figure 12(b) DUT 60456 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

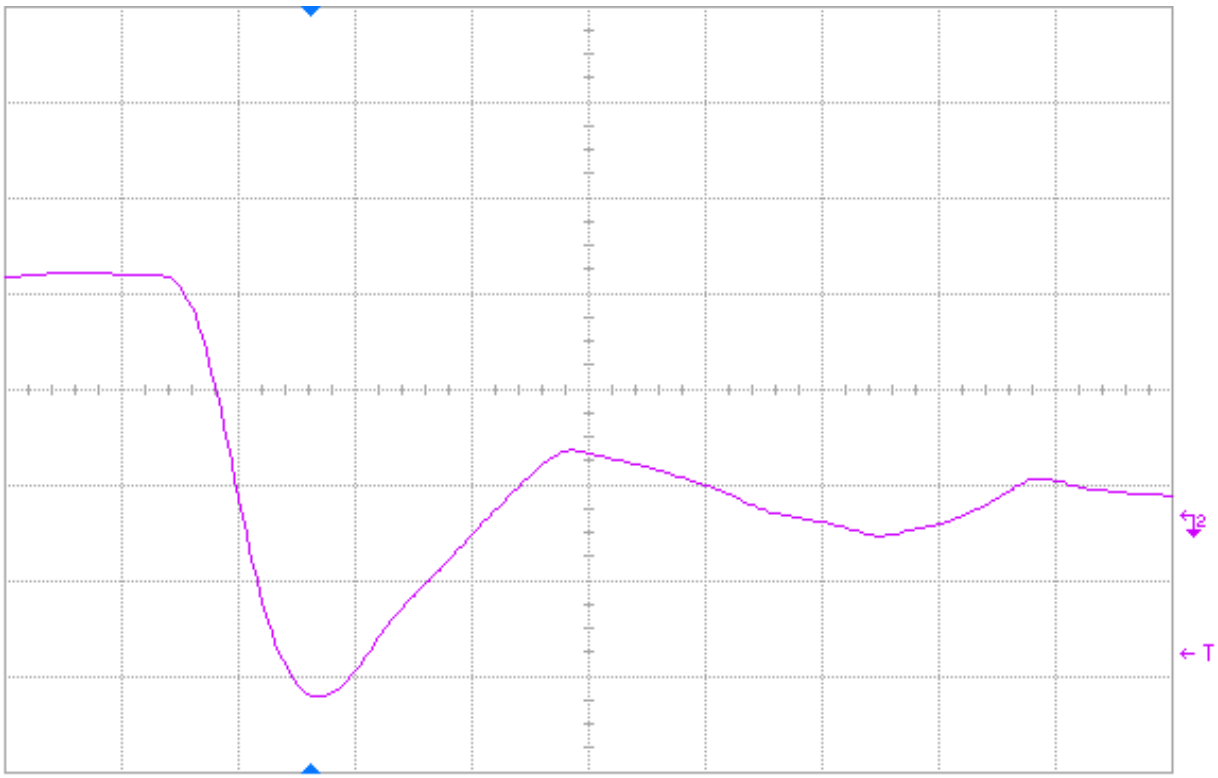


Figure 13(a) DUT 60574 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

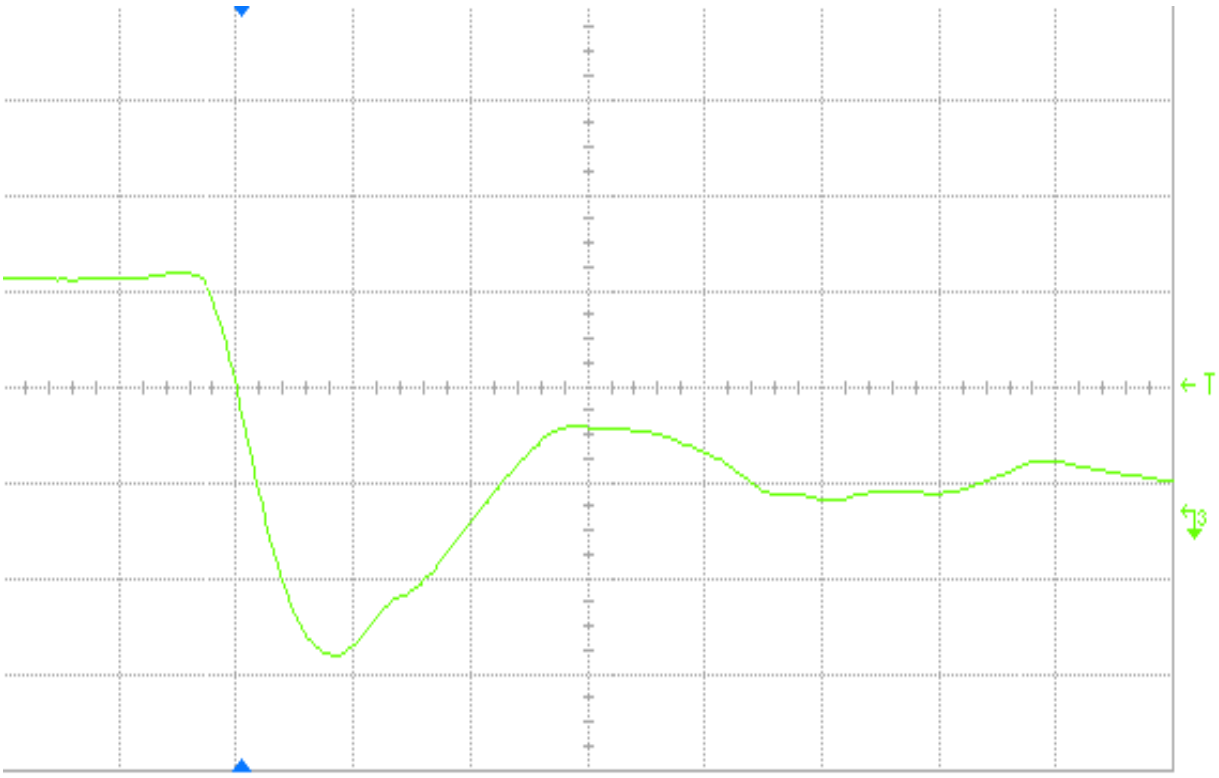


Figure 13(b) DUT 60574 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

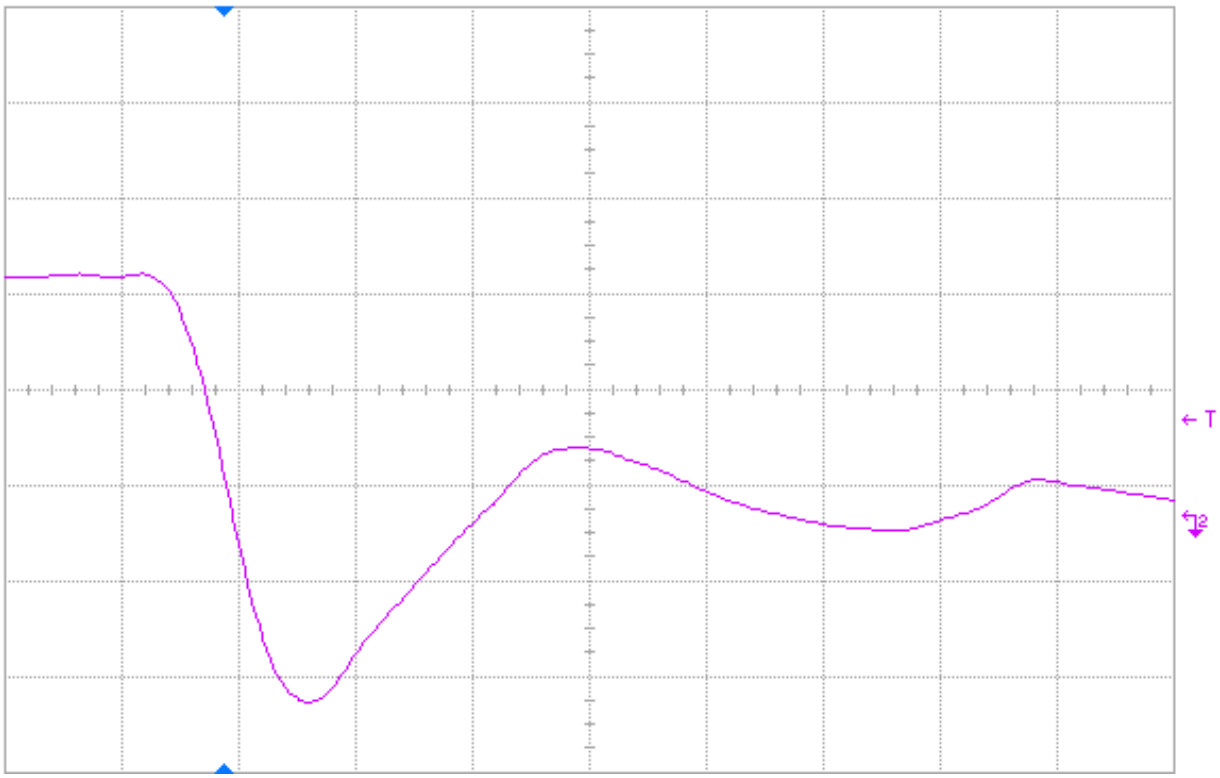


Figure 14(a) DUT 60578 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

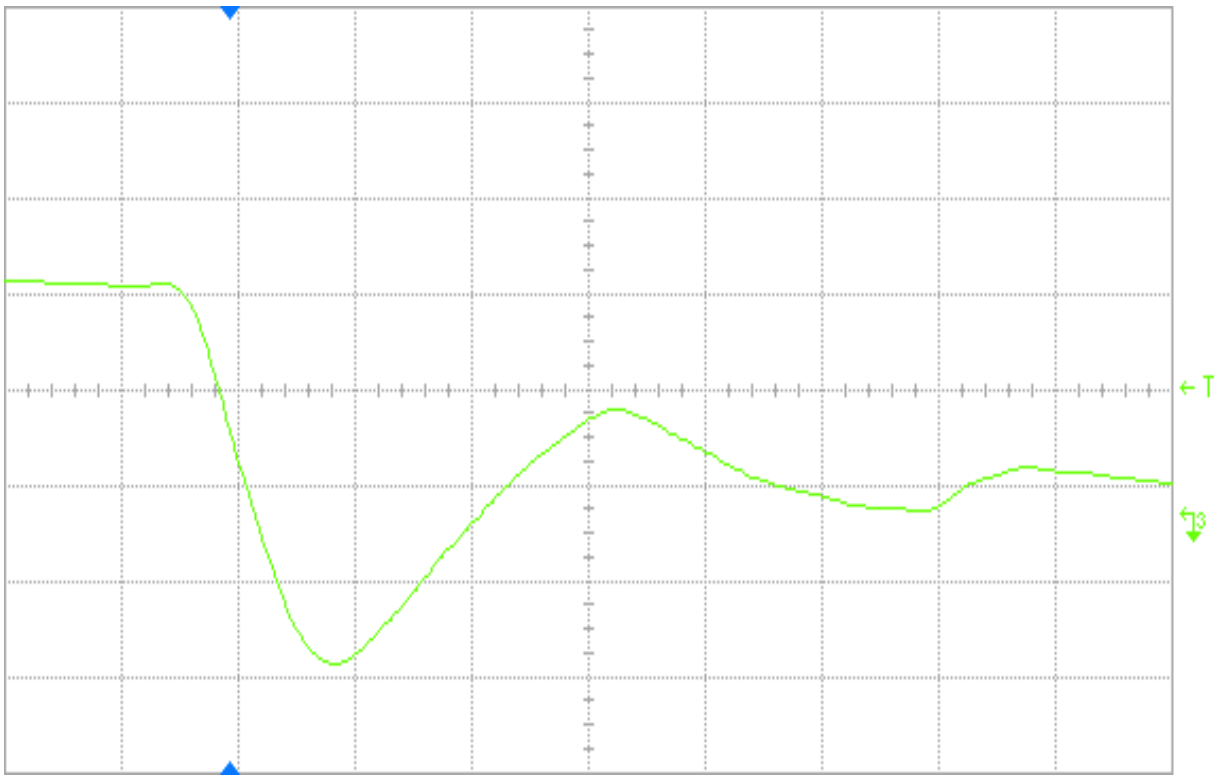


Figure 14(b) DUT 60578 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

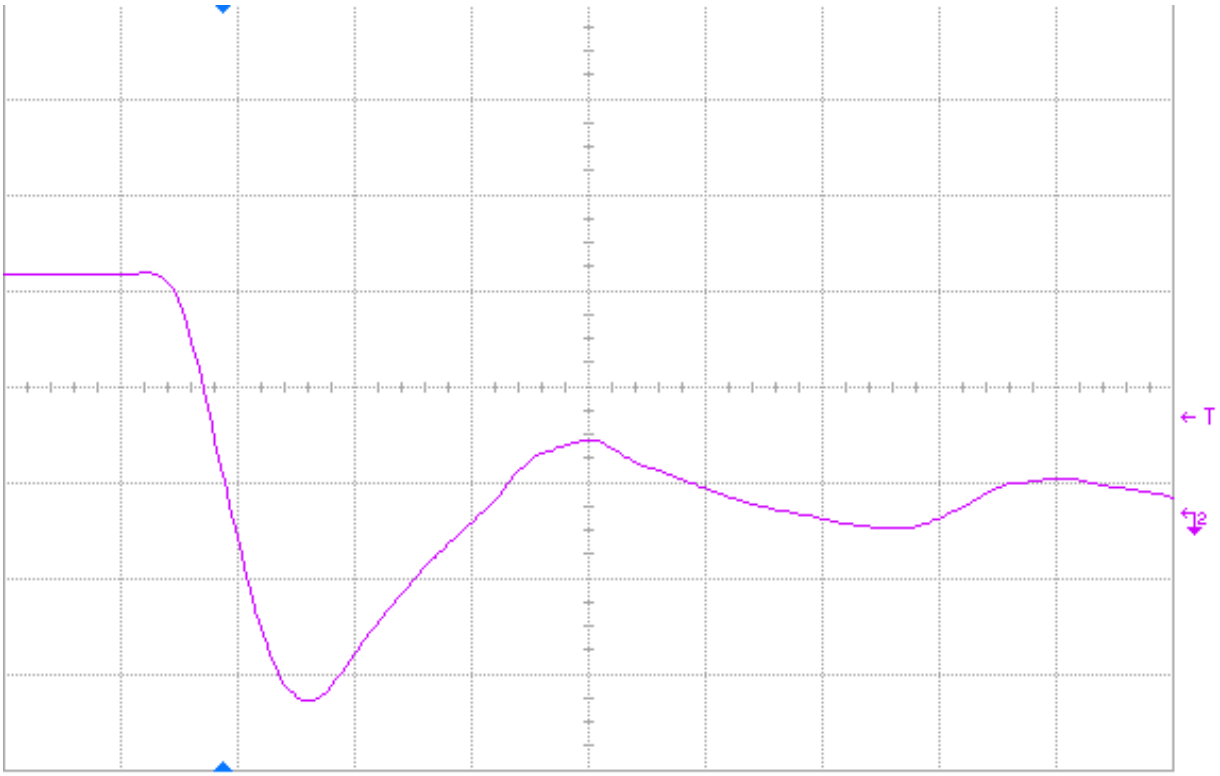


Figure 15(a) DUT 60580 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

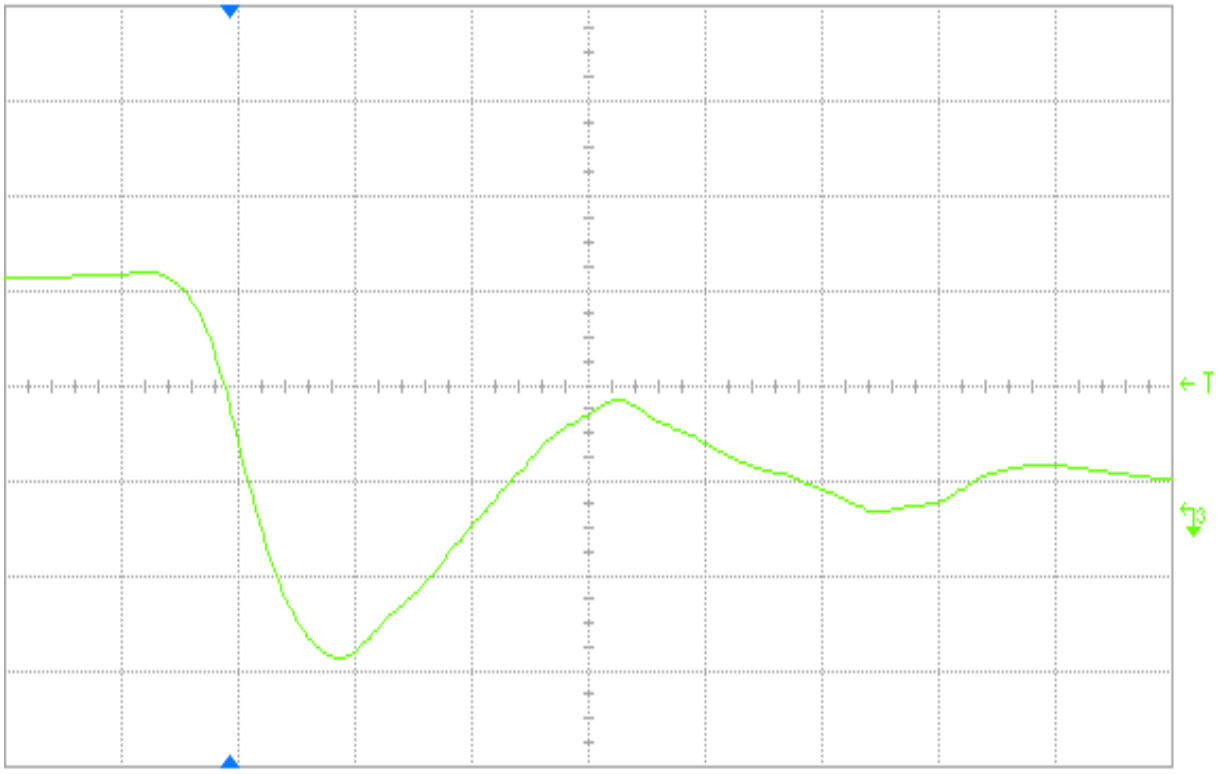


Figure 15(b) DUT 60580 post-annealing falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

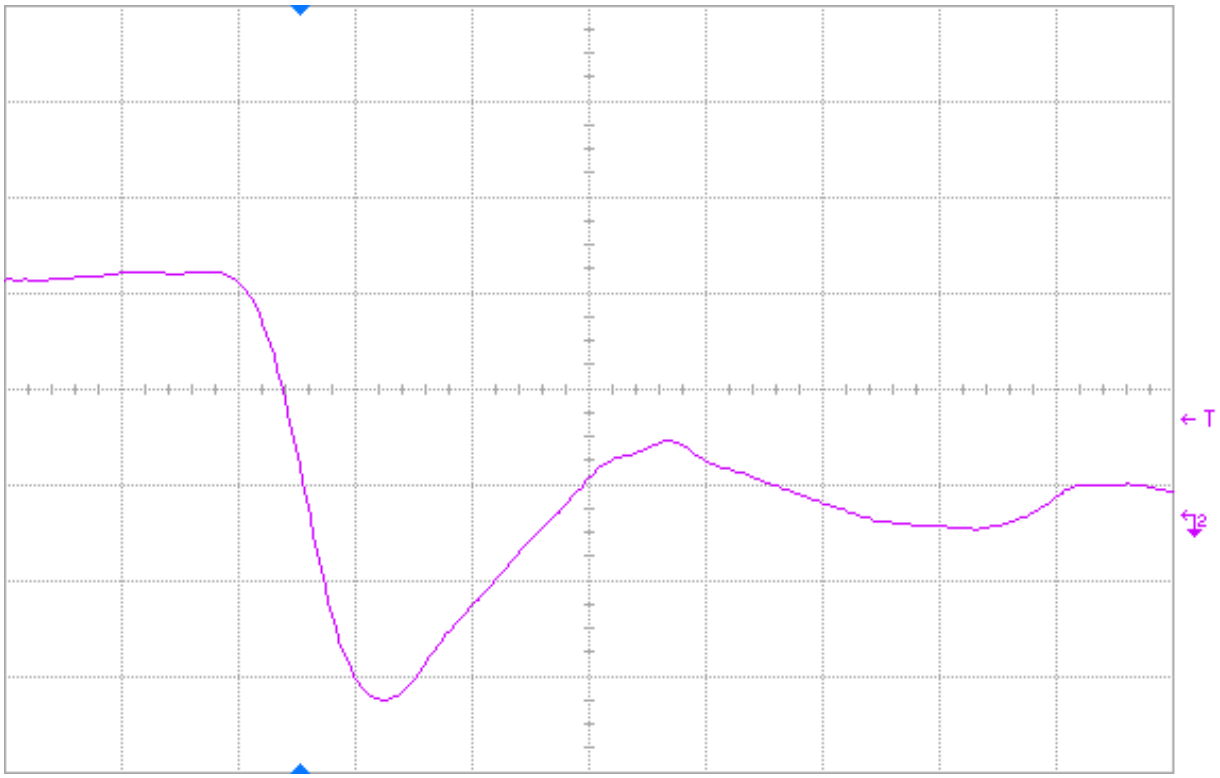


Figure 15(a) DUT 60588 pre-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

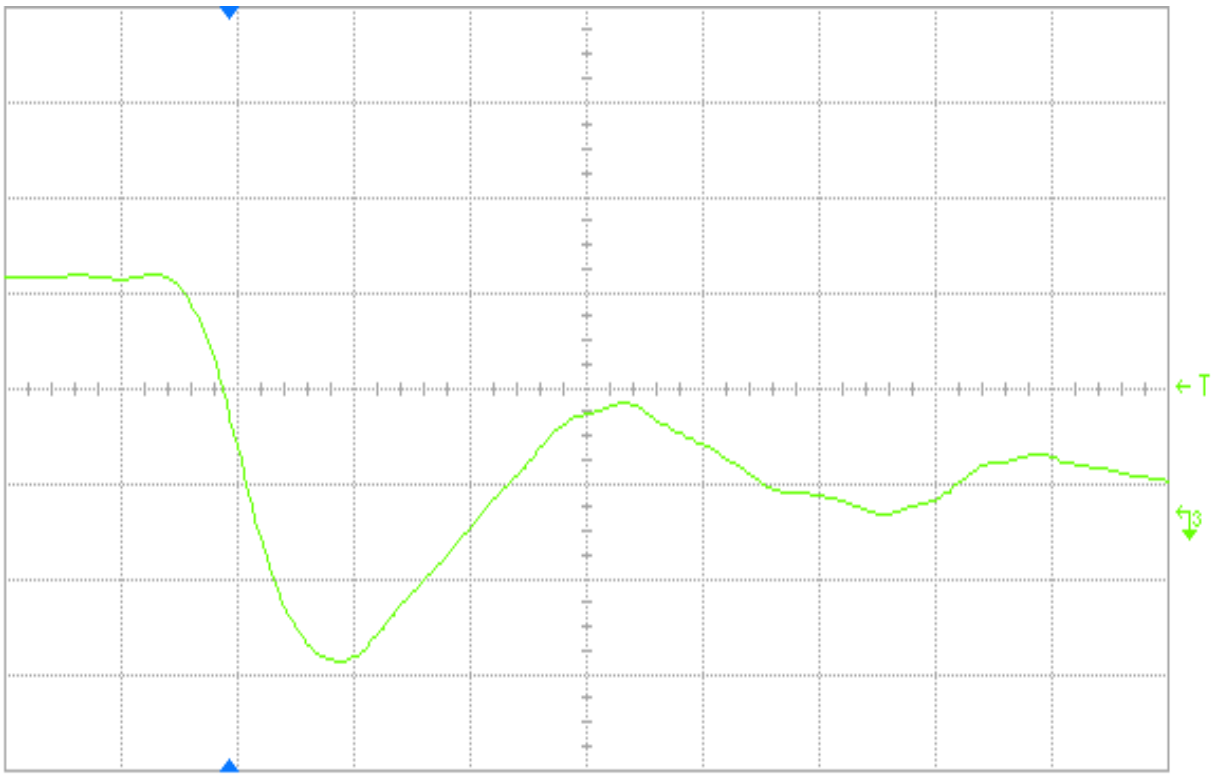
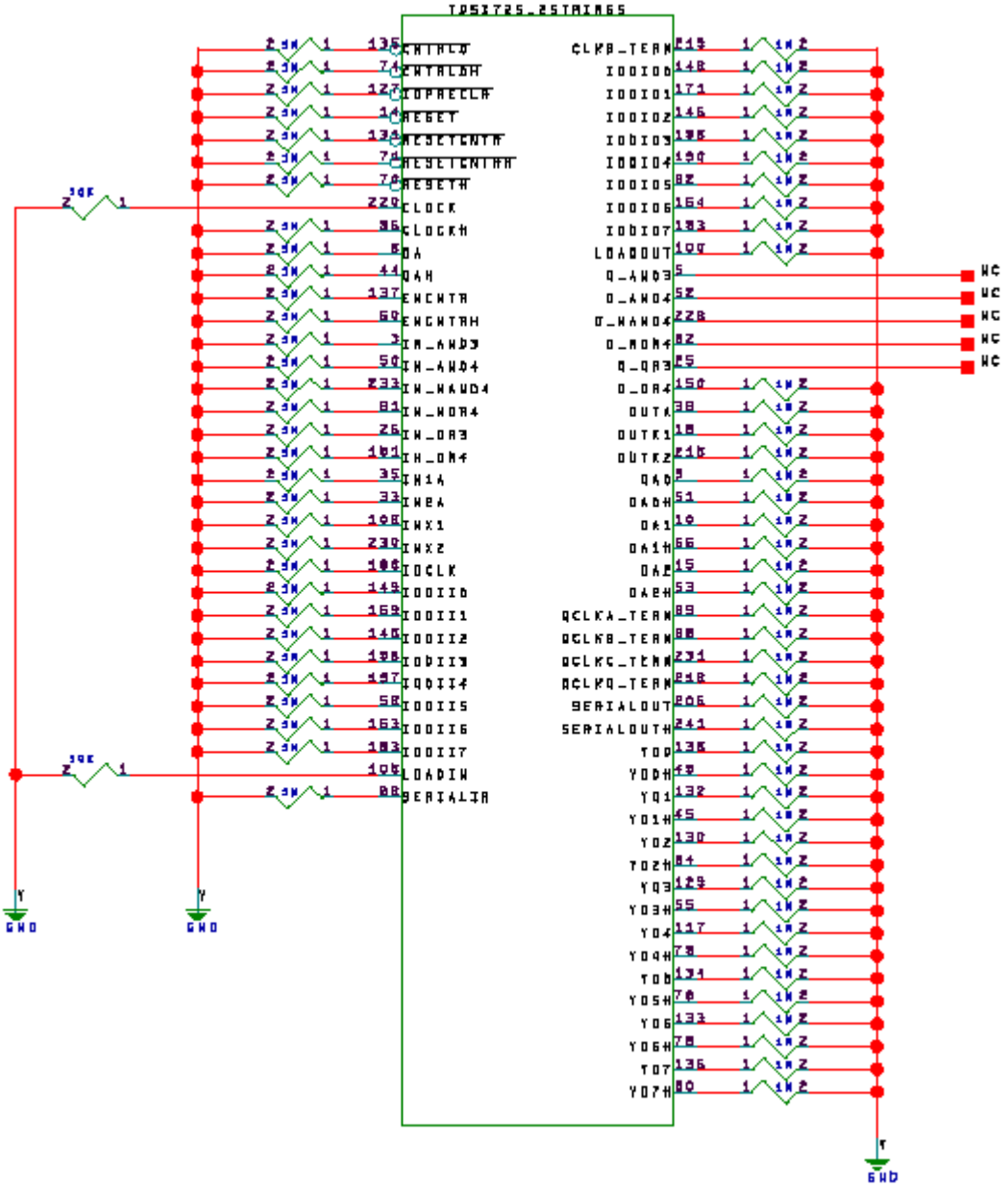
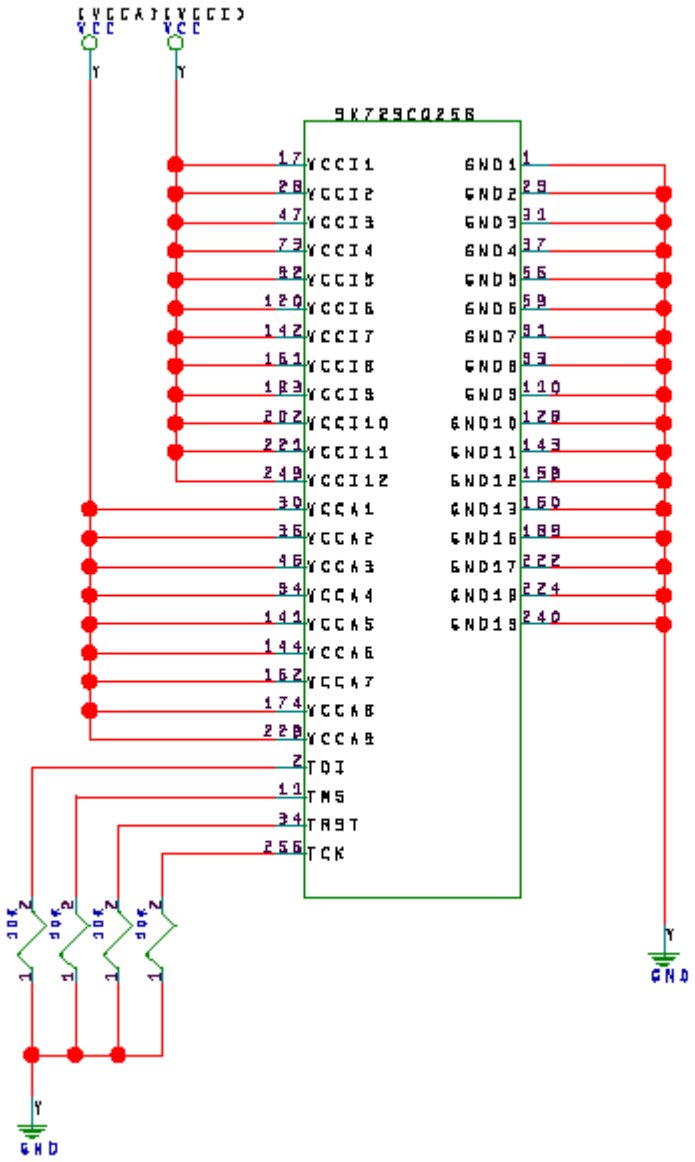


Figure 15(b) DUT 60588 post-irradiation falling edge, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

APPENDIX A DUT BIAS

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VCCI
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VCCI8
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VCCI11
VCCI12
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VCCA4
VCCA5
VCCA6
VCCA7
VCCA8
VCCA9
TDI
TMS
TRST
TCK
GND1
GND2
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GND4
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GND7
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GND15
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GND19
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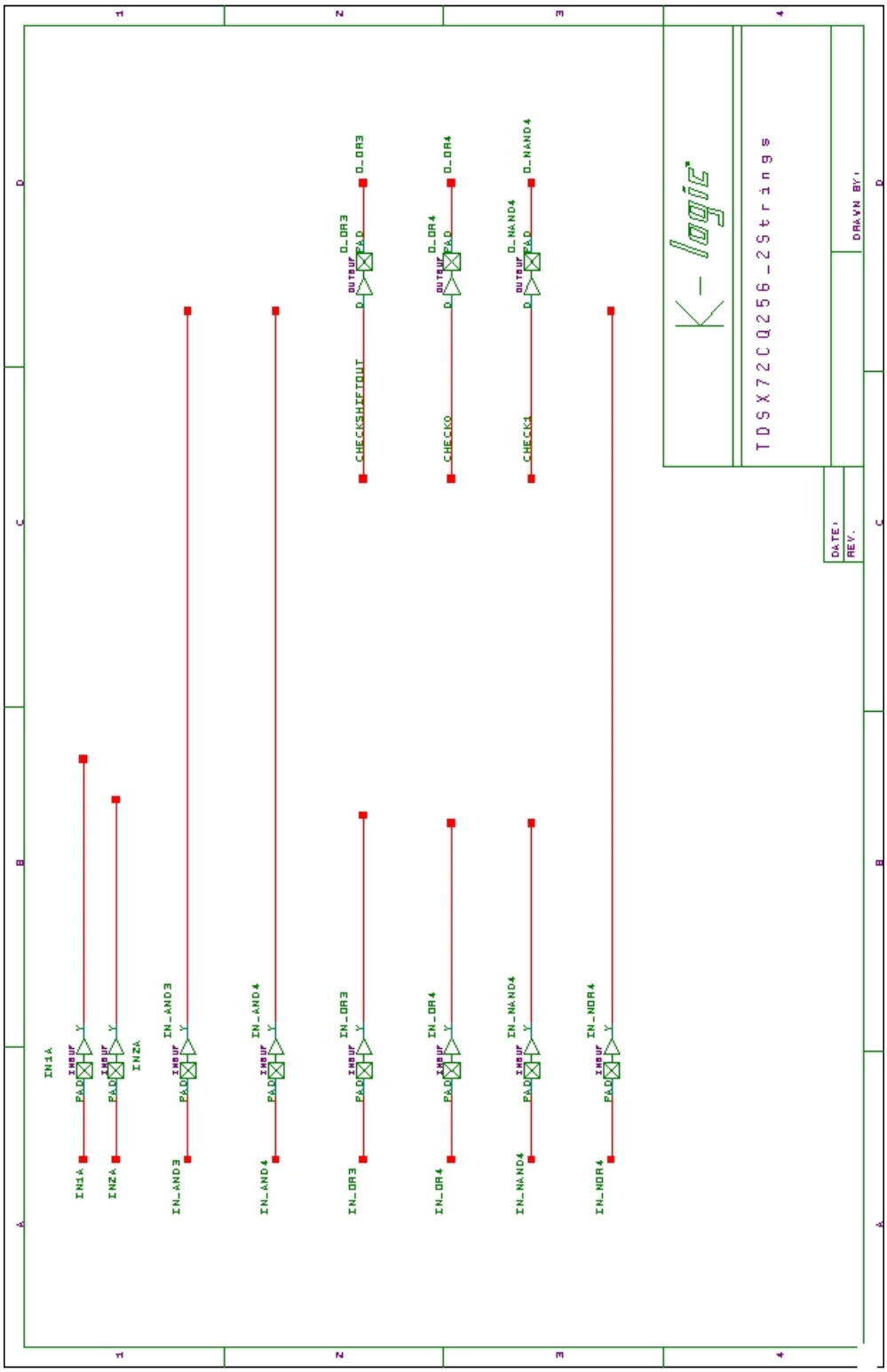
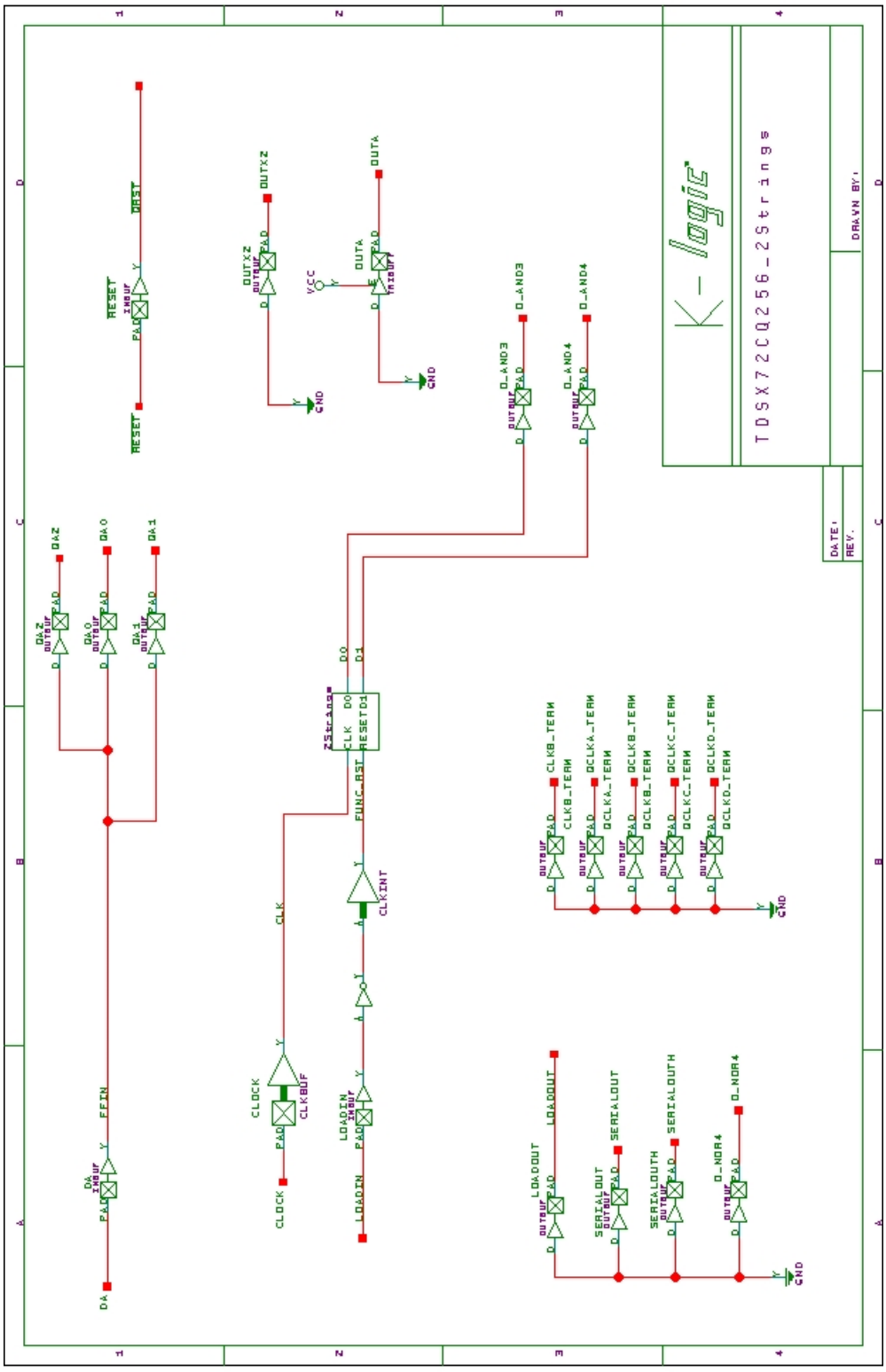
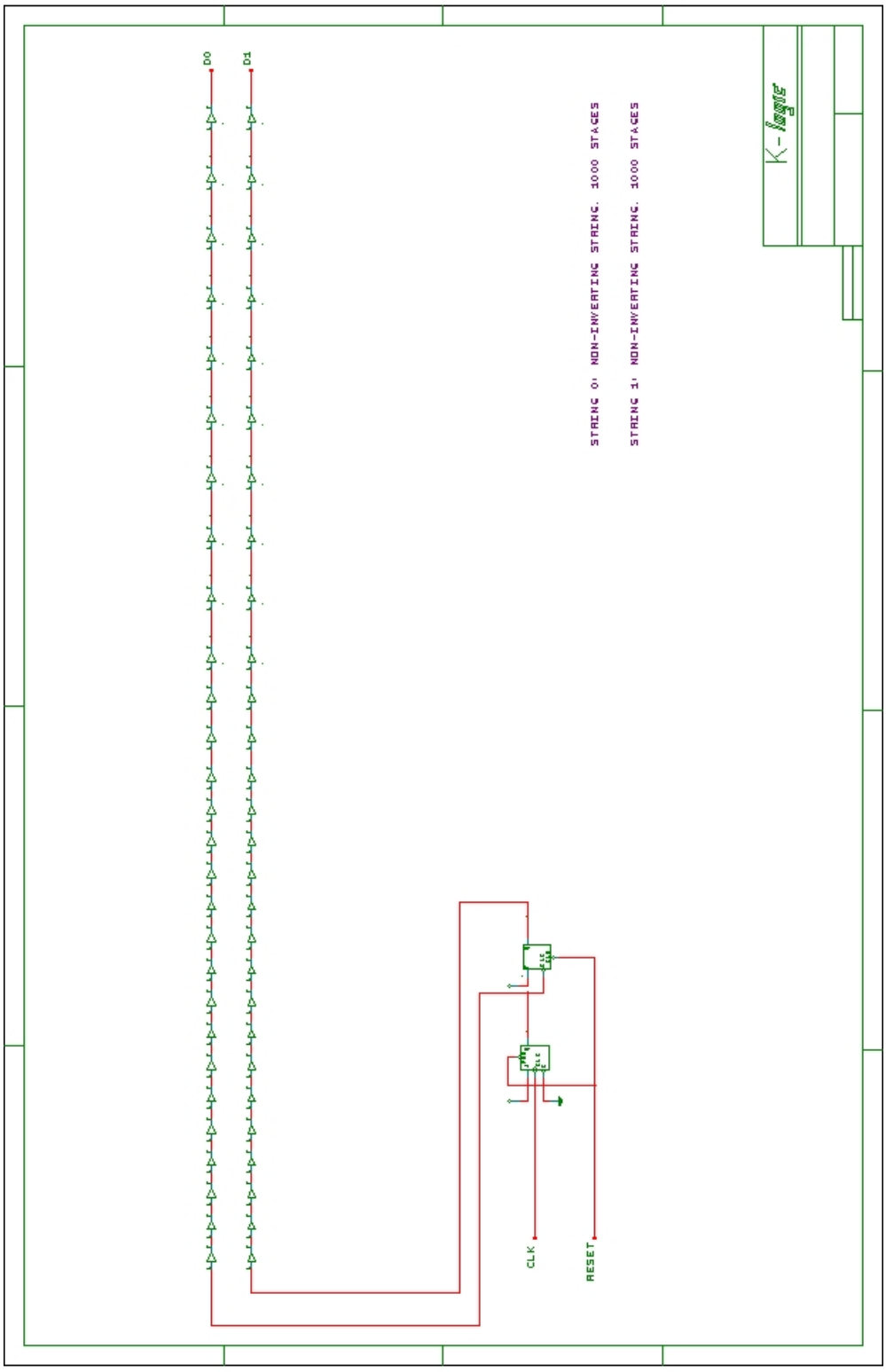
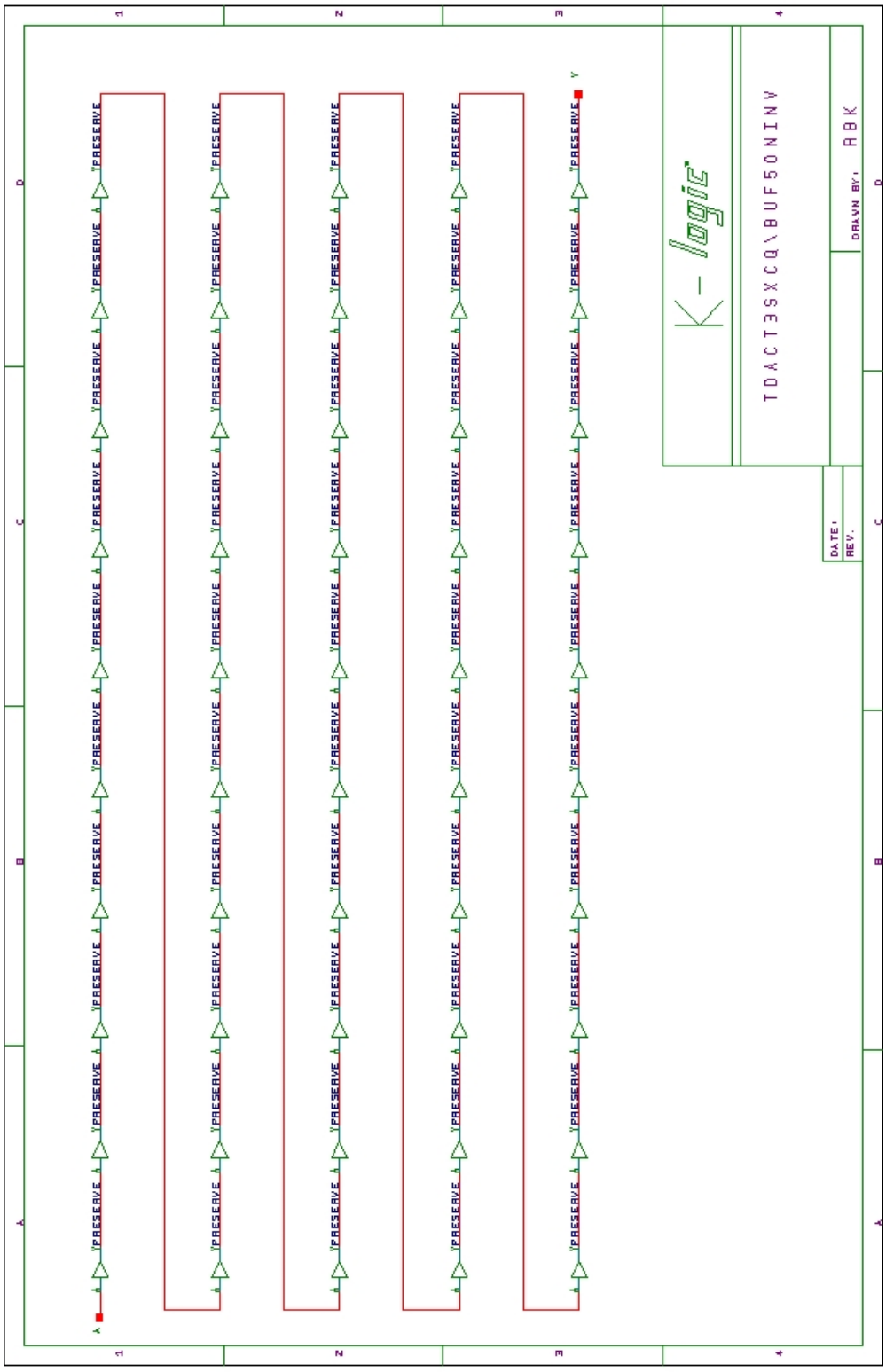
10K
10K
10K
GND
GND

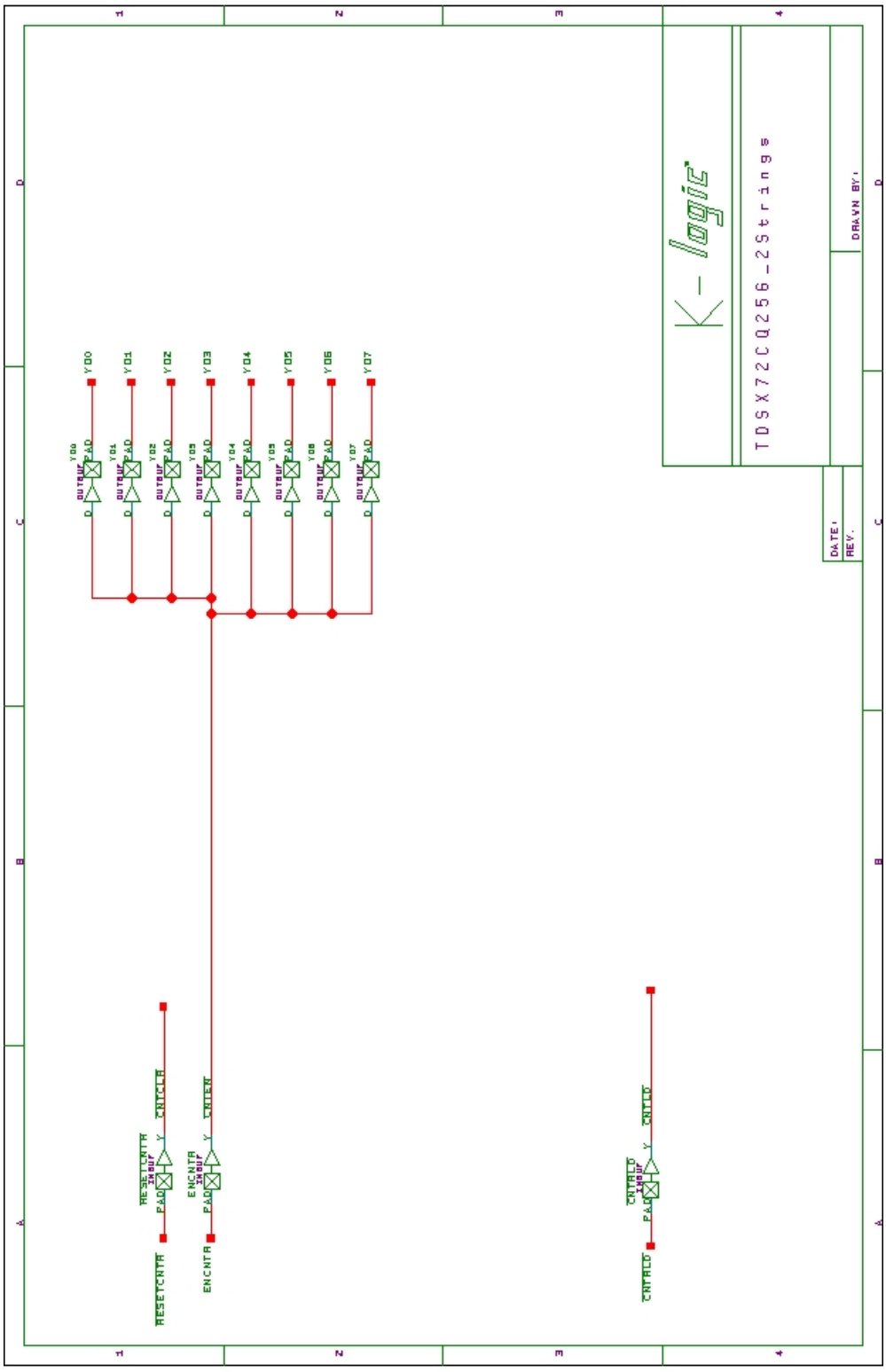
APPENDIX B DUT DESIGN SCHEMATICS

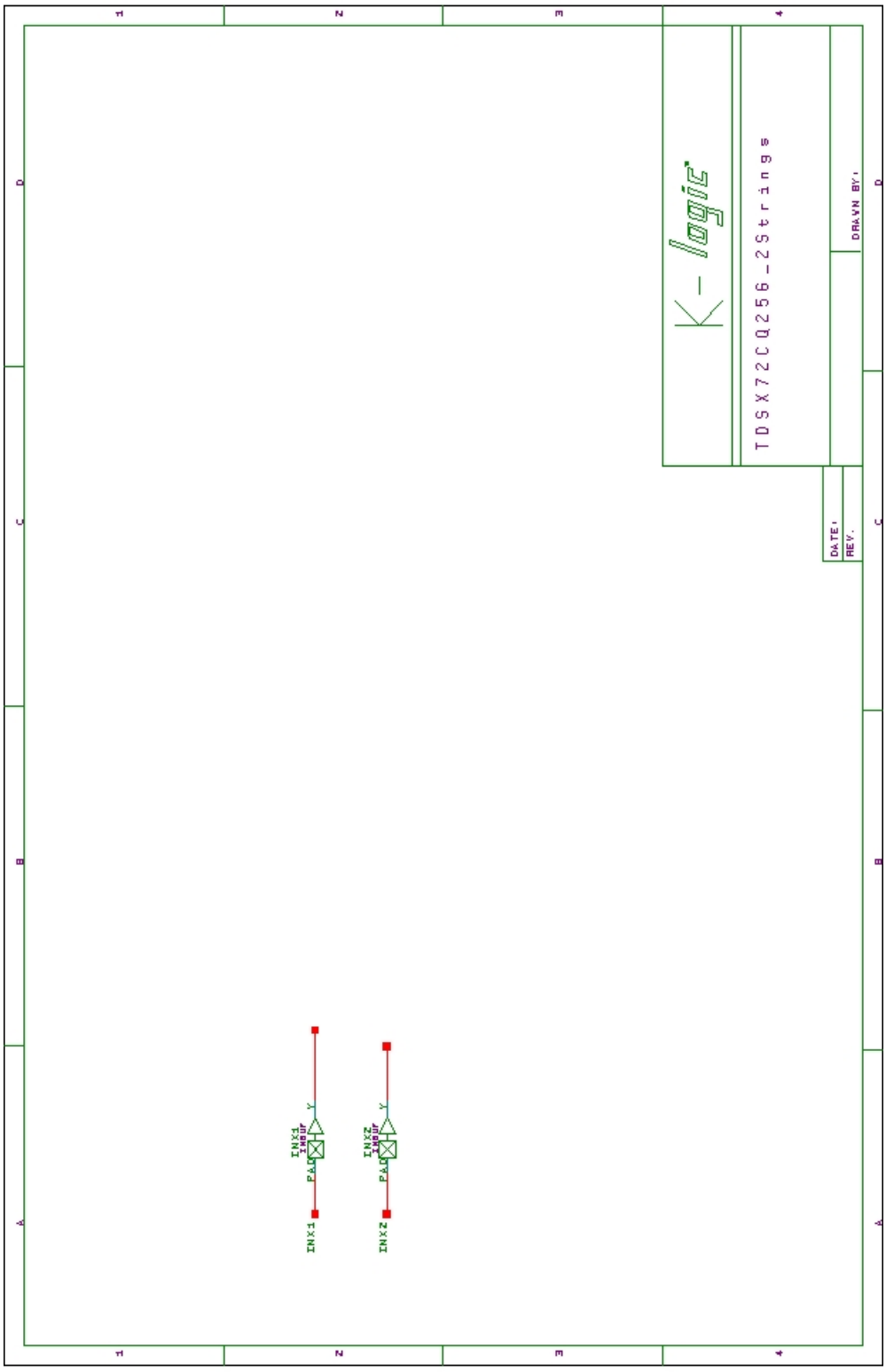


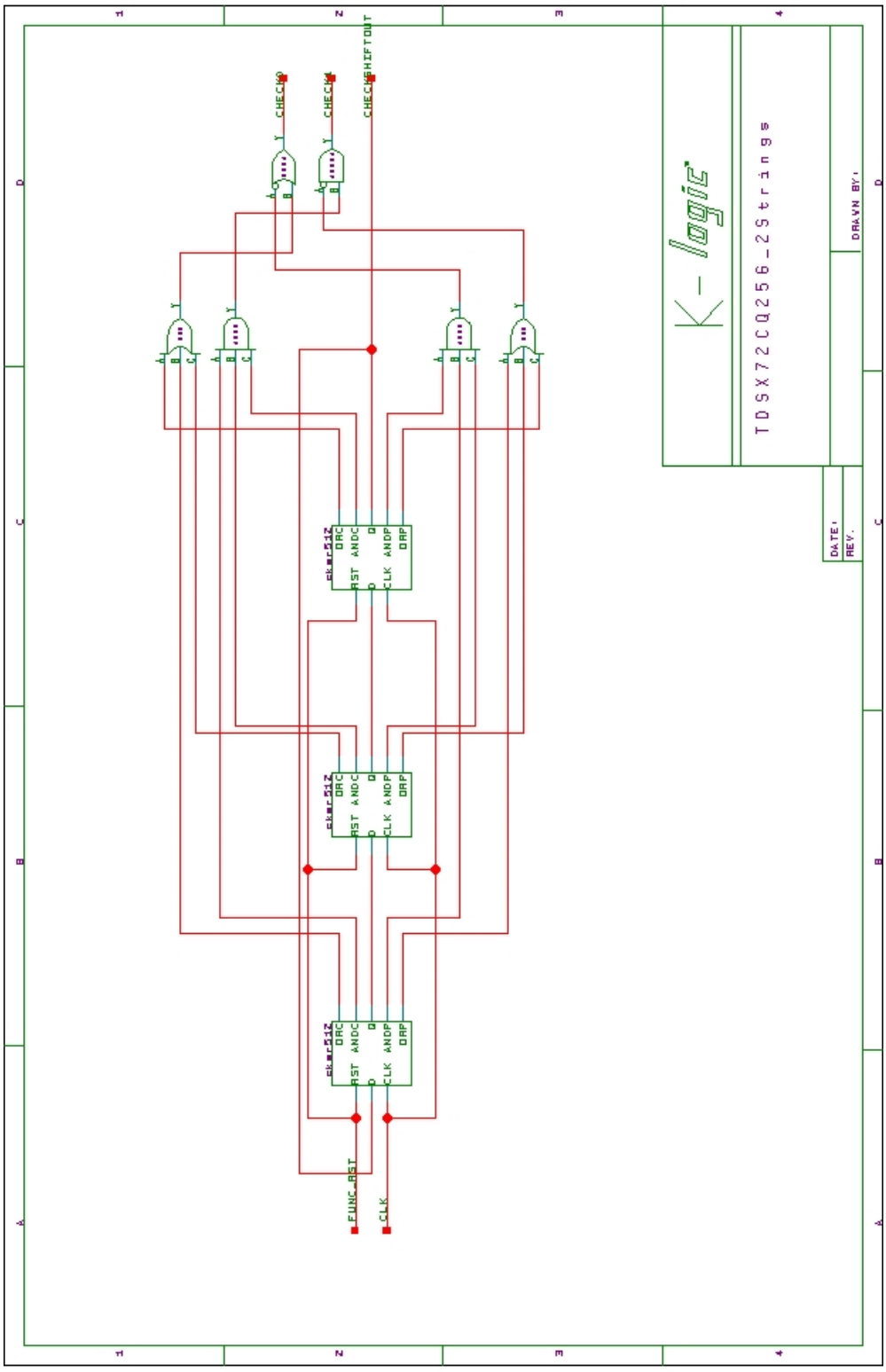

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
DAST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
ZStrings
CLK
D0
D1
RESET
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

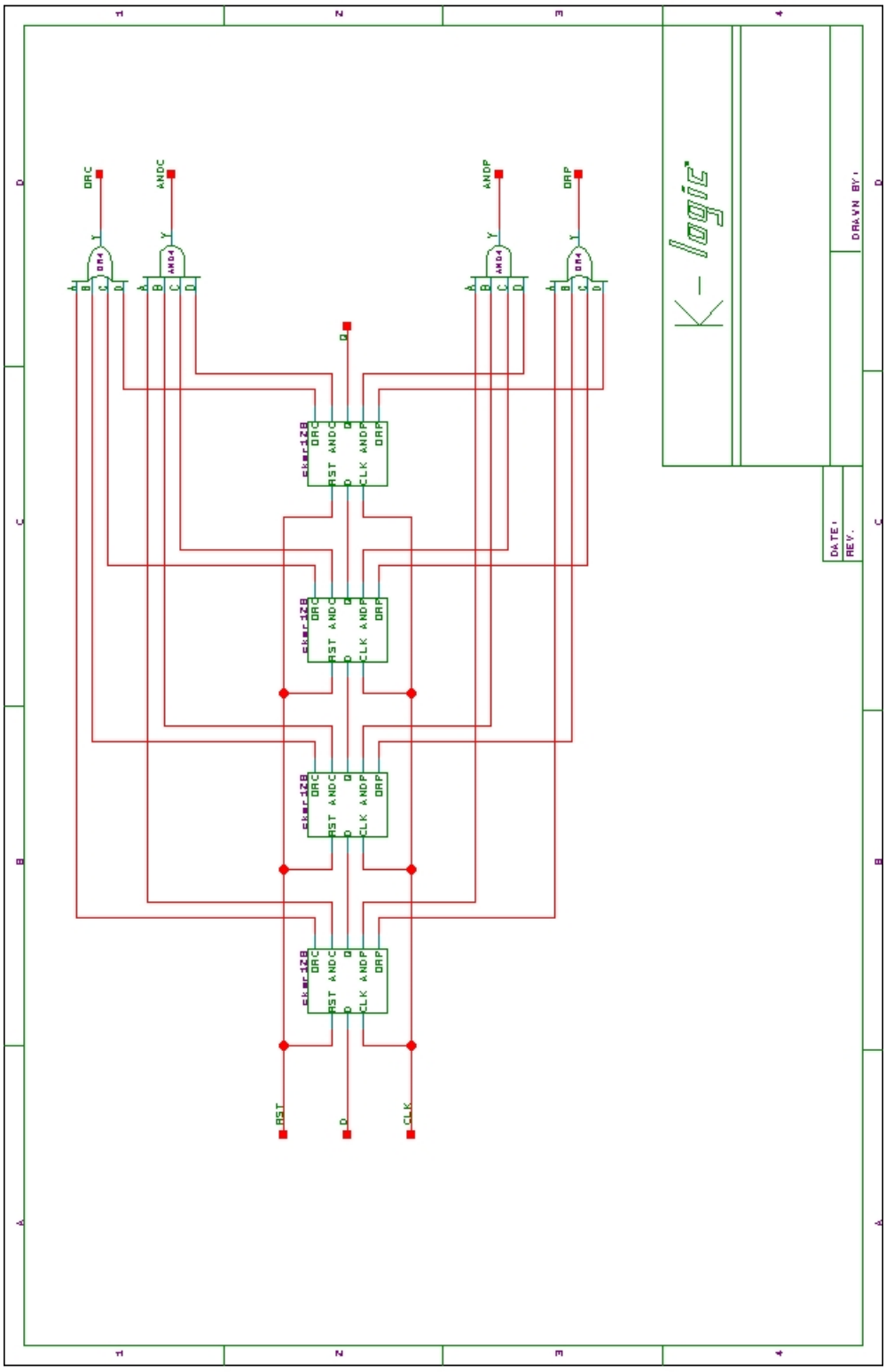

D0
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-logic
CLK
RESET

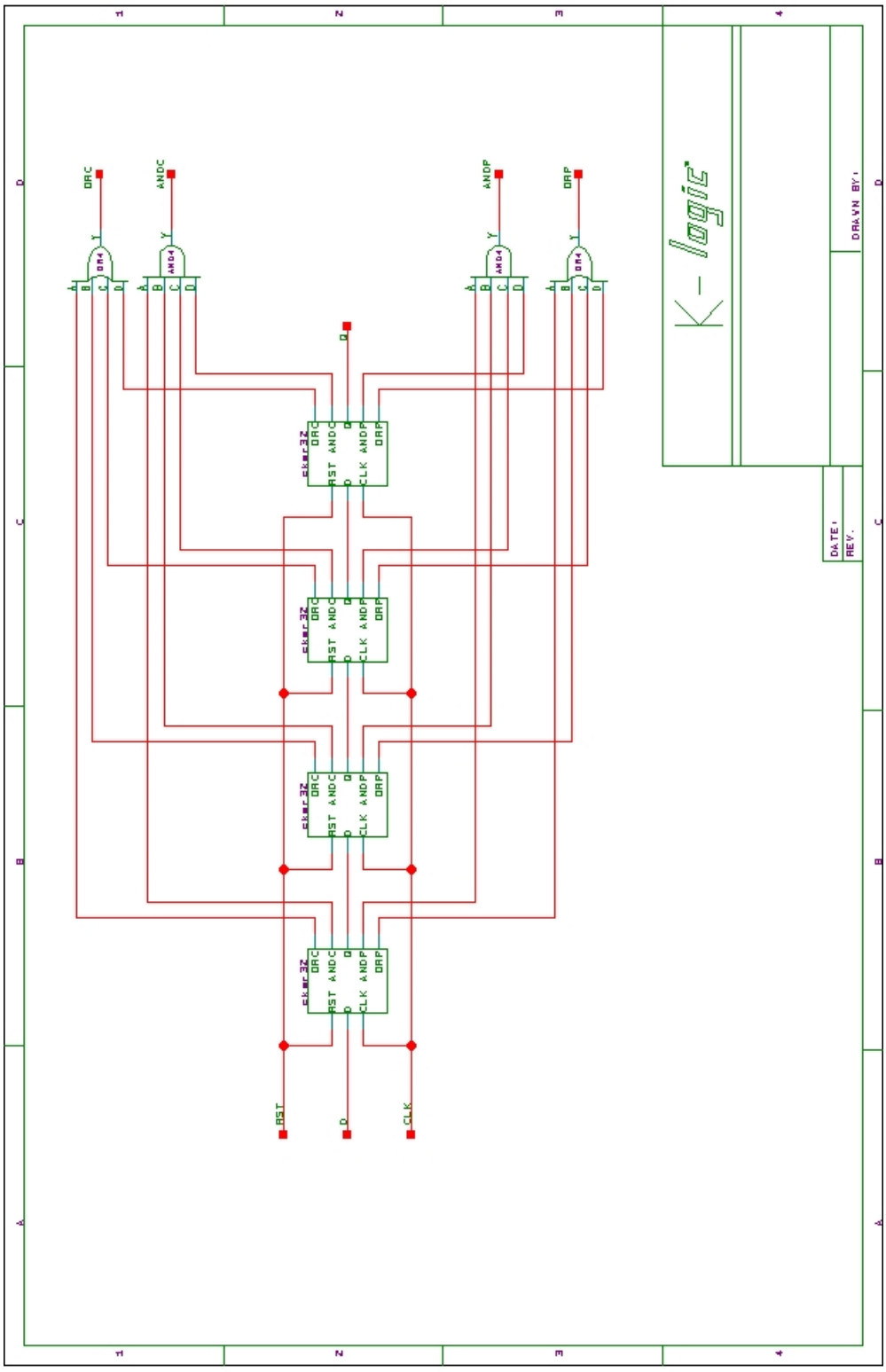

K- logic
TDACT35XCQ\BUF50NINV
DRAWN BY: ABK
DATE:
REV.
Y
PRESERVE

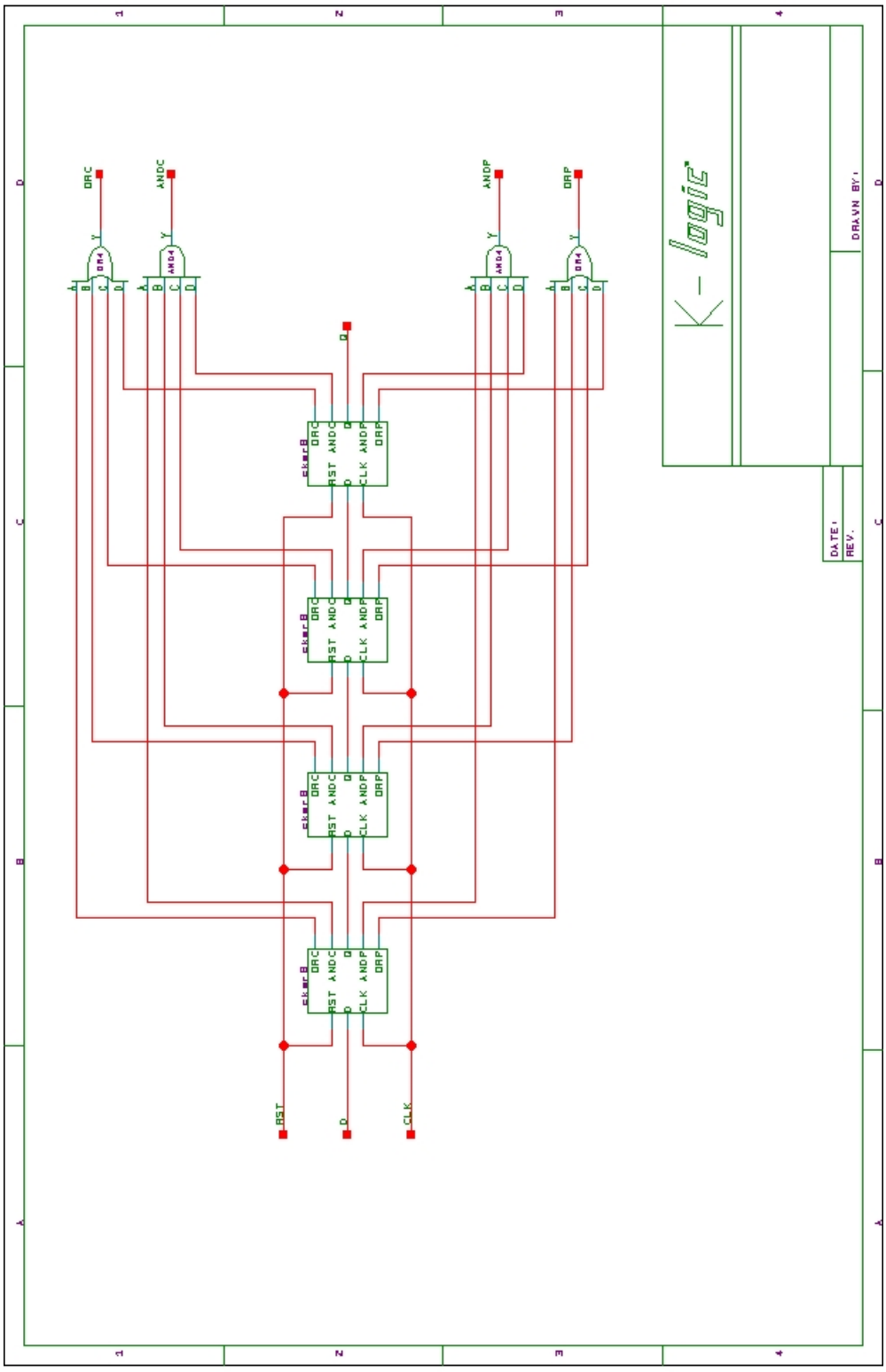

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00
Y01
Y02
Y03
Y04
Y05
Y06
Y07
OUTBUF
PAD
RESETCNTR
ENCNTR
CNTRLD
CNTCLK
CNTEN

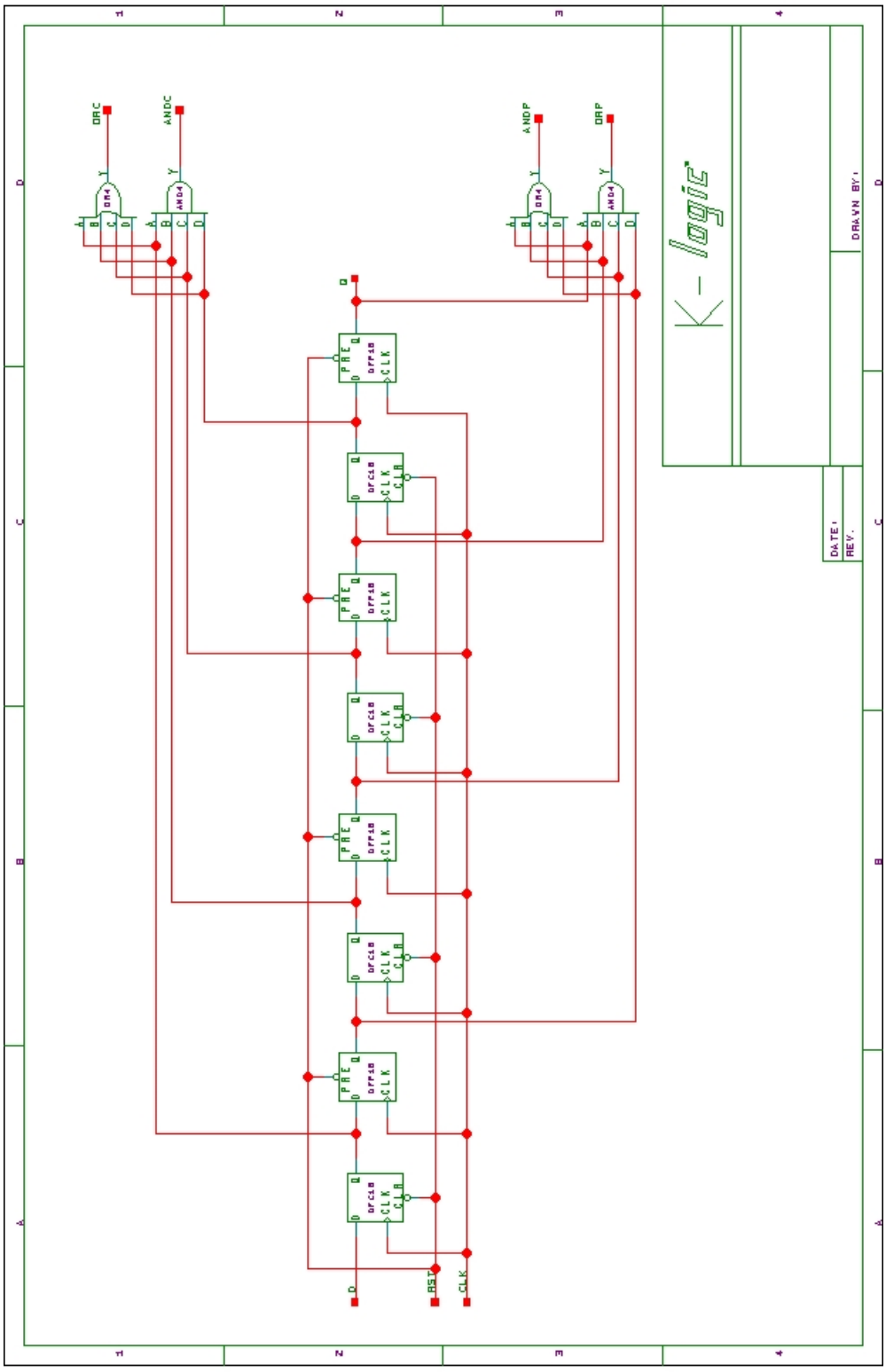

K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2

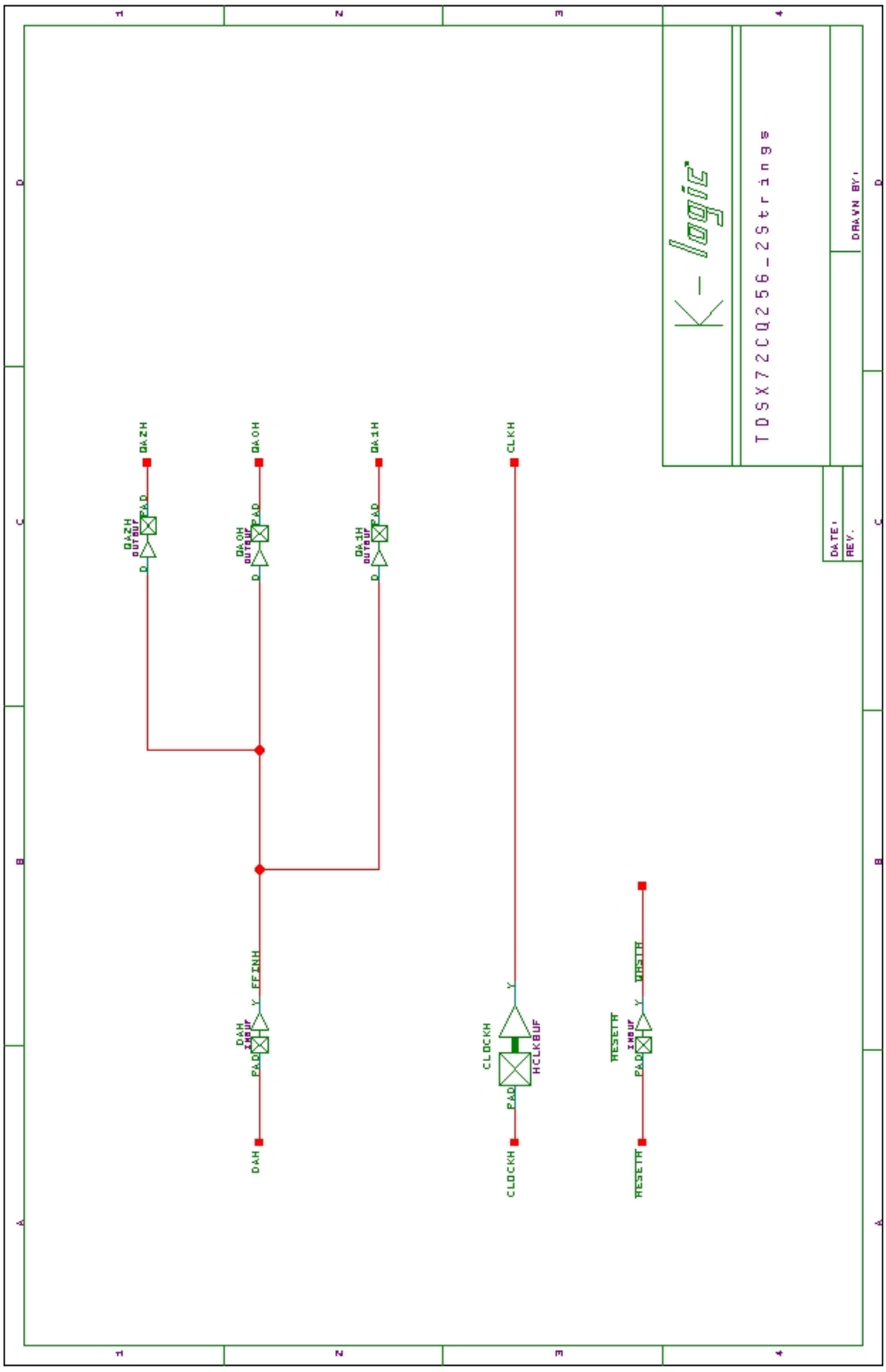

K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
CHECKSHIFTOUT
CHECK0
CHECK1
FUNC_RST
CLK

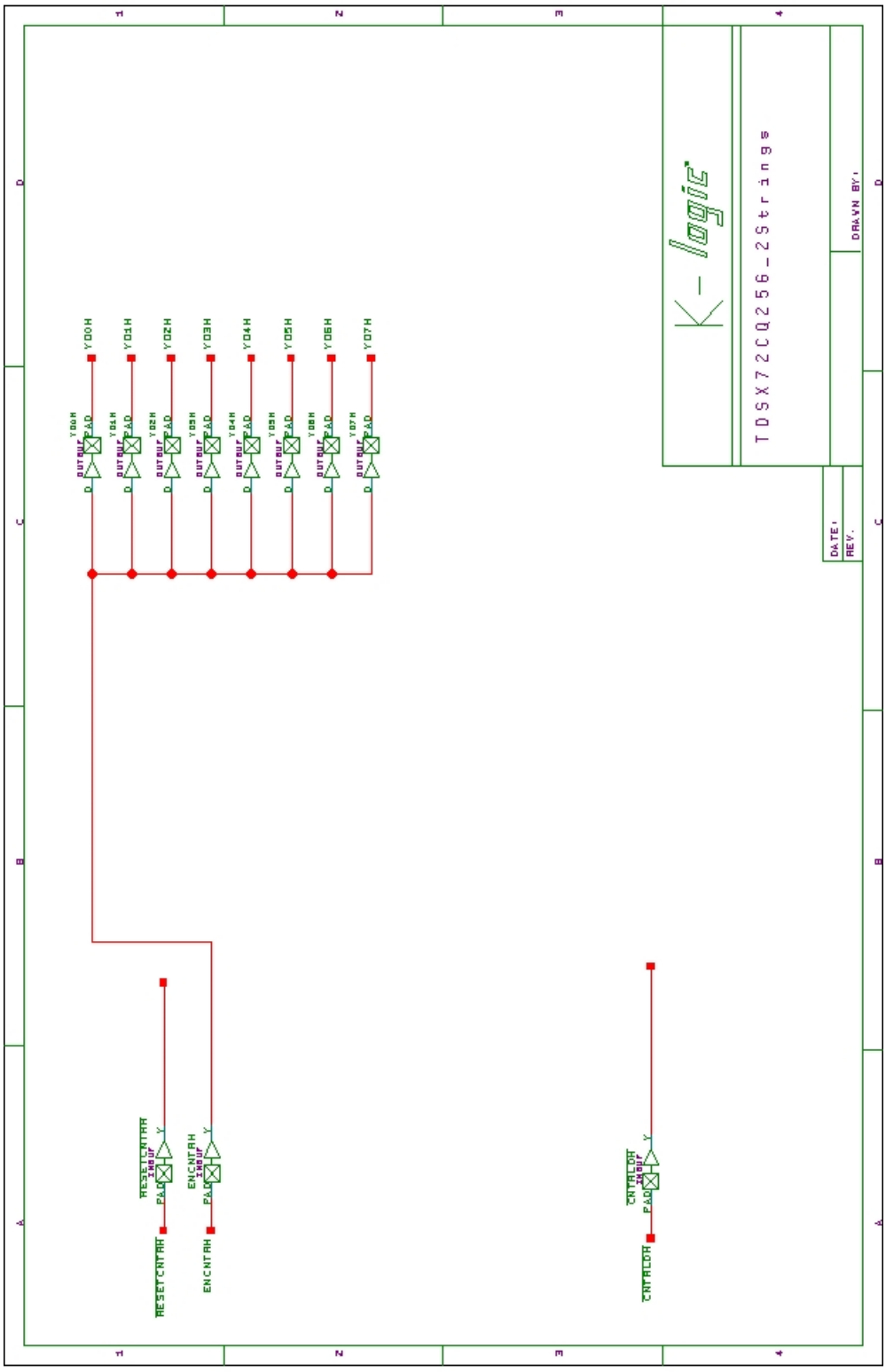

DRC
ANDC
ANDP
DRP
AND4
DR4
RST
D
CLK
K- logic
DRAWN BY:
DATE:
REV.

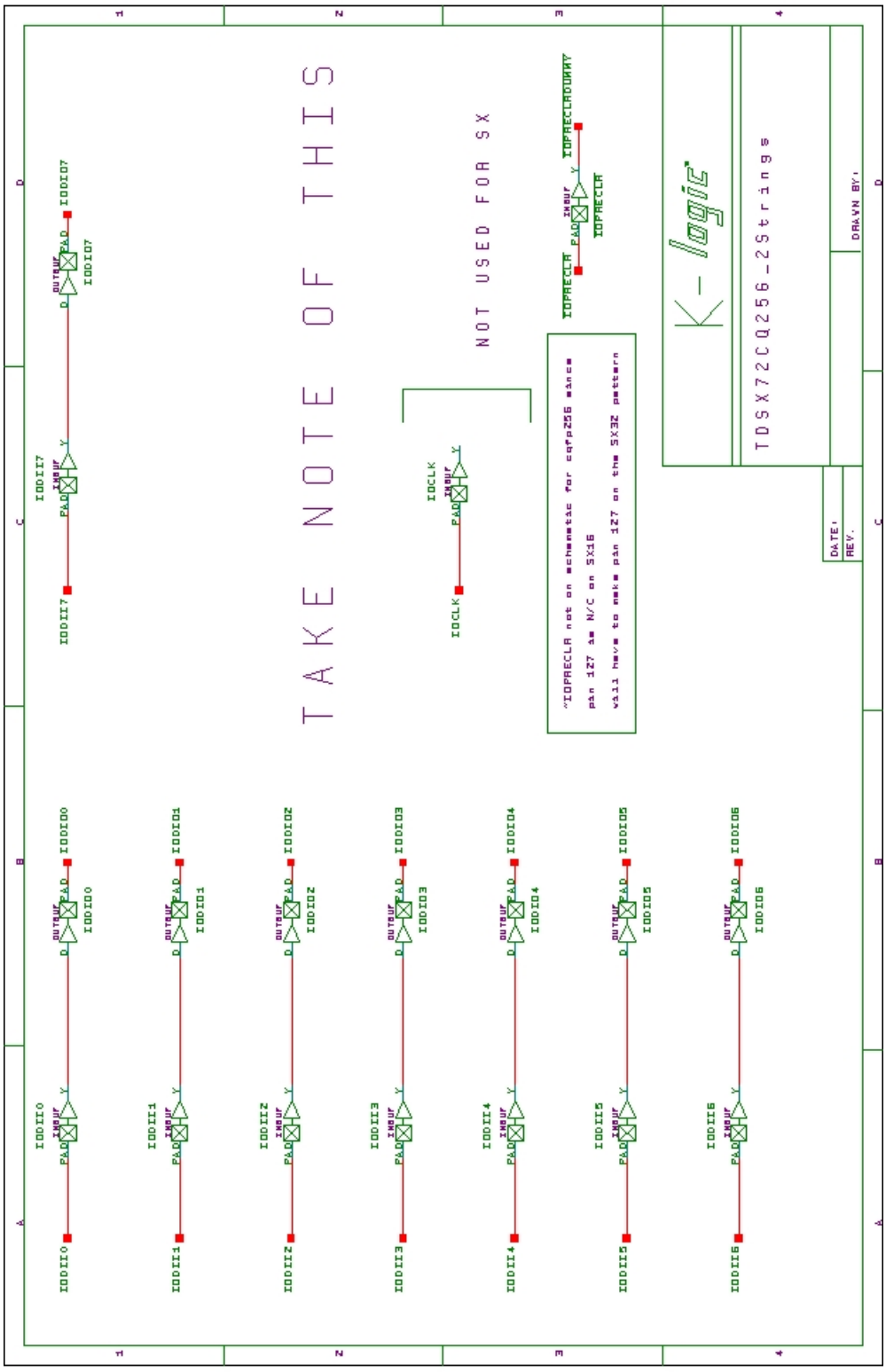

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDP
DRP
RST
D
CLK

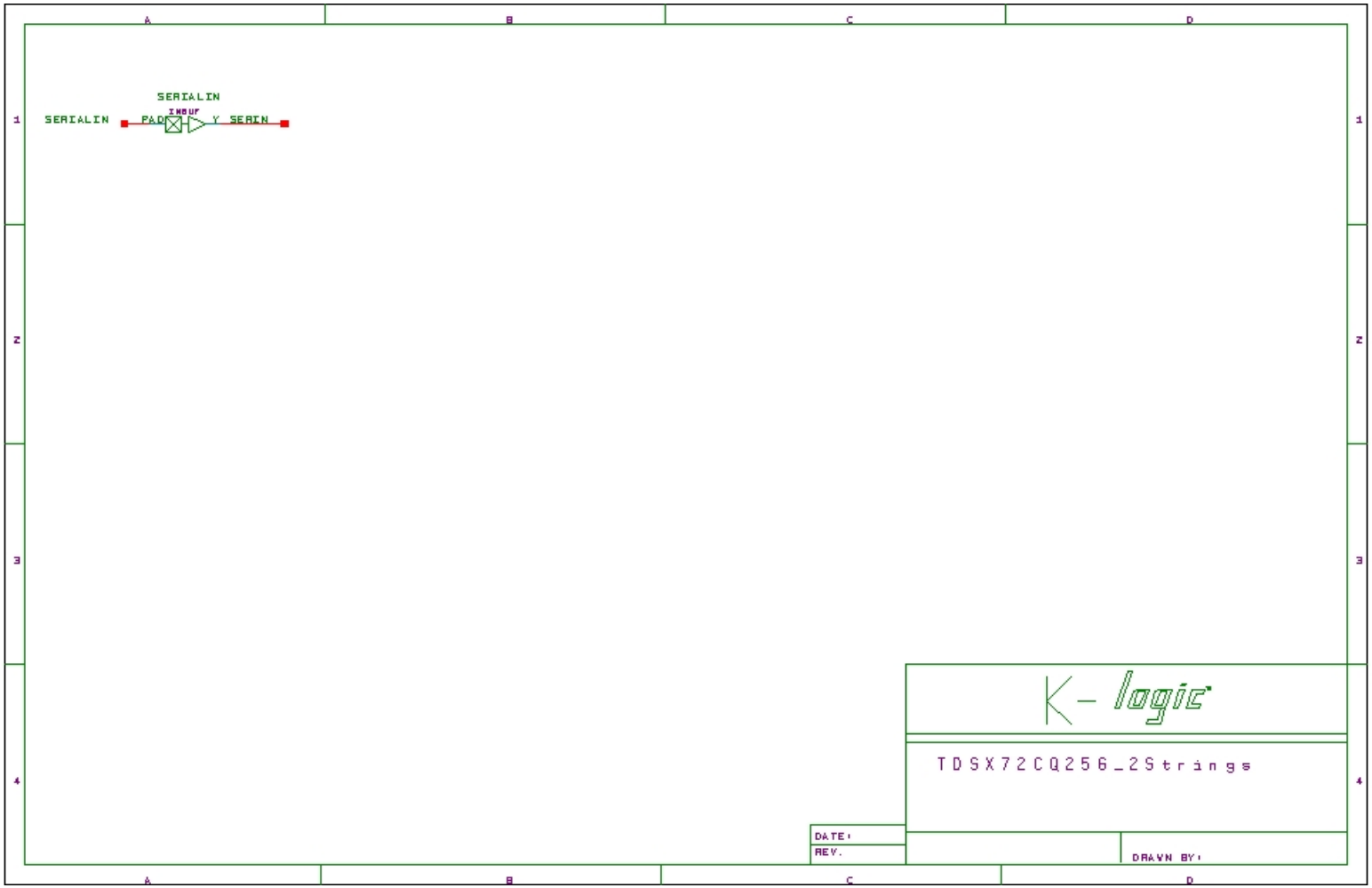

DRC
ANDC
ANDP
DRP
K- logic
DRAWN BY:
DATE:
REV.
RST
D
CLK

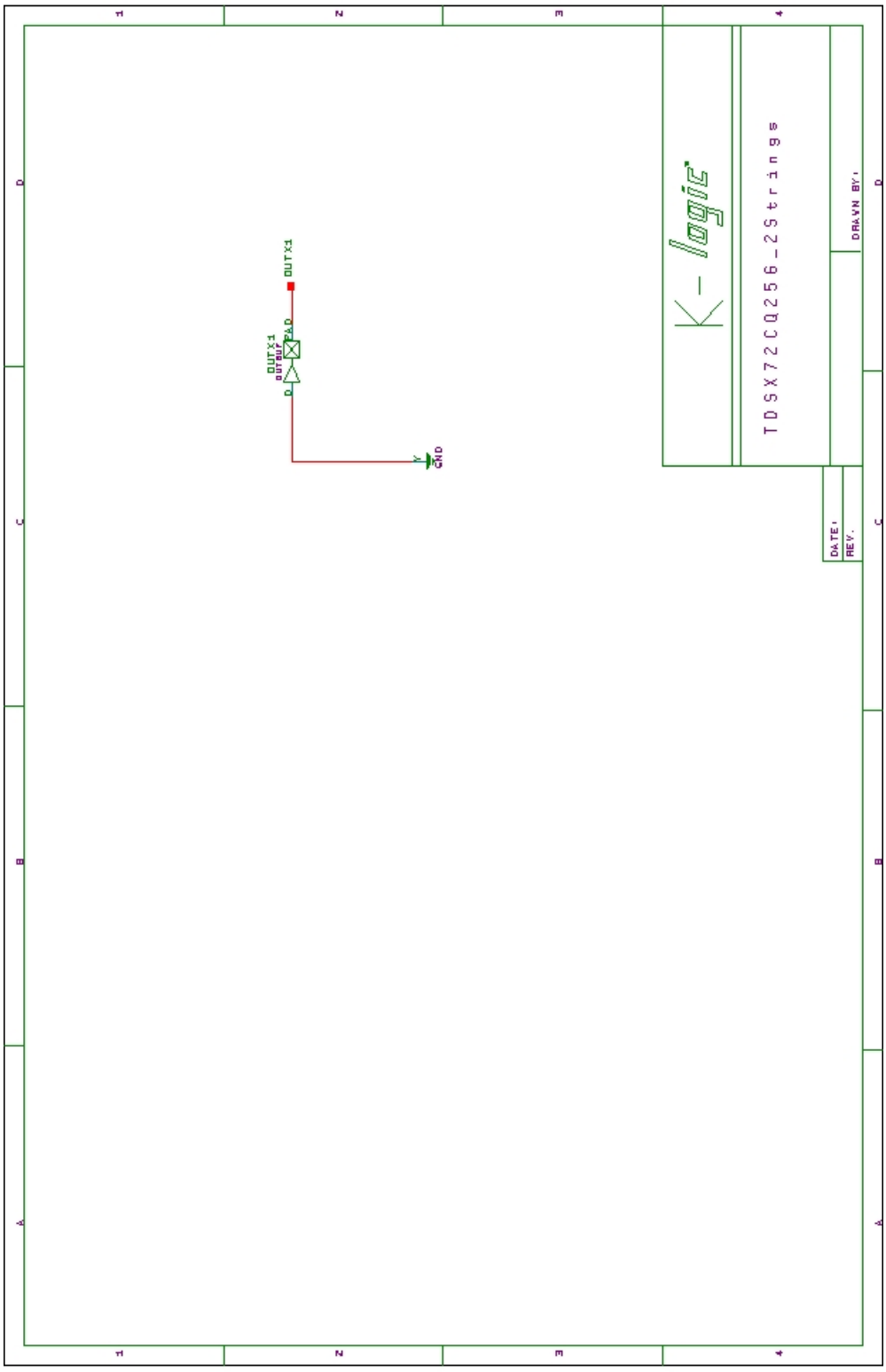

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDF
DRF
D
RST
CLK


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
DA2H OUTBUF PAD
DA0H OUTBUF PAD
DA1H OUTBUF PAD
DAH INBUF PAD Y FFINH
CLOCKH HCLKBUF PAD Y
RESETH INBUF PAD Y
DAH
CLOCKH
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALOH
IBUF


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IOCLK
IOPRECLR
IOPRECLRQUANY
*IOPRECLR not on schematic for csfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern


A
B
C
D
1
2
3
4
SERIALIN
SERIALIN
INBUF
PAD
Y
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
OUTX1
PAD
GND