TOTAL IONIZING DOSE TEST REPORT

No. 04T-RT54SX72S-BP15146-01
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad(Si)
2. I_{CC}	Passed 72 krad(Si) for 25 mA spec
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 100 krad(Si) for 10% degradation criterion
6. Transition Time	Passed 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT information and irradiation conditions

Part Number	RT54SX72S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 µm CMOS
DUT Design	TDSX72CQFP256_2Strings
Die Lot Number	BP15146-01
Quantity Tested	4
Serial Number	23839, 23844, 23873, 23943
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad(Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

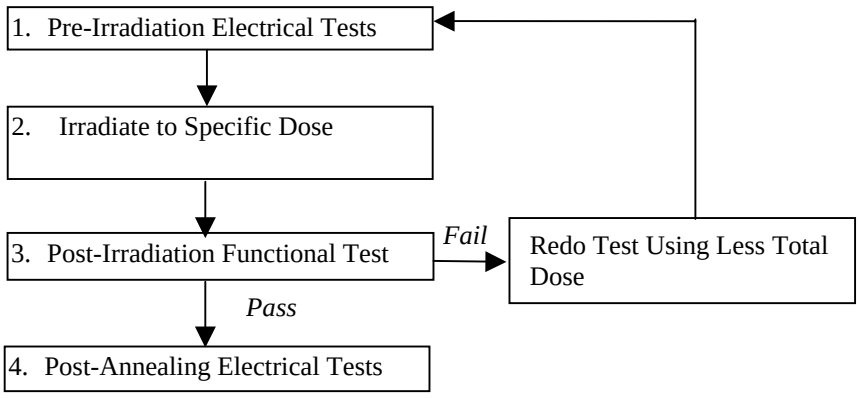


Figure 1 Parametric test flow chart

The parametric tests follow the military standard test method 1019.5. Fig 1 shows the testing flow. The time dependent effect (TDE) of this product was previously evaluated by comparing the results of a high dose rate (1 krad(Si)/min) against the results of a low dose rate (1 krad(Si)/hr). No adverse TDE was observed. Therefore the accelerated aging test (rebound test) is omitted. Room temperature annealing were performed for approximately one month after 100 krad(Si) of irradiation. DUTs were static biased during annealing.

C. Electrical Parameter Measurements

A high utilization design (TDSX72CQ256_2Strings) to address total dose effects in typical space applications is used. The circuit schematics are shown in appendix A.

Table 2 lists the electrical parameters measured. The functionality is measured pre-irradiation, post-irradiation, and post-annealing on the output pin (O_AND3 or O_AND4) of the two combinational buffer-strings and on the output pins (O_OR4 and O_NAND4) of the shift register. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively.

The input logic thresholds (V_{TIL}/V_{IH}) and output drives (V_{OL}/V_{OH}) are measured pre-irradiation and post-annealing on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured pre-irradiation and post-annealing on the O_AND4 output of one of the buffer strings. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the O_AND4. The transient times (rise and fall times) are measured post-annealing on the O_AND4.

Each unused input is grounded with an 1 M ohm resistor during irradiation and an 1.2K ohm resistor during annealing.

Table 2. Logic design for parametric tests

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)

III. Test Results

A. Functionality

Every DUT passed the gross functional test at pre-irradiation, post-irradiation, and post-annealing.

B. I_{CC}

Figure 2 to Figure 6 show the in-flux I_{CC} plots. An empirical equation is used to extract the total dose tolerance after a 10 years annealing. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA can be obtained by the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Use the worst-case $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ in DUT 23844 (Figure 3), the tolerance ($\gamma_{critical}$) is obtained as approximately 72 krad(Si). This extracted tolerance is very conservative because experiments showed that a DUT irradiated at high dose rate and then annealed for the duration of total mission time resulted a significantly higher I_{CC} than that of a DUT irradiated at a low, uniform dose rate throughout the total mission time.

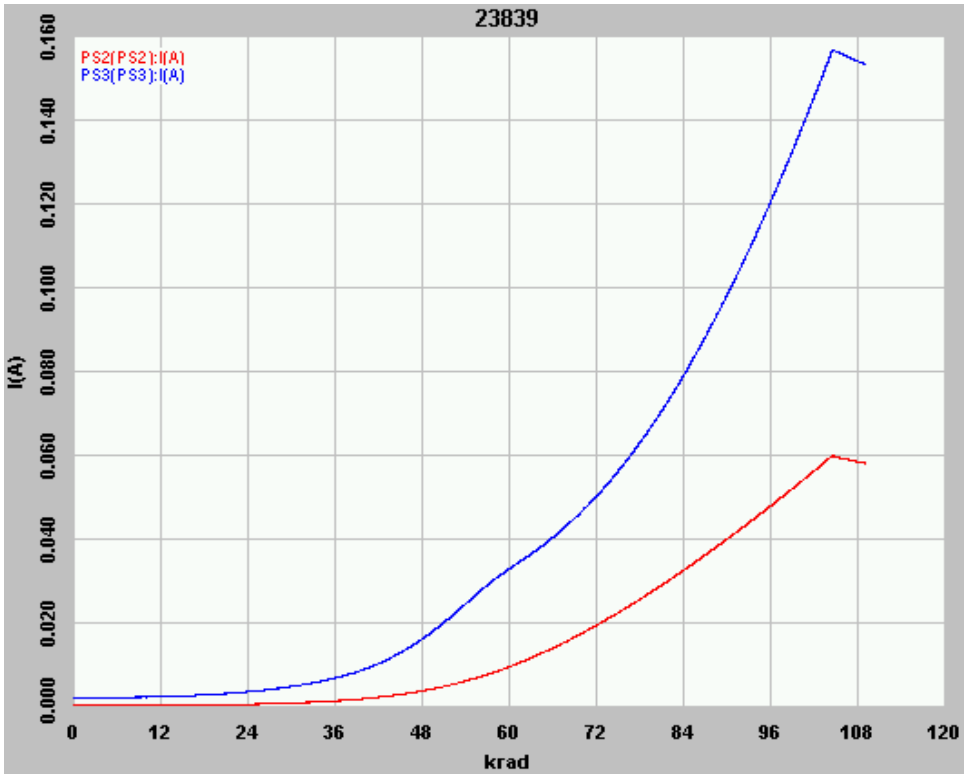


Figure 2 In-flux I_{CC} of DUT 23839, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

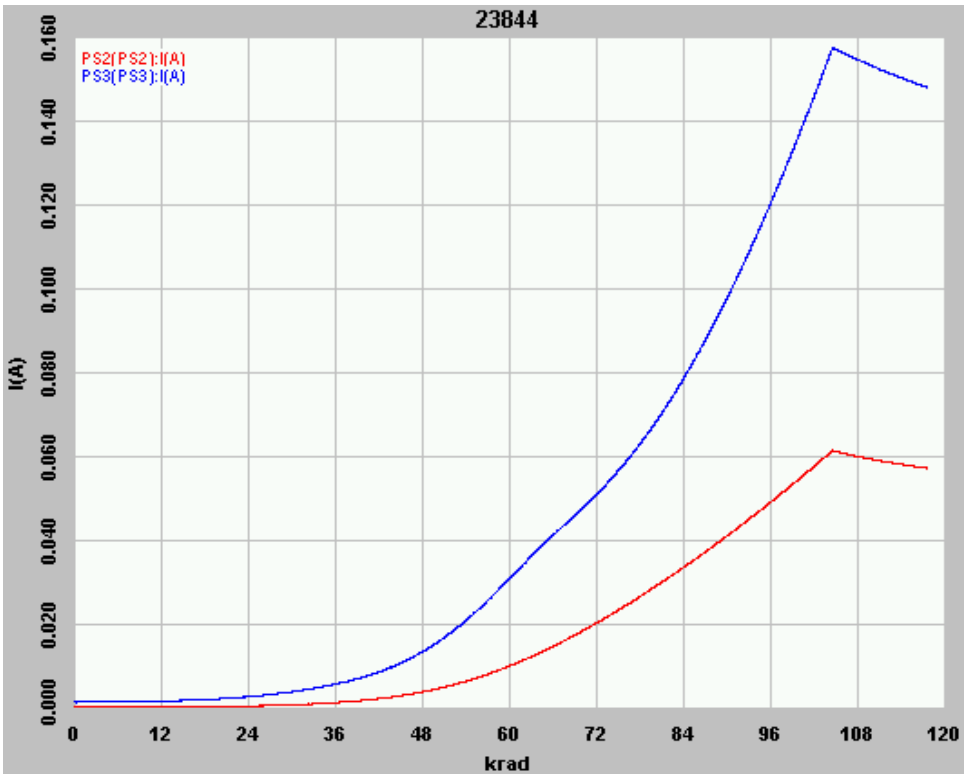


Figure 3 In-flux I_{CC} of DUT 23844, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

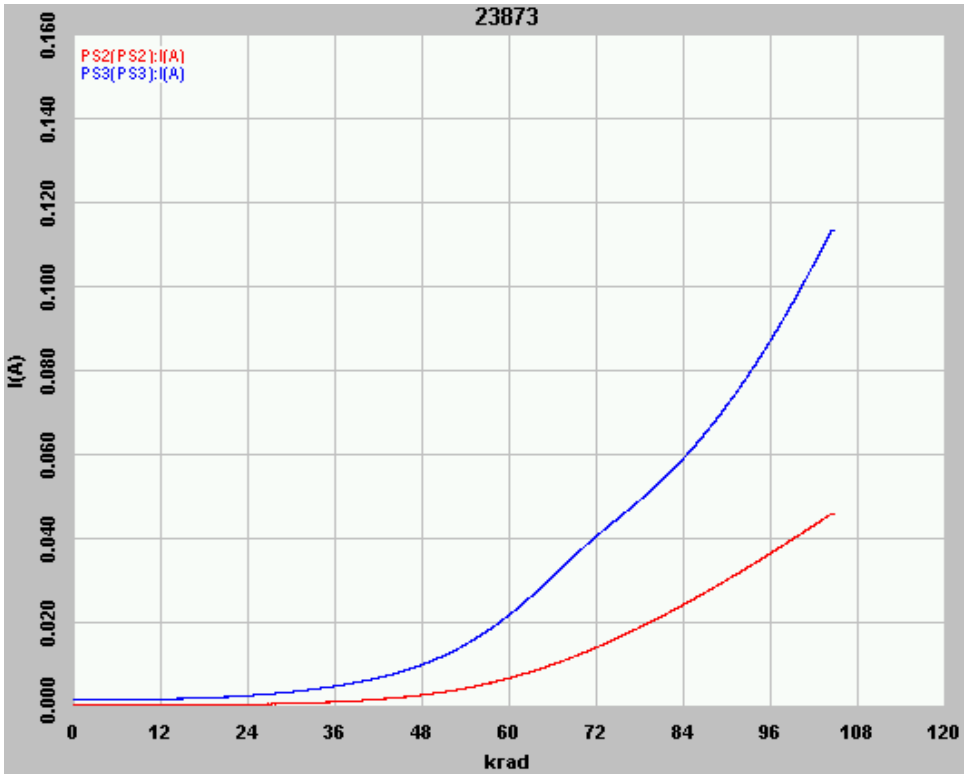


Figure4 In-flux I_{CC} of DUT 23873, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

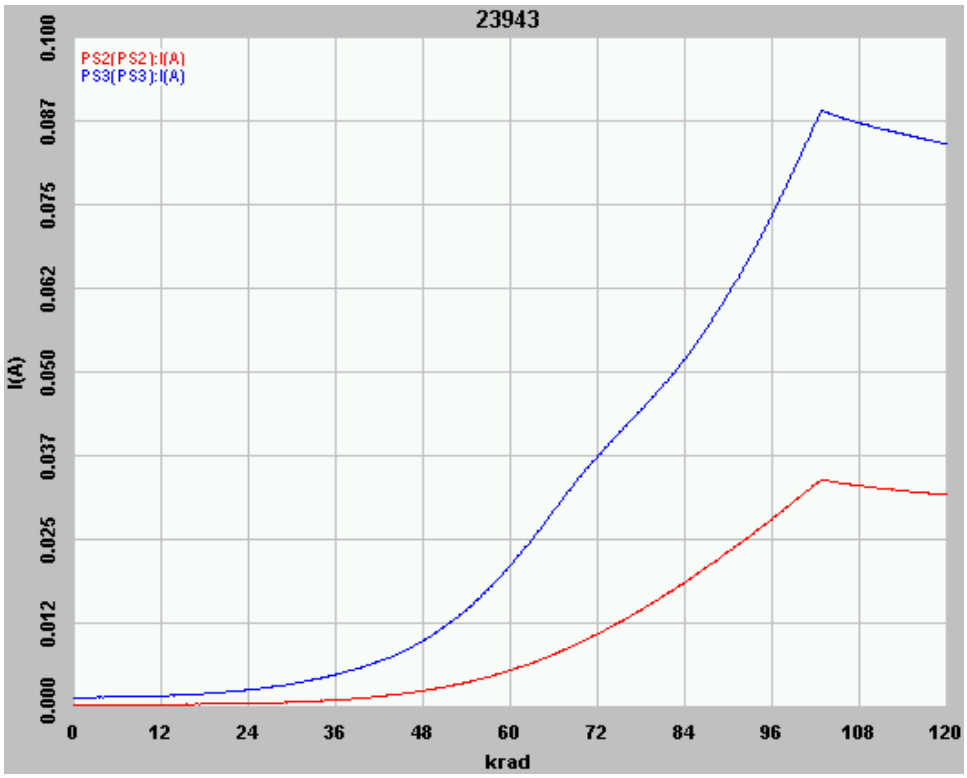


Figure5 In-flux I_{CC} of DUT 23943, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

C. *Input Logic Threshold (V_{IL}/V_{IH})*

Table 3 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 3 Pre-irradiation and post-annealing input logic threshold in volts

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL}	V_{IH}	V_{IL}	V_{IH}
23839	1.43	1.53	1.33	1.39
23844	1.44	1.54	1.33	1.39
23873	1.44	1.54	1.34	1.40
23943	1.40	1.50	1.35	1.41

D. *Output Characteristics (V_{OL}/V_{OH})*

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in table 4 and 5. The post-annealing data are within the spec limits, and 100 krad(Si) radiation has little effect on these parameters.

Table 4 Pre-irradiation and post-annealing V_{OL} (in volts) at various sinking current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
23839	0.009	0.009	0.103	0.102	0.171	0.170	0.432	0.430	0.887	0.883
23844	0.009	0.009	0.101	0.101	0.169	0.169	0.427	0.427	0.880	0.877
23873	0.009	0.009	0.102	0.101	0.171	0.169	0.431	0.426	0.886	0.877
23943	0.009	0.009	0.105	0.105	0.176	0.176	0.443	0.443	0.911	0.912

Table 5 Pre-irradiation and post-annealing V_{OH} (in volts) at various sourcing current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
23839	4.98	4.99	4.86	4.87	4.65	4.66	4.10	4.10	2.99	2.99
23844	4.98	4.98	4.86	4.86	4.64	4.65	4.08	4.09	2.94	2.94
23873	4.98	4.99	4.86	4.86	4.65	4.66	4.09	4.11	2.94	2.98
23943	4.98	4.98	4.86	4.86	4.64	4.64	4.06	4.06	2.87	2.87

E. *Propagation Delays*

Tables 6 and 7 list the pre-irradiation and post-annealing propagation delays, and radiation-induced degradations. The radiation-induced degradations are less than 10%.

Table 6 Low to high delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Anneal	Degradation (%)
23839	1326.5	1379.1	3.97
23844	1302.7	1360.1	4.41
23873	1299.3	1357.1	4.45
23943	1322.1	1404.6	6.24

Table 7 High to low delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Anneal	Degradation (%)
23839	1046.0	1099.1	5.11
23844	1073.9	1145.6	6.68
23873	1061.3	1120.5	5.58
23943	1118.8	1215.8	8.67

F. Transition Time

The pre-irradiation and post-annealing rising edges are plotted in Figure 6 to Figure 9, and the pre-irradiation and post-annealing falling edges are plotted in Figure 10 to Figure 13. These figures show that the radiation effect on the transition time is negligible.

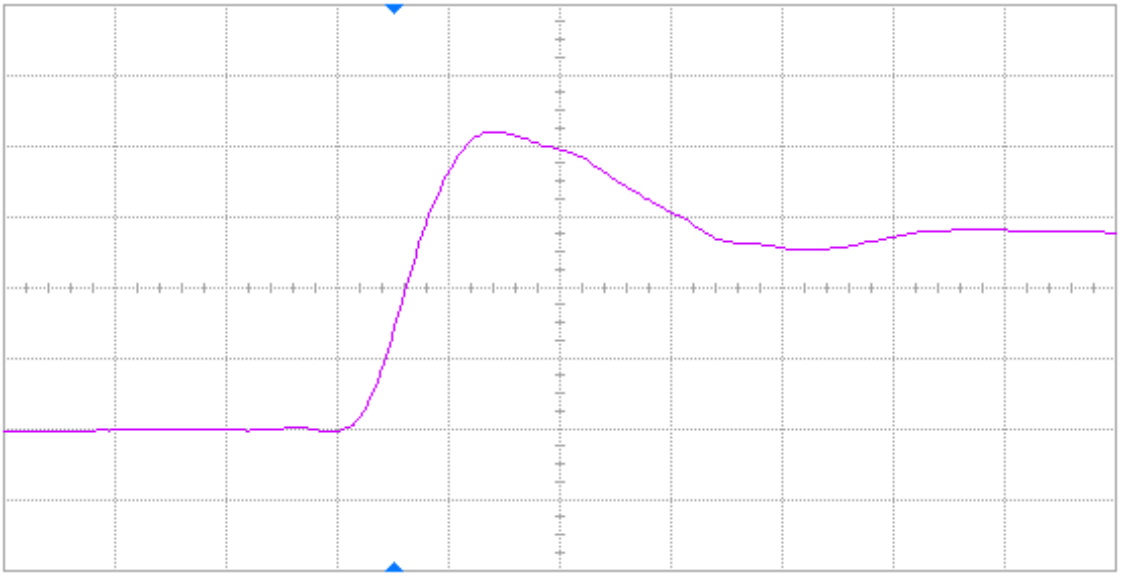


Figure 6(a) Pre-irradiation rising edge of DUT 23839, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

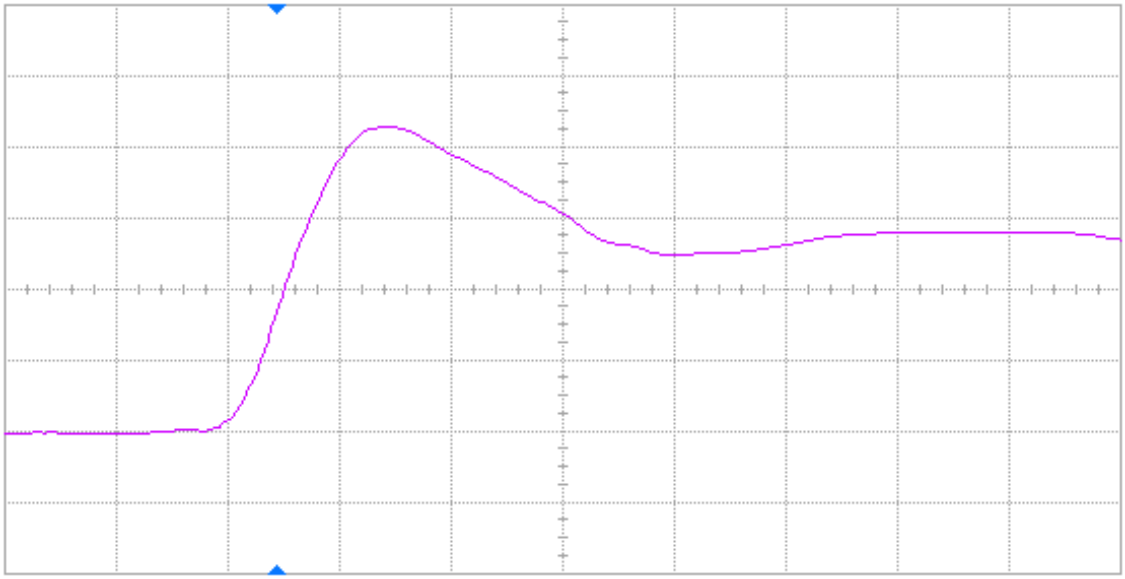


Figure 6(b) Post-annealing rising edge of DUT 23839, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

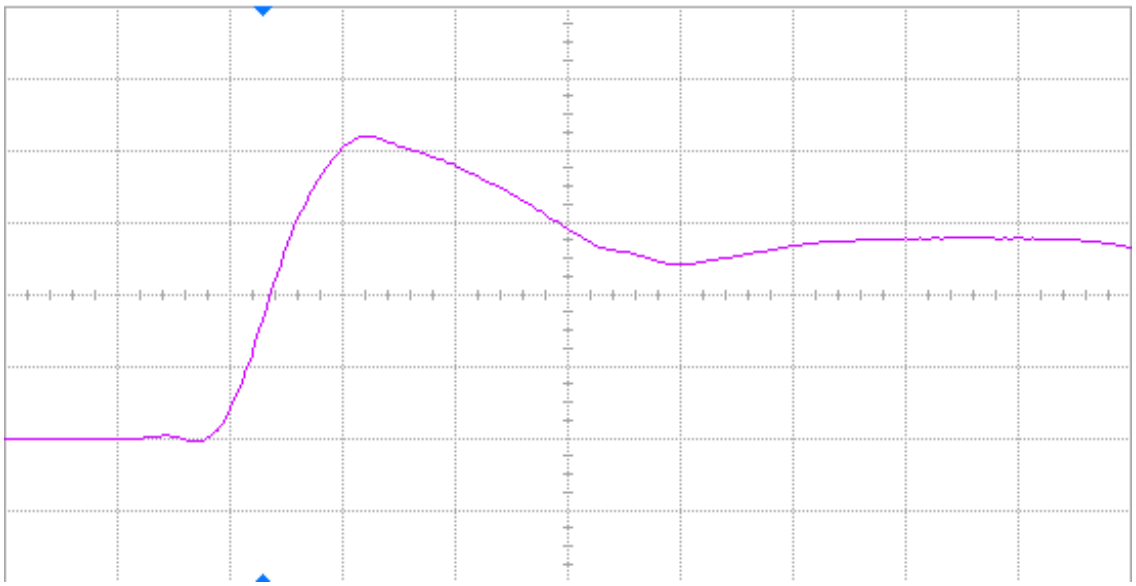


Figure 7 Post-annealing rising edge of DUT 23844, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

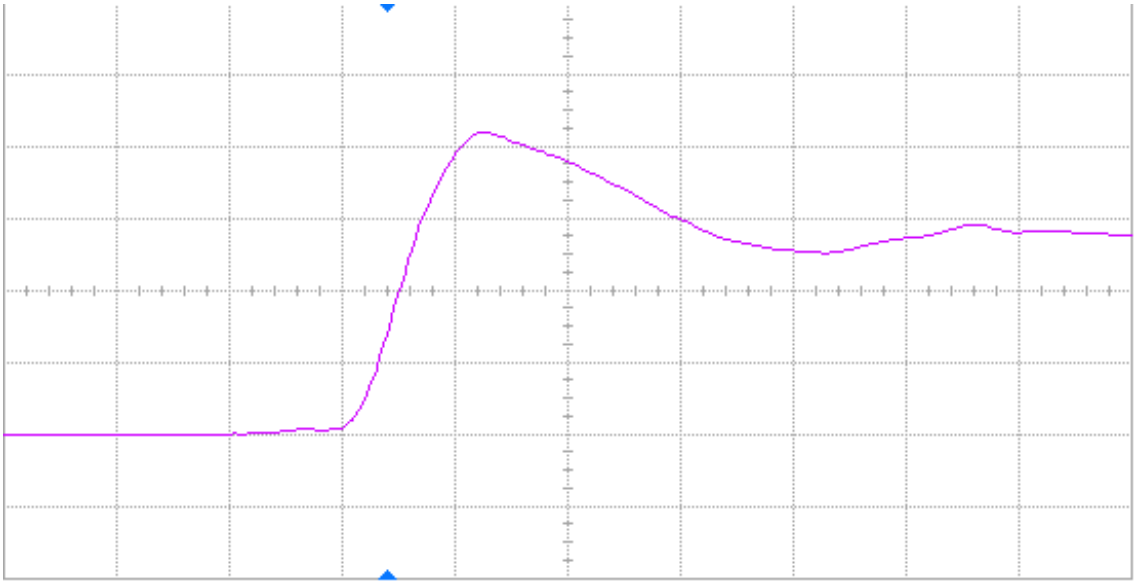


Figure 8(a) Pre-irradiation rising edge of DUT 23873, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

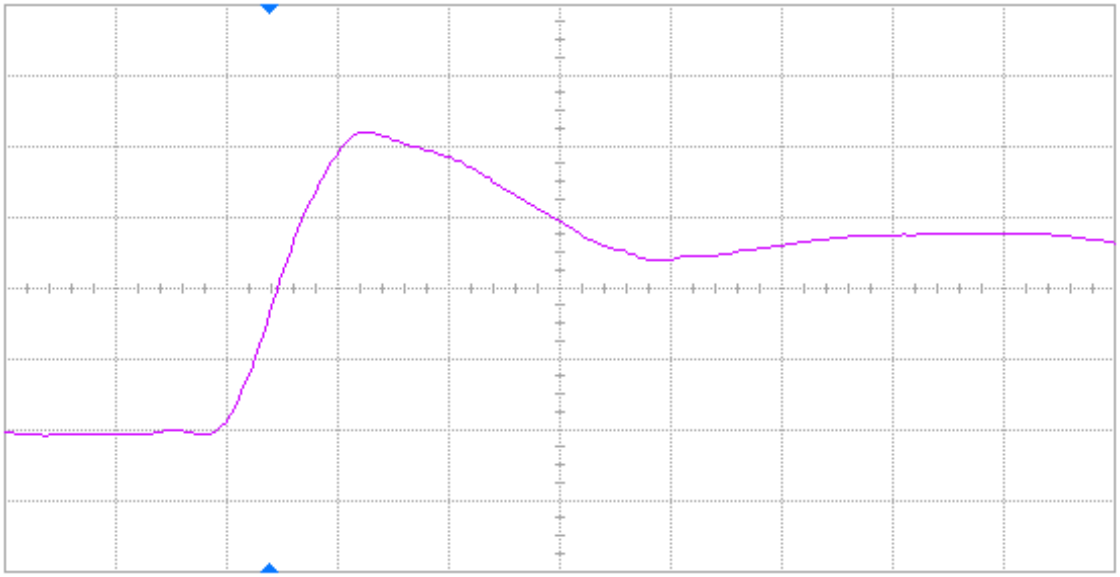


Figure 8(b) Post-annealing rising edge of DUT 23873, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

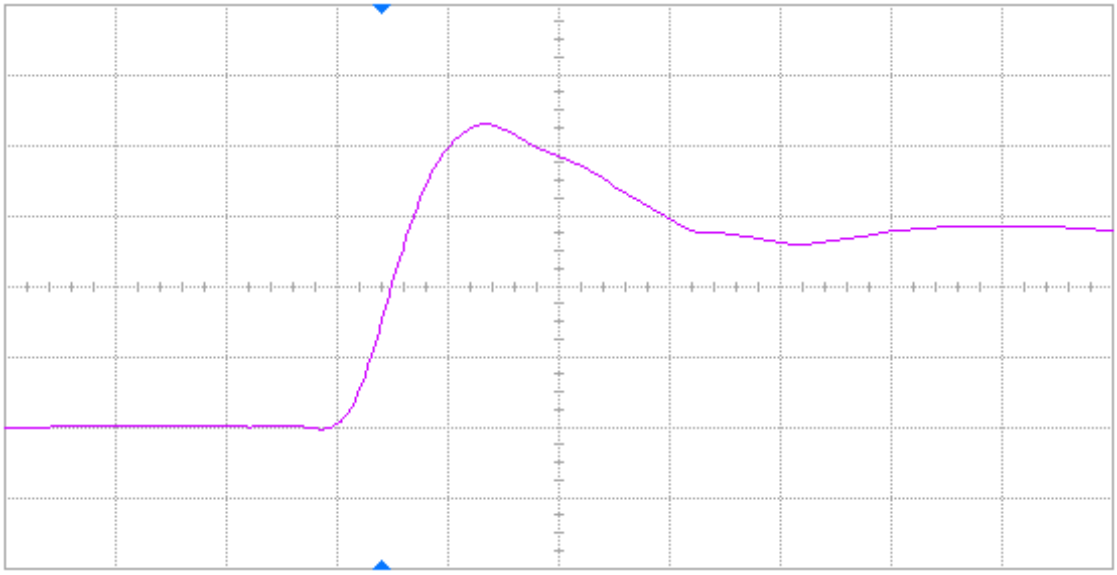


Figure 9(a) Pre-irradiation rising edge of DUT 23943, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

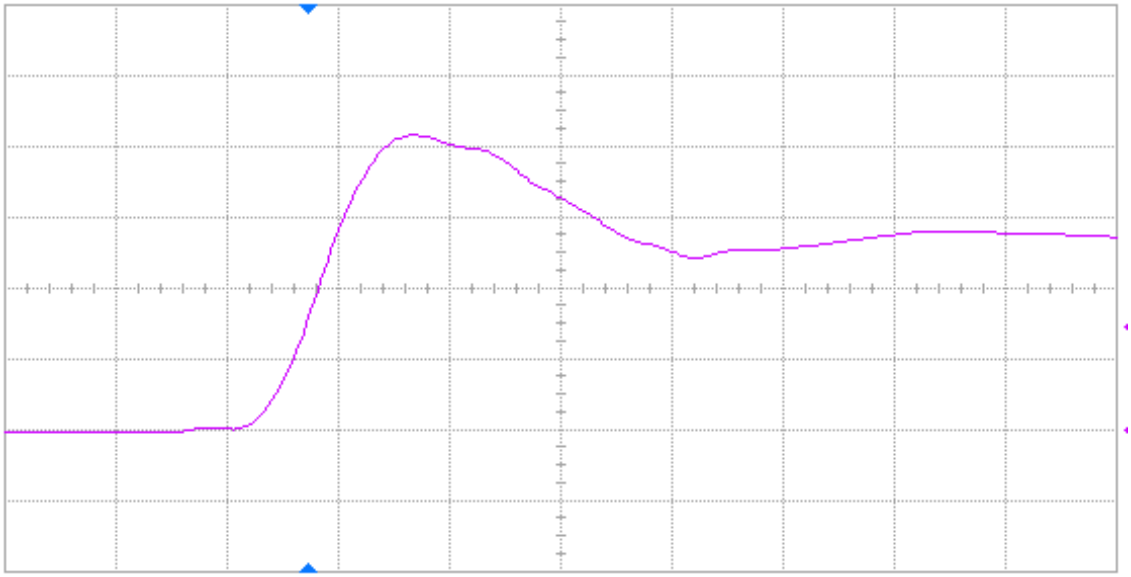


Figure 9(b) Post-annealing rising edge of DUT 23943, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

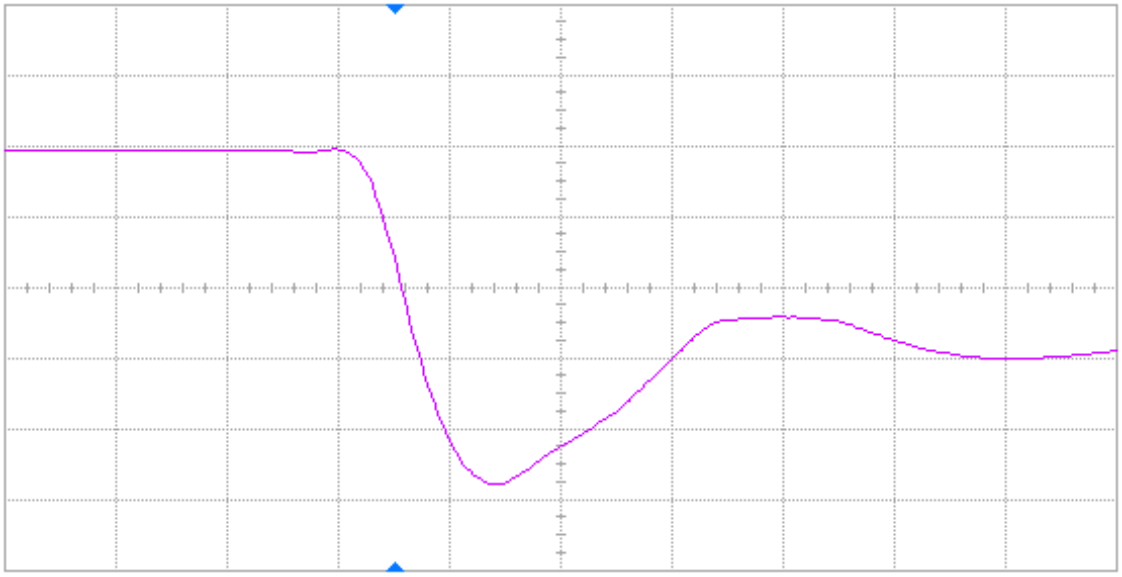


Figure 10(a) Pre-irradiation falling edge of DUT 23839, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

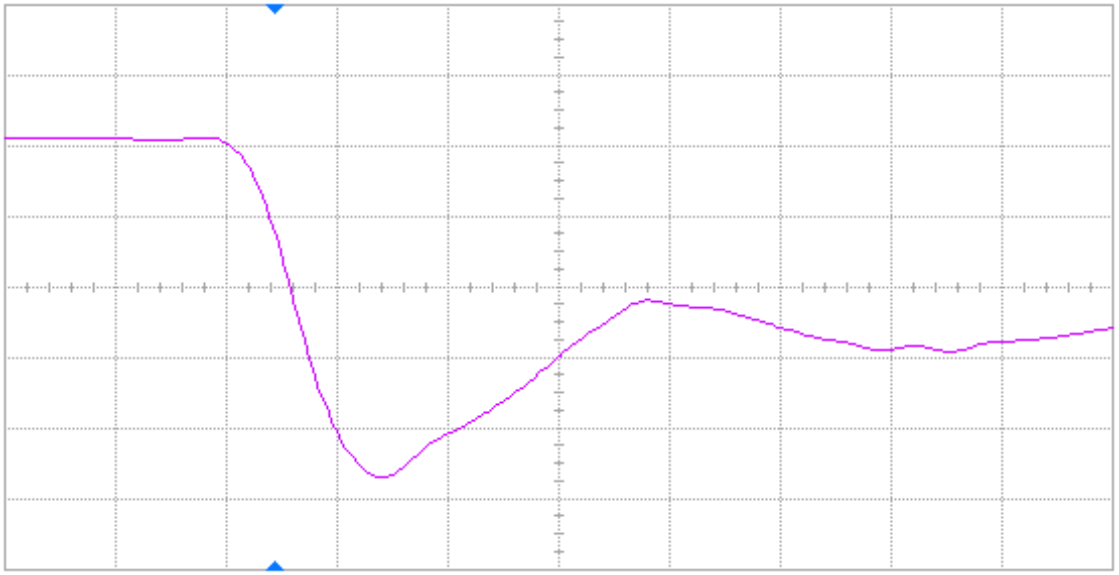


Figure 10(b) Post-annealing falling edge of DUT 23839, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

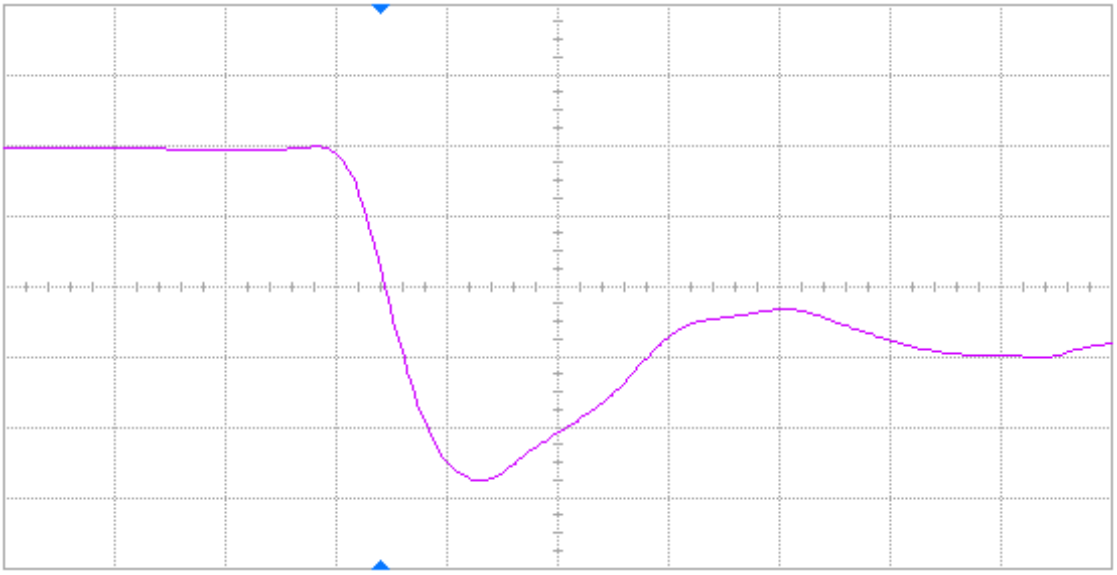


Figure 11(a) Pre-irradiation falling edge of DUT 23844, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

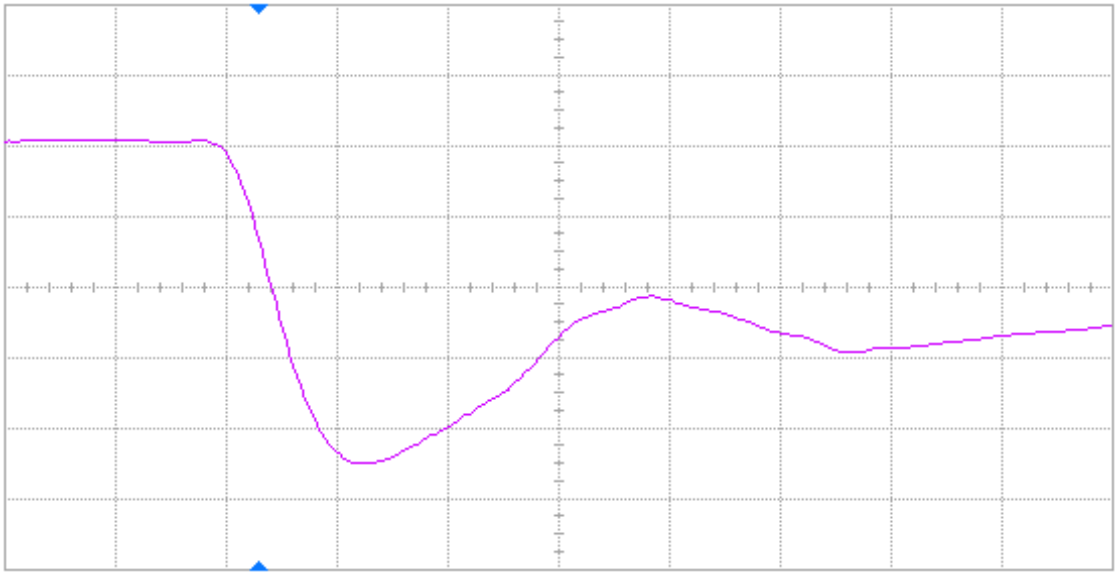


Figure 11(b) Post-annealing falling edge of DUT 23844, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

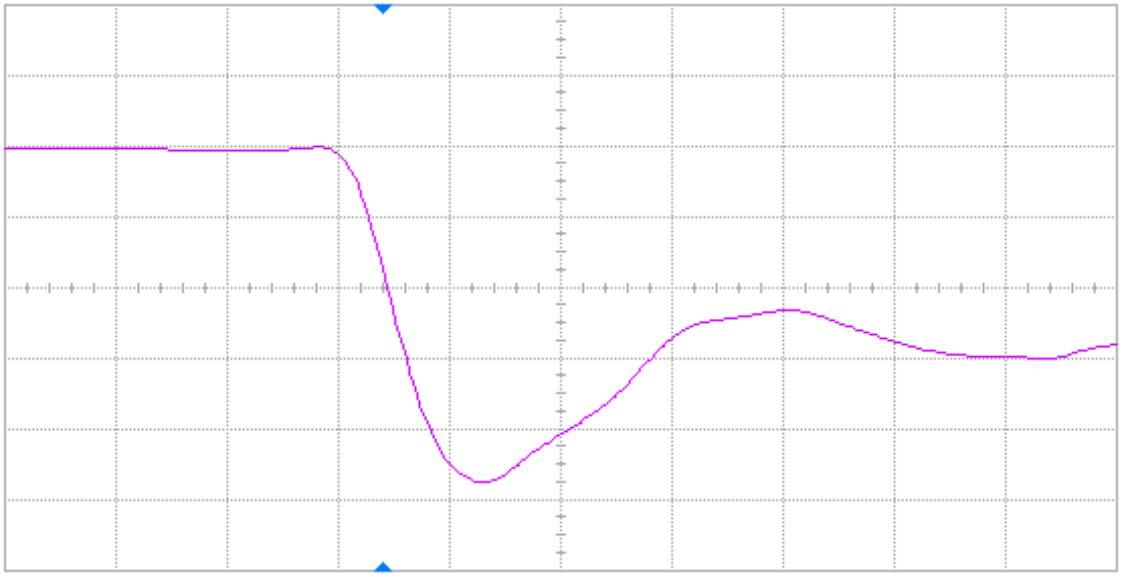


Figure 12(a) Pre-irradiation falling edge of DUT 23873, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

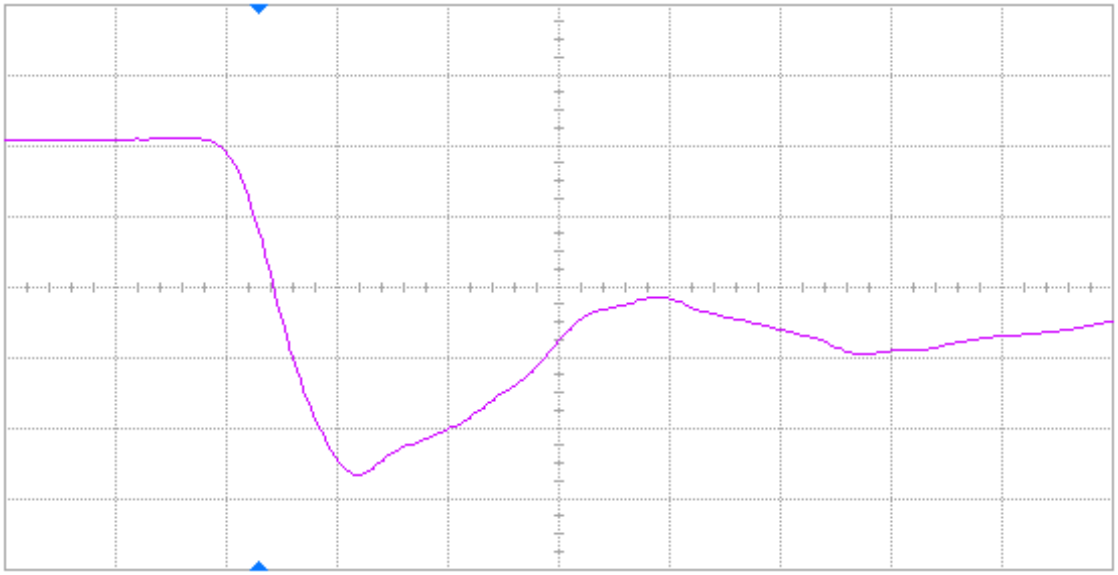


Figure 12(b) Post-annealing falling edge of DUT 23873, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

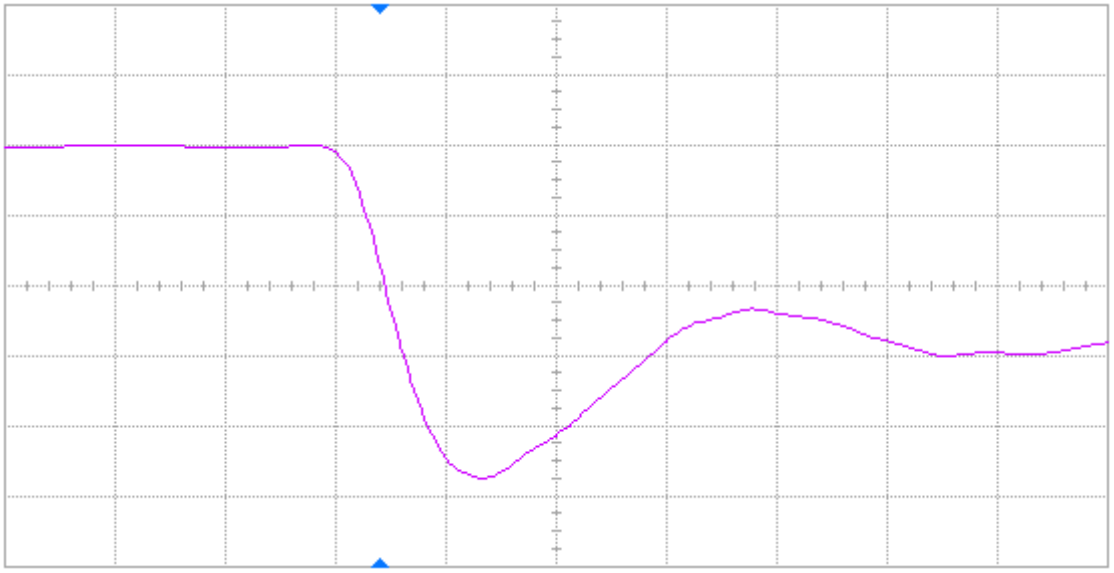


Figure 13(a) Pre-irradiation falling edge of DUT 23943, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

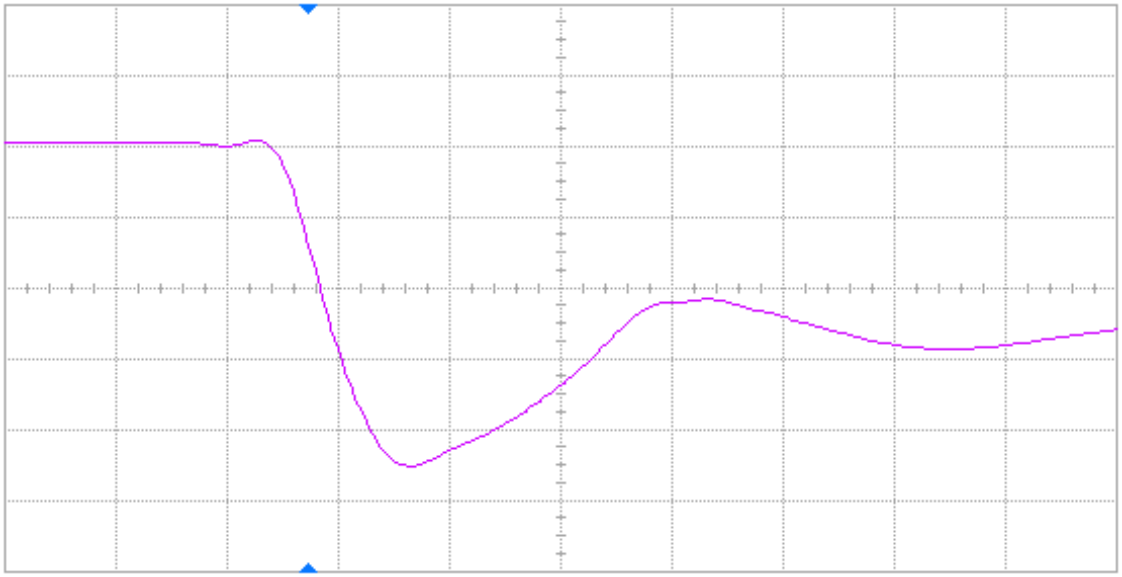
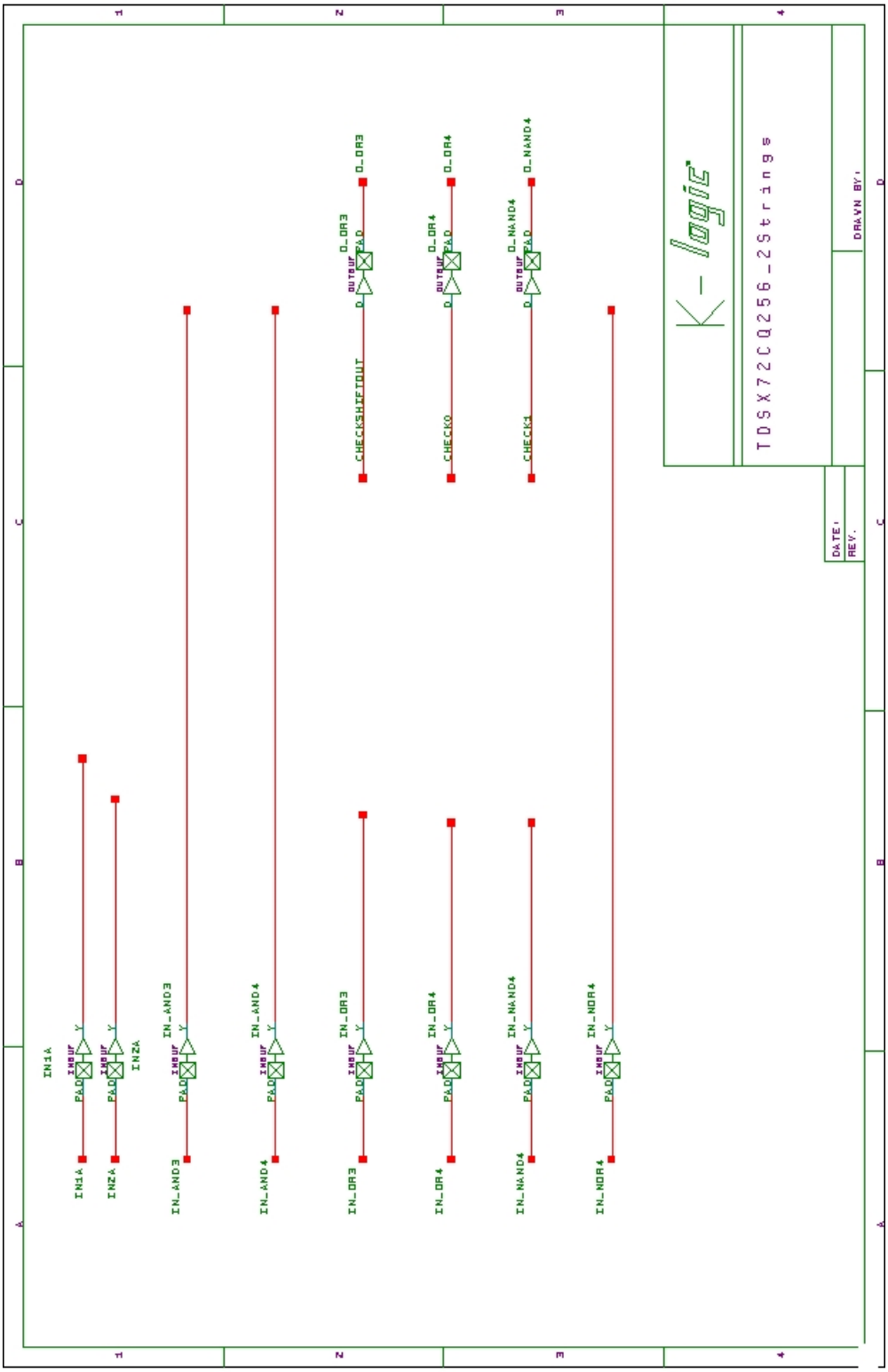
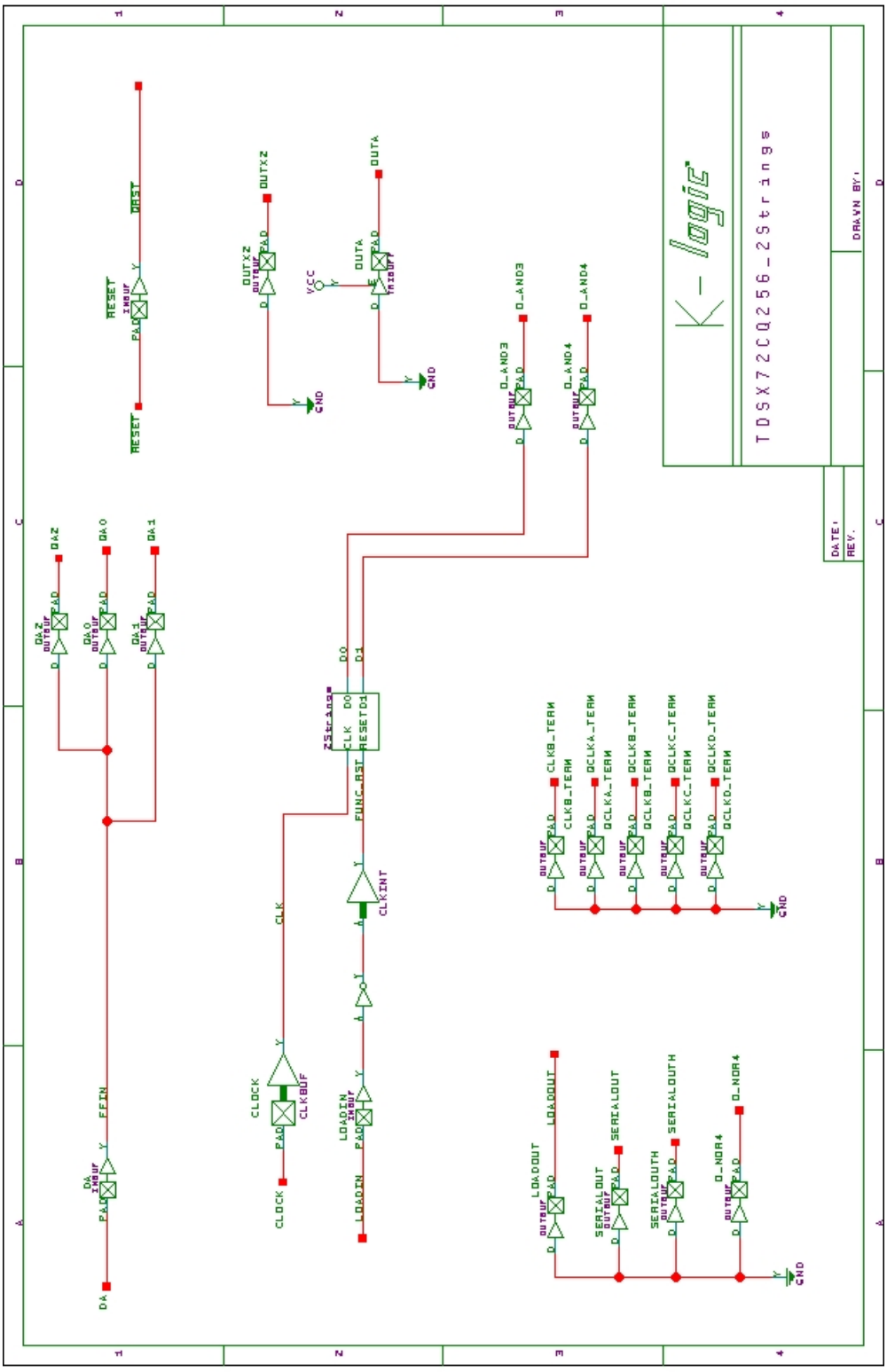


Figure 13(b) Post-annealing falling edge of DUT 23943, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

APPENDIX A DUT DESIGN SCHEMATICS

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TDSX72CQ256_2Strings
DRAWN BY:
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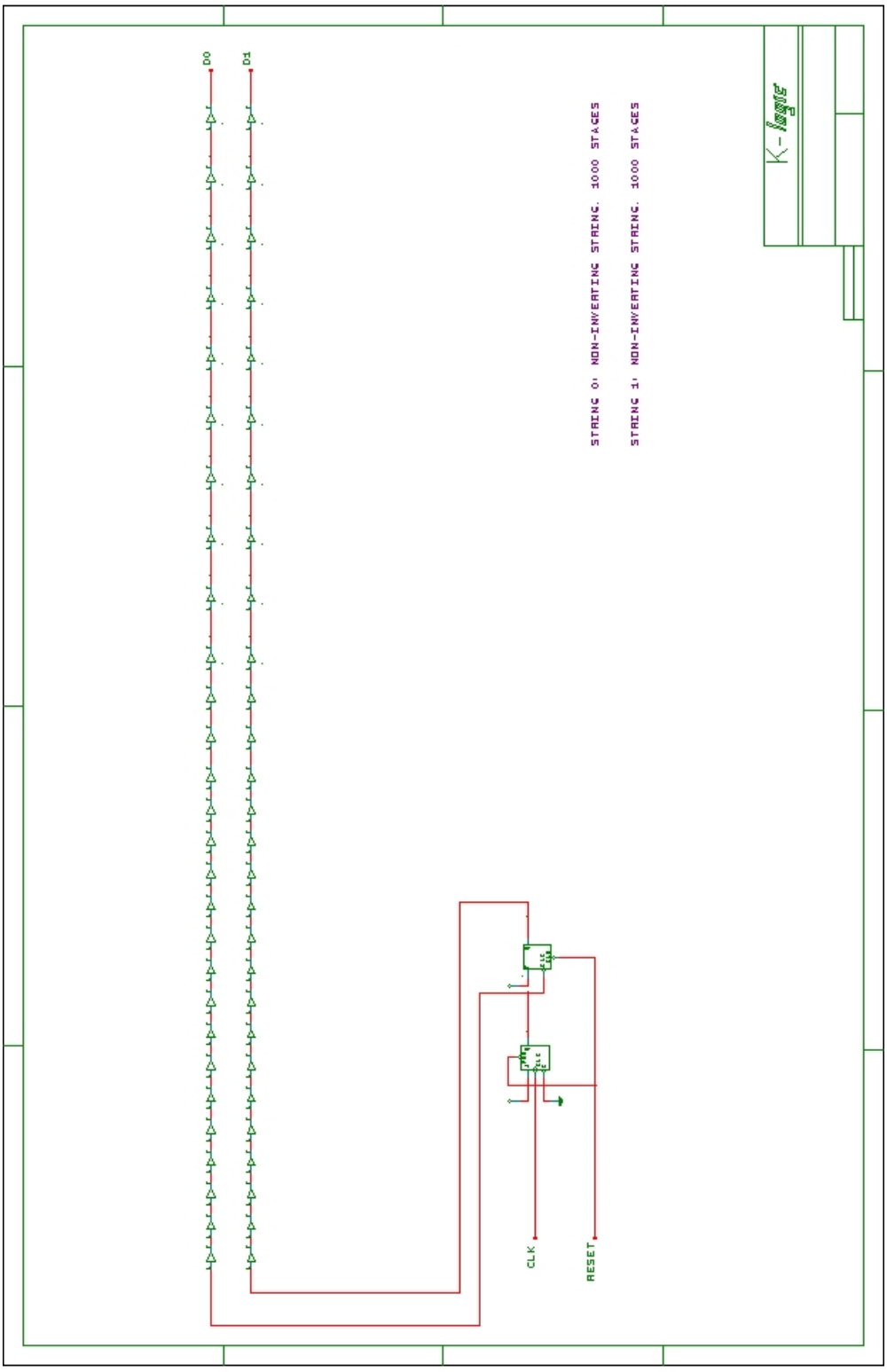
REV.
RESET
RST
OUTXZ
OUTA
VCC
GND
D_AND3
D_AND4
DA2
DA0
DA1
DA
FFIN
CLOCK
CLKBUF
CLK
CLKINT
LOADIN
2Strings
CLK D0
RESET D1
D0
D1
FUNC_RST
CLKB_TERM
DCLKA_TERM
DCLKB_TERM
DCLKC_TERM
DCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4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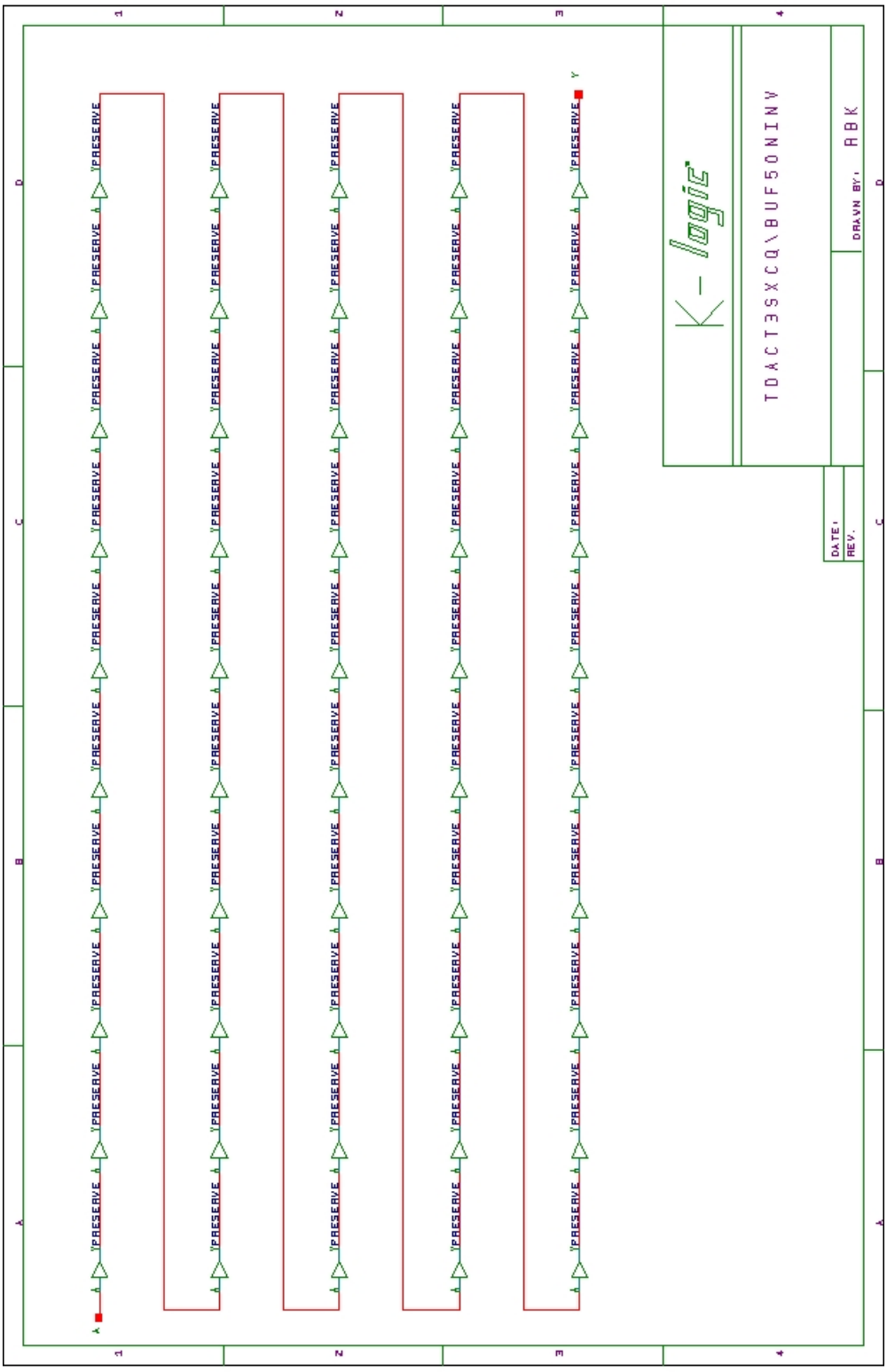
D1
STRING 0: NON-INVERTING STRING, 1000 STAGES
STRING 1: NON-INVERTING STRING, 1000 STAGES
K-logic
CLK
RESET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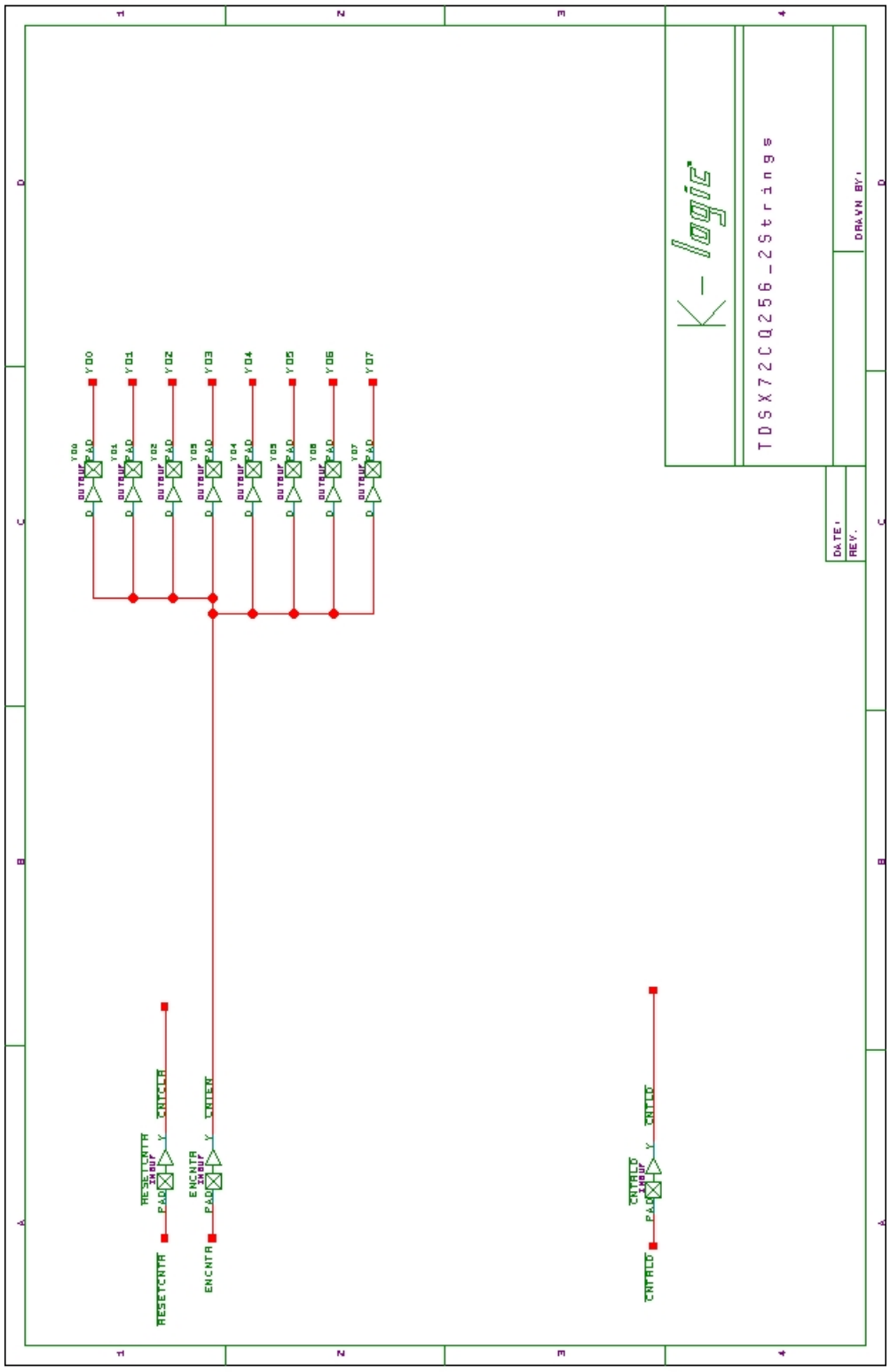
DRAWN BY: ABK
DATE:
REV.
Y
A
PRESERVE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TDSX72CQ256_2Strings
DRAWN BY:
DATE:
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Y01
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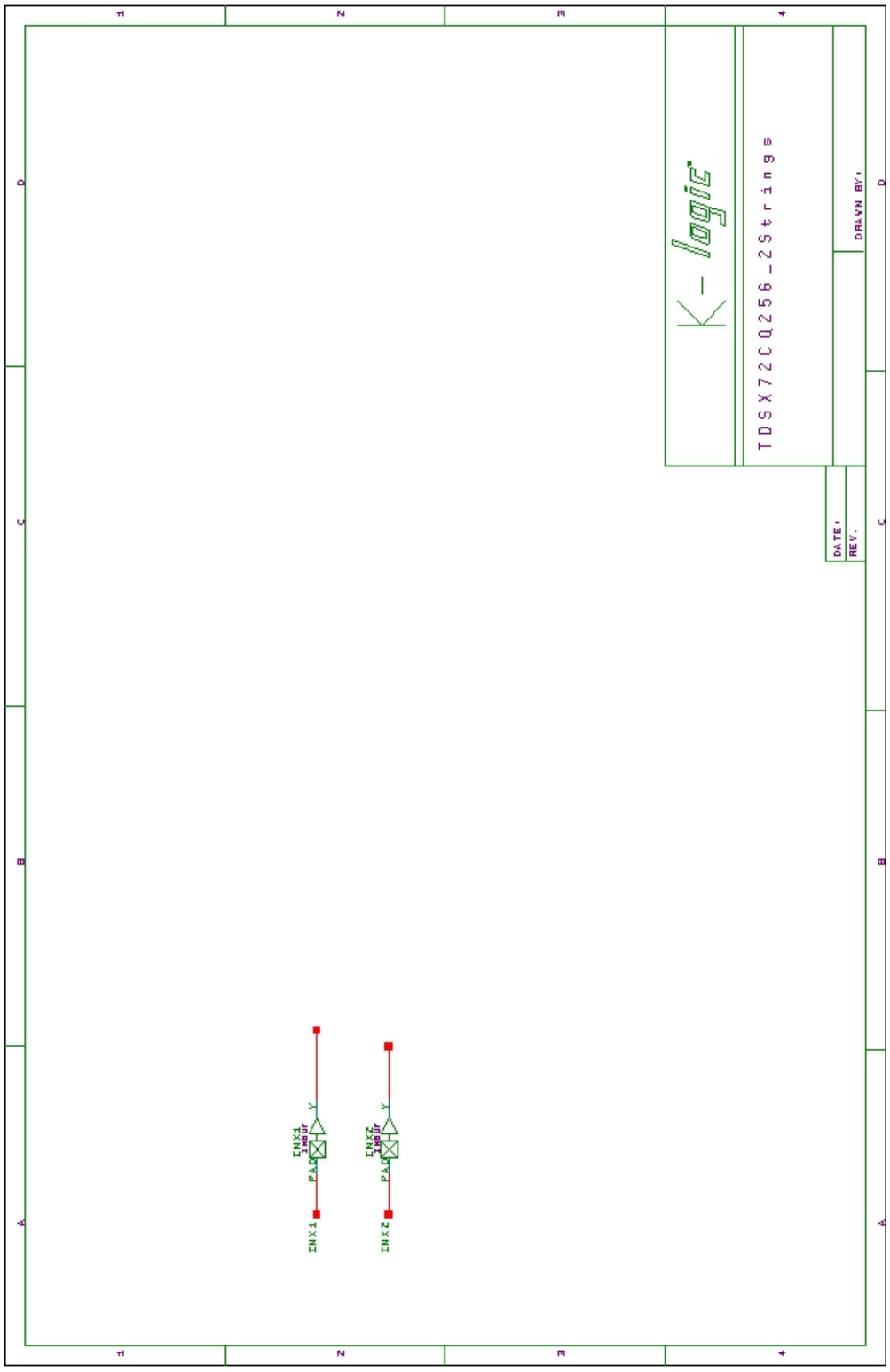
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REV.
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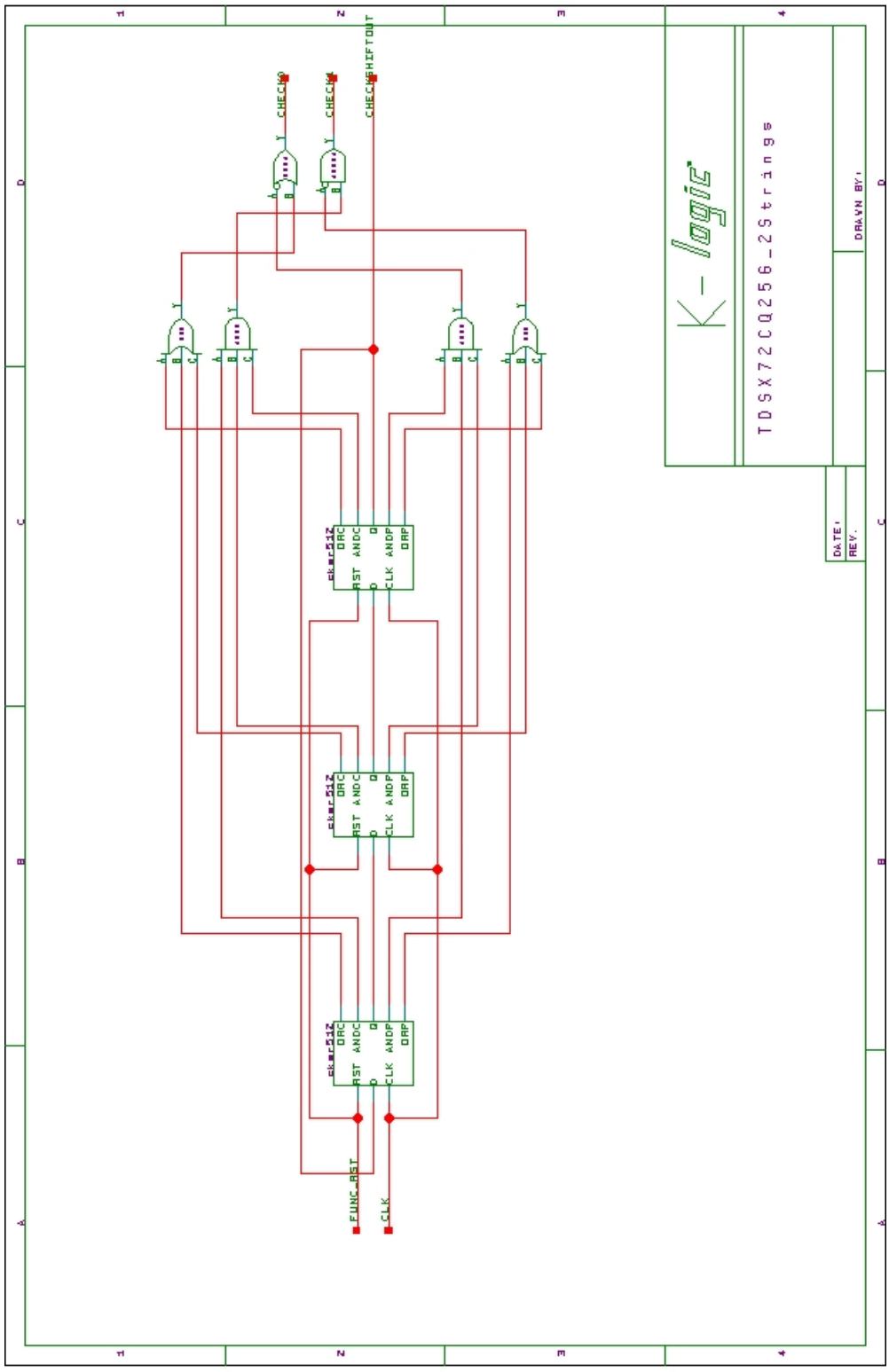
INX2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CHECK1
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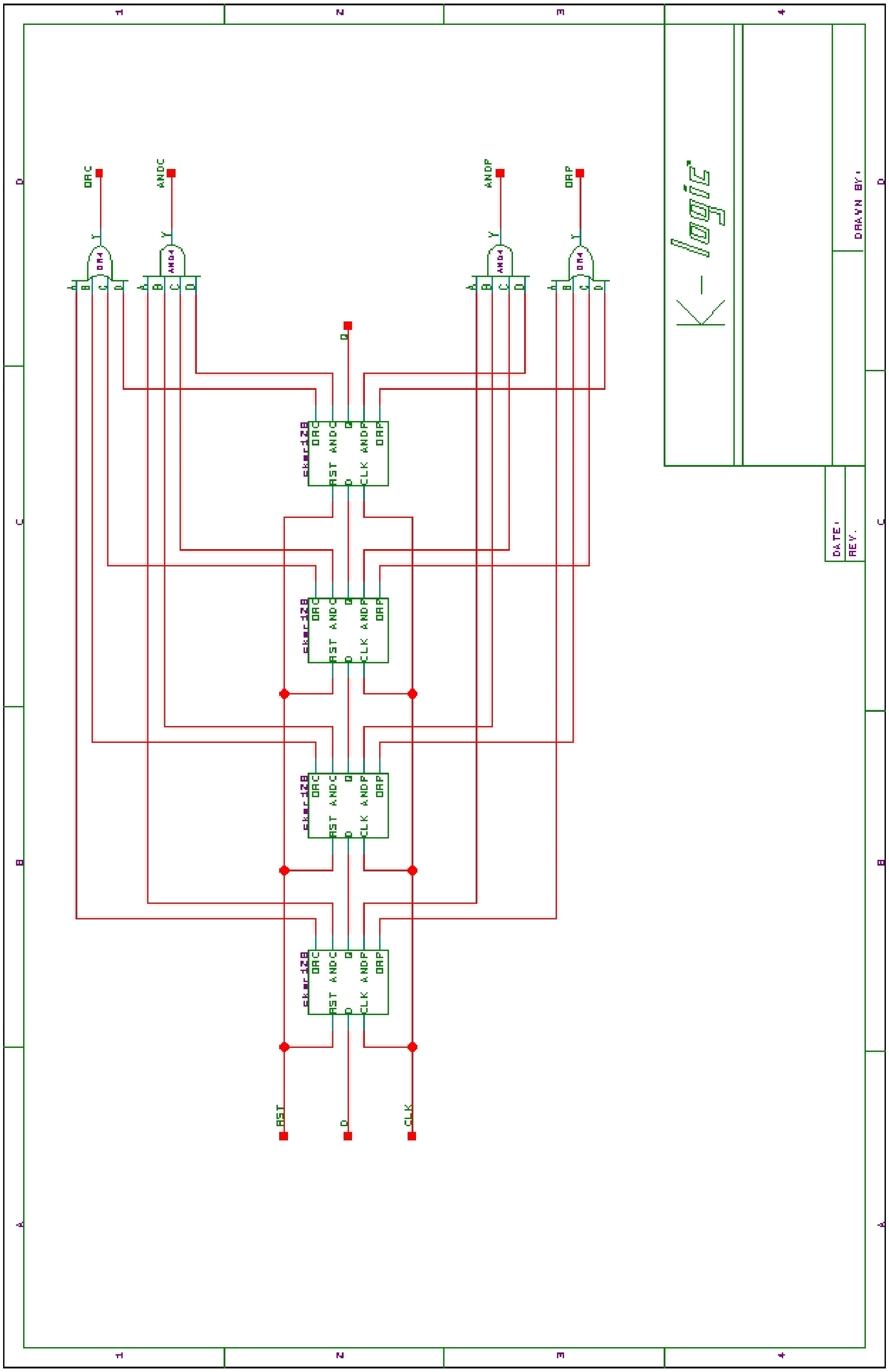
CLK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ANDP
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D
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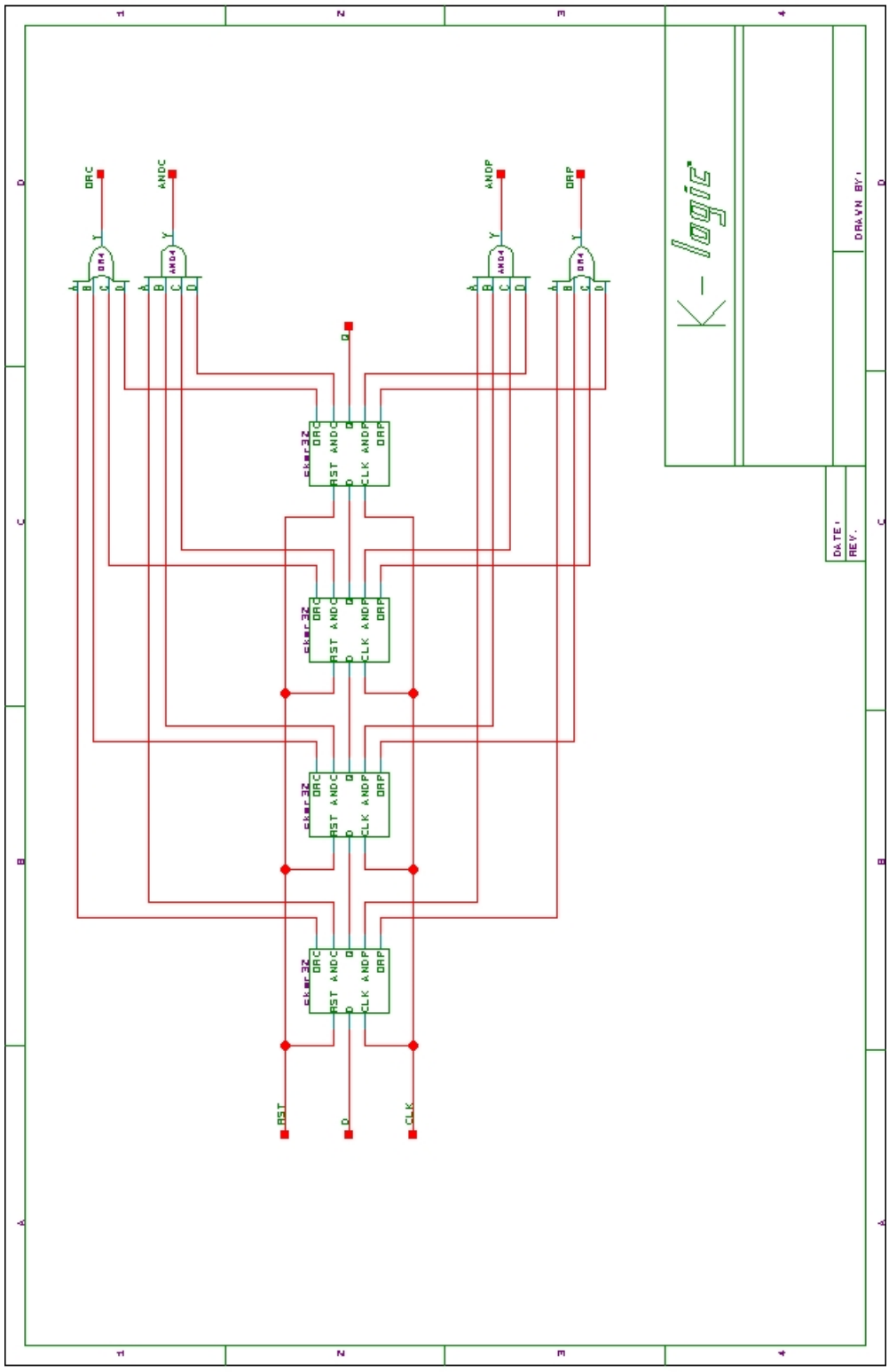
REV.
DRAWN BY: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ANDP
DRP
AND4
OR4
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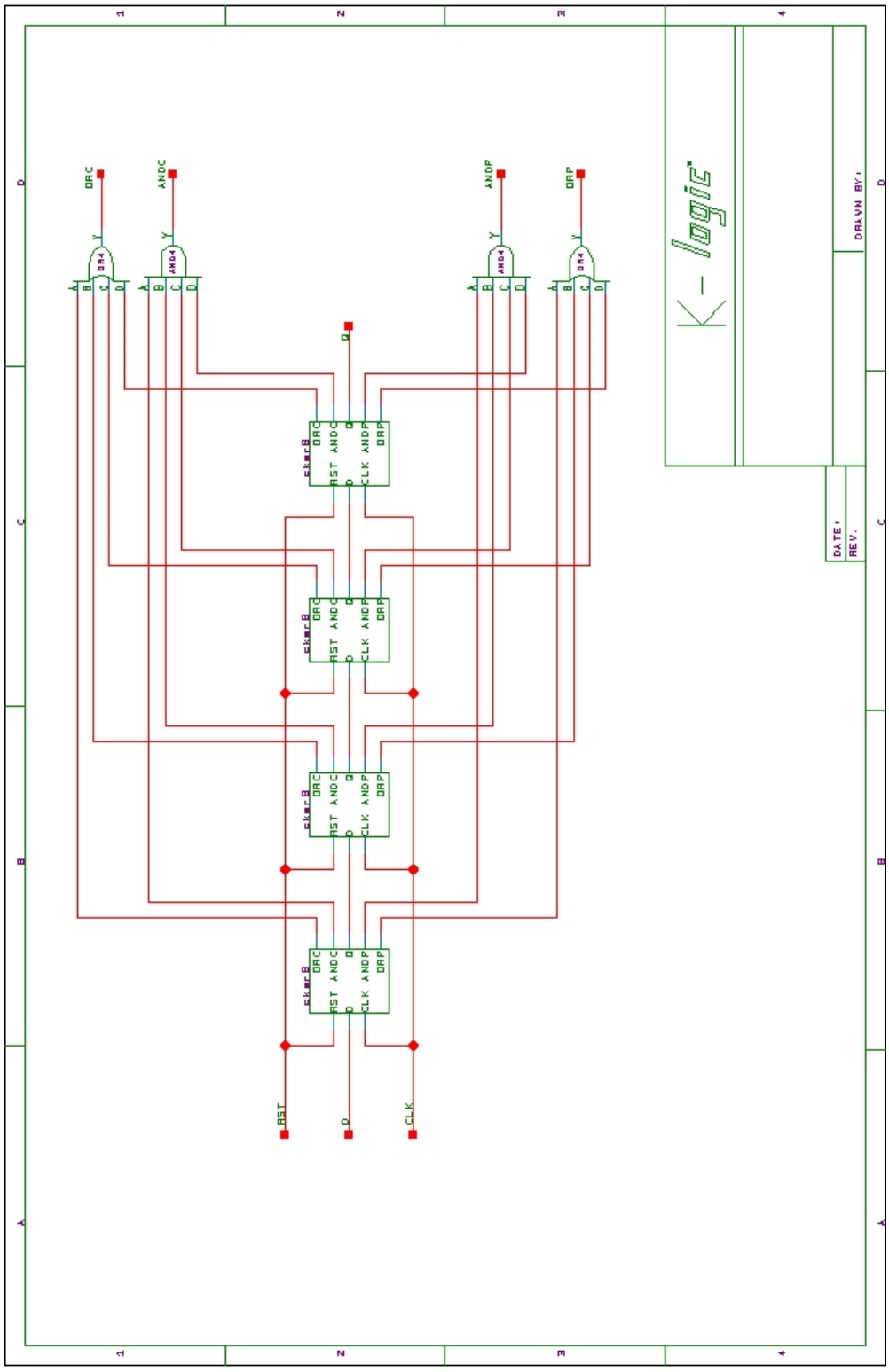
DATE:
REV.
RST
D
CLK


K- logic
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DATE:
REV.
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DRP
AND4
DR4
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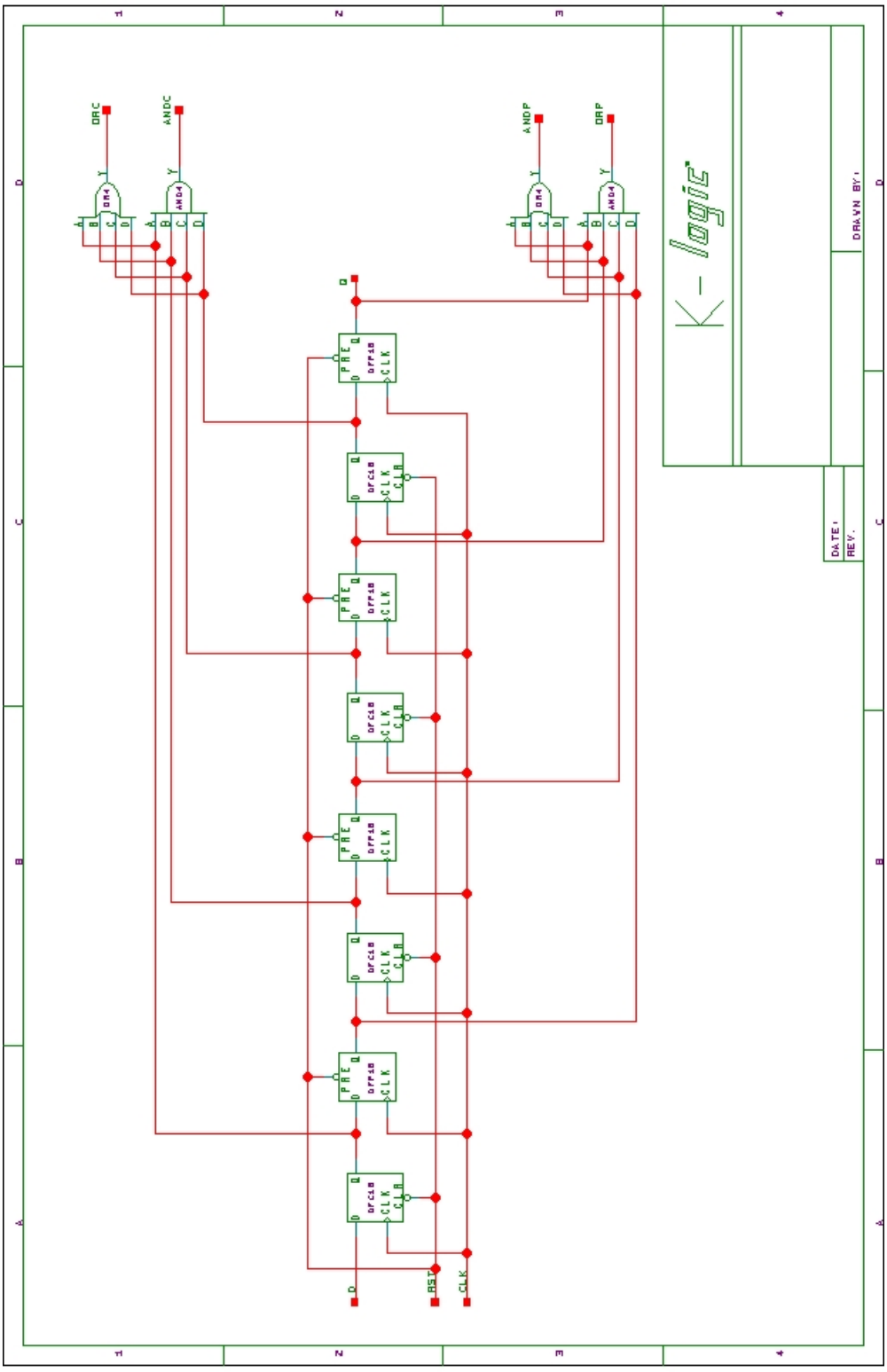
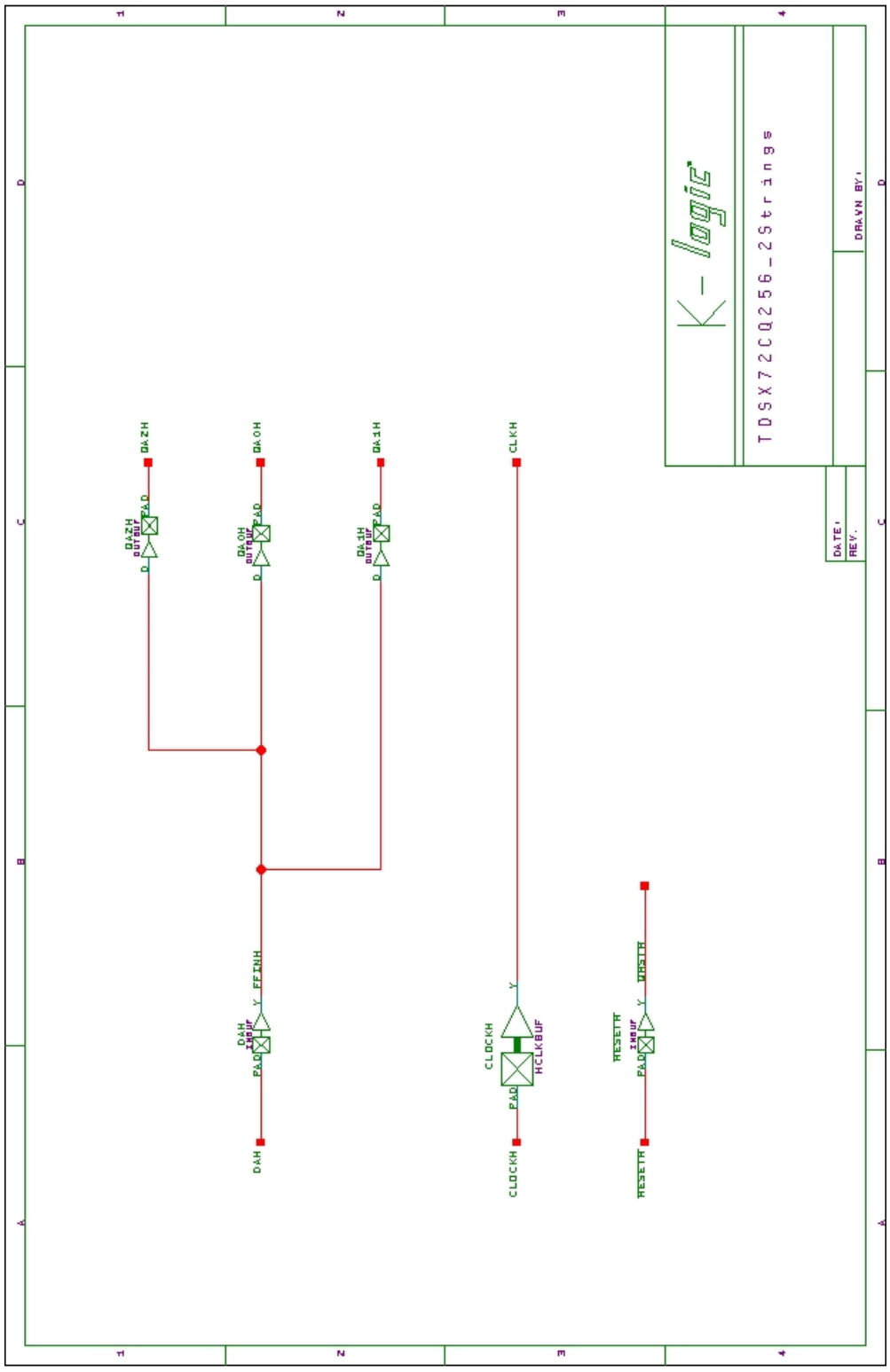
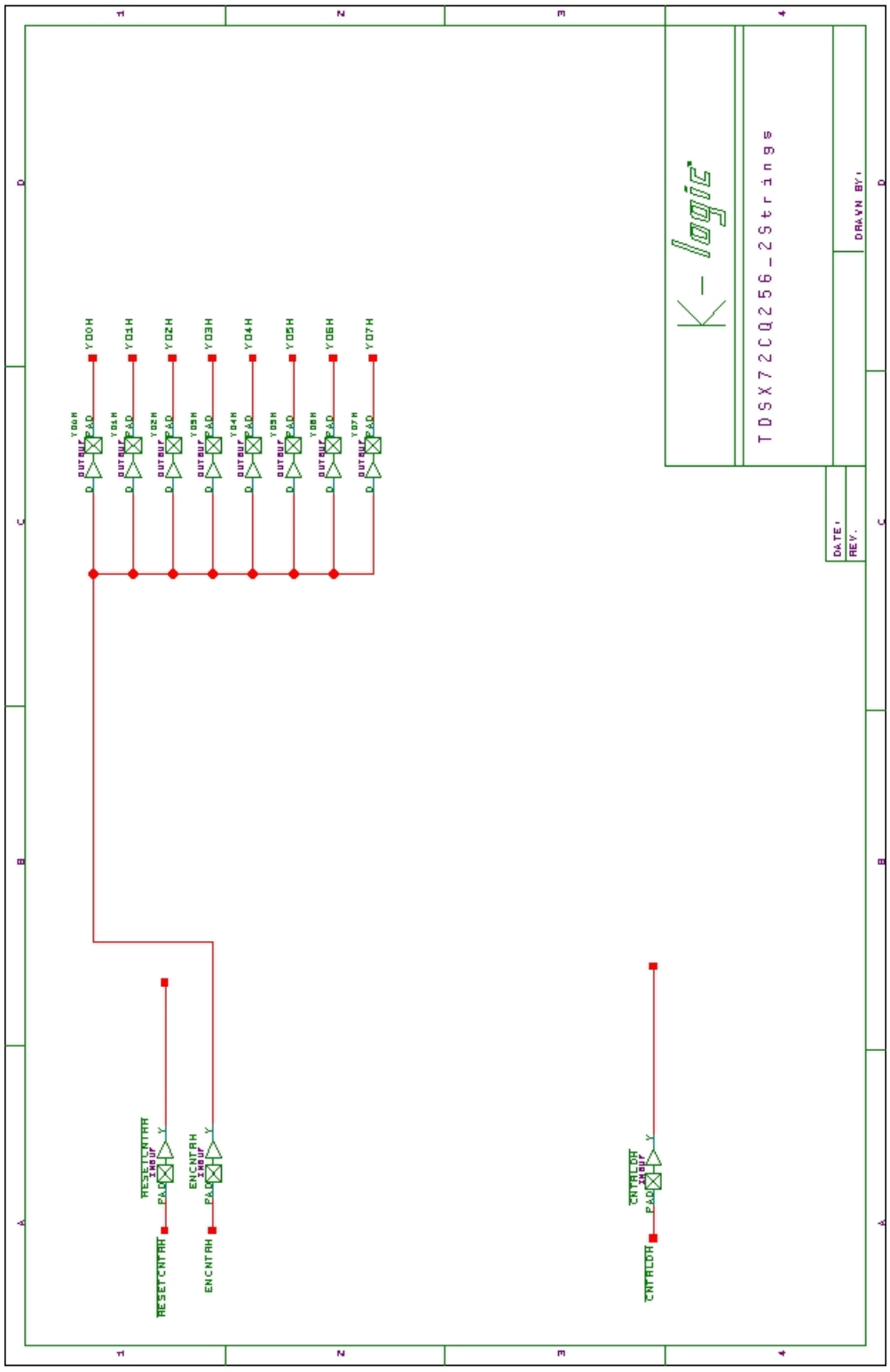
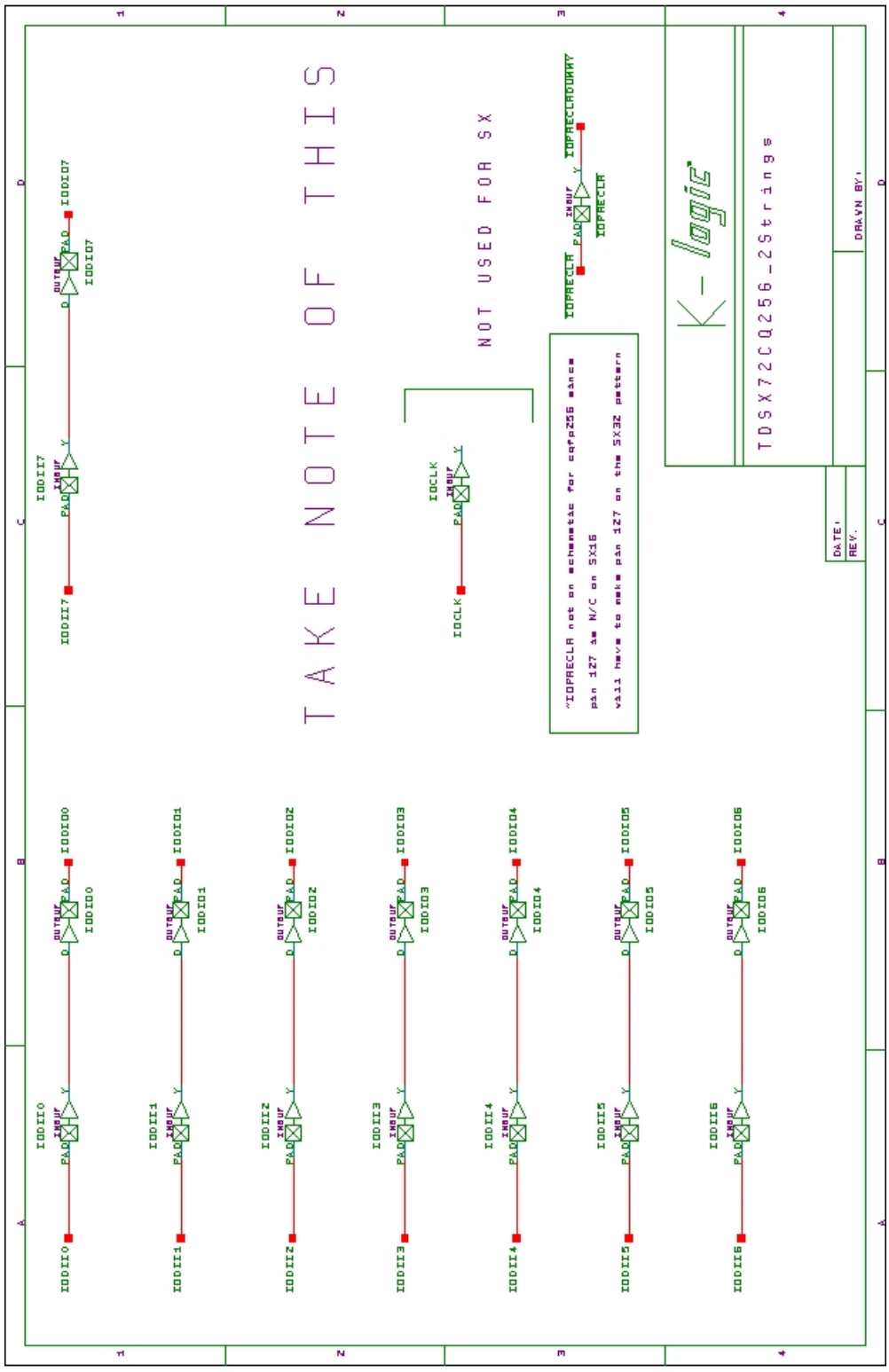
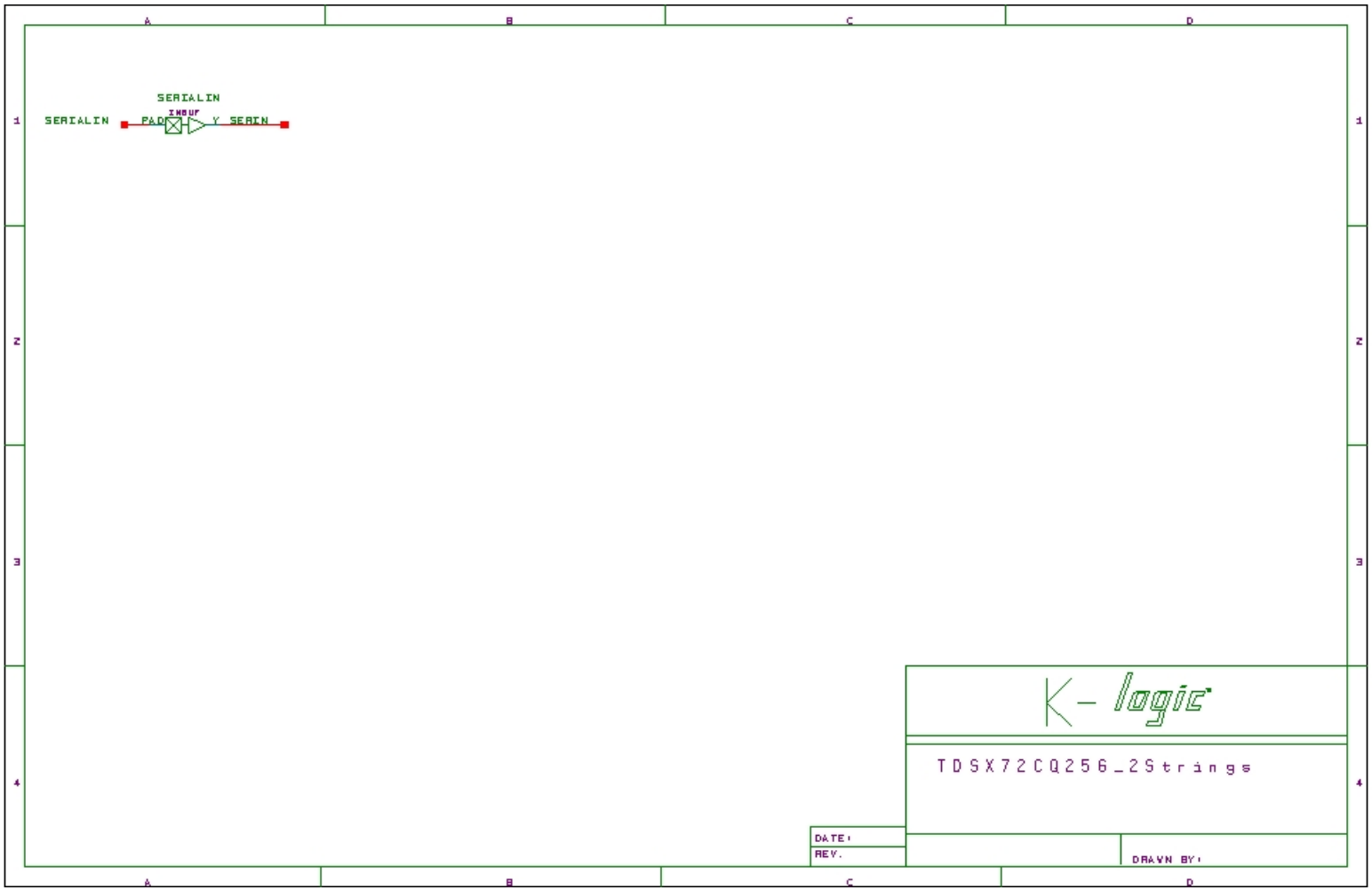
RST
CLK
D
Q

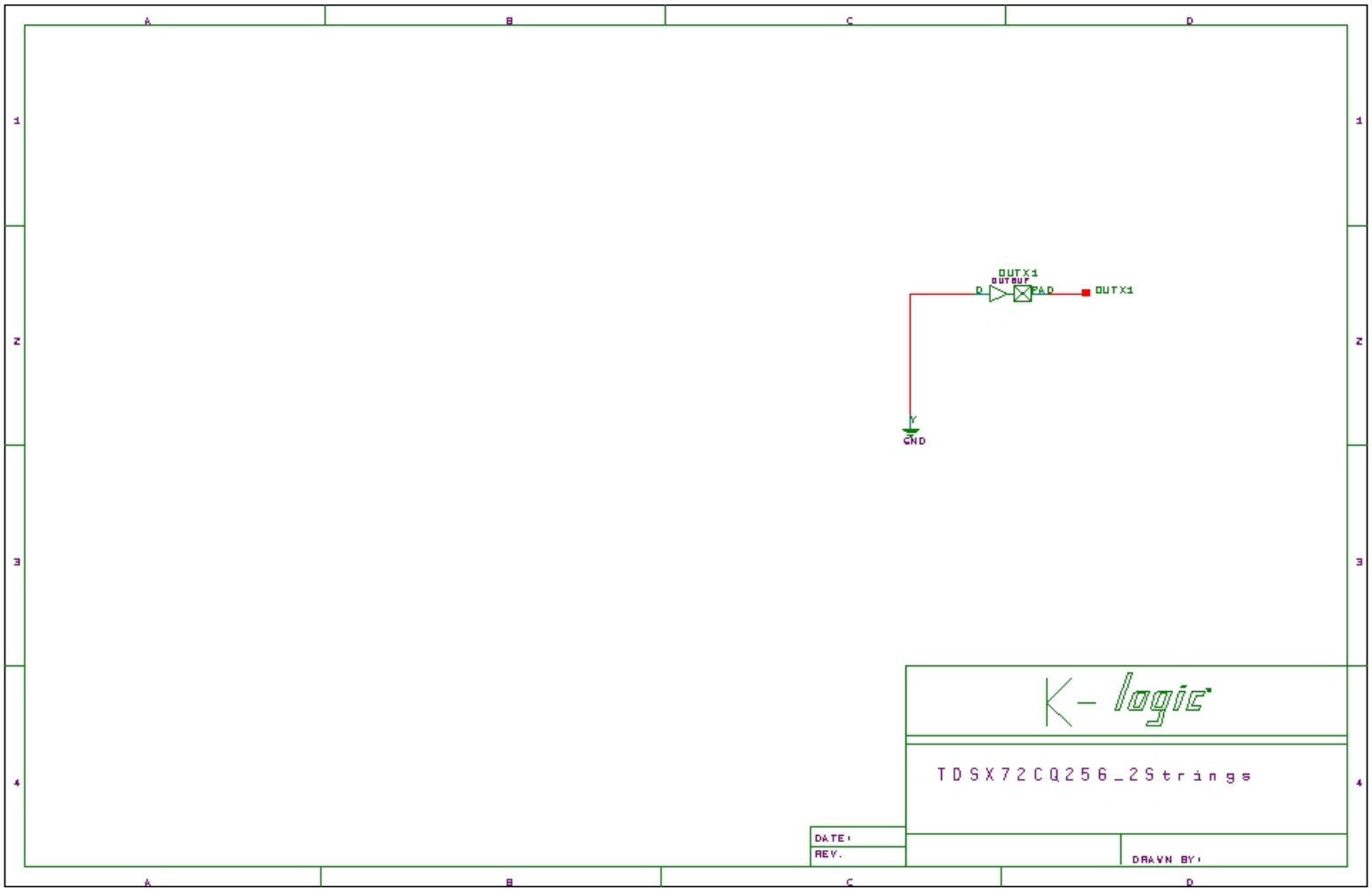

K- logic
DRAWN BY:
DATE:
REV.
DRC
ANDC
ANDF
DRF
CLK
RST


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
RESETH
DA2H OUTBUF PAD
DA0H OUTBUF PAD
DA1H OUTBUF PAD
DAH INBUF PAD Y FFXNH
CLOCKH HCLKBUF Y PAD
RESETH INBUF PAD Y WRSTH
DAH
CLOCKH
RESETH


K- logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YD0H
YD1H
YD2H
YD3H
YD4H
YD5H
YD6H
YD7H
RESETCNTAH
ENCNTAH
CNTALOH


TAKE NOTE OF THIS
NOT USED FOR SX
K-logic
TDSX72CQ256-2Strings
DRAWN BY:
DATE:
REV.
IODII7
IODII0
IODII1
IODII2
IODII3
IODII4
IODII5
IODII6
IODCLK
IODPRECLR
IODPRECLRDUMMY
IODIO7
IODIO0
IODIO1
IODIO2
IODIO3
IODIO4
IODIO5
IODIO6


SERIALIN
SERIALIN
IBUF
PAD
O
SERIN
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY:


A
B
C
D
1
2
3
4
OUTX1
OUTBUF
D
PAD
OUTX1
Y
GND
K- logic
TDSX72CQ256_2Strings
DATE:
REV.
DRAWN BY: