TOTAL IONIZING DOSE TEST REPORT

No. 04T-RT54SX32S-BP0083301
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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 100 krad(Si)
2. I_{CC}	Passed 77 krad(Si) for 25 mA spec, I_{CC} averaging 66.4 mA after 100 krad(Si) and room temp annealing
3. Input Threshold (V_{TIL}/V_{IH})	Passed 100 krad(Si)
4. Output Drives (V_{OL}/V_{OH})	Passed 100 krad(Si)
5. Propagation Delays	Passed 80 krad(Si) for 10% degradation criterion, degradation less than 15% after 100 krad(Si)
6. Transition Time	Passed 100 krad(Si)

II. TOTAL IONIZING DOSE (TID) TESTING

A. Device Under Test (DUT) and Irradiation

Table 1 lists the DUT information and irradiation conditions.

Table 1. DUT information and irradiation conditions

Part Number	RT54SX32S
Package	CQFP256
Foundry	Matsushita Electronics Corporation
Technology	0.25 μm CMOS
DUT Design	TDSX32CQFP256_2Strings
Die Lot Number	BP0083301
Quantity Tested	4
Serial Number	26841, 26924, 26931, 26937
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	1 krad(Si)/min (±5%)
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{CCI}/V_{CCA})	Static at 5.0 V/2.5 V

B. Test Method

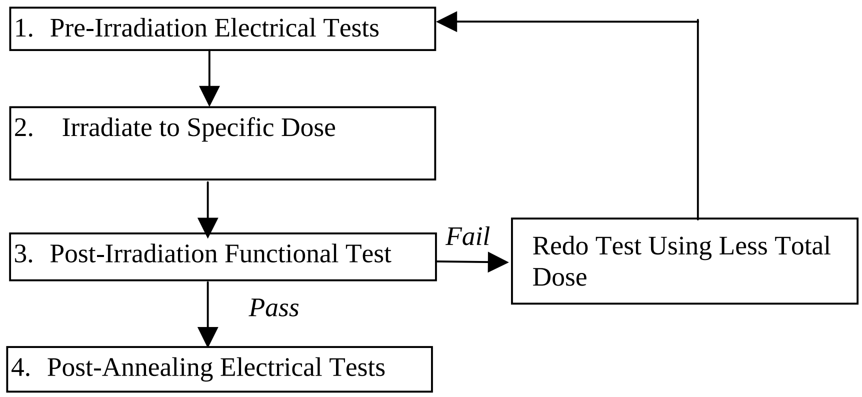


Fig 1 Parametric test flow chart

The parametric tests follow the military standard test method 1019.5. Fig 1 shows the testing flow. The time dependent effect (TDE) of this product was previously evaluated by comparing the results of a high dose rate (1 krad(Si)/min) against the results of a low dose rate (1 krad(Si)/hr). No adverse TDE was observed. Therefore the accelerated aging test (rebound test) is omitted. Room temperature annealing were performed for approximately two month after 100 krad(Si) of irradiation. DUTs were static biased during annealing.

C. Electrical Parameter Measurements

A high utilization design (TDSX32CQ256_2Strings) to address total dose effects in typical space applications is used. The circuit schematics are shown in appendix A.

Table 2 lists measured electrical parameters. The functionality is tested pre-irradiation, post-irradiation, and post-annealing on the output pin (O_AND3 or O_AND4) of the two combinational buffer-strings and on the output pins (O_OR4 and O_NAND4) of the shift register. I_{CC} is measured on the power supply of the logic-array (I_{CCA}) and I/O (I_{CCI}) respectively.

The input logic thresholds (V_{TIL}/V_{IH}) and output drives (V_{OL}/V_{OH}) are measured pre-irradiation and post-annealing on a combinational net, the input pin DA to the output pin QA0. The propagation delays are measured pre-irradiation and post-annealing on the O_AND4 output which belongs to one of the buffer strings. The delay is defined as the time delay from the time of triggering edge at the CLOCK input to the time of switching state at the O_AND4. The transient times (rise and fall times) are measured post-annealing on the O_AND4.

Each unused input is grounded with an 1 M ohm resistor during irradiation and an 1.2K ohm resistor during annealing.

Table 2. Logic design for parametric tests

Parameter/Characteristics	Logic Design
1. Functionality	All key architectural functions (pins O_AND3, O_AND4, O_OR3, O_OR4, and O_NAND4)
2. I_{CC} (I_{CCA}/I_{CCI})	DUT power supply
3. Input Threshold (V_{TIL}/V_{IH})	Input buffer (pin DA to QA0)
4. Output Drive (V_{OL}/V_{OH})	Output buffer (pin DA to QA0)
5. Propagation Delay	String of buffers (pin LOADIN to O_AND4)
6. Transition Time	D flip-flop output (O_AND4)

III. TEST RESULTS

A. *Functionality*

Every DUT passed the gross functional test at pre-irradiation, post-irradiation, and post-annealing.

B. I_{CC}

Figs 2-5 show the in-flux I_{CC} plots. Table 3 lists the post-annealing I_{CC}.

Table 3. Post-annealing I_{CC}

DUT	I_{CCA} (mA)	I_{CCI} (mA)
26841	50	12.6
26924	43.2	7.3
26931	50.9	14.5
26937	68.3	18.9

An empirical equation is used to extract the total dose tolerance after a 10 years annealing. The critical total dose ($\gamma_{critical}$) for a 10-year mission to induce I_{CC} to 25 mA is obtained from the equation:

$$I_{CCA}(\gamma_{critical}) \times 0.32 + I_{CCI}(\gamma_{critical}) \times 0.29 = 25mA$$

Where $I_{CCA}(\gamma)$ and $I_{CCI}(\gamma)$ are in-flux power-supply currents. Using the worst case (Fig 5, DUT 26937) in this test, the tolerance ($\gamma_{critical}$) is obtained as approximately 77 krad(Si). This equation produces a very conservative tolerance. Experiments show that high-dose-rate irradiation and annealing makes the DUT I_{CC} higher than that of a DUT when it is irradiated at a uniformly low dose rate.

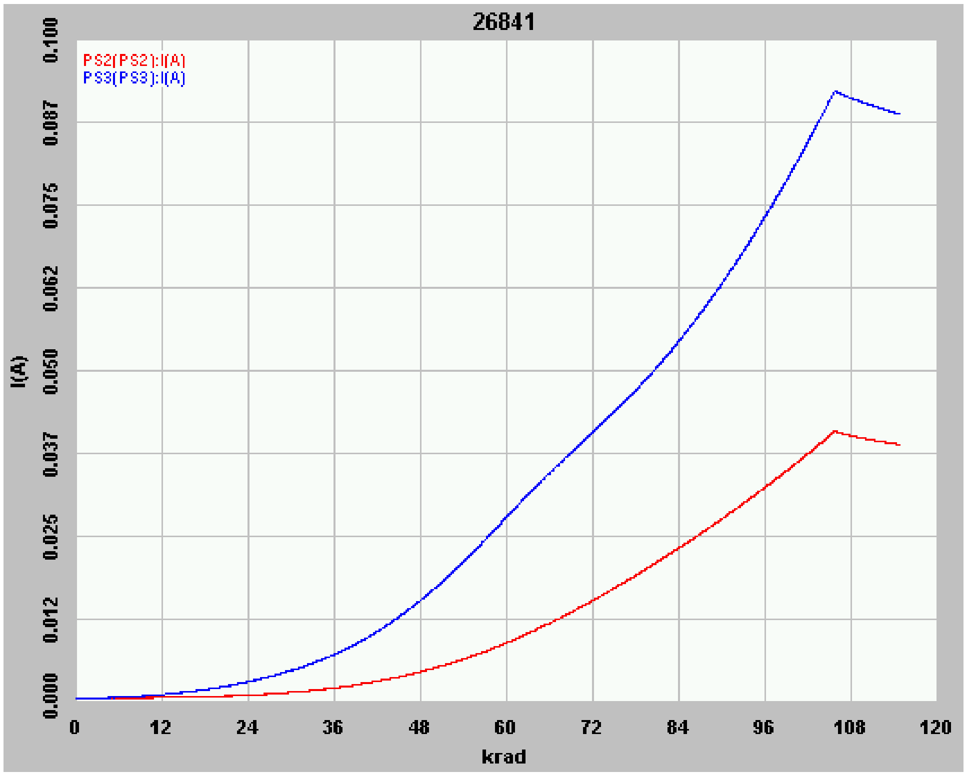


Fig 2 In-flux I_{CC} of DUT 26841, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

Fig 3 In-flux I_{CC} of DUT 26924, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

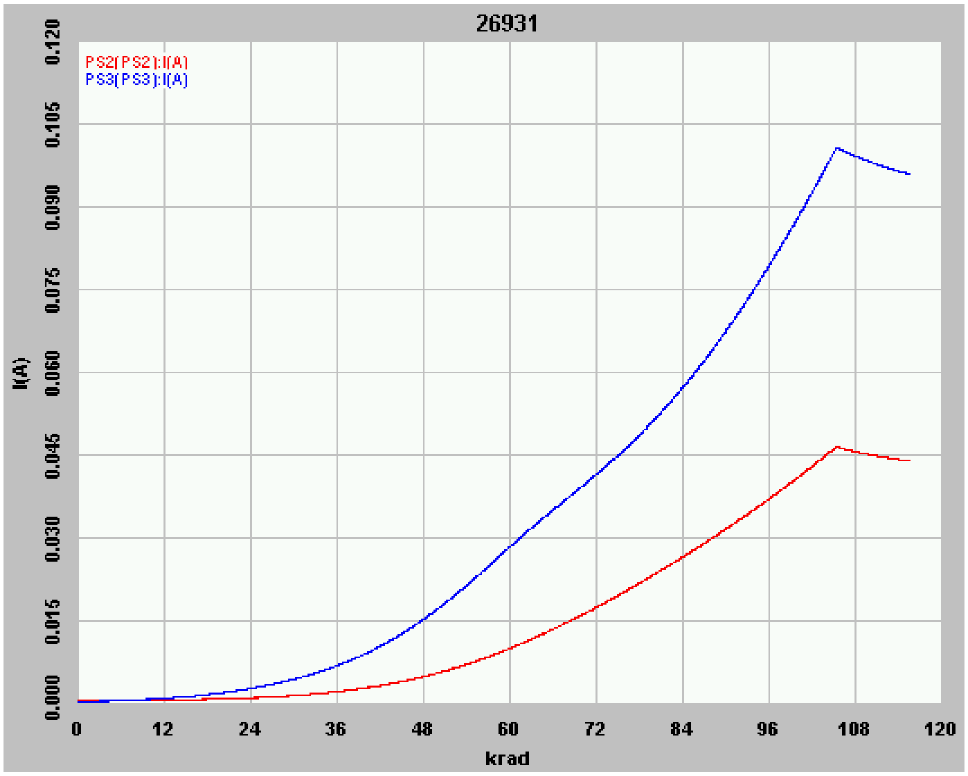


Fig 4 In-flux I_{CC} of DUT 26931, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

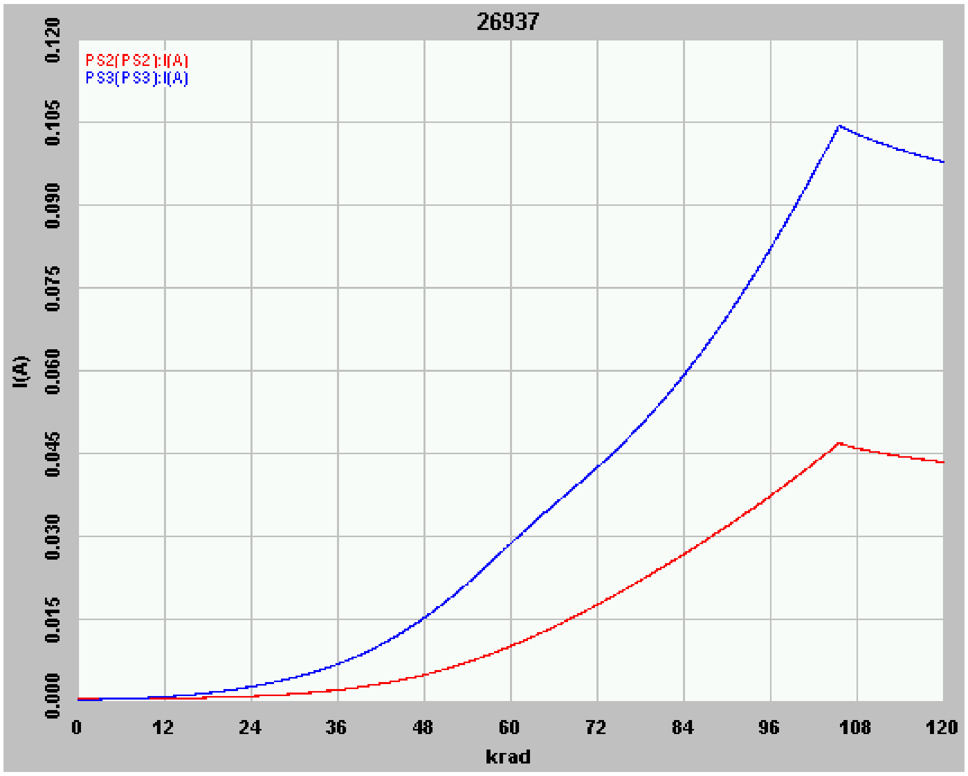


Fig 5 In-flux I_{CC} of DUT 26937, PS2 supplies I_{CCI} and PS3 supplies I_{CCA}.

C. Input Logic Threshold (V_{IL}/V_{IH})

Table 4 lists the pre-irradiation and post-annealing input logic threshold. All data are within the spec limits.

Table 4 Pre-irradiation and post-annealing input logic threshold in volts

DUT	Pre-Irradiation		Post-Annealing	
	V_{IL}	V_{IH}	V_{IL}	V_{IH}
26841	1.34	1.42	1.30	1.45
26924	1.35	1.42	1.33	1.43
26931	1.37	1.43	1.32	1.44
26937	1.22	1.49	1.32	1.43

D. Output Characteristics (V_{OL}/V_{OH})

The pre-irradiation and post-annealing V_{OL}/V_{OH} are listed in table 5 and 6. The post-annealing data are within the spec limits, and 100 krad(Si) radiation has little effect on these parameters.

Table 5 Pre-irradiation and post-annealing V_{OL} (in volts) at various sinking current

DUT	1 mA		12 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
26841	0.009	0.009	0.104	0.105	0.173	0.175	0.436	0.441	0.899	0.908
26924	0.009	0.009	0.104	0.105	0.173	0.174	0.437	0.44	0.901	0.905
26931	0.009	0.009	0.105	0.105	0.174	0.175	0.440	0.442	0.907	0.912
26937	0.009	0.009	0.105	0.106	0.175	0.176	0.441	0.445	0.907	0.916

Table 6 Pre-irradiation and post-annealing V_{OH} (in volts) at various sourcing current

DUT	1 mA		8 mA		20 mA		50 mA		100 mA	
	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an	Pre-rad	Pos-an
26841	4.99	4.98	4.87	4.86	4.66	4.65	4.11	4.1	3.02	3
26924	4.99	4.98	4.87	4.87	4.66	4.66	4.12	4.12	3.04	3.04
26931	4.99	4.98	4.87	4.86	4.66	4.65	4.11	4.1	3	2.99
26937	4.99	4.98	4.87	4.86	4.66	4.65	4.11	4.1	3	2.98

E. Propagation Delays

Tables 7 and 8 list the pre-irradiation and post-annealing propagation delays, and radiation-induced degradations. The worst-case degradation is 14.95%. To extract the tolerance of 10% degradation, a piece-wise linear fitting curve of propagation delay against total dose is used. This approach is based on experimental data measured on SXS products. The piece-wise linear fitting curve has two regions, region 1 from 0 krad(Si) to 40 krad(Si) has 0% degradation, and region 2 from 40 krad(Si) to 100 krad(Si) has a slope defined in the equation,

$$Slope = \frac{TPD(Max\ Dose) - TPD(Initial)}{Maximum\ Dose - 40krad}$$

Where TPD is measured in percentage. In this case, TPD(Max Dose) is 14.95%, and TPD(Initial) is 0%. The maximum dose is 100 krad(Si). The total dose corresponding to 10% degradation on the linear curve in region 2 is the standard 10% degradation tolerance, which is obtained as 80 krad(Si).

Table 7 Low to high delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Annealing	Degradation
26841	507.13	569.7	12.34%
26924	511.89	582.32	13.76%
26931	519.38	597.03	14.95%
26937	525.63	599.7	14.09%

Table 8 High to low delays (in nanoseconds)

DUT	Pre-Irradiation	Post-Annealing	Degradation
26841	428.97	486.25	13.35%
26924	434.79	492.57	13.29%
26931	441.56	505.27	14.43%
26937	447.41	512.56	14.56%

F. Transition Time

The pre-irradiation and post-annealing transition edges are plotted in Figs 6-13. The radiation-induced transition time degradation in every case is not significant.

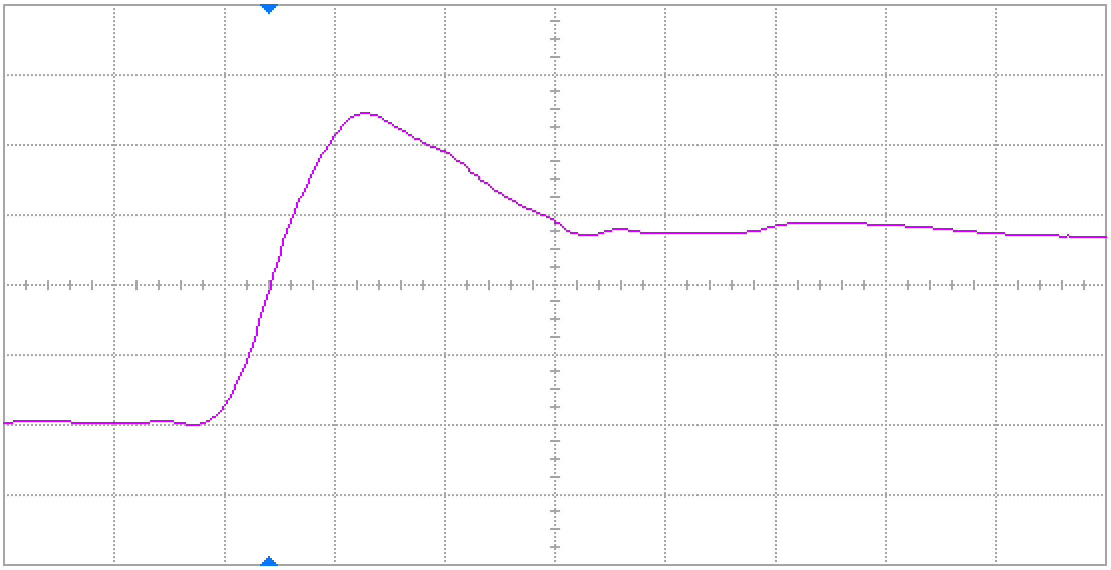


Fig 6(a) Pre-irradiation rising edge of DUT 26841, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

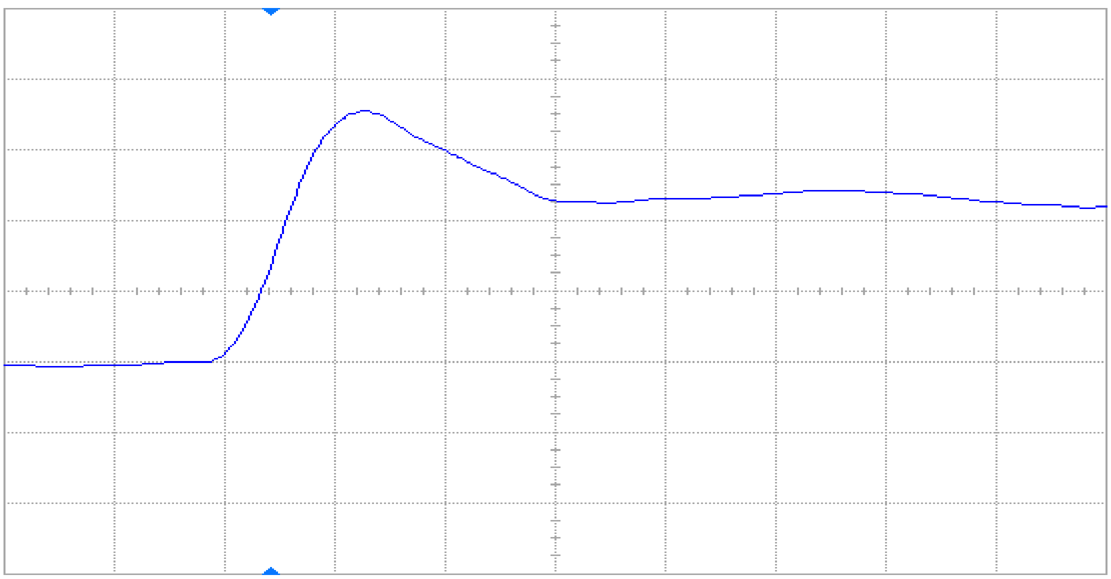


Fig 6(b) Post-annealing rising edge of DUT 26841, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

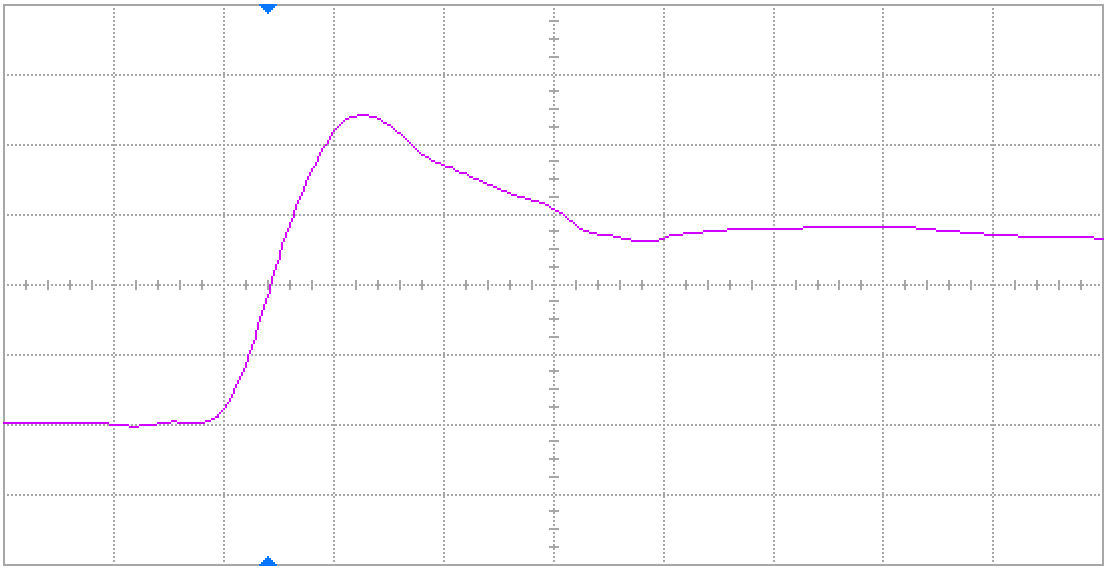


Fig 7(a) Pre-irradiation rising edge of DUT 26924, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

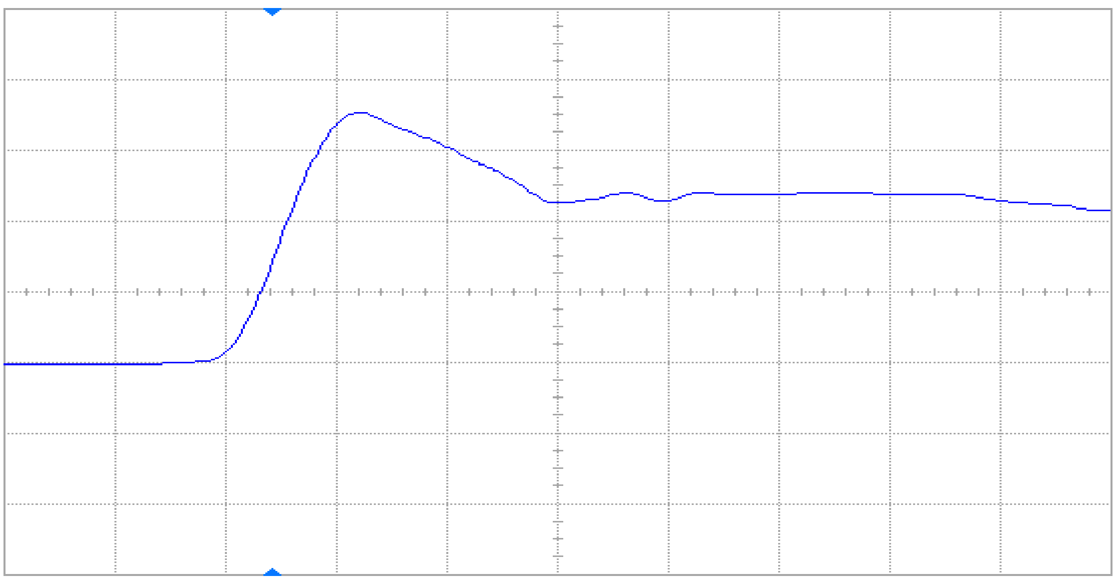


Fig 7(b) Post-annealing rising edge of DUT 26924, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

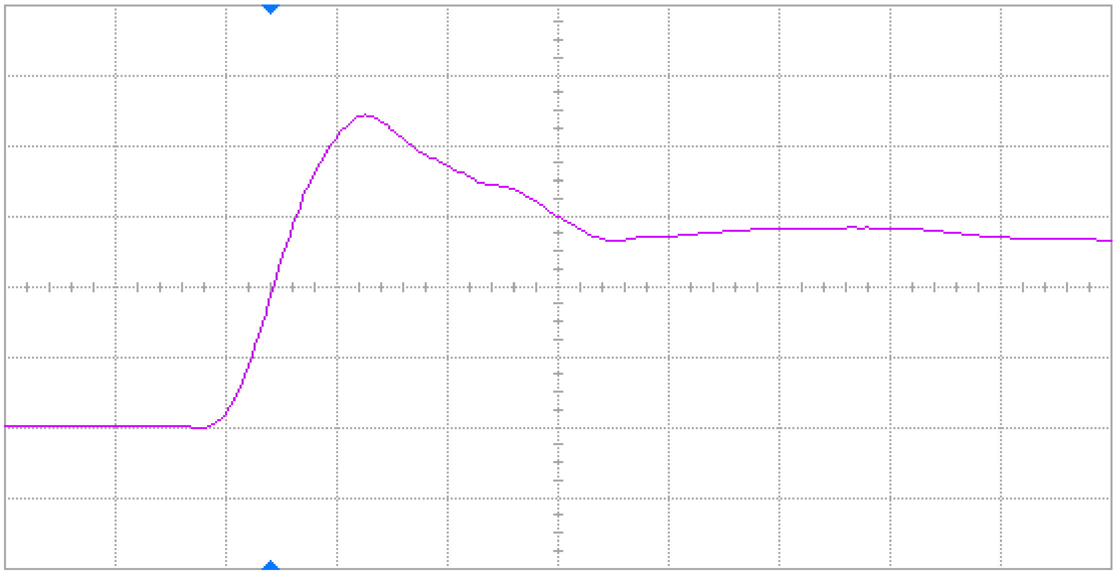


Fig 8(a) Pre-irradiation rising edge of DUT 26931, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

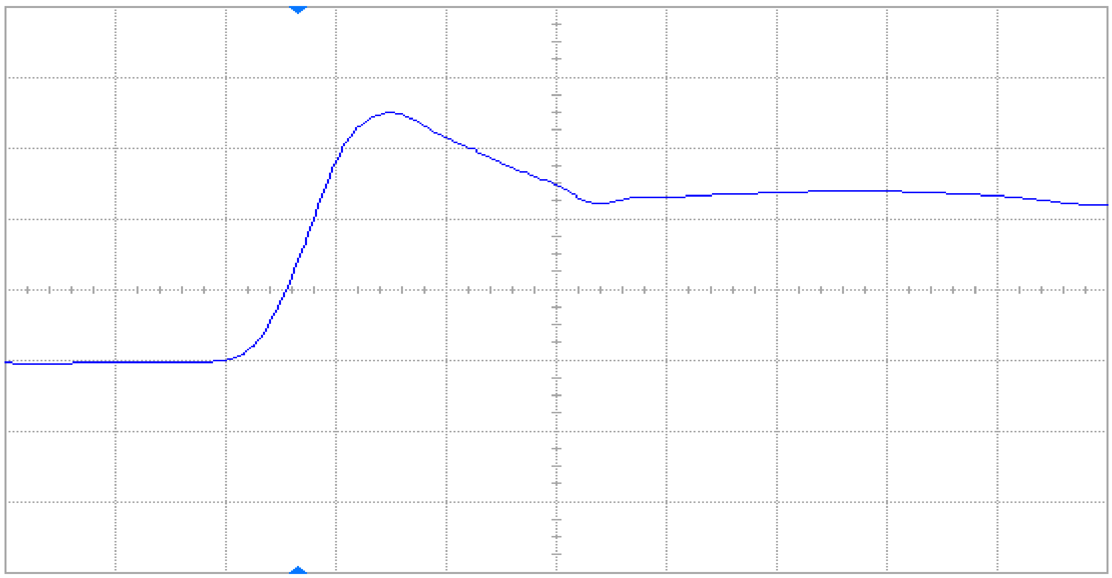


Fig 8(b) Post-annealing rising edge of DUT 26931, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

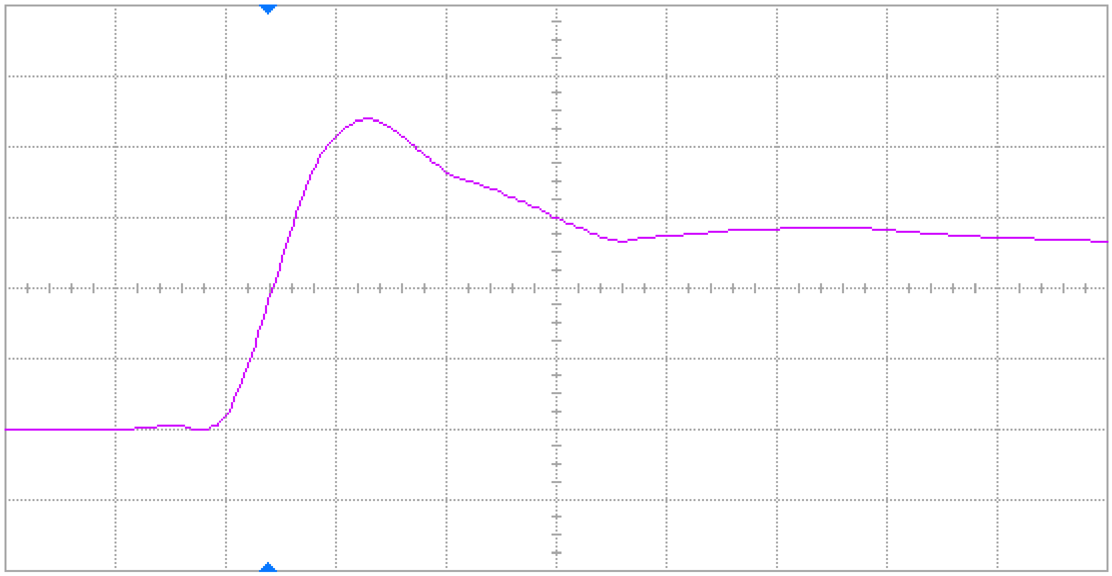


Fig 9(a) Pre-irradiation rising edge of DUT 26937, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

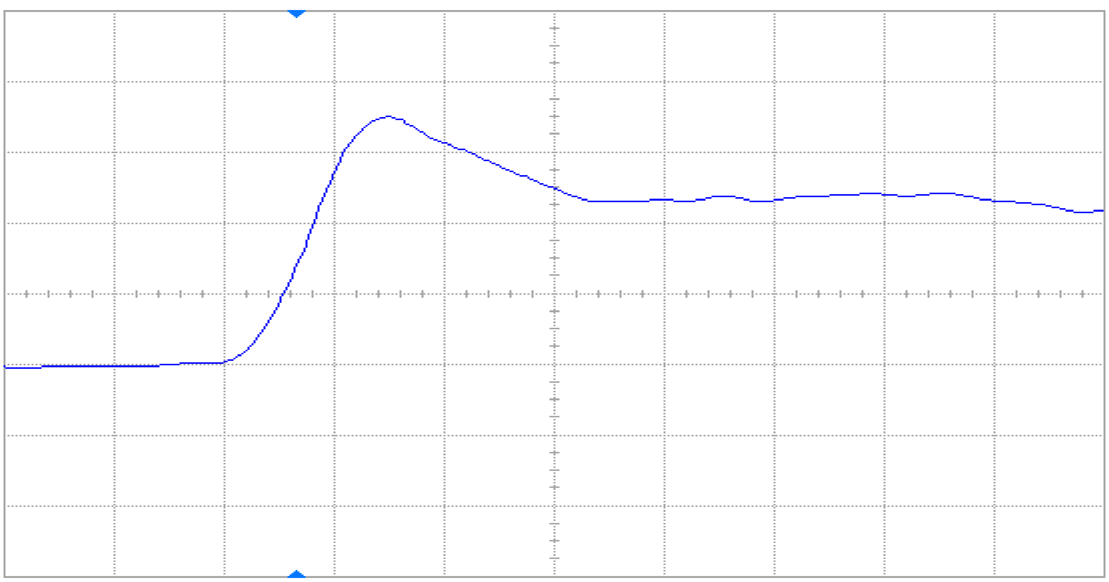


Fig 9(b) Post-annealing rising edge of DUT 26937, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

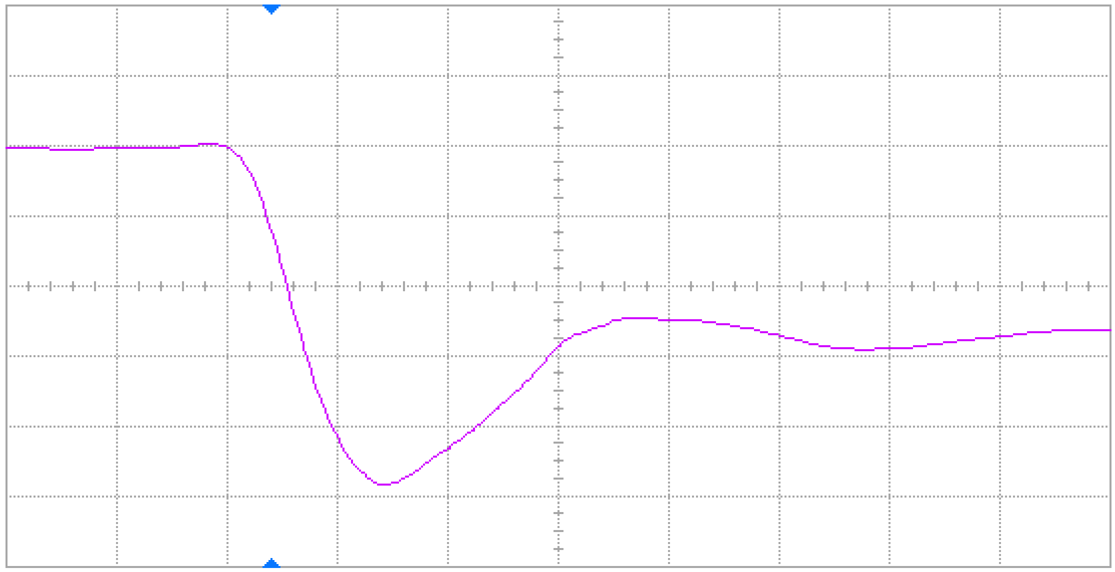


Fig 10(a) Pre-irradiation falling edge of DUT 26841, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

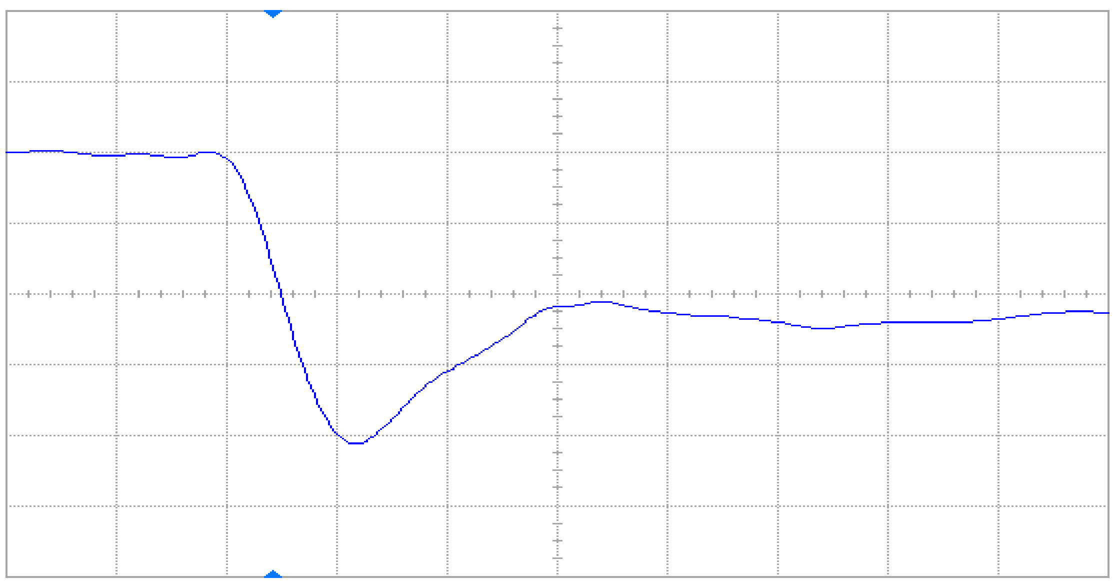


Fig 10(b) Post-annealing falling edge of DUT 26841, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

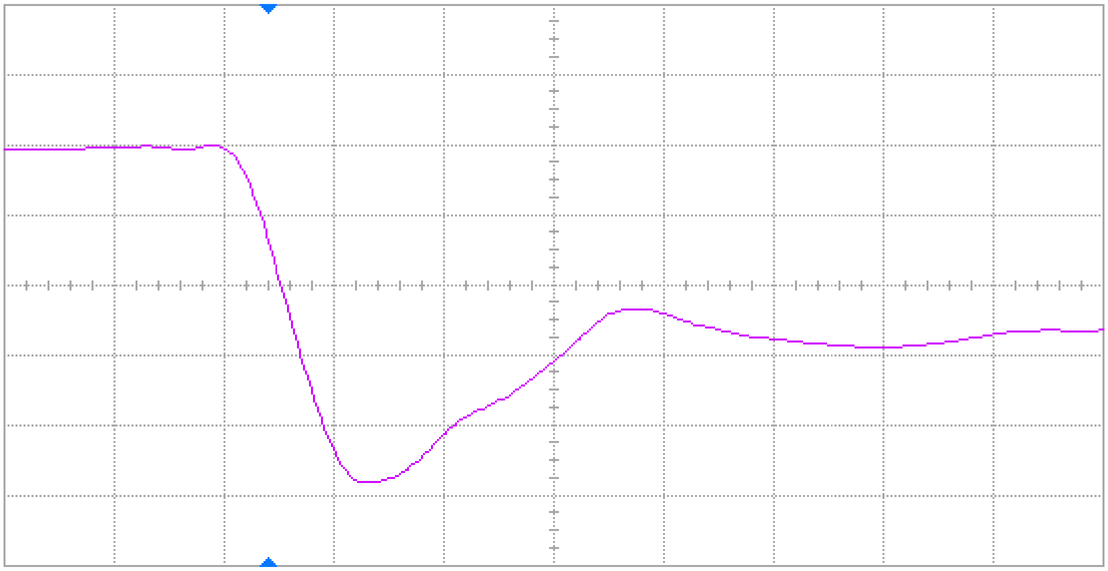


Fig 11(a) Pre-irradiation falling edge of DUT 26924, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

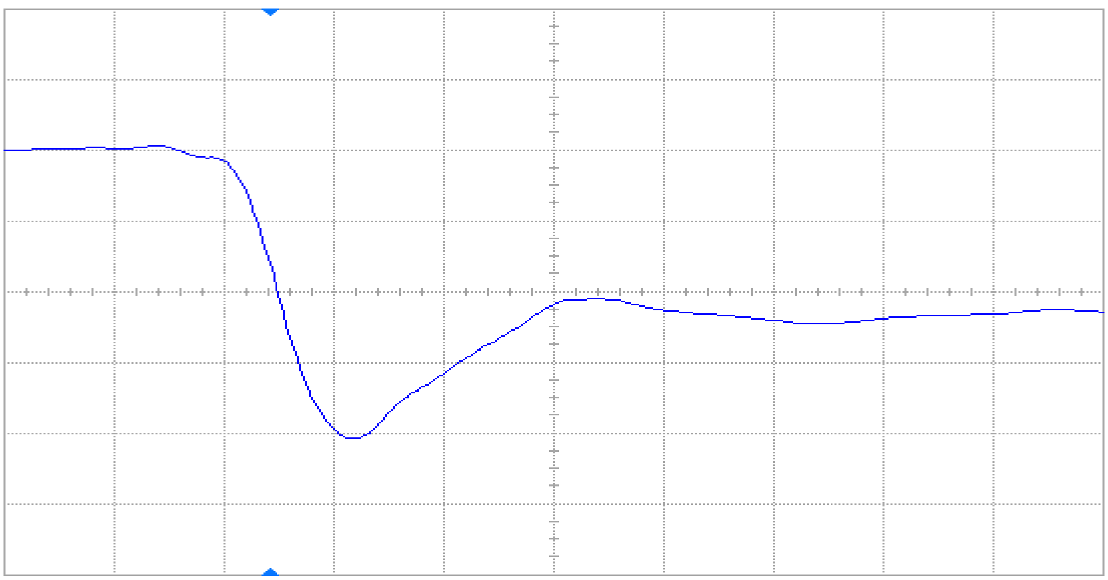


Fig 11(b) Post-annealing falling edge of DUT 26924, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

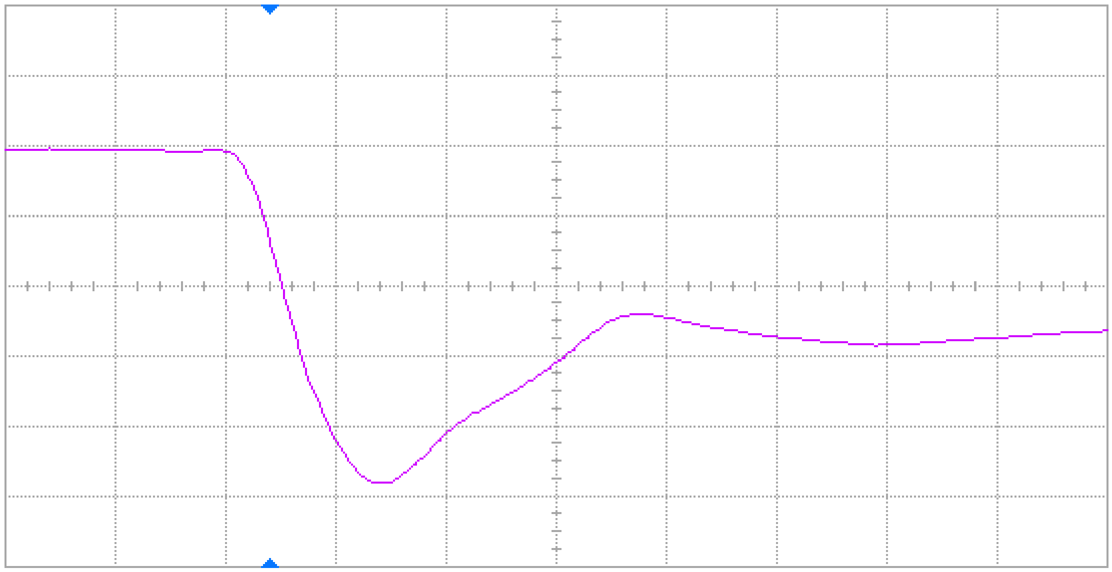


Fig 12(a) Pre-irradiation falling edge of DUT 26931, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

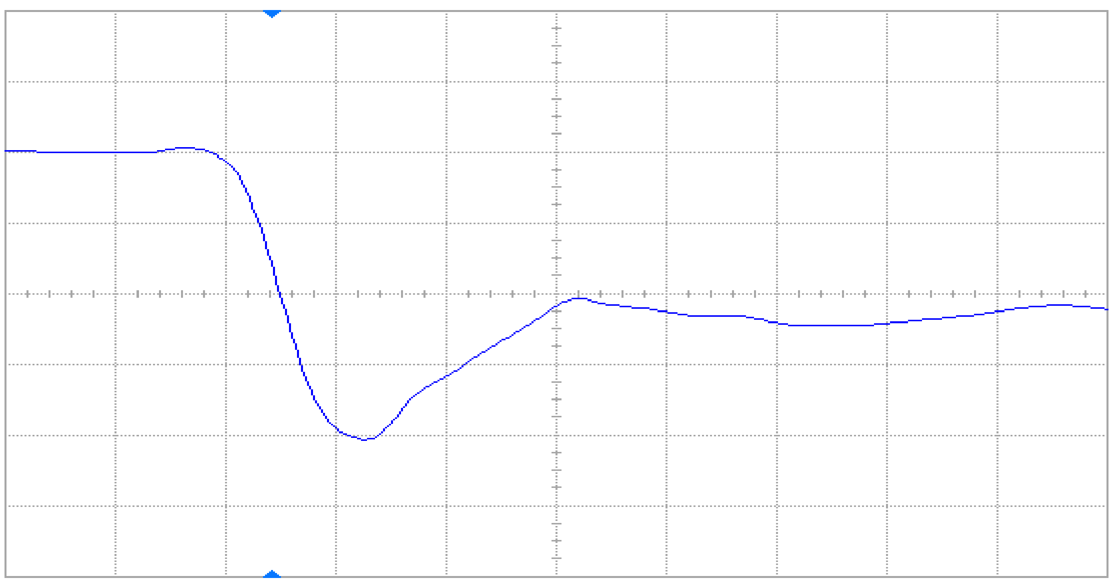


Fig 12(b) Post-annealing falling edge of DUT 26931, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

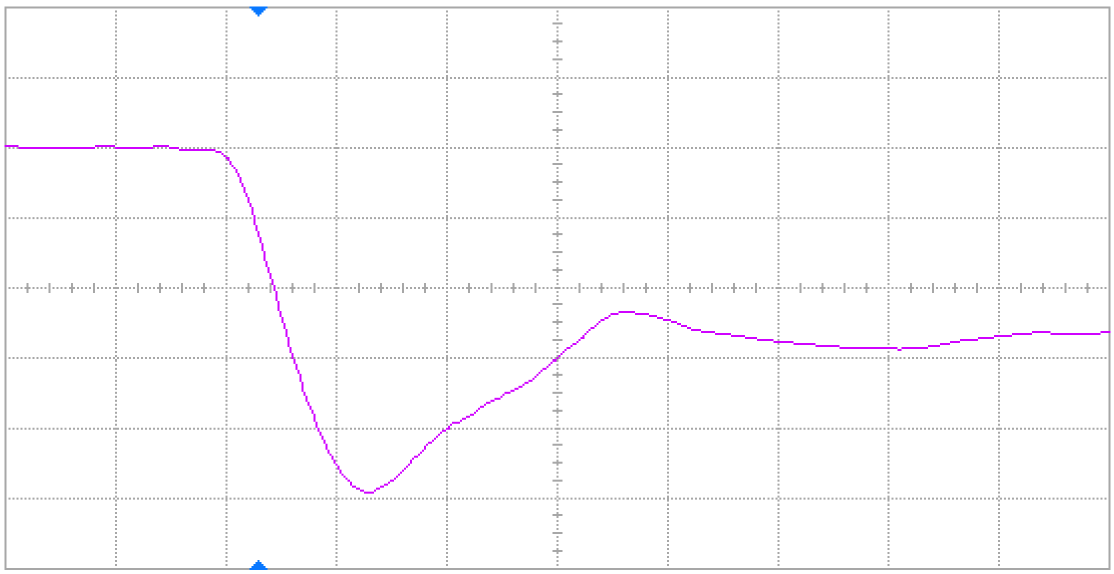


Fig 13(a) Pre-irradiation falling edge of DUT 26937, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

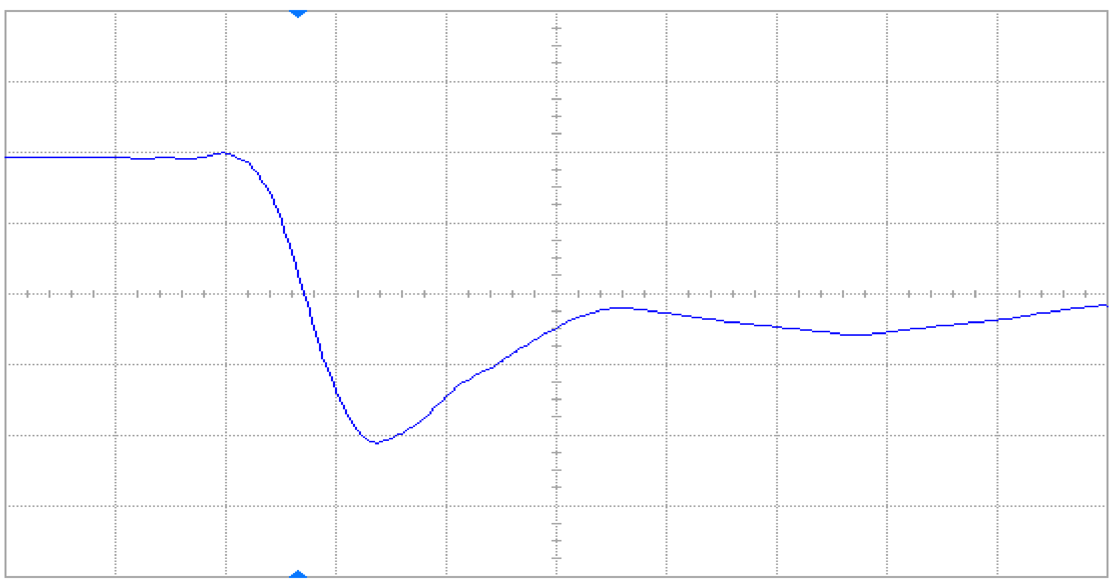
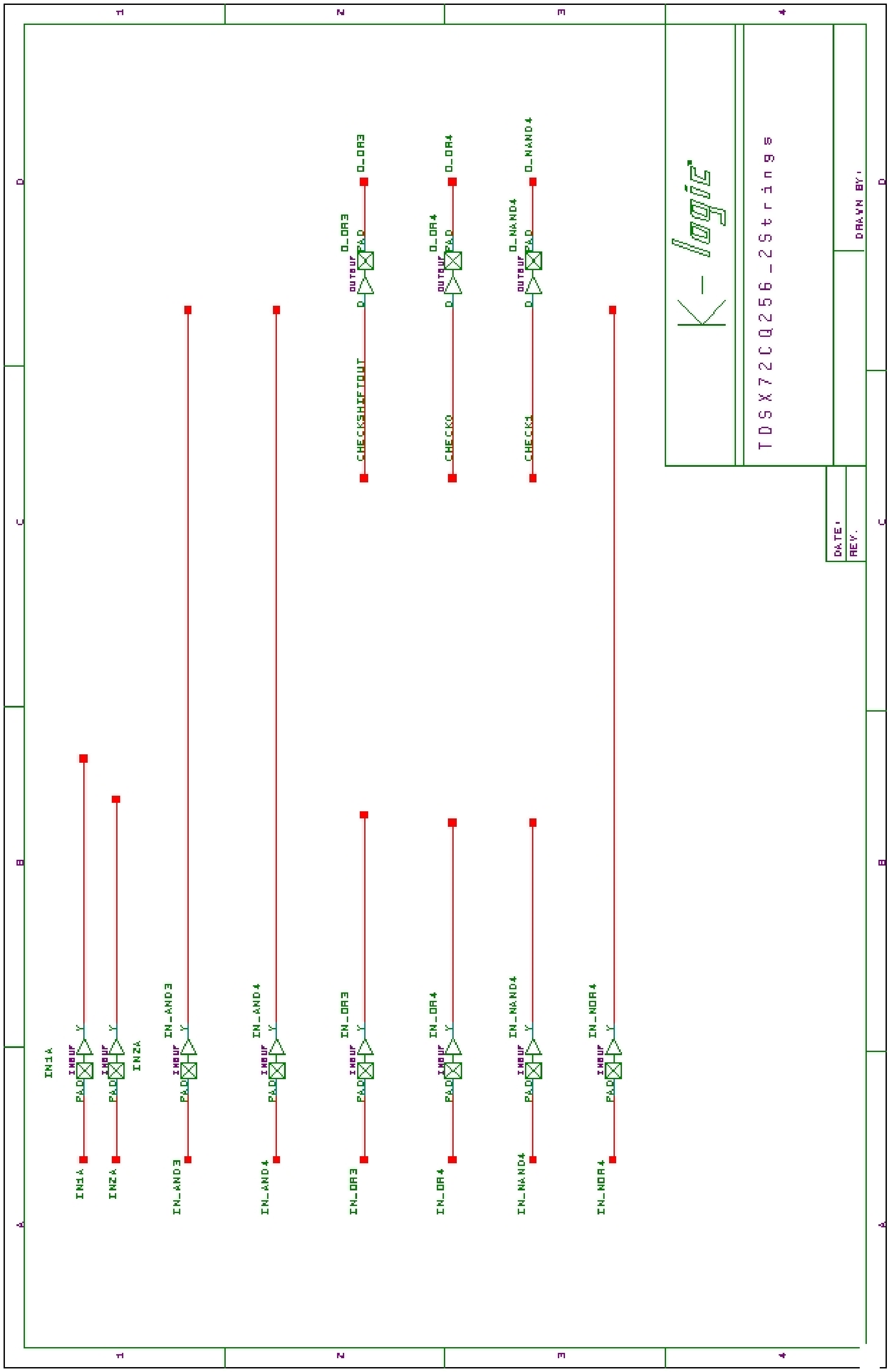
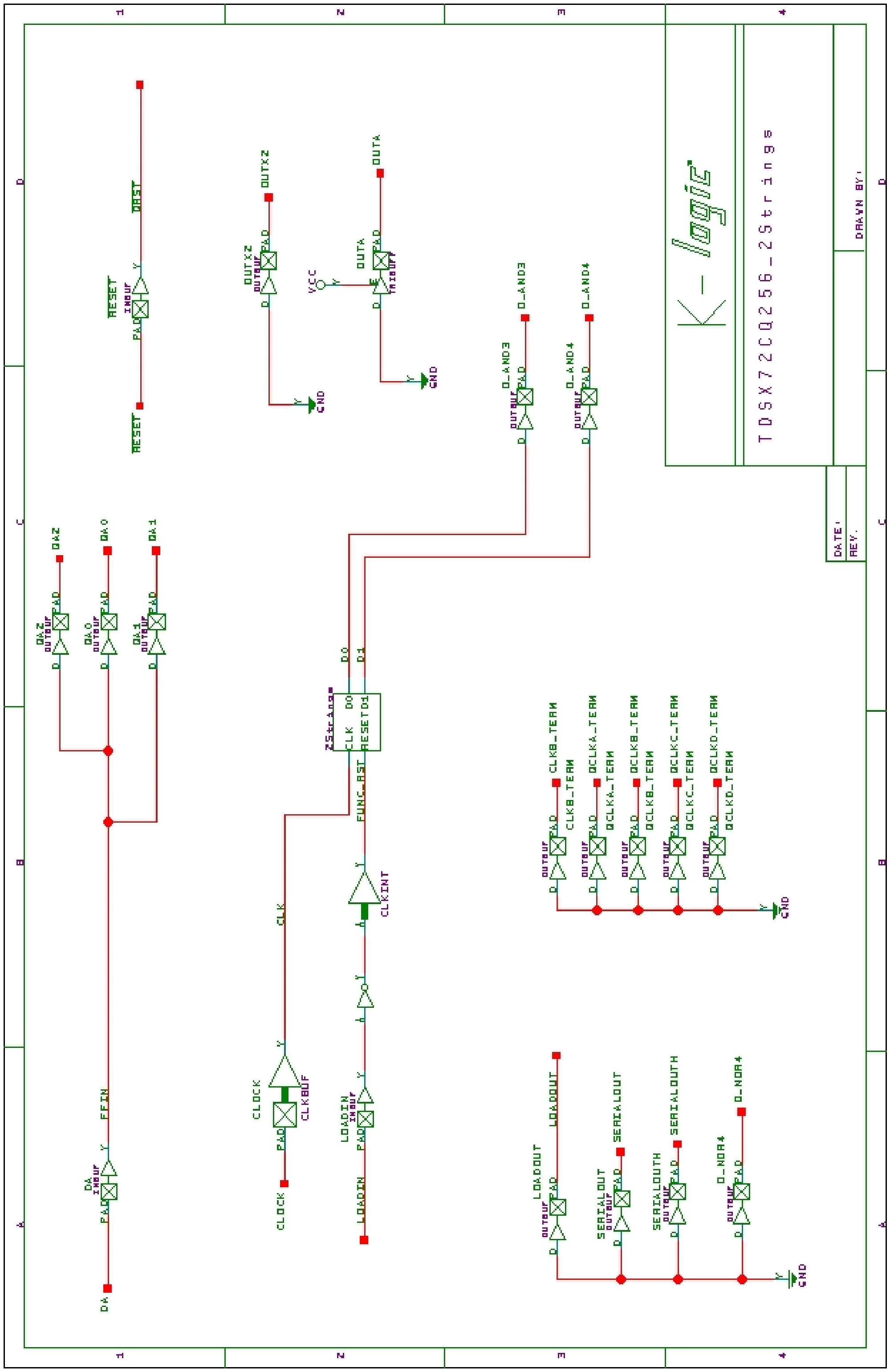


Fig 13(b) Post-annealing falling edge of DUT 26937, abscissa scale is 2 V/div and ordinate scale is 2 ns/div.

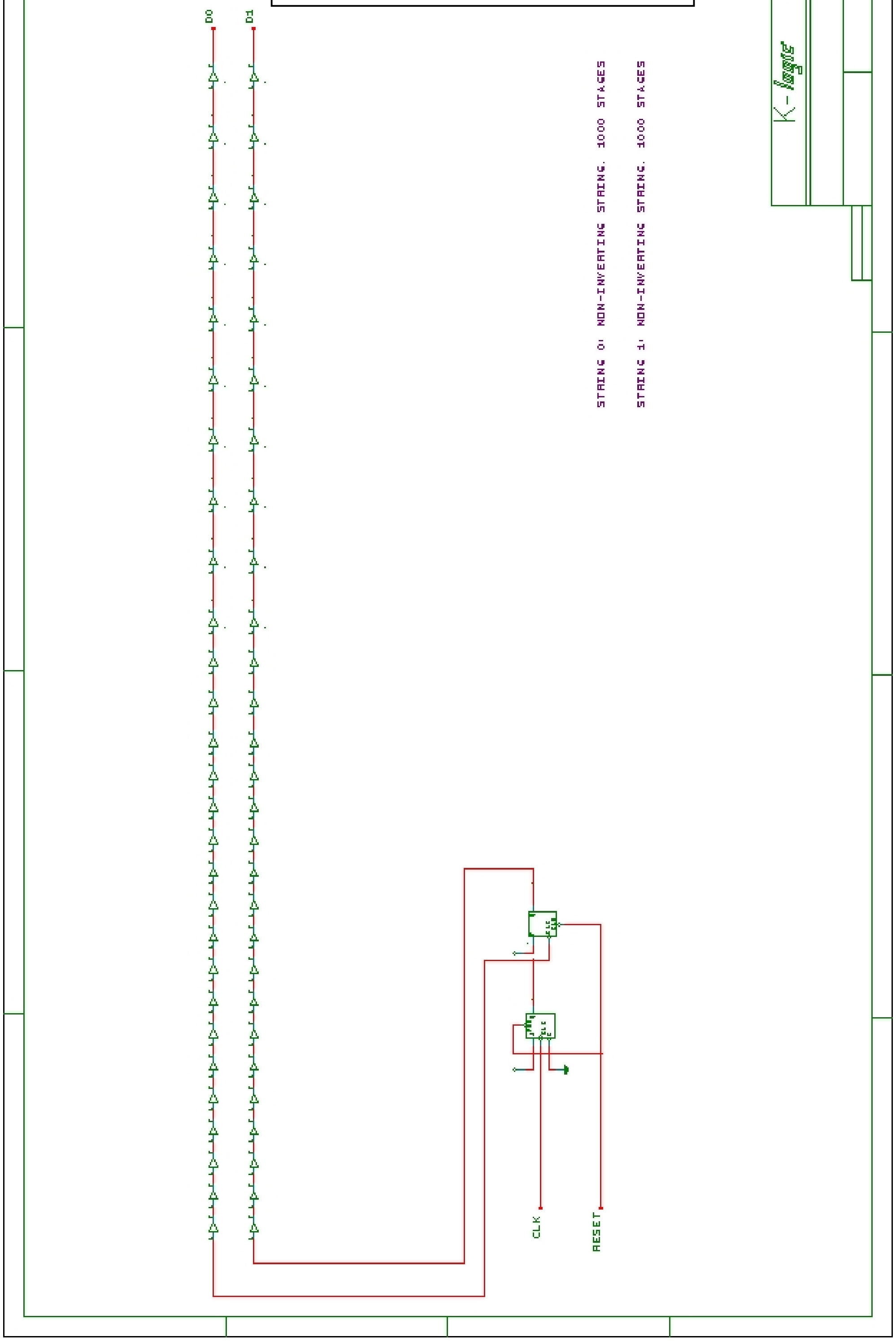
APPENDIX A DUT DESIGN SCHEMATICS




K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
RESET
ORST
OUTX2
OUTA
VCC
GND
D_AND3
D_AND4
QAZ
QA0
QA1
2Strings
CLK
RESET
D0
D1
FUNC_RST
CLKINT
CLOCK
CLKBUF
LOADIN
DA
FFIN
CLKB_TERM
QCLKA_TERM
QCLKB_TERM
QCLKC_TERM
QCLKD_TERM
LOADOUT
SERIALOUT
SERIALOUTH
D_NOR4

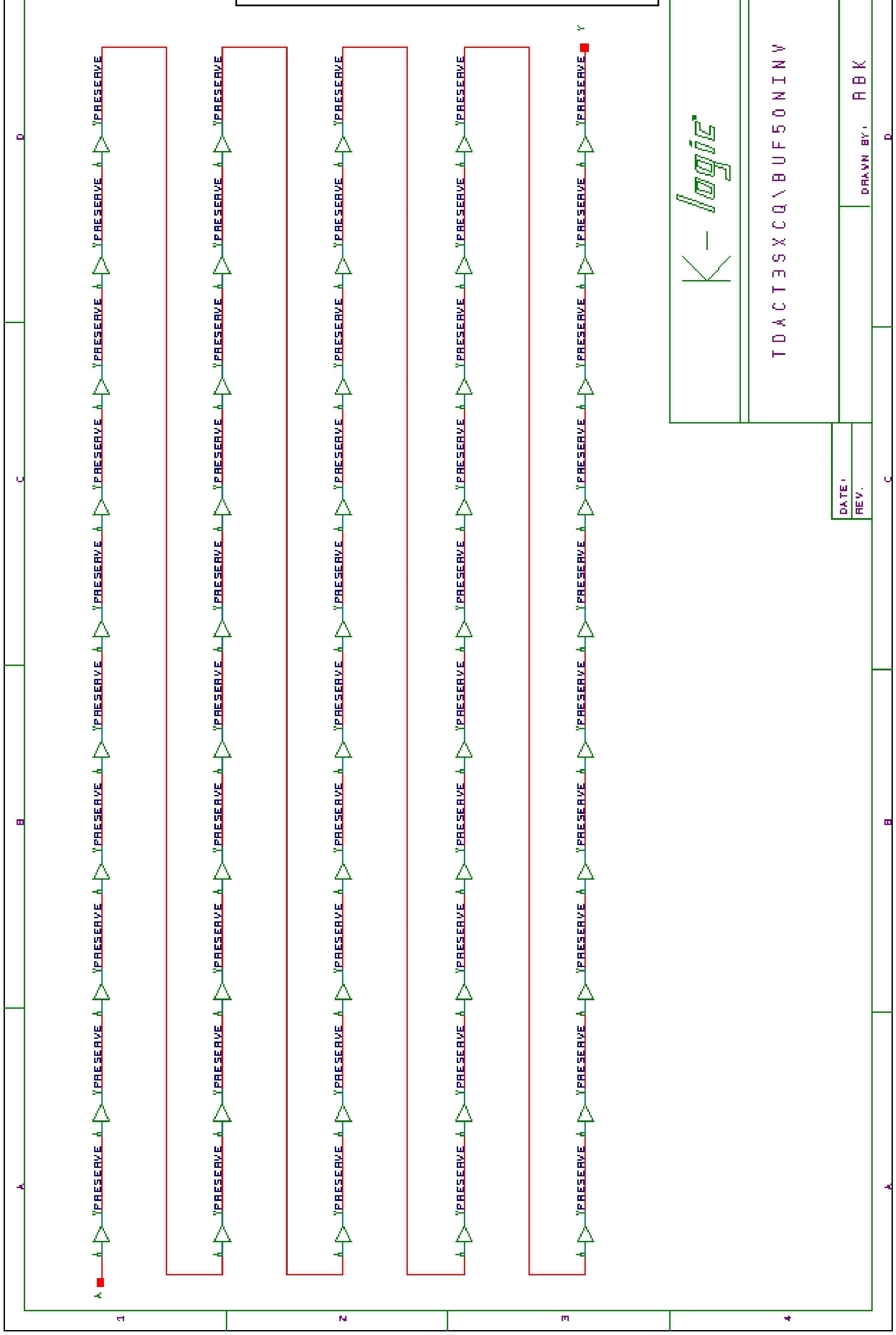
Note for TDSX32CQFP256_2Strings design

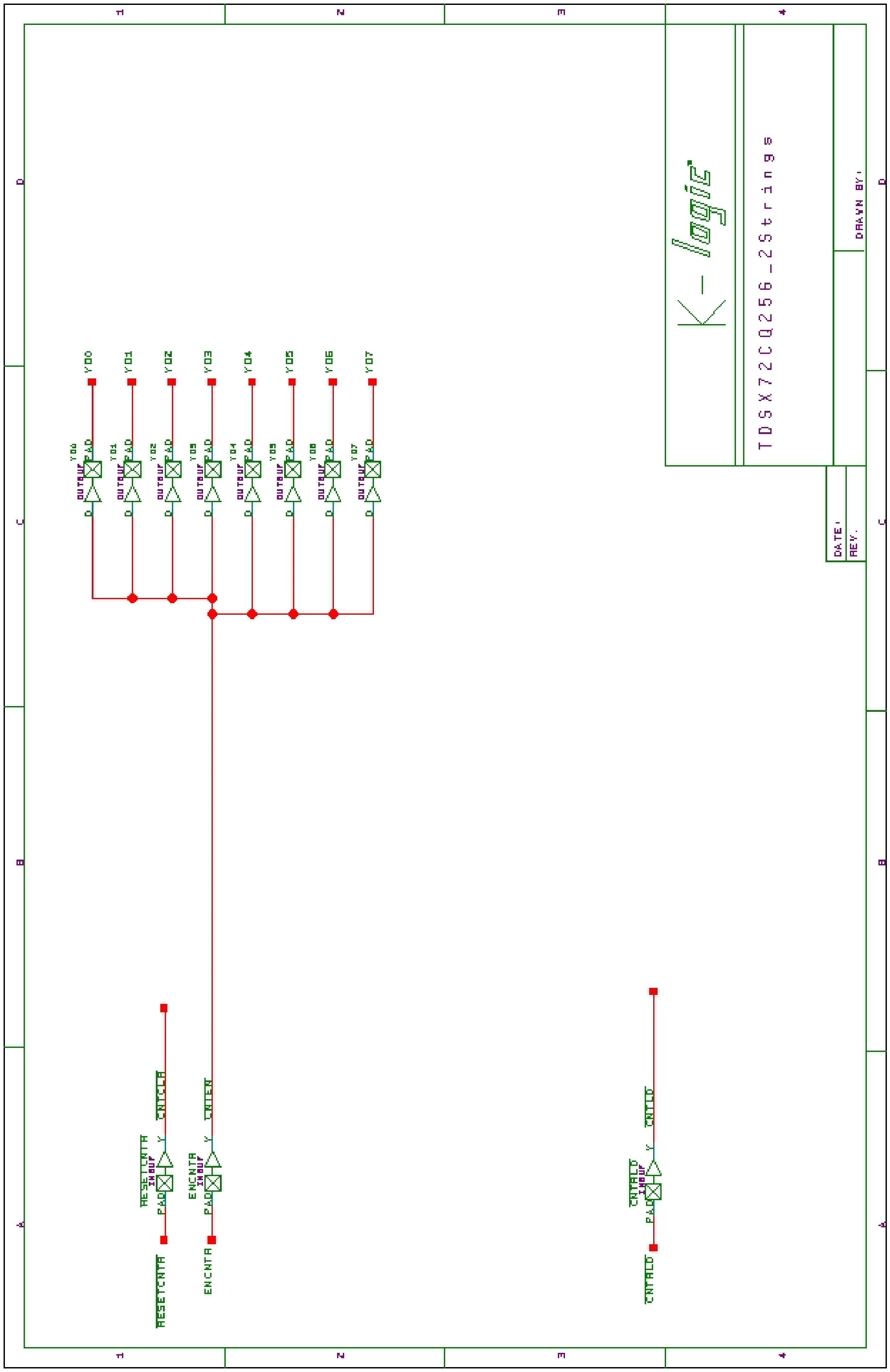
- Each string has 560 buffers.

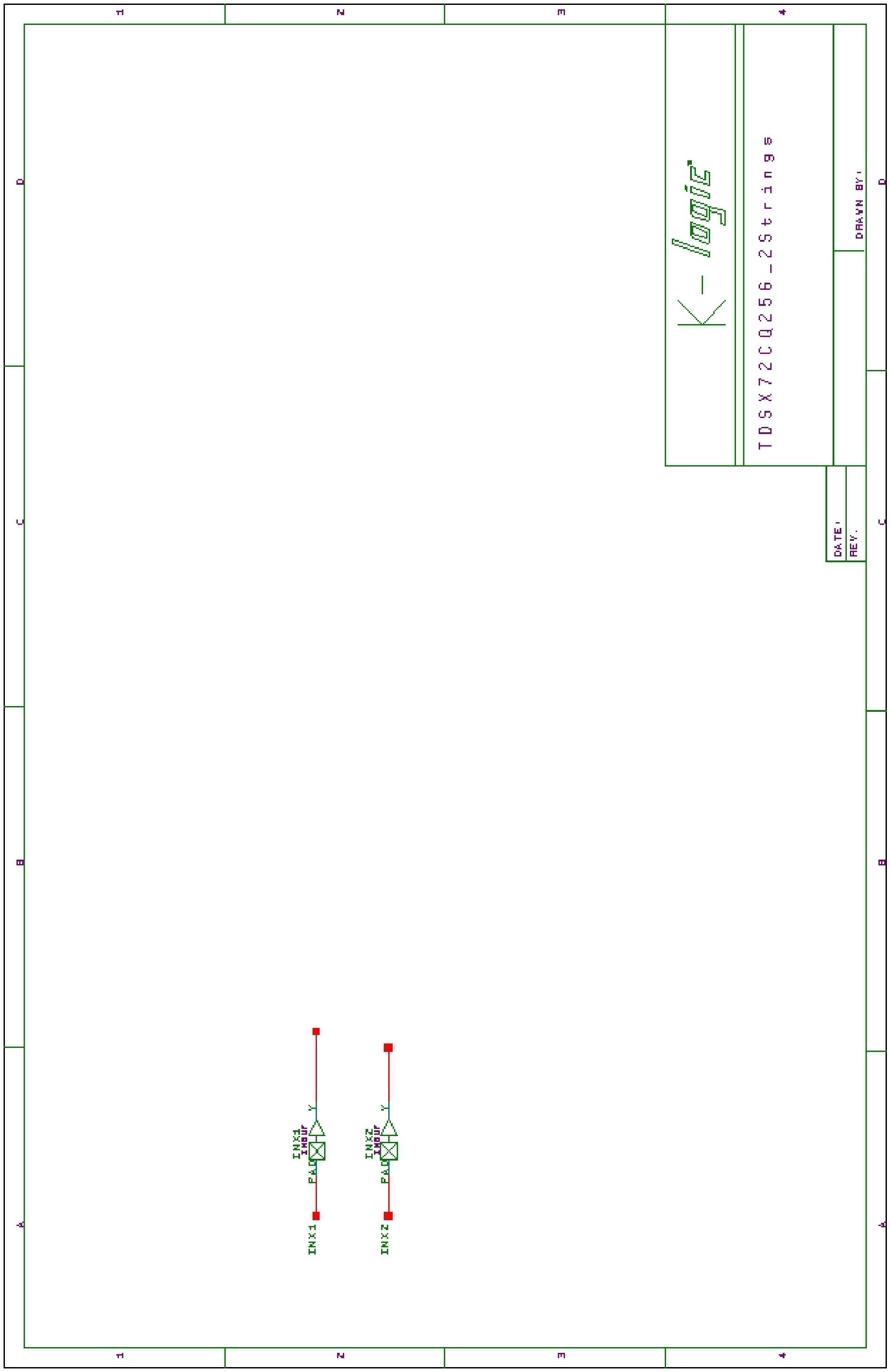


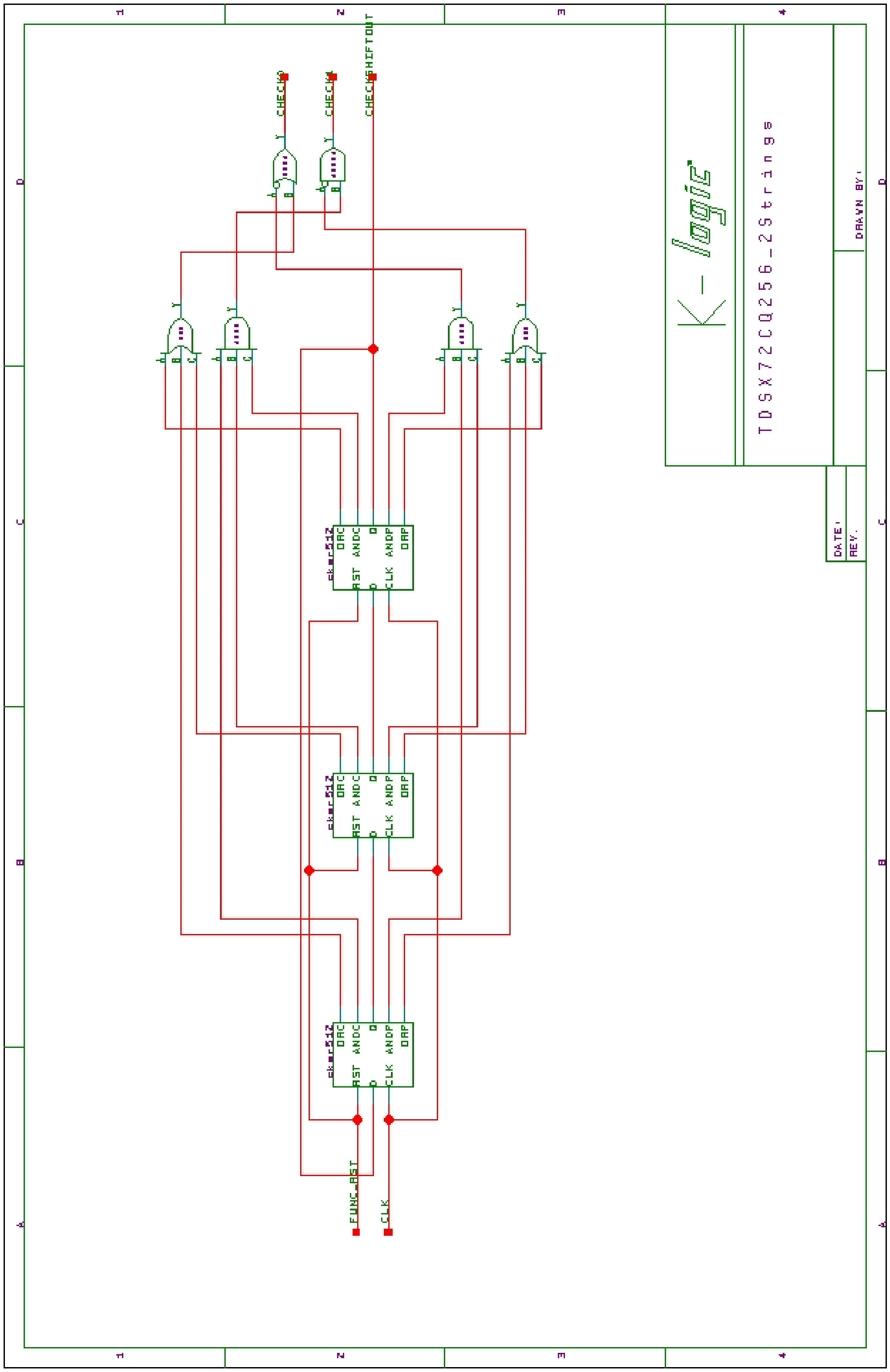
Note for TDSX32CQFP256_2Strings design

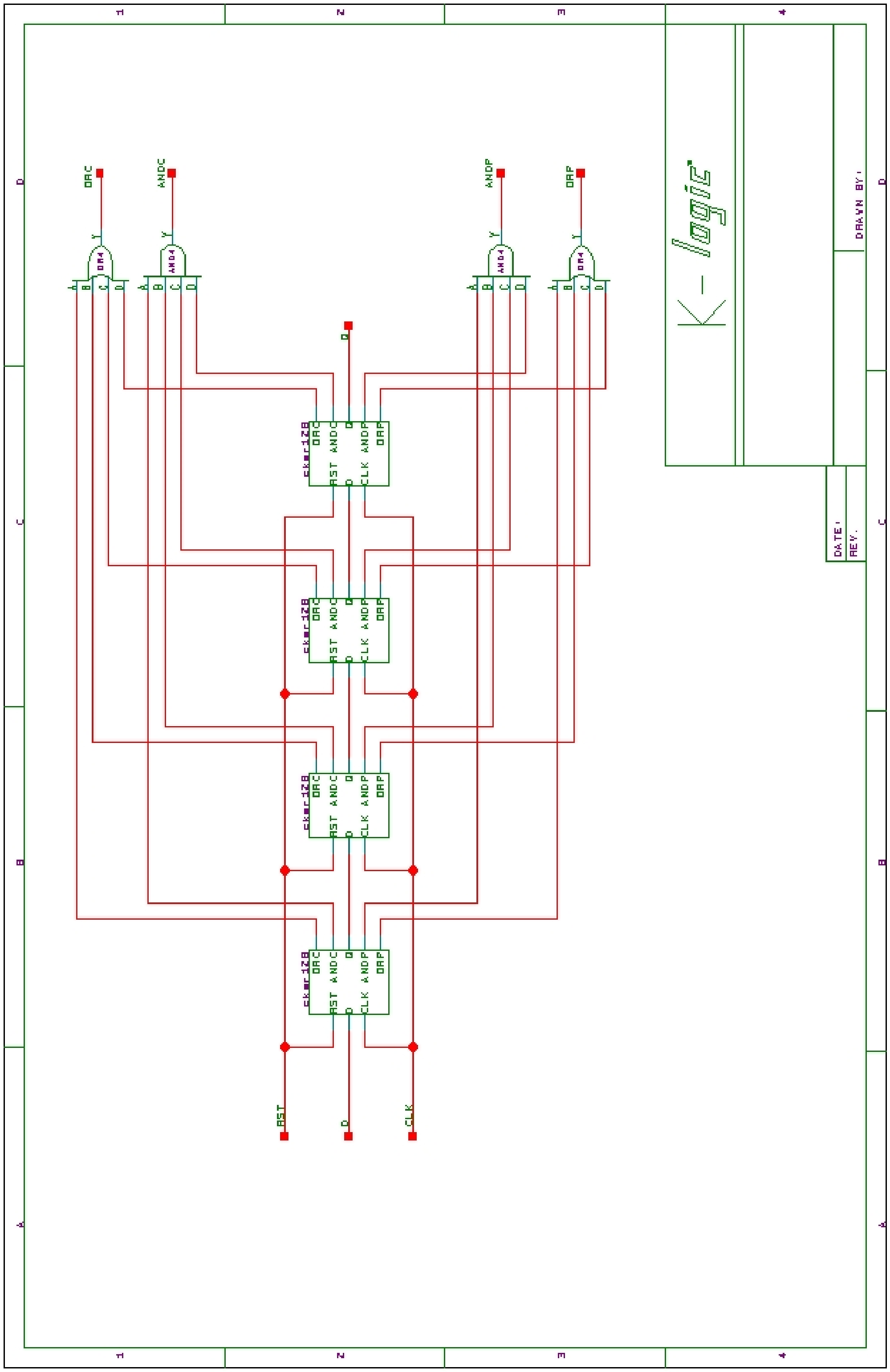
- There are only 20 buffers in this page.

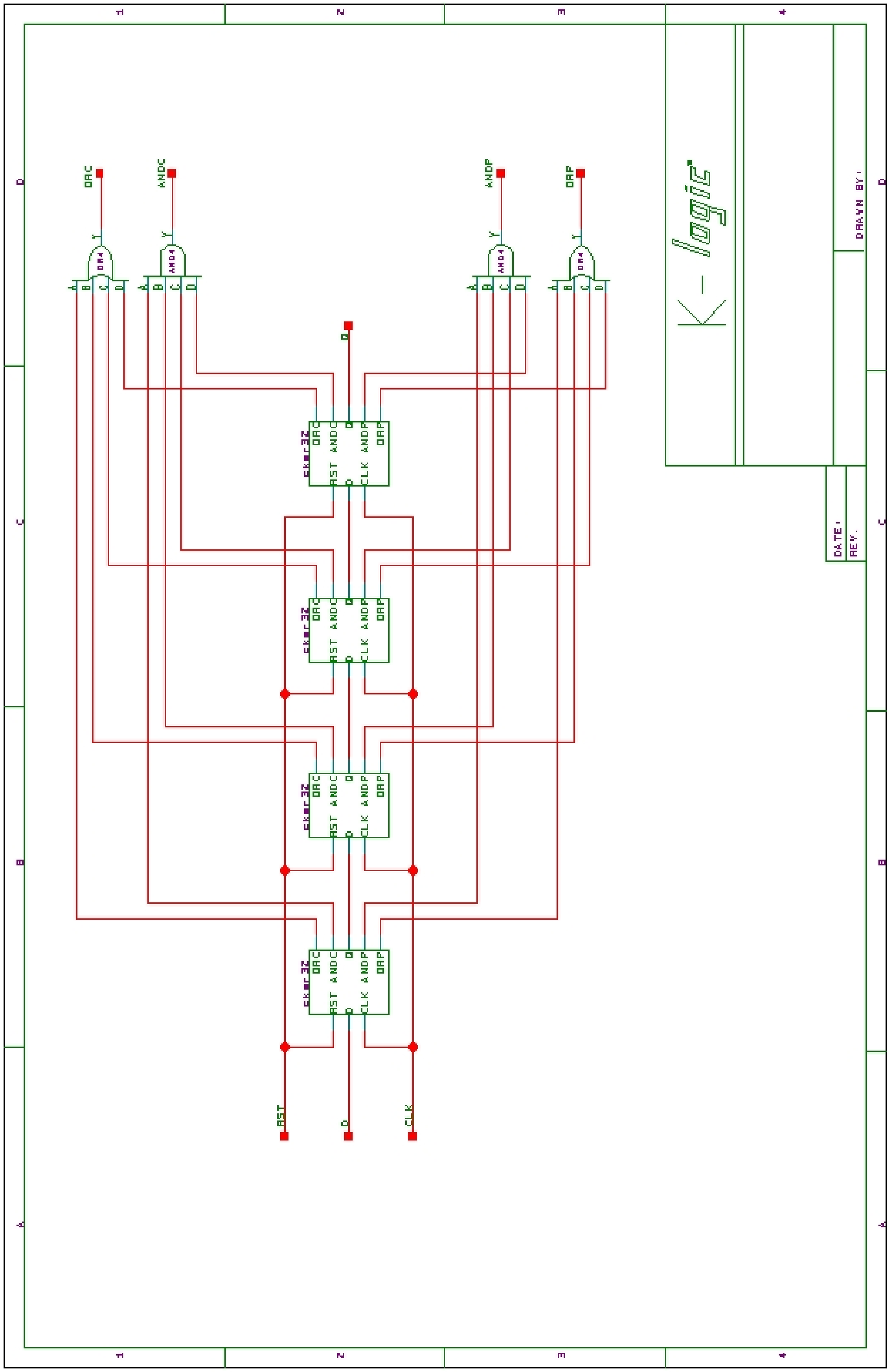


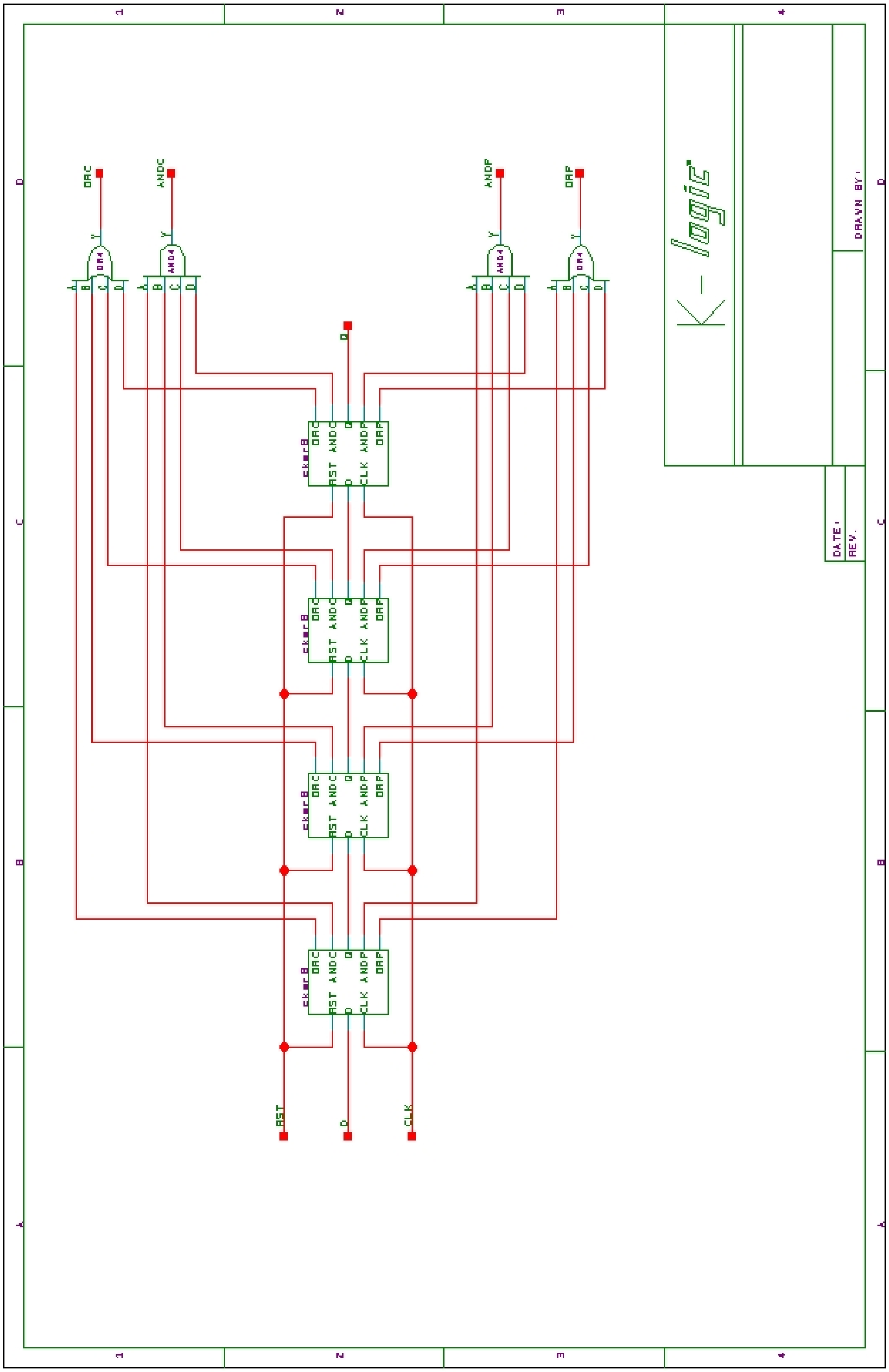

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
YO0
YO1
YO2
YO3
YO4
YO5
YO6
YO7
RESETCNTA
ENCNTA
CNTALD
CNTCLR
CNTEN
CNTLD

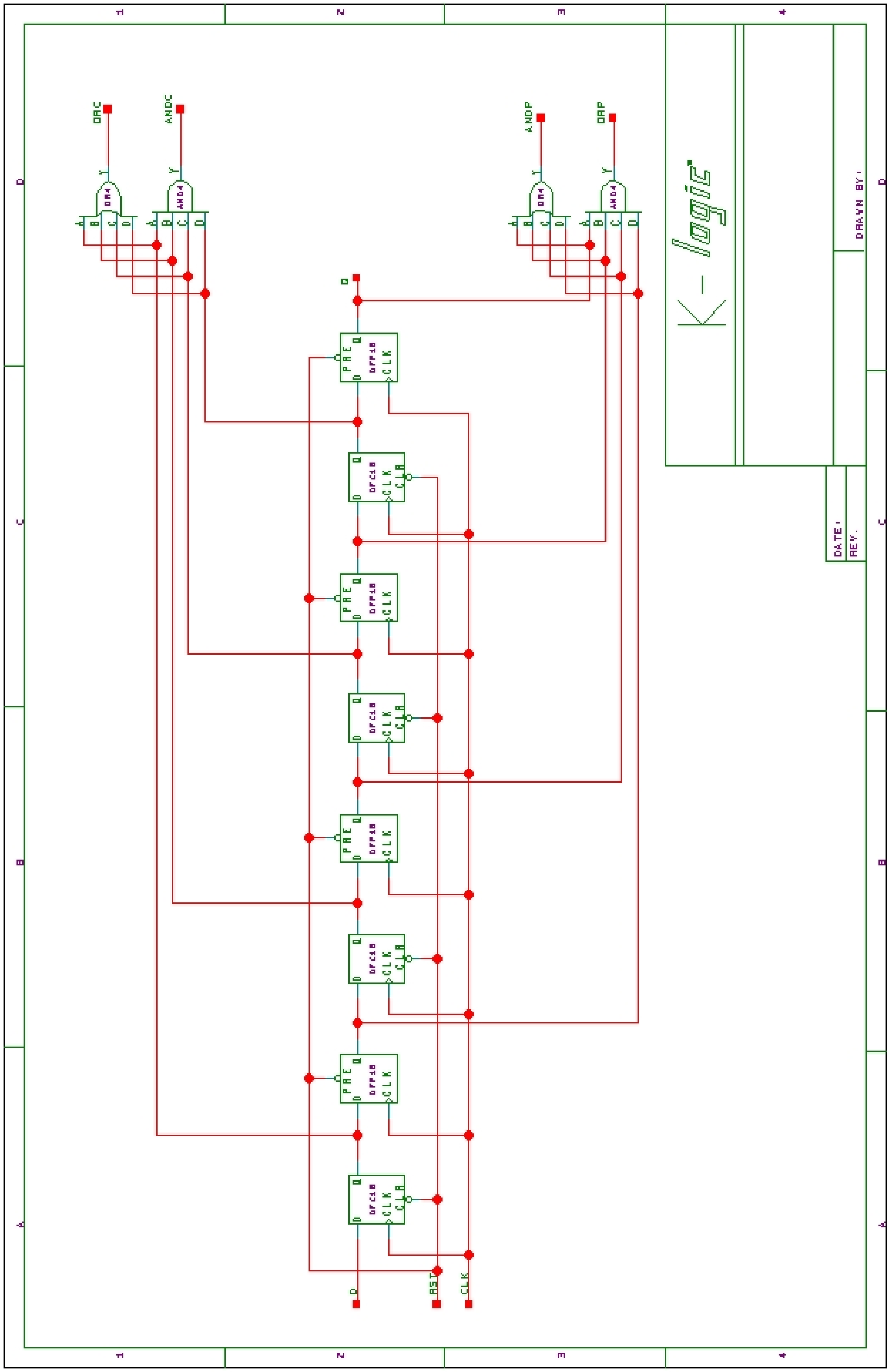

TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
INX1
INX2
INX1
INX2

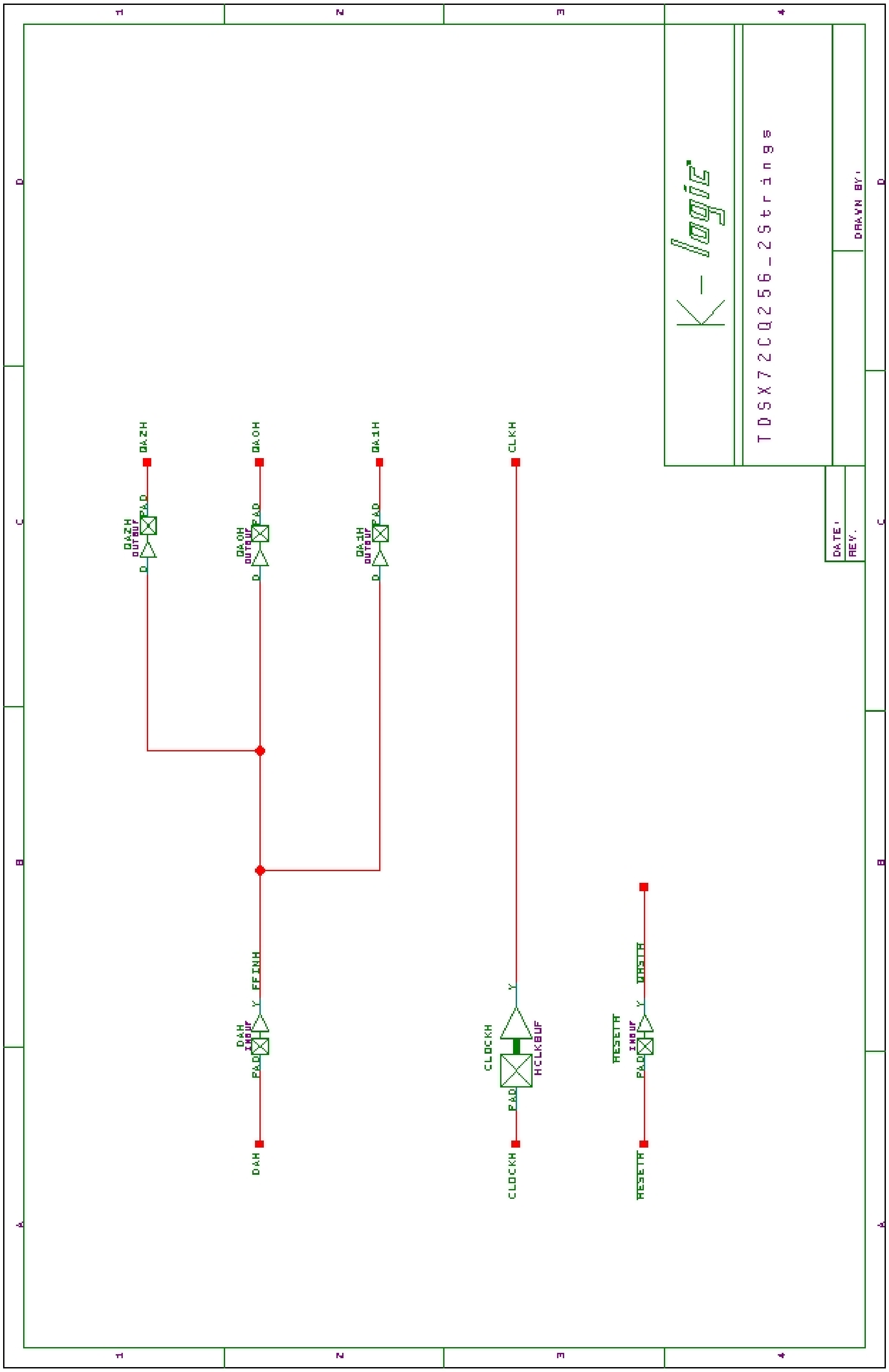

CHECK0
CHECK1
CHECKSHIFTOUT
ORC
ANDC
Q
RST
D
CLK
ANDP
ORP
FUNC_RST
CLK
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.

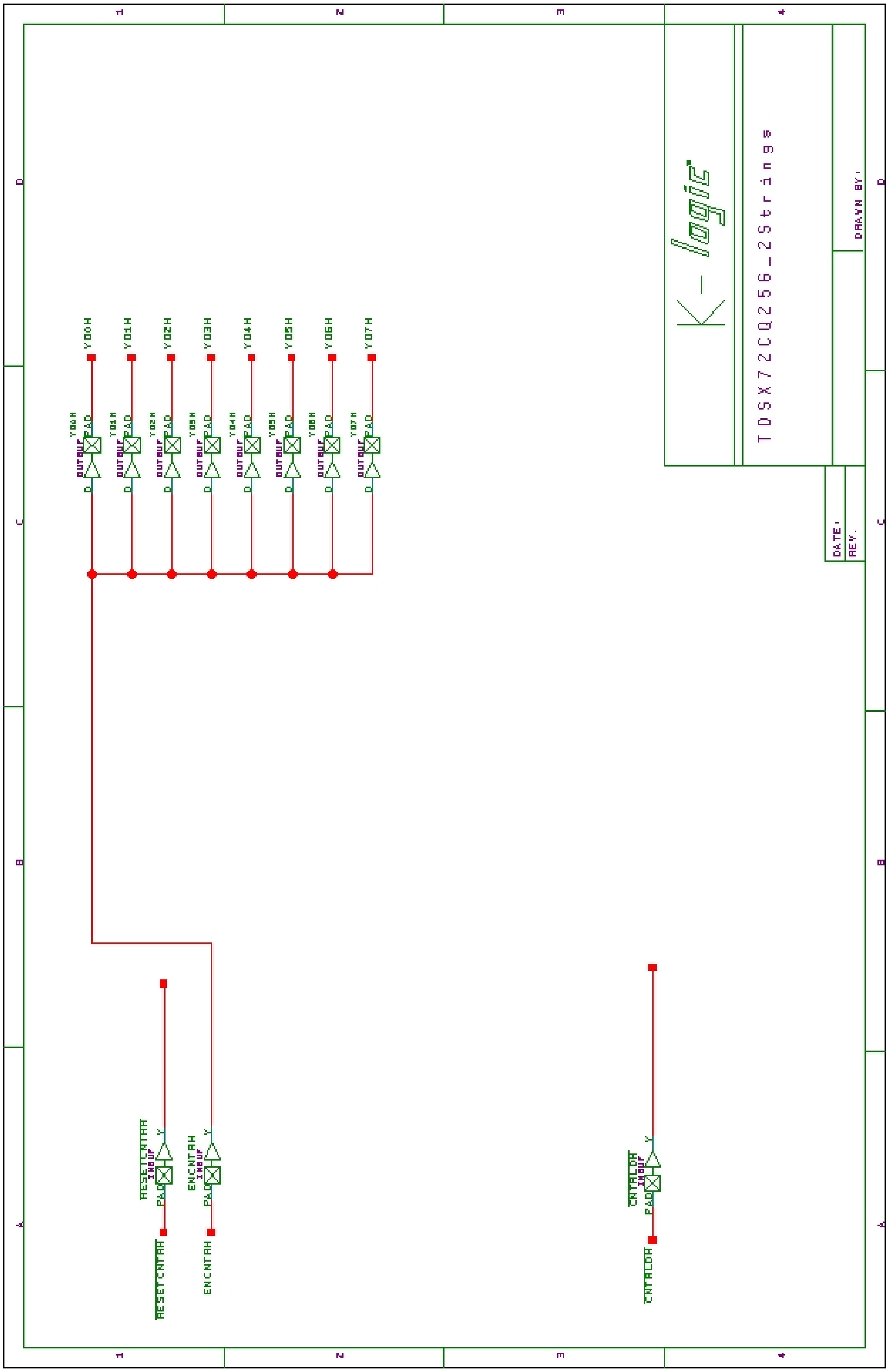

ORC
ANDC
ANDP
ORP
Q
ckmr128
RST
D
CLK
ANDC
ANDP
DATE:
REV.
DRAWN BY:

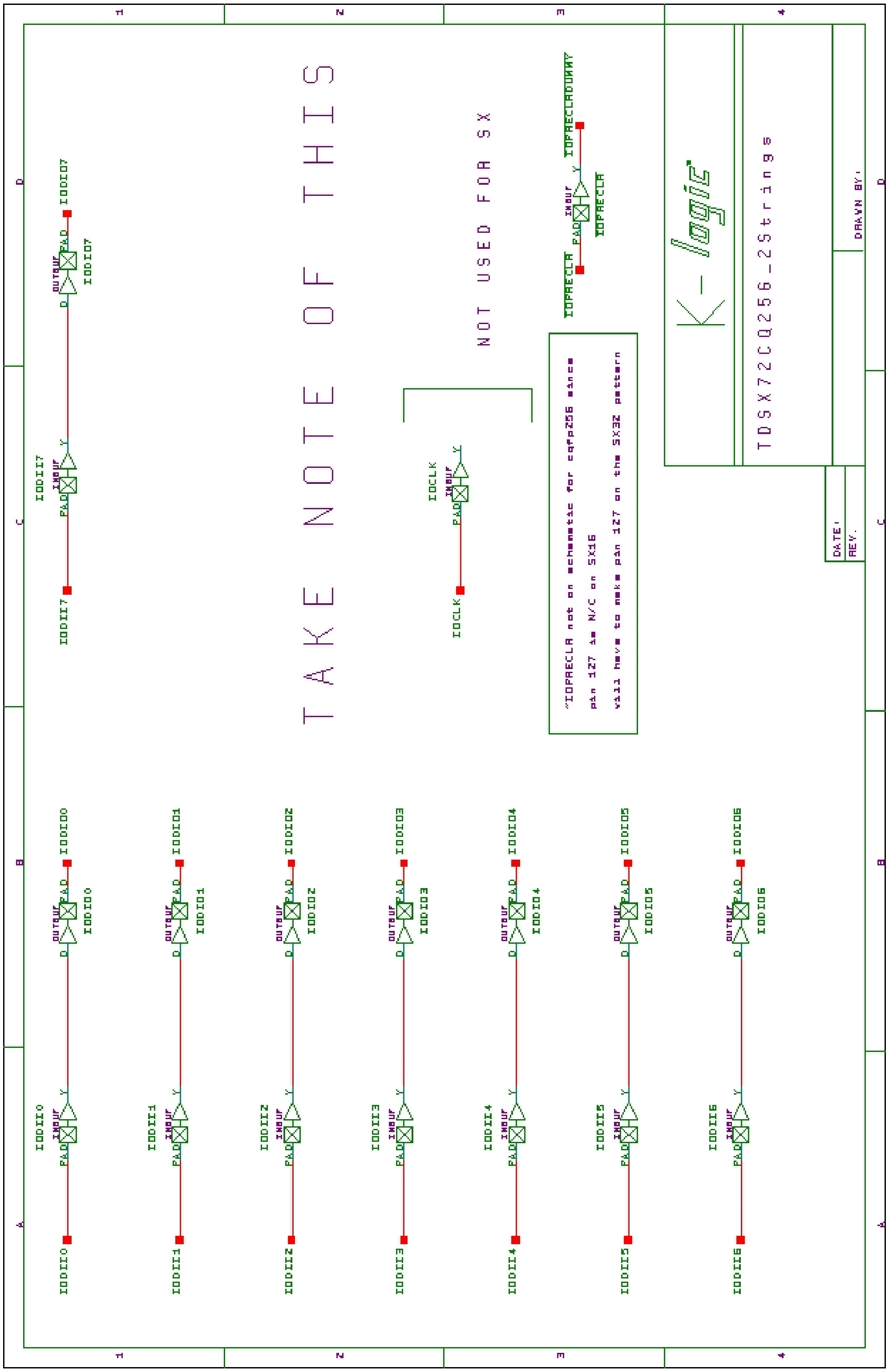

ORC
ANDC
ANDP
ORP
Q
RST
D
CLK
ckmr32
DATE:
REV.
DRAWN BY:
K-logic

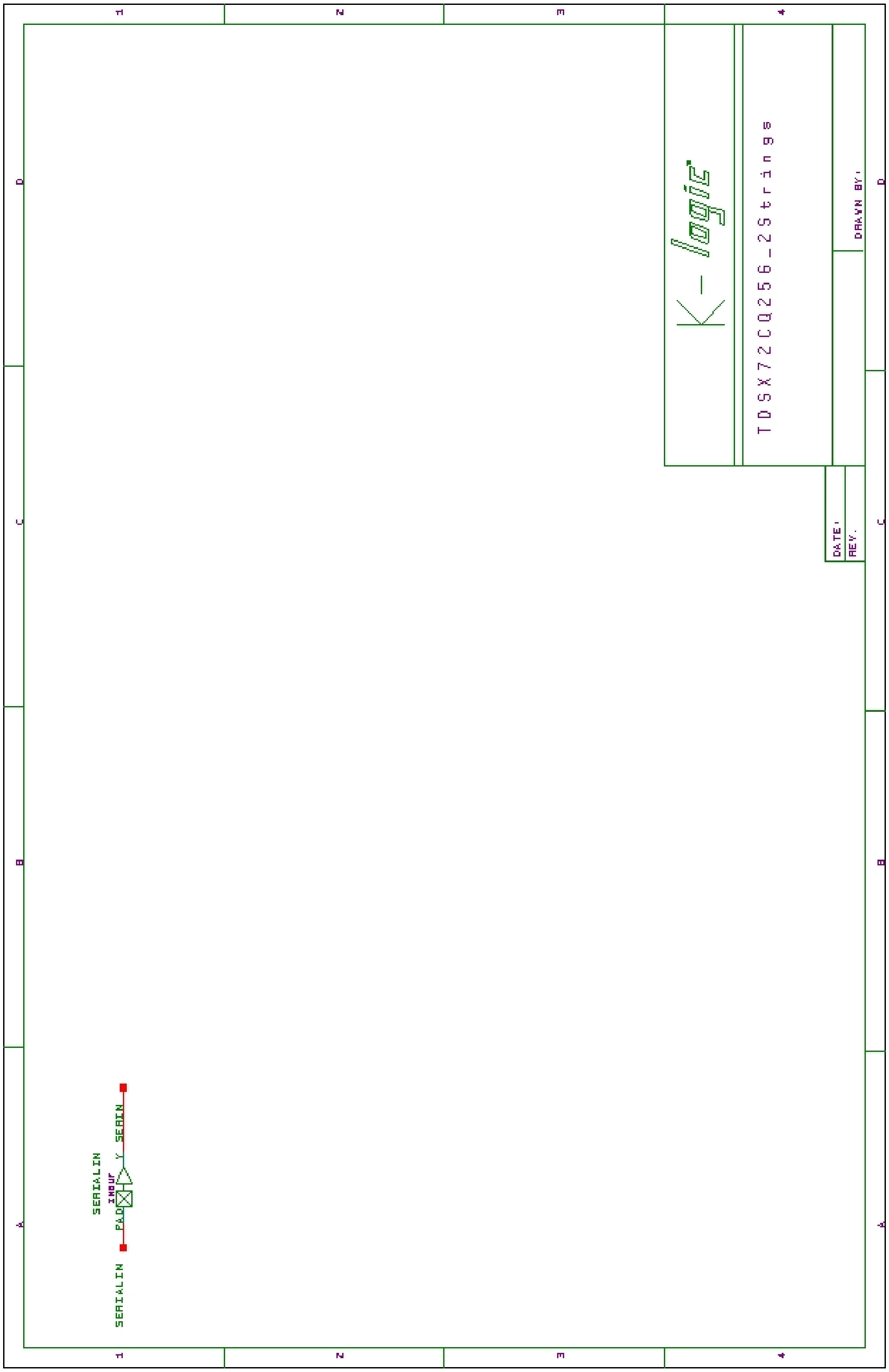

ORC
ANDC
ANDP
ORP
Q
ckmrB
RST
D
CLK
OR4
AND4
K – logic
DRAWN BY:
DATE:
REV.


ORC
ANDC
ANDP
ORP
Q
D
RST
CLK
DATE:
REV.
DRAWN BY:


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
DA2H
DA0H
DA1H
CLKH
OUTBUF
INBUF
HCLKBUF
DAH
FFINH
CLOCKH
RESETH


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.
Y00H
Y01H
Y02H
Y03H
Y04H
Y05H
Y06H
Y07H
OUTBUF
PAD
RESETCNTAH
ENCNTAH
CNTALDH
INBUF


TAKE NOTE OF THIS
NOT USED FOR SX
*IOPRECLR not on schematic for cqfp256 since
pin 127 is N/C on SX16
will have to make pin 127 on the SX32 pattern
IOPRECLR
IOPRECLRDUMMY
IOCLK
IODII0
IODIO0
IODII1
IODIO1
IODII2
IODIO2
IODII3
IODIO3
IODII4
IODIO4
IODII5
IODIO5
IODII6
IODIO6
IODII7
IODIO7
INBUF
OUTBUF
PAD
K-logic
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.


TDSX72CQ256_2Strings
DRAWN BY:
DATE:
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SERIALIN
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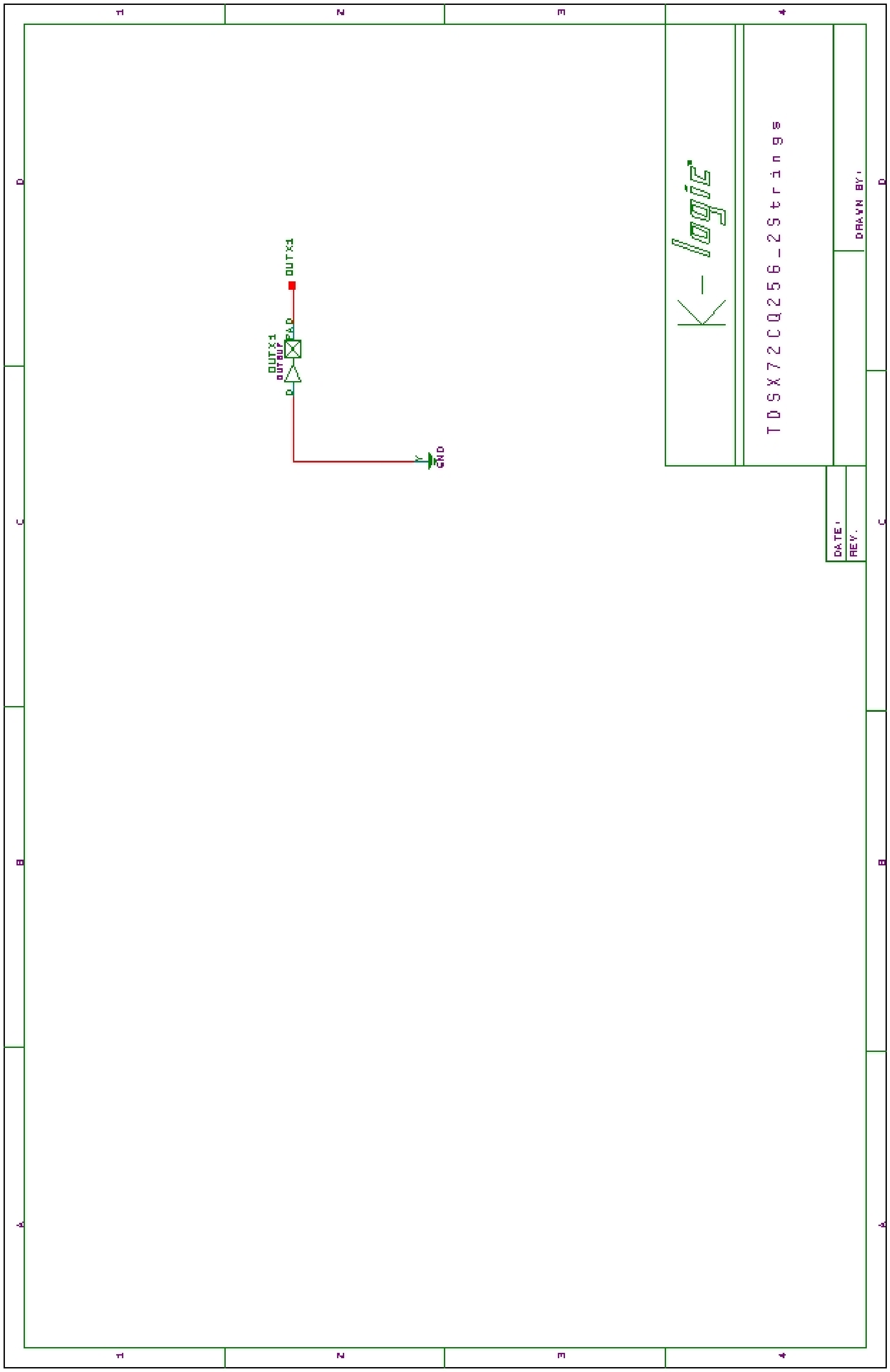
OUTX1
PAD
OUTX1
OUTBUF
GND
TDSX72CQ256_2Strings
DRAWN BY:
DATE:
REV.