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# RT54SX-S $T_r/T_f$ Experiment

**June 14, 2002**

**BY**

**Actel**

**Product Engineering**

**DATE:** June 14, 2002

**WAFER LOT CODE:** T25KS005

**DEVICE TYPE:** RT54SX72S-CQ256B

**DATE CODE:** 0151

**NUMBER OF UNITS:** 4

## 1. ISSUE

Actel understands that customers may have difficulty meeting the 10ns $T_r$ and $T_f$ specification of the RT54SX-S devices for certain applications (see Note 1 Electrical Specifications). As reported by customers in their application of RT54SX-S programmed parts the maximum fall transition time specification could exceed the limits of the Actel data book for these parts (See Note 2 for other discussions on this). This may occur during a bus tri-state operation where there is no active pull up or pull down of the bus voltage and only a passive resistor of large value (~100 KΩ) to ground to discharge the bus. In this type of application, the only concern will be when the customer design has implemented an input or bi-directional user I/O function connected to the bus. The tri-state buffer implementation in an RT54SX-S device disables the input buffer and will not be a concern. With a corresponding large bus capacitance (~2700pF) the resulting fall times for input pins from the tri-stated bus operation on these or any similar Actel parts would be on the order of 500µs, exceeding the specified 10ns maximum transition time. There may be concerns for functionality issues during the tri-state conditions as well as long-term reliability concerns. This report summarizes the findings of fall time experiments completed to determine any potential reliability issues with slow fall times.

## 2. EXPERIMENT

In order to study the potential reliability issues Actel programmed four RT54SX72S-CQ256B units with the different I/O buffer configurations available. A mix of PCI, LVTTL, TTL/PCI and CMOS I/Os were configured in order to test the effects of slow fall times on each of the available I/Os (See Note 1). Two units were programmed for 3.3V I/O operation (Table 1) and two units for 5V I/O operation (Table 2). The internal array (Vcca) was biased at 2.5 volts. External RC networks consisting of a 100KΩ resistor in parallel with a 2700pF capacitor created slow fall time signals on the order of 500µs. An I/O output buffer is first enabled to charge the RC network to Vcci, and then tri-stated, allowing the RC network to control the subsequent fall time.

With reference to Figure 1, a total of eight I/Os were incorporated into the experimental design (See also Appendix A). The direction of each I/O is controlled via a low speed 500Hz clock signal. A multiplexor selects between either the low speed clock signal or an asserted active low reset signal. The reset signal allows all RC networks to be discharged during initialization. After initialization each alternate cycle of the external clock switches the I/O from input mode (tri-stated) to output mode. The I/Os are further configured in pairs, whereby the output of an input buffer is directed through an internal logic array inverter to the input of another I/O buffer. This design allows for monitoring the effect of a slow fall times on internal logic module circuits and subsequent input buffers. On any given cycle of the clock, half of the I/Os are acting as input buffers. The charge will decay from the external capacitor and the signal will approach the input threshold transition region. The logic propagates through the I/O input buffer and through an inverter into the other half of the I/O buffers, which are

now acting as output drivers charging the external capacitor for the next half of the clock cycle. When the clock input changes state the role of each I/O buffer reverses, I/Os previously set as drivers are now tri-stated and behave as input buffers.

*Note 1: http://www.actel.com/documents/RT54SXS_DS.pdf*

*Note 2: http://www.actel.com/documents/SchmittTrigger_AN.pdf*

*Table 1 Summary of 3.3Volt I/O Configurations*

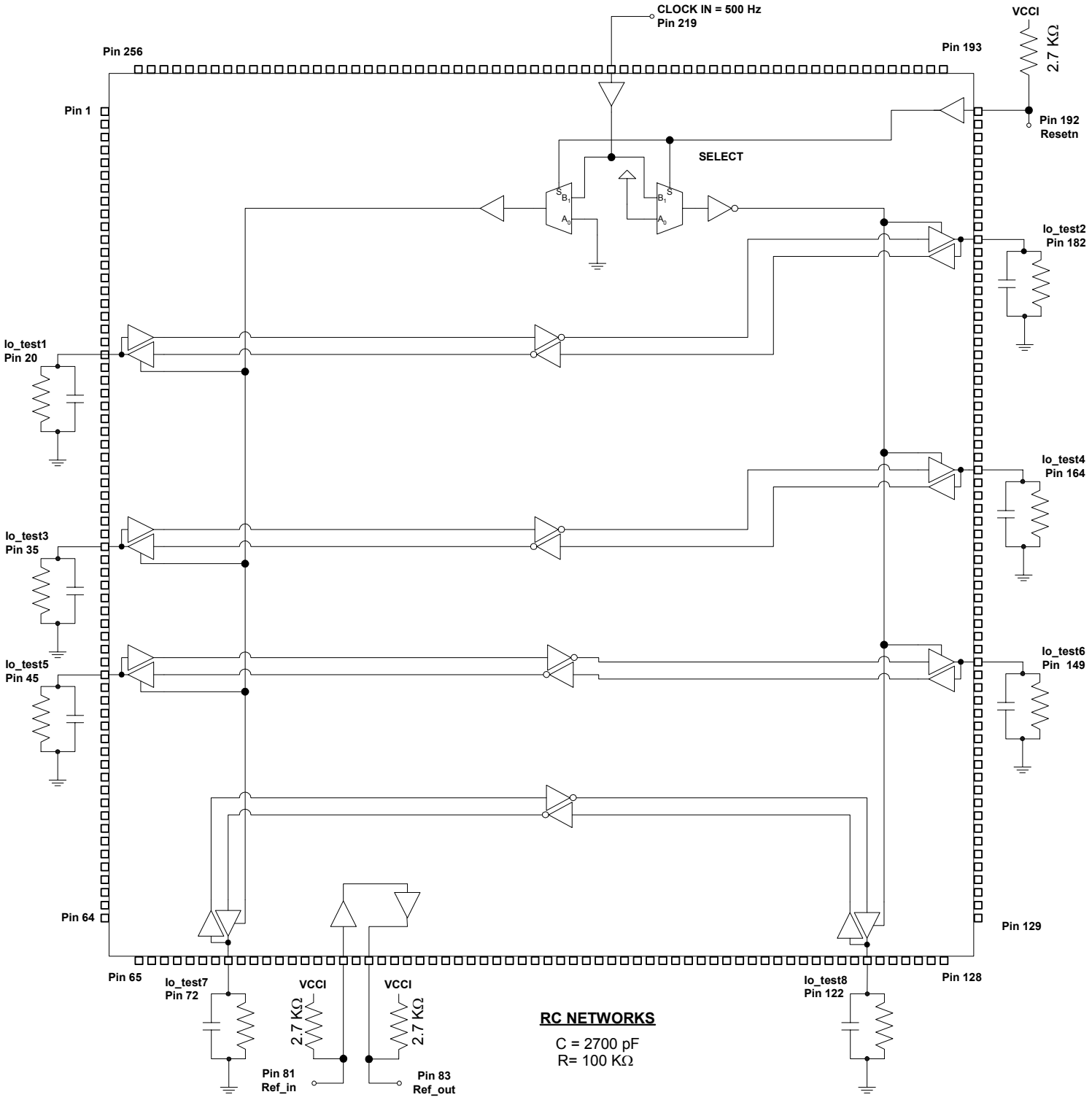
| PORT NAME | MACRO CELL | PIN # | I/O TYPE |
|---|---|---|---|
| Io_test1 | ADLIB:BIBUF | 20 | PCI |
| Io_test2 | ADLIB:BIBUF | 182 | LVTTL |
| Io_test3 | ADLIB:BIBUF | 35 | PCI |
| Io_test4 | ADLIB:BIBUF | 164 | LVTTL |
| Io_test5 | ADLIB:BIBUF | 45 | PCI |
| Io_test6 | ADLIB:BIBUF | 149 | LVTTL |
| Io_test7 | ADLIB:BIBUF | 72 | PCI |
| Io_test8 | ADLIB:BIBUF | 122 | LVTTL |
| Ref_in | ADLIB:INBUF | 81 | PCI |
| Ref_out | ADLIB:OUTBUF | 83 | PCI |
| Resetn | ADLIB:INBUF | 192 | PCI |
| Switch | ADLIB:INBUF | 219 | PCI |

*Table 2 Summary of 5.0 Volt I/O Configurations*

| PORT NAME | MACRO CELL | PIN # | I/O TYPE |
|---|---|---|---|
| Io_test1 | ADLIB:BIBUF | 20 | PCI |
| Io_test2 | ADLIB:BIBUF | 182 | TTL |
| Io_test3 | ADLIB:BIBUF | 35 | PCI |
| Io_test4 | ADLIB:BIBUF | 164 | CMOS |
| Io_test5 | ADLIB:BIBUF | 45 | TTL |
| Io_test6 | ADLIB:BIBUF | 149 | CMOS |
| Io_test7 | ADLIB:BIBUF | 72 | PCI |
| Io_test8 | ADLIB:BIBUF | 122 | CMOS |
| Ref_in | ADLIB:INBUF | 81 | PCI |
| Ref_out | ADLIB:OUTBUF | 83 | PCI |
| Resetn | ADLIB:INBUF | 192 | PCI |
| Switch | ADLIB:INBUF | 219 | PCI |

The four programmed units were then subjected to a 125°C dynamic burn-in with the RC networks in place. The Vcci was set at 5.5 volts for the two 5 Volt I/O parts and 3.3 volts for the two 3.3 Volt I/O parts. The Vcca was set to 2.5 Volts. Burn-in time for the 3.3 Volt units was 202 hours and for the 5.0 Volt units the time for burn-in was 160 hours.

*Figure 1 RT54SX72S Fall Time Experiment Burn-in Schematic*



## 3. RESULTS:

Prior to burn-in I/O signals were verified operational on all four units. The Vcci currents were monitored both before and after burn-in. For the 3.3 Volt Vcci case, dynamic current was measured just under 1.0mA both before and after burn-in. For the 5.0 Volt Vcci case, dynamic currents were below 2.8mA. Static currents for the two cases were 0.6mA and 1.0mA respectively. There was less than +/- 0.1 mA change in current overall from pre to post burn-in, most probably measurement differences. Each I/O toggles with relatively fast rise times and slow fall times created by the RC load, as can be seen in the captured scope waveforms in Figure 2 and Figure 3 from the programmed devices post burn-in. In the first photo (Figure 2), note on the falling edge of the input clock (Pink signal) one of the I/Os is tri-stated (Green signal) with the fall time determined by the RC time constant. This signal is routed to another I/O (Purple signal) via an internal inverter, which then switches to an active high at about half of Vcci on its input. Since the output is now active it is able to drive high the RC network easily. Note in the expanded waveform (Figure 3), there are about 2 microseconds of oscillation on the rising edge of the waveform. This is a direct result of the slowly falling input signal remaining a long time in the I/O buffer transition region where both P-channel and N-channel devices are conducting. Slight changes in currents result in small changes in voltages, which sets up oscillatory conditions until the input signal falls below the point where both transistors are conducting heavily. It is this region of oscillation that could be of concern as this is the point of maximum conduction. From the waveform it is most likely that there would be **"logic upsets"** occurring during this transition time however as the burn-in results indicates, there were no circuit failures or large increases in standby or dynamic currents found.

*Figure 2 Waveforms of input clock & I/Os under test*

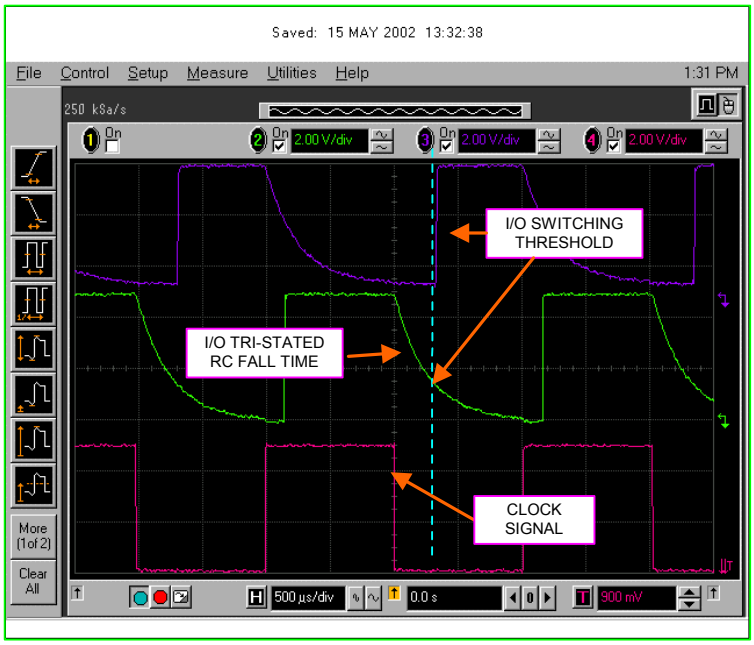
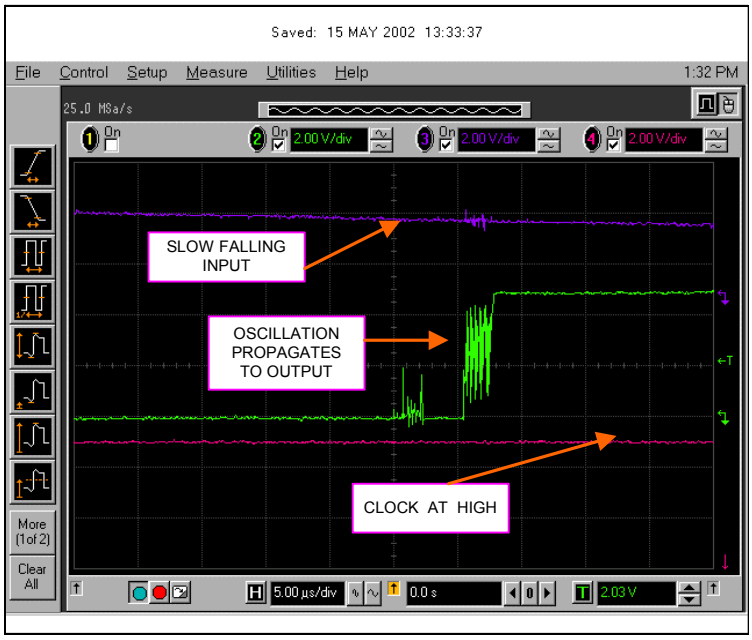
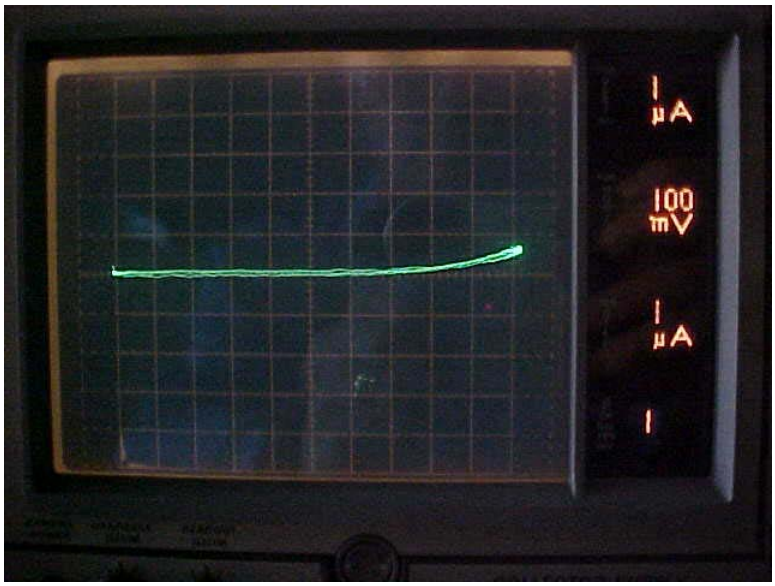


*Figure 3 Expanded waveform of input clock & I/Os under test*




Post burn-in input pin leakage currents were measured on all four units. Both input to Vcci and input to Ground currents were measured on each of the test pins plus several unused pins. The typical leakage current characteristic is observed below in Figure 4. It was found that for all four units that leakage at 1.0 Volts on the input was approximately 500 nA in all cases, whether to Ground or to Vcci or between used and unused pins.

*Figure 4 Typical Post Burn-in Input Pin Leakage Current to Gnd/Vcci*



## 4. ELECTRO-MIGRATION (EM) ANALYSIS:

A slowly falling (or rising) input signal to an I/O buffer may lead to high currents in the input circuitry, therefore an examination was made to determine the possibility of electro-migration conditions. In examining the waveform photos of Figure 2 and Figure 3 there are time periods during the slowly falling input signal (or a rising signal) in which the signal is oscillating and remains in the transition region for several microseconds. During this oscillatory time, current flowing in the input buffer drivers, as well as through subsequent logic circuitry, are at or near their peak values. Figure 5 below calculates this peak current for the RTSX-S input buffer transistor pair T5-T6 as shown in the schematic of Figure 7.

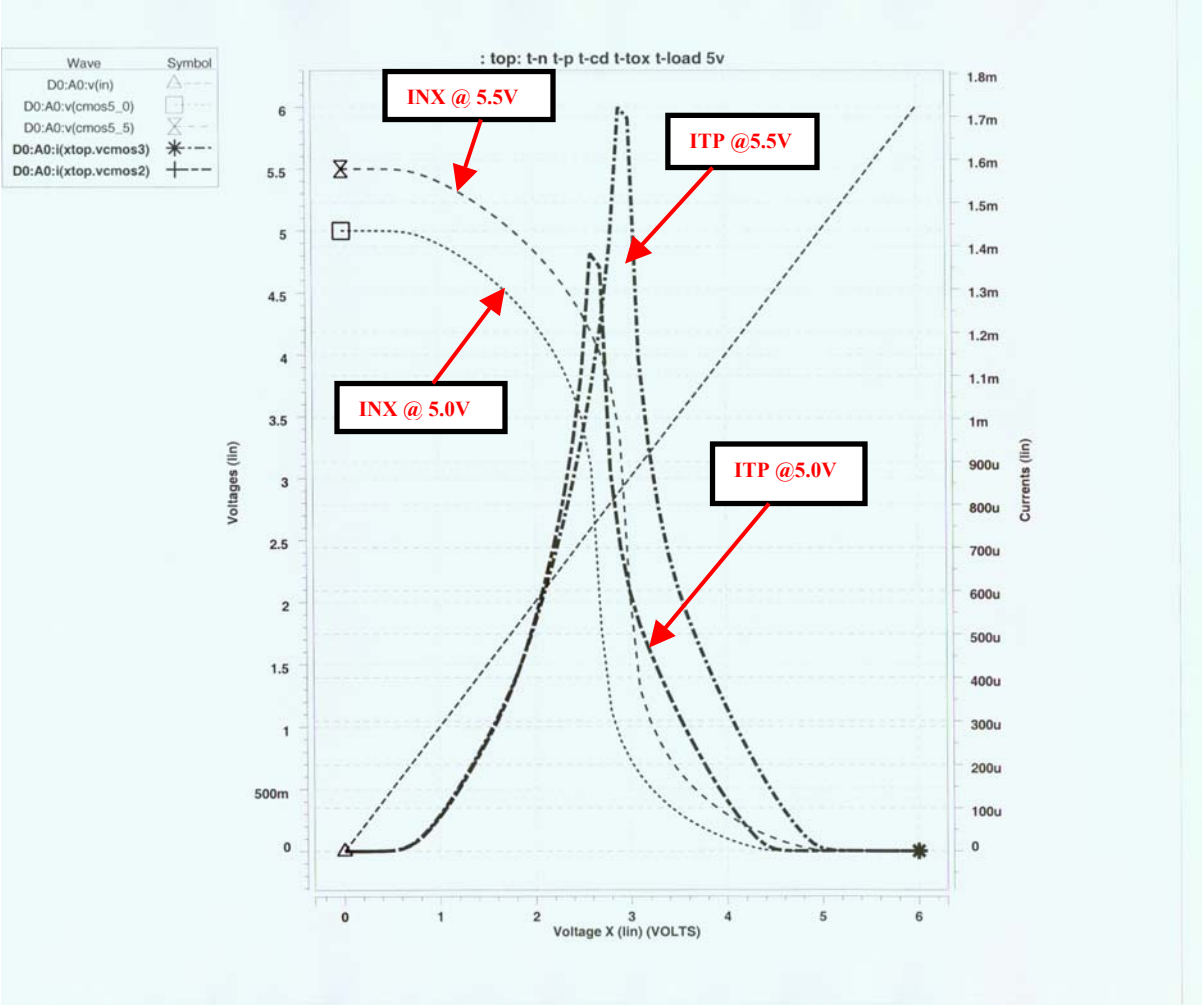



*Figure 5 HSPICE simulation for totem pole current at 50°C*

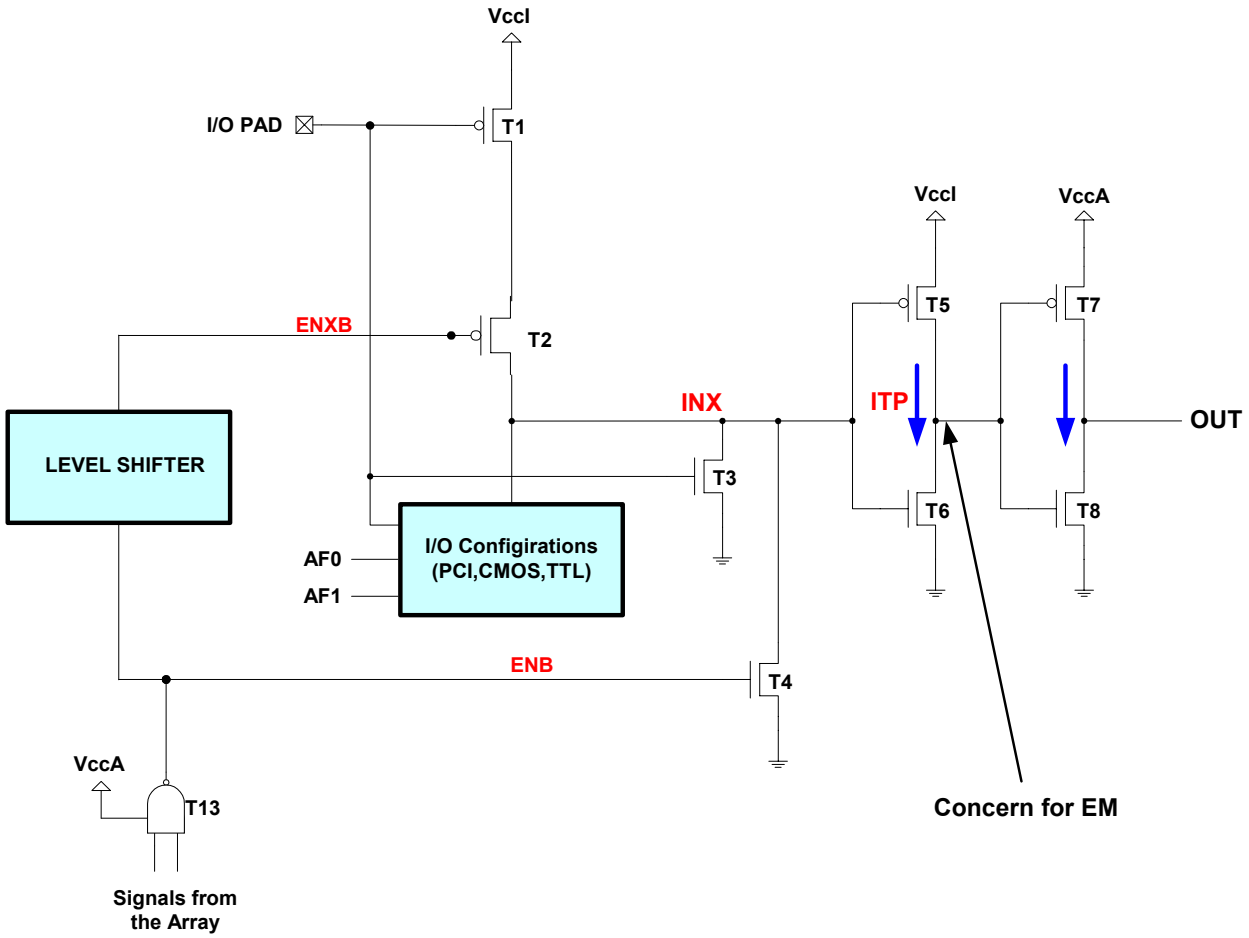



*Figure 6 Simplified Schematic for a General Purpose I/O*

From examining the input buffer schematic shown above, the T5-T6 transistor driver pair represents the circuitry exhibiting maximum totem pole current flow densities in the input buffer circuit. This is due to a higher supply voltage Vcci, and smaller line widths than the T7-T8 pair. In further examination of the input buffer layout, minimum line width for the T5-T6 combination occurs on the first metal layer, M1. As shown in above Figure 5, data from the simulation of this pair results in a worse case maximum current of 1.72 mA for the condition of input voltage being exactly at the point of peak current.

For a slow falling input signal of 500 µs, the photo of Figure 2 indicates less than 5 µs of time for residing in the transition region thus peak currents occur only for 1% of the signal transition time, however current does flow for most of the whole signal range. To consider current throughout the signal excursion, a conservative calculation is to examine the case for a 100% duty cycle (both rise and fall signals exhibiting slow transition times). In examining Figure 5, current will flow for close to 80% of the cycle, with an average value less than 25% of its peak value. For a 100% duty cycle case, the average current in the T5-T6 pair calculates less than 0.43 mA for both a slow rise and slow fall time of the input signal (500 µs). Utilizing Actel's metal Electro-Migration (EM) guidelines for assurance of 20-year reliability, this conservatively calculated average current is well below the allowable design rule limits. Thus, applications that allow for very slow fall times do not create EM concerns in input buffers.

Also examined were the effects on output driver transistors. Noting the oscillations of an output signal from Figure 3, an application with slow transition times following through internal logic to an output driver may create totem pole currents in the output transistor pair as well. In this case because the output voltage does not switch until near the middle transition region, the output driver totem pole currents are limited to a smaller percentage of the fall or rise transition times. From Figure 3, this would be less than 5 µs, or 1% of the signal time. Further examination of metal line widths and maximum output driver transistor currents revealed current densities well below those required for electro-migration to occur.

## 5. CONCLUSION:

Based on the data and results collected from the transition time experiments after high temperature dynamic burn-in following conclusions can be made:

a. Oscillations will occur on input buffers and subsequent internal logic modules when fall times are well beyond those allowed in Actel specifications.

b. Logic levels will most likely be disturbed, as signals will oscillate around the transition region of the particular input buffer and logic modules.

c. Average current levels are relatively low per I/O subjected to the lengthy fall times with approximately 125 μA per I/O measured for the 5.0 Volt Vcci application

d. No I/O or logic module in the burn-in test failed functionality.

e. Post Burn-in current levels remained the same as pre Burn-in.

f. Input leakage currents on I/Os with slow fall times are at the same levels as I/Os with no programming, (in the nA range) thus indicating no damage to the I/O circuitry.

g. Special purpose pins like TDI, TCK, TDO and TMS would show similar behavior as regular I/Os due to the input buffer structure being same.

h. Clock pins with slow rise and fall times are to be considered in subsequent testing of RTSX16 and RTSX32 parts.

i. EM concern was analyzed and for worse case operating conditions, a 20-year reliability is assured for the input buffer circuitry as well as the output driver circuitry.

j. Same analysis applies to RTSX32S product line.

*In conclusion, Actel "**guarantees Reliability"** of the RTSXS part for a 20 year period for the slow transition time issue on the I/O circuitry, but does **"Not guarantee functionality"** of the part if subjected to the above conditions. Actel will not change the datasheet, and recommends Designer's stay within the 10ns $T_r$ / $T_f$ specification.*

Please feel free to contact us if any clarifications or additional information is required.

Product Engineering
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*Appendix A*

*Figure 7 Hierarchical view of design*

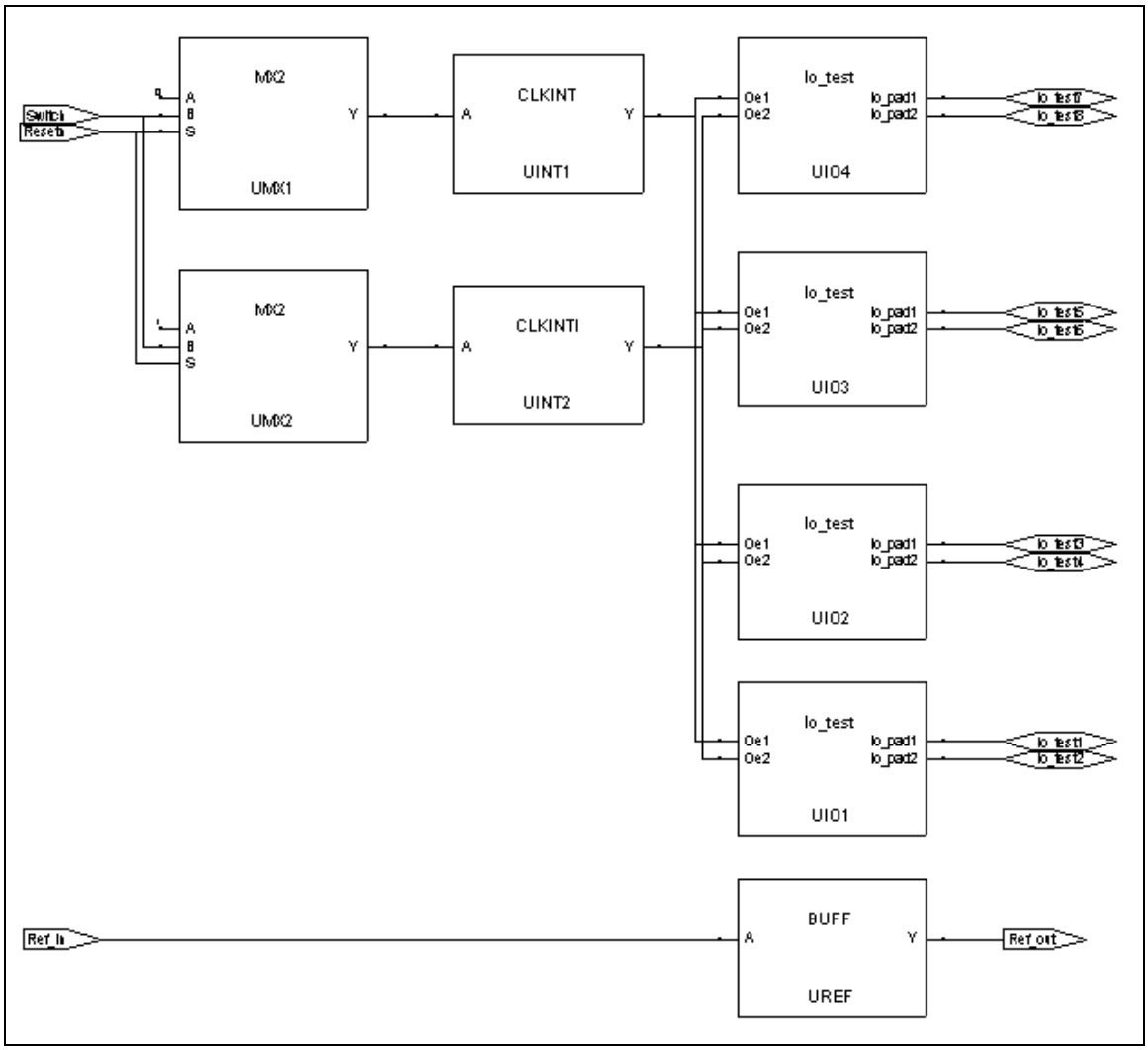


*Figure 8 Push in view of Io_test block from Figure 7 Hierarchical view of design*