Modifications of COTS FPGA Devices for Space Applications

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Abstract

A review of the ongoing efforts to improve the applicability of standard CMOS COTS devices to space environments. Discussions will center on specific design and processing techniques that will include methods of increasing total dose survivability levels and decreasing single event upset susceptibility. These concepts were guided by observations and measurements made on the Actel OTP FPGAs through seven process generations (2.0 um to 0.35 um). Both one-time and reprogrammable FPGA futures will be reviewed.

I. Introduction

This paper will review the history of radiation testing and subsequent design and process modifications used to improve the radiation performance of Actel FPGA devices. We will look at four key radiation parameters, Single Event Latchup (SEL), Single Event Dielectric Rupture (SEDR), Total Ionizing Dose (TID) and Single Event Upset (SEU). We will finish with a look at the future of RadHard and RadTolerant devices from Actel.

First, a brief history of Actel. The company was formed in 1986 and shipped the first commercial ACT 1 devices in 1989. The first devices qualified for military applications were shipped in 1990, and in 1991 the space community started taking a look at the Actel technology for radiation survivability. Several orders were placed with space level processing requirements with the intent to use these parts in space applications.

In 1992, the Jet Propulsion Laboratories (JPL) published a Compendium on the Actel A1020 device. The level of interest warranted more direct involvement from Actel and in 1993 we became directly involved in radiation testing and the effects of the Actel architecture on the responses. From 1992 on, Actel was shipping devices with increased screening levels for space and other high reliability applications.

In 1994, we attended our first Nuclear and Space Radiation Effects Conference (NSREC). Also in 1994, we signed an agreement with Lockheed-Martin Federal Systems (LMFS) to produce RadHard versions of the Actel devices. In 1996, we shipped the first RH1280 devices and added the RH1020 in 1997. In 1997, the HiRel Strategic Business Unit was formed to focus Actel's efforts in this market. In 1998 we have added Plastic QML certification and ISO9002 qualification and are working towards full QML certification by year end.

Over 16 different Actel products have been tested, from 2.0 um to 0.35 um technologies. The summary of these results can be found in the document titled "Radiation Performance of Actel Products" [1] found at:

http://www.actel.com/products/aero

Throughout this history, we have been learning more about radiation requirements and our products, been publishing papers and technical reports, and, most importantly, modifying our behaviors to respond to customer requirements.

II. Single Event Latchup

Single Event Latchup is one of the most basic requirements of any space qualified device. This becomes a Must Have by the user. If a device fails to survive this testing, it is generally unusable in space.

Most Actel devices are immune to SEL due to several factors. One of the reasons is that all Actel space level devices are produced on thin epi wafers, making the device less susceptible to latchup effects.

Many Actel devices include Guardrings in the logic circuits and Super-Guardrings in the areas near the high voltage circuitry used to program the devices and throughout the devices. Figures 1 and 2 show the structure of these Guardrings.

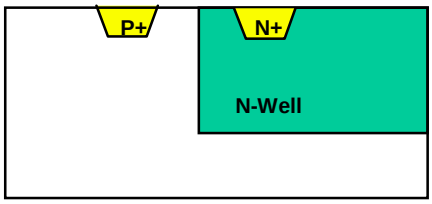


FIGURE 1: Guardring

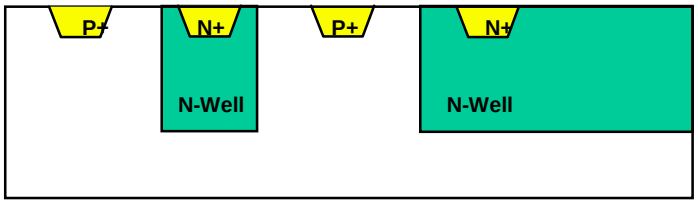


FIGURE 2: Super-Guardring in High Voltage

As an example, an experiment was held at Brookhaven National Laboratory on the RH1280 device using FIFO structures programmed into the FPGA. Test conditions were 4 MHz, 125°C, V_{DD} = 5.5V and there were 592 S-module bits and 270 C-module bits used. This test showed no latchup to an LET threshold > 125 MeV/cm^2-mg.

In order to save die size and cost, the commercial 3200DX devices with embedded dual port SRAM were introduced with the Guardrings removed. These devices then showed SEL at a LET threshold of 16 MeV/cm^2-mg. Other members of the commercial 3200DX family which did not have embedded SRAM are SEL immune.

A summary of SEL data taken on Actel devices can be found in [1].

Modified Behavior

As a result of these tests and observations, Actel now ensures that all products intended for the space level market include both an epi process and “tricks” such as Guardrings. These techniques apply to both the OTP and the reprogrammable technologies.

III. Single Event Dielectric Rupture

SEDR is a phenomenon found only in ground tests to date. Although the detailed mechanism and mathematical models are still under study, these findings did cause concern in the space radiation community. To address the concern, provisions to reduce SEDR were sought and implemented. These provisions are described briefly in the following paragraphs.

The ONO antifuse, patented by Actel, is a highly reliable one-time programmable connection. It can be used to provide high speed interconnect and allows the use of a fine-grained architecture. The antifuse gives predictable delays due to its predictable programmed impedance, offers very high utilization and a fully automatic layout.

The structure of the ONO antifuse is shown in Figure 3. The composition of the ONO antifuse is a Polysilicon/ONO/N++ structure with heavily As+ doped Poly and N++. The typical thickness of the ONO is around 86A, and this thickness is controlled by the CVD nitride. Good ONO quality is crucial to controlling the TDDB, the time to breakdown of the antifuse. The antifuses have very high resistance (>1 T ohm) in the off state and low resistance (300-600 ohm) in the on state.

SEDR can be caused when a heavy ion strike initiates the breakdown of a biased (non-programmed) ONO antifuse. After a SEDR, the antifuse is partially programmed with a resistance of 3-10K ohms or greater. This results in discrete and small increases in the supply current I_{DD}. Typically this is acceptable for the majority of missions, especially the shorter term missions and those closer to earth since the likelihood of high energy heavy ions is reduced.

The probability of an SEDR event is low and one rupture does not cause permanent damage to the device. Typically it would take at least 10

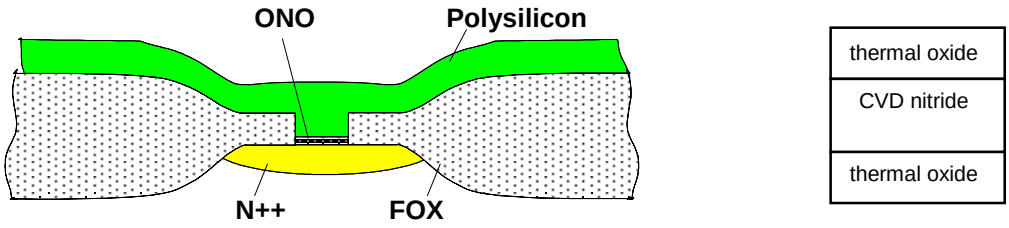


FIGURE 3: Actel ONO Antifuse Structure

ruptures to cause a functional failure, further reducing the probability of loss of functionality due to SEDR effects.

Modified Behavior

Several studies [2], [3], [4] have shown that there is a strong electric field dependence on the probability of an SEDR event. The Actel goal was to reduce the E-field strength to minimize the probability of an SEDR event.

This was accomplished by increasing the total thickness of the ONO structure. As mentioned earlier, the nominal thickness of Actel antifuses is 86A. By increasing this thickness to 93A for the RH1020 and 99A for the RH1280, Actel was able to increase the LET threshold to > 40 MeV-cm^2/mg.

Actel has recently introduced products (the SX family) using a Metal-to-Metal (M2M) antifuse. The structure of the M2M antifuse is shown in Figure 4. The M2M fuse offers lower impedance, higher speed and density, more routing resources and leads to smaller die sizes.

Actel has found a recipe for the M2M fuse that is immune to SEDR effects to a currently tested LET threshold of 80 MeV-cm^2/mg.

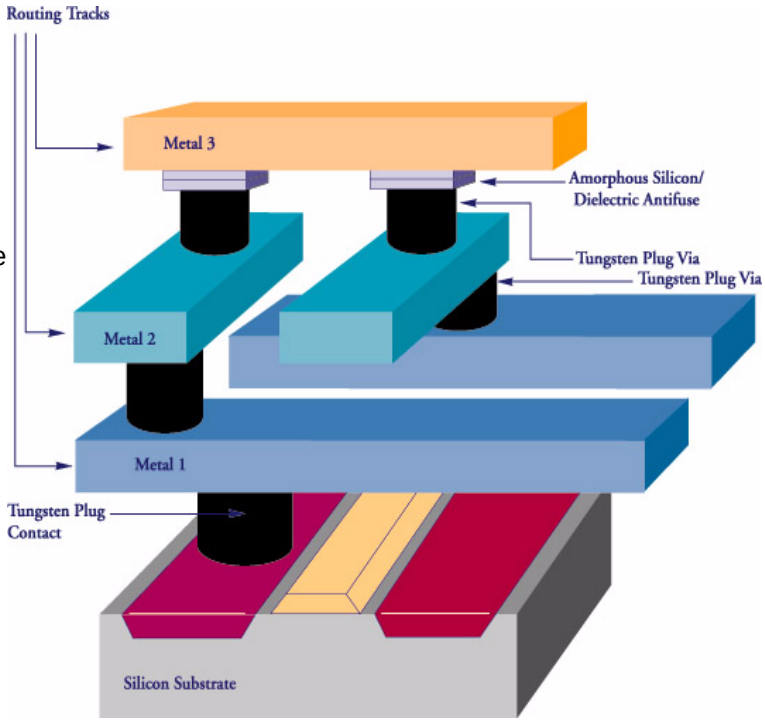


FIGURE 4: Actel ONO Antifuse Structure

IV. Total Ionizing Dose

The first device type that was tested for Total Dose survivability was the A1020 2.0 um from the Matsushita (MEC) fabrication facility. We found results to be in the range of 50-100K rads (Si) [1], and the A1020A 1.2 um device showed similar results. Other fabrication facilities such as Texas Instruments showed a much lower level for these device types. When we introduced the 1.2 um A1280 and 1.0 um A1280A, the test data showed much lower numbers from MEC, in the range of 5-10K rads [1]. We undertook a study to understand why there was this large difference from A1020 to A1280A.

We discovered that the major reason for the reduced TID performance was due to the Charge Pump (CP) circuitry [6]. The methodology to study and understand this phenomenon included measuring the transistor I(V)s both pre- and post-radiation, creating Spice models and simulating the CP circuitry, and micro-probing the CP circuits. We then correlated these results with the CP design and transistor parameters to fully understand the characteristics of the Charge Pump.

We did determine that the performance of the Charge Pump directly affected the TID performance.

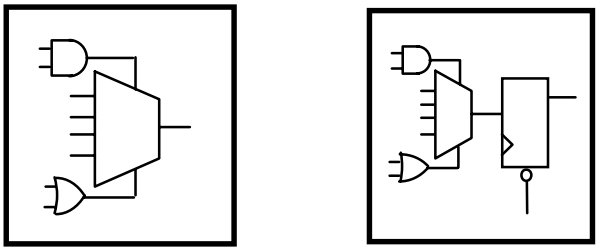
Modified Behavior

There were two methods taken to respond to the increased knowledge gained in our studies of total dose radiation on our FPGAs.

First we used a straight forward method which was to transfer the 1280 and 1020 device types into a RadHard fab. The deal with LMFS allowed us to offer guaranteed 300K rad TID performance for both of these products.

Our investigation of the Charge Pump circuitry and its effect on TID performance allowed us to learn a great deal about the techniques necessary to improve the TID performance of devices from a commercial fabrication facility.

We then proceeded to characterize all products and processes with a special focus on the M2M



Combinatorial **Sequential**

FIGURE 5: Actel Logic Modules

process and the new SX devices. We have obtained results to 100K rads (Si) (I_{DD}) for these products and now understand how to control certain processing parameters to target improved TID performance. We expect to regularly achieve results in the ≥ 100K rad (I_{DD}) and ≥ 240K rad (functional) range, from a commercial foundry.

V. Single Event Upset

Single Event Upset results were not improved with the transfer of the 1020 and 1280 to the RadHard facility at LMFS. The processes that improve the TID performance do not affect the SEU results.

First, some background on the architecture of Actel devices. All antifuse devices except ACT 1 and the new SX family include two types of logic modules, Combinatorial (C-modules) and Sequential (S-modules). These modules are shown in Figure 5. This module design is very synthesis friendly since the simple structure is easy to synthesize, and the 4:1 MUX is the basis for CASE statements. Also, this architecture leads to highly efficient designs and little of the available logic is wasted.

Through repeated testing we have discovered that the SEU rates and LET thresholds vary depending on the type of module used. Table 1 shows the results for three types of flip-flops: 1) FFs created by using the sequential portion of the S-module (S FFs); 2) FFs created by using two C-modules (C-C FFs); and 3) FFs created by using the combinatorial portion of the S-modules (Modified S or MS FFs).

Device	FF Type	LET th MeV-cm^2/mg	X-section cm^2/bit
RH1280	S FFs	4	3.2×10^{-6}
RH1280	C-C FFs	17	1.1×10^{-6}
RH1280	MS FFs	26	5.1×10^{-6}

TABLE 1. SEU Results

Heavy ion testing was performed at BNL and proton testing at Harvard. The test methodology used was a FIFO test structure with 592 S-module bits, 270 C-module bits and 270 modified S-module bits. The bit pattern used was Checkerboard/Checkerboard bar. Test condition were V_{DD} = 4.5V, T_A = 40°C, 80°C and 125°C, Clock rate = 4 MHz with 20% and 50% duty cycles. This testing helped us to develop device/circuit models for the SEU effects on Actel FPGAs.

Modified Behavior

There were two distinct changes that we made to address the SEU issues with our devices. First, we focused on software support for the current products to help customers obtain improved SEU rates. Second, we implemented design changes to improve the performance in silicon.

Actel Designer software now supports designs in three modes – Default, Combinatorial and Triple Voting. Default uses the S-modules freely when implementing flip-flops. Combinatorial uses only C-C and modified S modules. Triple Voting implements Triple Modular Redundancy for all flip-flop implementations. In addition, tools from Synopsys and Synplicity now support all three of the design methodologies.

When we designed the new SX family we changed the architecture to separate the flip-flops from the combinatorial portion of the circuitry. This new sequential element is designated as an R-cell. This change has resulted in better LET thresholds for the current SX device, typically in the 11-12 MeV-cm^2/mg. We are in the midst of an enhancement process on the SX family to increase the LET threshold to > 37 MeV-cm^2/mg.

VI. The Future

Actel continues to learn more about the radiation characteristics of the space environments and its effects on our FPGA products. Current efforts include more studies of the effect of clock and logic upsets on logic circuits [7], the improvement of software tools to enable synthesis design support [8] and the ongoing redesign of the SX family for improved SEU performance [9]. Also, Actel will soon be undertaking radiation testing on two new families: an SRAM-based reprogrammable family and a flash-based non-volatile reprogrammable family. Results on these two new families can be expected in 1999.

Acknowledgements

The authors thank the ongoing efforts of many commercial, civilian and military organizations for their continued interest in Actel products and their applicability in space. The test results provided from many sources have been invaluable in our ongoing efforts to understand the radiation effects on our devices and has given us the knowledge to address these issues.

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