Product Update

Revision Date: September 20, 1999

JTAG Issues and the Use of RT54SX Devices

BACKGROUND

The attached paper authored by Richard B. Katz of NASA GSFC and J. J. Wang of Actel describes anomalies observed in the JTAG circuitry in the RTSX16 FPGA during heavy ion testing. These tests are performed on the first device type noted, the RT54SX16-CQ256BXB45.

RESPONSE

In response to these results, Actel has produced two new versions of this device type that include a TRST pin which will eliminate the problem by allowing the user to asynchronously hold the JTAG TAP controller in the benign TEST-LOGIC-RESET state.

DEVICE SUMMARY

Revision No.	Part Number(s)	TRST Pin Status
Revision 0	RT54SX16-CQ256BXB45	no TRST pin, internal POR
	RT54SX16-CQ208BXB45	no TRST pin, internal POR

NOTE: The Revision 0 devices can experience TAP controller upsets, although the probability is low. These devices will be offered at a discount off the Rev. 1 pricing. All designs and timing are the same as the Rev. 1 devices, and the user can trade off the price advantage versus the minimal risk of JTAG upsets.

Revision 1	RT54SX16-CQ256B	external TRST pin, no internal POR
	RT54SX16-CQ208B	external TRST pin, no internal POR
	RT54SX32-CQ256B	external TRST pin, no internal POR
	RT54SX32-CQ208B	external TRST pin, no internal POR

NOTE: The Revision 1 devices will not experience TAP controller upsets if the TRST pin is grounded. These devices are the standard product offering.

Revision 2	RT54SX32S-CQ256B	external TRST pin and internal POR
	RT54SX32S-CQ208B	external TRST pin and internal POR
	RT54SX72S-CQ256B	external TRST pin and internal POR
	RT54SX72S-CQ208B	external TRST pin and internal POR

NOTE: The Revision 2 devices will not experience TAP controller upsets if the TRST pin is grounded. Rev. 2 devices are an upgraded version of the RT54SX family and will include several new features including 5V CMOS drive capability, 3.3V and 5V PCI compliance and SEU LET threshold of > 37 MeV-cm^2/mg.

PIN COMPATIBILITY

All device types shown above will be pin-for-pin compatible - the only exception is that the Revision 0 devices do not have a TRST pin (Pin #34 on the CQ256 and Pin #30 on the CQ208). This will not change the placement or routing of the design and all designs can be easily interchanged between revisions.

AVAILABILITY

Availability dates for each of the three revisions are shown below. This is the currently planned availability as of September 20, 1999. These dates are approximate and are subject to change based on a number of factors, including completion of qualification and normal production lead times. Please contact your local Actel salesperson for the most up to date information on availability.

Revision No.	Part Number(s)	Expected Qualification Dates
Revision 0	RT54SX16-CQ256BXB45	Done
	RT54SX16-CQ208BXB45	Done
Revision 1	RT54SX16-CQ256B	Q4 1999
	RT54SX16-CQ208B	Q4 1999
	RT54SX32-CQ256B	Q4 1999
	RT54SX32-CQ208B	Q4 1999
Revision 2	RT54SX32S-CQ256B	Q3 2000
	RT54SX32S-CQ208B	Q3 2000
	RT54SX72S-CQ256B	Q1 2001
	RT54SX72S-CQ208B	Q1 2001

TECHNICAL SUMMARY - Revisions 1 and 2

Users of the Revision 1 and Revision 2 devices do not have to concern themselves with the JTAG TAP controller upset as long as the TRST pin is grounded on their flight boards. This will ensure that the TAP controller cannot be upset.

TECHNICAL SUMMARY - Revision 0

Users of the Revision 0 parts in a space environment will want to take measures outlined in this paper to hold the JTAG TAP controller in the TEST-LOGIC-RESET state. This is accomplished at the system level by holding the JTAG TMS pin high while applying a clock pulse to the JTAG TCK pin. Heavy ion testing in this mode of operation show that, while the anomalies can still occur, they cause no permanent damage to the part and are cleared within 5 pulses on TCK.

Table 1 lists the JTAG SEU effect for two product revisions available by Actel. The shaded boxes are the recommended designs if SEU is an issue.

Table 1

Product Revision	**4 Pin JTAG[1]**		**5 Pin JTAG[2]**	
	Reset for SEU[3]	**Not Reset**	**Reset for SEU[4]**	**Not Reset**
Rev 0	Global data soft error until reset, no high static current[5]	Functional failure, high static current	No such option	No such option
Rev 1	No such option	No such option	No SEU effect	Functional failure, high static current

[1]The 4 JTAG pins are TMS, TCK, TDI and TDO.
[2]The 5 JTAG pins are TMS, TCK, TDI, TDO and TRST.
[3]Set TMS = *High*, and TCK = Free running clock. Should use as high clock frequency as possible to reduce the transient period (5 clock cycles), however, 1MHz is believed sufficient.
[4]Set TRST = *Low*.
[5]Since the upset is global, chip-level redundancy such as TMR (Triple Module Redundancy) design is limited by the JTAG SEU rate.

Testing using 195 MeV protons did not detect any JTAG upsets up to a fluence of 4E12 protons/cm^2, showing that it is proton insensitive.

The rate of occurrence of on-orbit anomalies is conservatively calculated from the measured JTAG cross-section, 3E-7 cm^2/device, and the LET threshold of 18 MeV-cm^2/mg.

Orbit (with 100 Mil AL shielding)	Upset Rate (upsets/device-day)
GEO	1.44E-7
Teledesic	4.77E-8

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USING IEEE 1149.1 JTAG CIRCUITRY IN ACTEL SX DEVICES

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1.0 BACKGROUND AND SUMMARY

This report summarizes the use of the JTAG 1149.1 circuitry in SX devices. JTAG circuitry was originally designed to standardize testing of boards via a simple control port interface electrically without having to use devices such as a bed of nails tester. JTAG is also used for other functions such as executing built-in-test sequences, identifying devices, or, through custom instructions, other functions designed in by the chip designer. The JTAG circuitry is designed for test only; it has no functional use in the integrated circuit during normal operations.

The JTAG circuitry and the mode of the device is controlled by a circuit block known as the 'TAP Controller,' which is a sixteen-state state machine along with various registers. The controller is normally in an operational state known as TEST-LOGIC-RESET. In this state, the device is held in a fully functional, operational mode. However, a Single Event Upset (SEU) may remove the TAP Controller from this state, causing a loss of control of the integrated circuit, unless certain precautions are taken, such as grounding the optional JTAG TRST signal.

This application note covers three devices:

RT54SX16-CQ256BXB45	no TRST signal implemented, internal POR
RT54SX16-CQ256B	external TRST, no internal POR
RT54SX16S-CQ256B	external TRST and internal POR

Each of these three devices must be treated in a unique fashion and understood for proper application.

2.0 IEEE 1149.1 JTAG

2.1 REVIEW OF THE SPECIFICATION AND EFFECTS

The JTAG specification is defined by the IEEE in Reference 1; a good introduction is given in Reference 2. Refer to the specification for a more detailed explanation and further background. An overview of the test concept is shown in Figure 1, where the core logic of the device is surrounded by a set of scan cells.

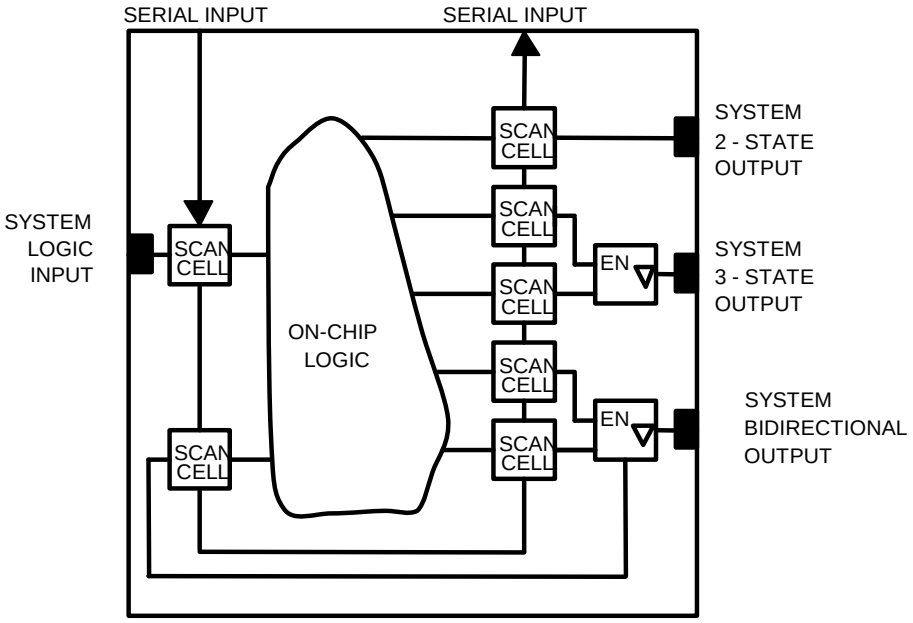

Figure 1: An Overview of the JTAG Scan Path

Each of the scan cells is linked into a shift register and multiple devices on a board are linked together in a serial fashion. A scan cell is shown in Figure 2.

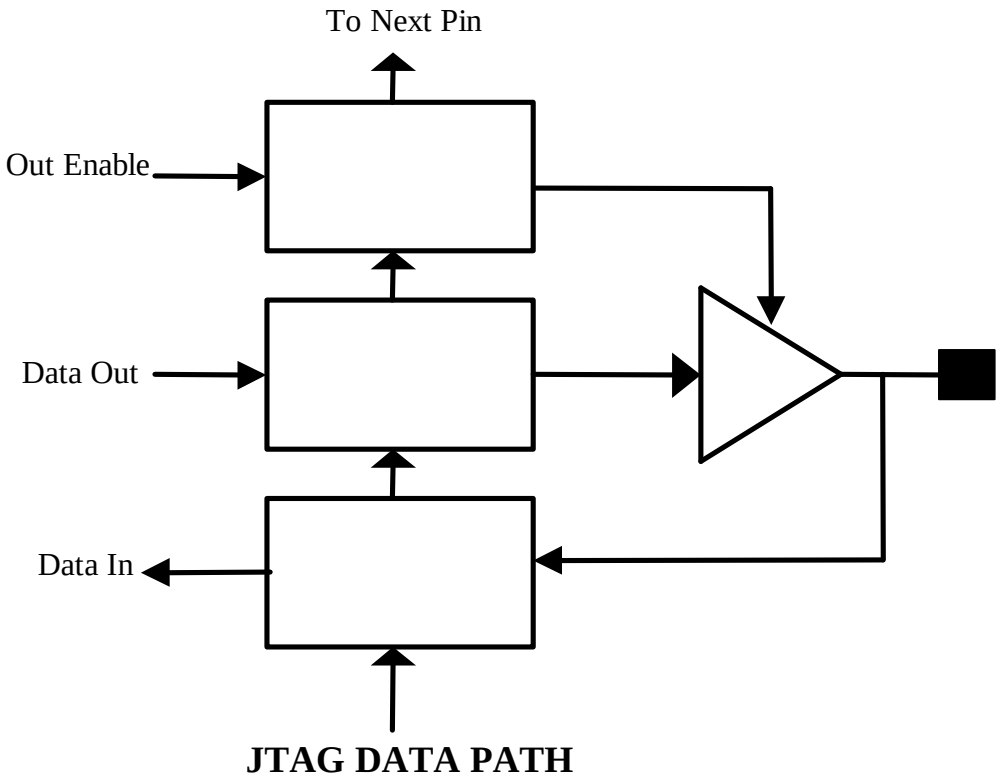

Figure 2. JTAG Scan Cell

Depending on the configuration of the chip and the values in the shift registers, the device I/O's can either function normally or provide a variety of test functions. Examples include sampling external data from the board and 'capturing' it, driving test equipment specified values onto the board, or placing specific values into the core circuitry for test. Other possibilities include capturing a device's outputs, reading special registers, programming, or other device specific functions.

Many problems can arise from a loss of control of the JTAG circuitry. For example, FPGA device inputs can be turned into outputs causing driver contention, board inputs can be blocked isolating the device core, various internal device resources can be configured improperly, etc.

The TAP Controller controls the chip mode as well as shifting data into various registers. The most important register is the Instruction Register, which consists of two halves. One half is for shifting in new data and the other is for latching the new command, shown in Figure 3.

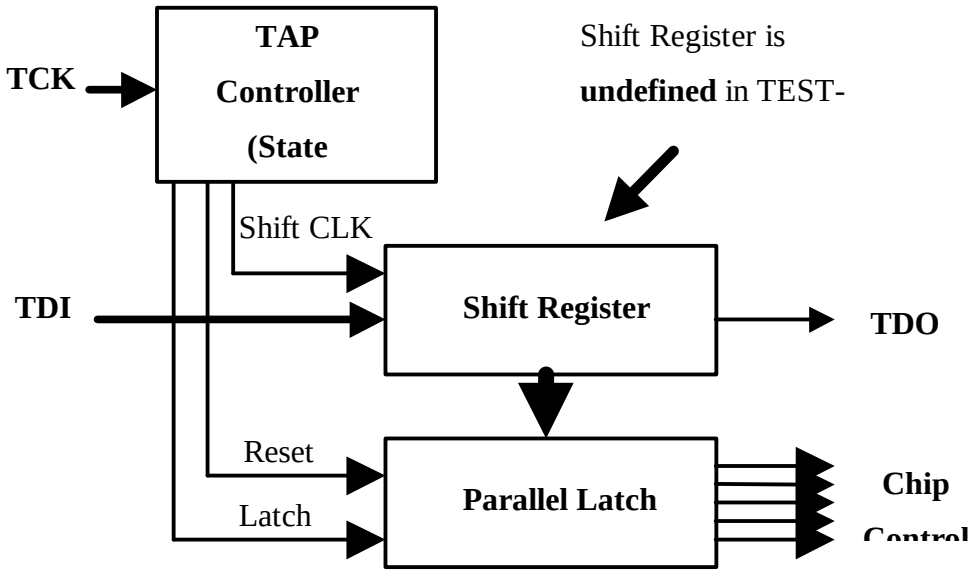

Figure 3: TAP Controller and Instruction Register

As shown in Figure 3, the instruction register is loaded from TDI (test data input) and is latched under command from the TAP Controller. When the TAP Controller is in the TEST-LOGIC-RESET state, the parallel latch, whose outputs control the chip, is asynchronously held in an operational state independent of values stored in other data registers. This is similar to grounding the MODE pin in the Actel ACT 1, ACT 2 and ACT 3 families.

It is critical to note that the state of the shift register is undefined in many of the TAP Controller states and is not controlled by Reset. The contents of the shift register can be random values from the power-on condition or may be altered by SEUs. If the TAP Controller passes through the IR-Update (instruction register update) state, then the contents of the shift register will be jam loaded into the parallel latch with generally unpredictable results.

A brief examination of the operation of the TAP Controller's state machine shows the effects of radiation on this circuitry and how the effects can be mitigated. Three signals control the TAP Controller: TMS (test mode select), TCK (test clock), and TRST (test reset), with the last signal being optional. The state machine is shown in Figure 4.

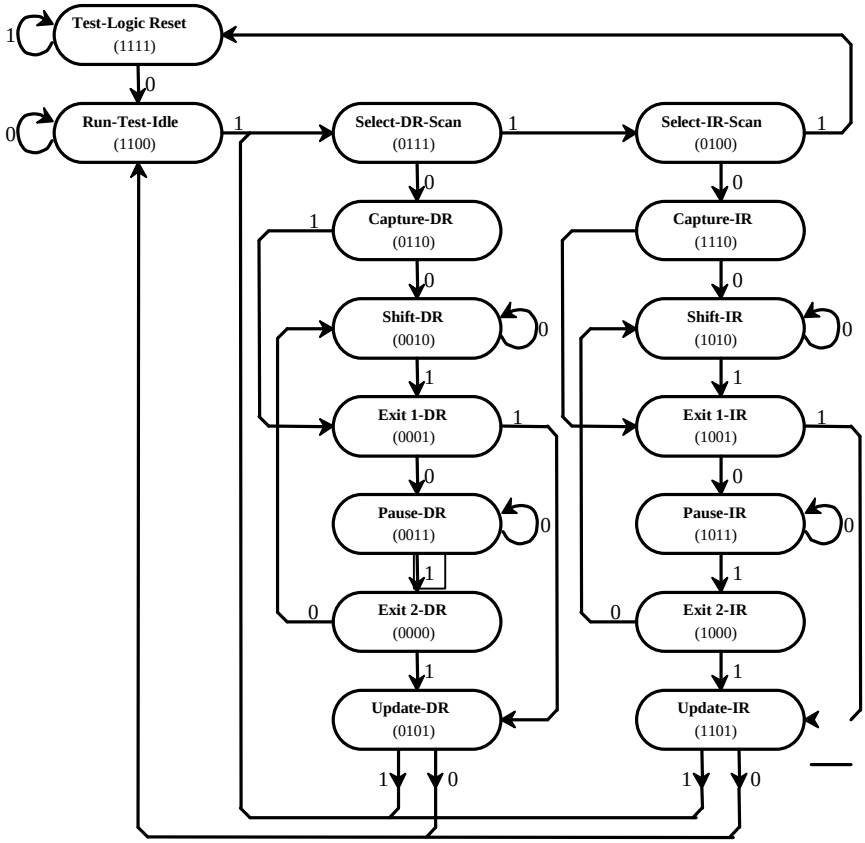

Figure 4:TAP Controller State Diagram

The value of TMS is shown on the state transitions. The state machine will return to the TEST-LOGIC-RESET state in no more than five clock cycles if TMS is held high, the normal configuration. There are two other ways of entering or maintaining the TEST-LOGIC-RESET state. The first is by holding the TRST signal to ground. The second is by a power-on-reset signal derived in the integrated circuit. Both of these two mechanisms may or may not be present. If both of these signals are present, then they are logically OR'd. Different members of the SX family of devices have different configurations. The TAP Controller in the SX family can not be disabled.

As shown in Figure 4, the TAP Controller is quite robust to *expected* faults. For example, an indefinite short to ground on TMS and then removal does not alter the state of the chip. However, with this state encoding, a single bit fault, from an event such as an SEU, can cause the TAP Controller to move from the TEST-LOGIC-RESET state through the following set of transitions: TEST-LOGIC-RESET → CAPTURE-IR → EXIT-1-IR → UPDATE-IR → SELECT-DR-SCAN → SELECT-IR-SCAN → TEST-LOGIC-RESET. When the TAP Controller passes through the UPDATE-IR state, the Instruction Register latches the contents of the shift register, whose contents are not controlled, changing the chip's mode.

Data taken during heavy ion testing shows some examples of device configuration errors. Figure 5 shows the device shutting down, with the inputs effectively disabled and the device drawing static power. Figure 6 shows the device drawing large currents; in some runs, currents exceeding 800 mA were observed.

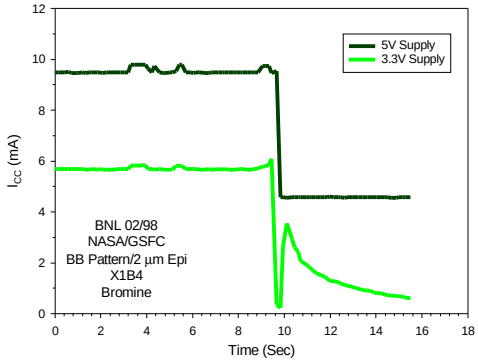

Figure 5: SX Prototype 'Shutting Down' During Heavy Ion Test

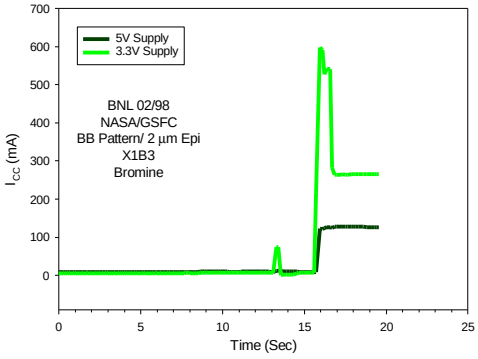

Figure 6: SX Prototype Showing a High Current Mode During Heavy Ion Test

3.0 DESIGN RECOMMENDATIONS

3.1 GENERAL RECOMMENDATIONS AND OVERVIEW

There are three devices currently planned for the RTSX series. For the SX16 they are summarized, with respect to JTAG, as follows:

1. RT54SX16-CQ256BXB45 no TRST signal implemented, internal POR
2. RT54SX16-CQ256B external TRST, no internal POR
3. RT54SX16S-CQ256B external TRST and internal POR

Each of these configurations needs to be understood for proper operation of the device. As a general note, the SX series may have the JTAG inputs disabled (normal I/O operation) or enabled, if they have JTAG functionality. The JTAG functionality cab be controlled by the 'P-Fuse' and should be programmed for the JTAG inputs to be active and the mitigation techniques here to function properly. After programming and installation on the board, the device's configuration can be verified by the presence of an internal pull-up resistor of approximately 10 kΩ on the TMS pin when in JTAG mode. By grounding this pin, an appropriate increase in I_{CC} should be observed.

3.2 RT54SX16-CQ256BXB45

In this model, the TRST signal is not implemented and the TAP Controller is initialized and sent to the TEST-LOGIC-RESET state when power is applied by an internal Power-On-Reset circuit. The power supply must rise within the specified time and with an appropriate waveform. Since the TAP Controller can be upset, the TCK pin should be connected to a free running clock (up to 20 MHz) and the TMS pin held high. This will minimize the time that the device's configuration is in error.

Heavy ion test data, while not a guarantee, shows the device losing configuration and then returning to an operational state. Figure 7 shows jumps in the error counters when the TAP Controller is upset by a heavy ion. The JTAG cross-section, while not yet accurately measured, is relatively small, on the order of 10^{-6} cm^2/device, making the probability of a failure on-orbit low, but not zero.

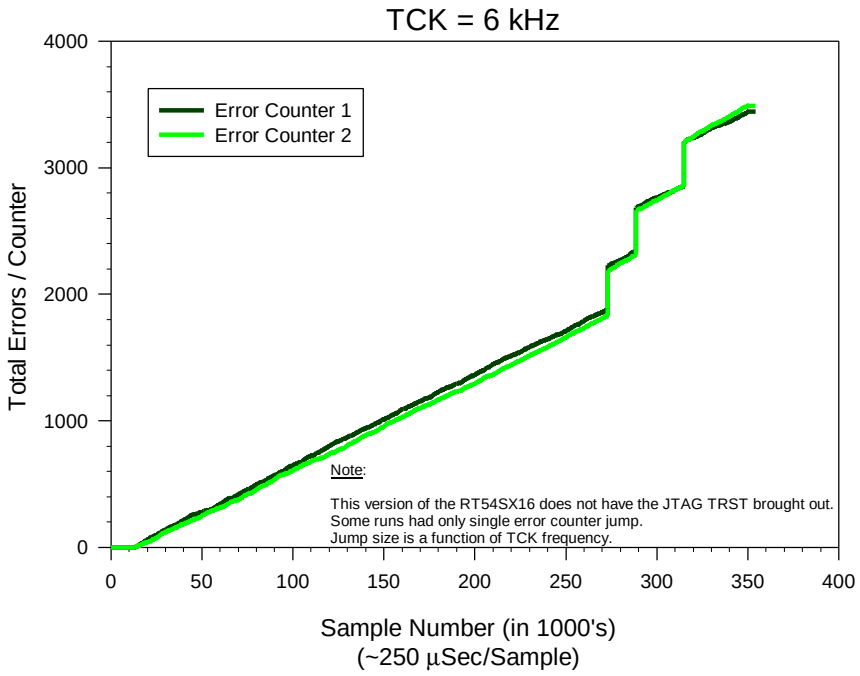

Figure 7: JTAG Upset and Recovery with Heavy Ions at TCK = 6 kHz

3.3 RT54SX16-CQ256B

In this model, there is an external TRST pin but no internal POR signal. The TRST pin must be grounded and verified prior to the application of power to the device, otherwise the device can be powered in an illegal configuration. Large currents can be drawn in an illegal configuration, exceeding 800 mA, with an unknown impact to device reliability. Properly configured, this device is immune to any JTAG upsets, because the TAP Controller is held directly in the TEST-LOGIC-RESET state.

Verifying that the TRST pin is grounded is extremely important. The JTAG 1149.1 specification requires that an unconnected TRST be pulled high, preventing the TAP Controller from being reset.

3.4 RT54SX16S-CQ256B

In this model, there is both an external TRST pin and an internal POR signal. This permits both an SEU-hard TAP Controller for flight and worry-free use of the JTAG port for ground test. The device will, independent of the state of the TRST pin, power up into an operational configuration. If TRST is held high during power-up, a proper V_{CC} rise time and waveform is required. JTAG test equipment can be connected to the device for functions such as observing internal nets.

For flight, verifying that the TRST pin is grounded is extremely important. In this configuration, this device is immune to any JTAG upsets in flight, because the TAP Controller is held directly in the TEST-LOGIC-RESET state.

4.0 REFERENCES

1. **IEEE Standard Test Access Port and Boundary-Scan Architecture,** IEEE Std. 1149.1-1990 (Includes IEEE Std 1149.1a-1993), IEEE, October 21, 1993.
2. **Scan Tutorial Handbook Volume I**, National Semiconductor and Teradyne, 1994 Edition.

5.0 Acknowledgements

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