MultiView Navigator v9.1 User's Guide

NetList Viewer, PinEditor, I/O Attribute Editor, ChipPlanner

Actel®
POWER MATTERS

Actel Corporation, Mountain View, CA 94043

Printed in the United States of America

Part Number: 5-02-0003-17

Release: November 2010

Trademarks

Table of Contents

Overview 9

Getting Started 10
Starting MultiView Navigator 11
Components of the MultiView Navigator Interface 12

Hierarchy Window 13
Overview of Hierarchy Window 14
Floating and Docking Windows 17
Selecting Objects 18
Highlighting and Unhighlighting Objects 19
Changing the Highlight Color 21
Finding Objects 22
Using the Prelayout Checker 30
Using the Global Checker 31
Using the Global Planner 32
Flash*Freeze Pins 34
Reserving Pins for Device Migration 35
Committing Changes in MVN 37

NetlistViewer 38
Starting NetlistViewer in MultiView Navigator 39
Displaying Your Netlist 40
Bundling Nets 41
Navigating Through Your Netlist 42
Selecting Objects in NetlistViewer (MVN) 50
Identifying Paths 51
What is a Logical Cone? 55
Creating a Logical Cone 56
Changing the Name of a Cone 58
Deleting a Logical Cone 59
Setting the Active Cone 60
Hiding Logic in a Hierarchical Instance 61
Displaying Logic Hidden Within a Hierarchical Instance 62
Adding Selected Objects to a Cone 63
Adding a Group of Highlighted Objects to a Cone 64
Clearing All Objects from a Cone 65
Removing Selected Objects from a Cone 66

Removing a Group of Highlighted Objects from a Cone 67
Adding Drivers to a Cone 68
Adding Driven Instances to a Cone 69
Adding Adjacent Objects to a Cone 70
Cross-probing Between NetlistViewer and ChipPlanner 71
Cross-probing Between NetlistViewer and SmartTime 73
Viewing Buffers 77

PinEditor 78
About PinEditor in MultiView Navigator 79
Starting PinEditor in MultiView Navigator (MVN) 80
Colors and Symbols 81
Assigning Pins 82
Unassigning Pins 83
Locking and Unlocking Pin Assignments 84
Closing and Committing Pin Assignments 85
Setting PinEditor Properties 86
Changing an Object's Color 87
Editing I/O Attributes 89

I/O Attribute Editor 90
About I/O Attribute Editor 91
Starting I/O Attribute Editor 92
Assigning pins in Package Pins View 93
Editing I/O Attributes 94
Editing Multiple Rows 95
Sorting Attributes 96
Formatting Rows and Columns 97
Specifying an I/O Standard 98
Common I/O Attributes (All Families) 99
I/O Attributes by Family (in MVN) 100

ChipPlanner 102
About ChipPlanner in MultiView Navigator 103
Starting ChipPlanner 104
Colors and Symbols 105
Setting ChipPlanner Properties 107
Changing Colors 108

Floorplanning 110
About Floorplanning 111
About Regions 112
Creating Regions 114

Using Empty Regions 116
Using Logic Regions 117
Using Local Clock and Quadrant Clock Regions 118
Editing Regions 119
Assigning a Macro to a Region 121
Assigning a Net to a Region 123
Unassigning a Macro from a Region 125
Creating Local Clock Regions 126
Renaming a Local Clock Region 128
About Quadrant Clocks 129
Creating Quadrant Clock Regions 131
Assigning a Clock to a QuadrantClock Region 132
Locking Quadrant Clock Regions 134
Assigning Logic to Locations 135
Unassigning All Logic from a Location 136
Moving Logic to Other Locations 137
Locking Logic to Locations 138

Block Ports 139
About Block Ports 140
Selecting Connected Ports 142

Viewing Resources 143
Ratsnest View 144
Route View 145
Clusters and Super Clusters 147
Cross-probing between ChipPlanner and SmartTime 148

Using I/O Banks 151
About I/O Banks 152
Support for VREF I/Os 155
Specifying Technologies for an I/O Bank 156
Automatically Assigning Technologies to I/O Banks 157
Manually Assigning Technologies to I/O Banks 158
Assigning Pins in IGLOOe, Fusion, ProASIC3L, and ProASIC3E 162
Assigning VREF Pins 163
Displaying Pins in a VREF Range 165

Using Active Lists 166
What are Active Lists? 167
Displaying Active Lists 169
Creating Active Lists 170
Copying Active Lists 175

Editing Active Lists 176
Deleting Active Lists 177

Reference 178
Tools Window 179
World Window 180
Log Window 181
Message Bar 182
Status Bar 183

Hierarchy Window 184
Overview of Hierarchy Window 185
Logical Tab 188
Physical Tab 189
Ports Tab 190
Nets Tab 191
Regions Tab 192
Logical Cones Tab 193
Block Tab 194

Menus, Toolbar Buttons, and Shortcut Keys 195
Command Overview 196
File Menu 197
Edit Menu 198
View Menu 200
Logic Menu 201
Nets Menu 202
Region Menu 203
Package Menu 204
Schematic Menu 205
LogicalCone Menu 206
Format Menu 207
Tools Menu 208
Window Menu 209
Help Menu 210

Dialog Boxes 211
Assign Instances to Regions Dialog Box 212
Assign Nets to Regions Dialog Box 214
ChipPlanner Properties Dialog Box 216
Create or Edit Active Lists Dialog Box 217
I/O Bank Settings Dialog Box (IGLOO and ProASIC3 only) 219
I/O Bank Settings Dialog Box 220

More I/O Bank Attributes Dialog Box 221
Logic Instance Properties Dialog Box 222
More Active Lists Dialog Box 223
Net Properties Dialog Box 224
Path Properties Dialog Box 225
Block Port Properties Dialog Box 226
PinEditor Properties Dialog Box 227
Pin List Dialog Box 228
Region Properties Dialog Box 229
Reserve Pins for Migration Dialog Box 231
Routing Details Dialog Box 232
Designer Block Properties Dialog Box 233

Product Support 235

Overview

MultiView Navigator is the physical design viewing and editing interface for the IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, Axcelerator, SX-A, and eX families. With this interface, you can view, edit, and floorplan your design in many different views. Its four tools also include powerful find and undo/redo features as well as cross-probing features:

- NetlistViewer generates a schematic view of your design.
- PinEditor displays a view of the I/O macros assigned to the pins in your design.
- I/O Attribute Editor displays a table of the I/O attributes in your design.
- ChipPlanner displays a view of the I/O and logic macros in your design.

You can view your design in all of these tools at the same time. From within MultiView Navigator, simply select a tool from the Tools menu, or click its toolbar button.

Note: Note: The MultiView Navigator tools also work with SmartTime and SmartPower.

See Also

Starting MultiView Navigator

About NetlistViewer in MultiView Navigator

About PinEditor in MultiView Navigator

About I/O Attribute Editor

About ChipPlanner

Getting Started

Starting MultiView Navigator

You must compile your design before using NetlistViewer, ChipPlanner, PinEditor, or I/O Attribute Editor in MultiView Navigator.

To start MultiView Navigator from Designer:

1. Compile your design.
2. Click one of the following tools: **NetlistViewer**, **PinEditor**, **ChipPlanner**, or **I/O Attribute Editor**. If you have not compiled your design, Designer compiles it for you before opening your selected tool.

MultiView Navigator reads your design and opens it in the tool you selected.

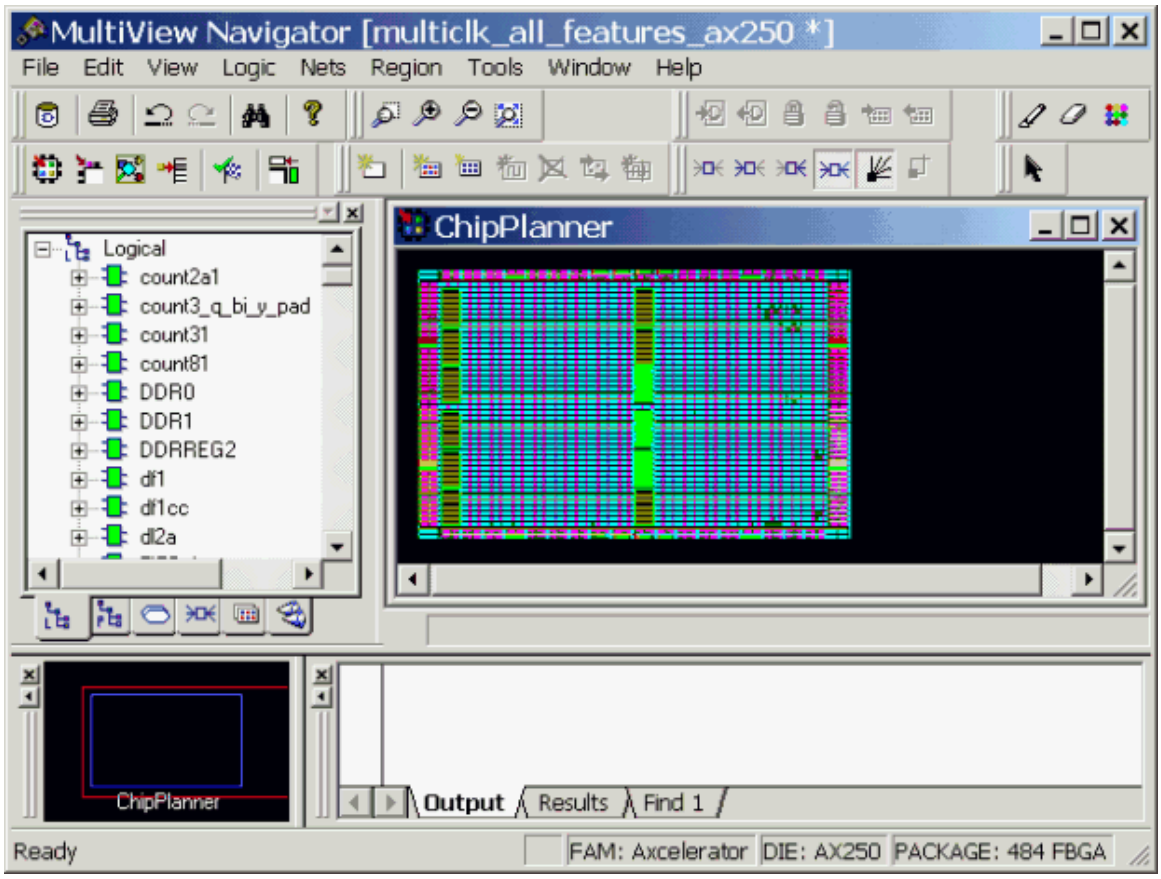


Figure 1 · ChipPlanner in MultiView Navigator

Components of the MultiView Navigator Interface

The MultiView Navigator interface is divided into four windows:

In addition, this interface includes a menu bar, toolbar buttons, a message bar, and a status bar.

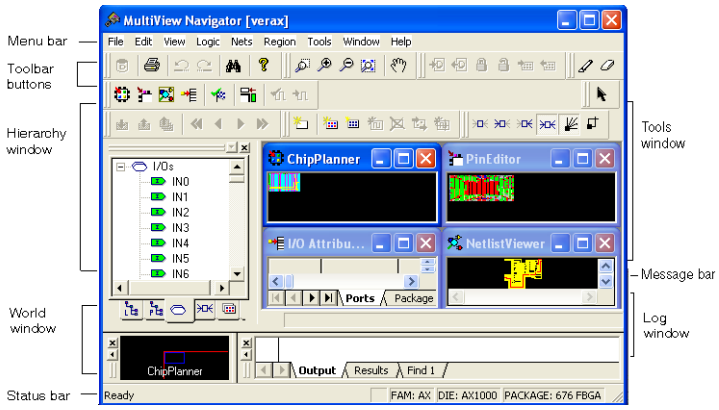


Figure 2 · MultiView Navigator Interface

Use the menus or toolbar buttons to initiate commands.

See Also

Tools Window

World Window

Log Window

Message Bar

Status Bar

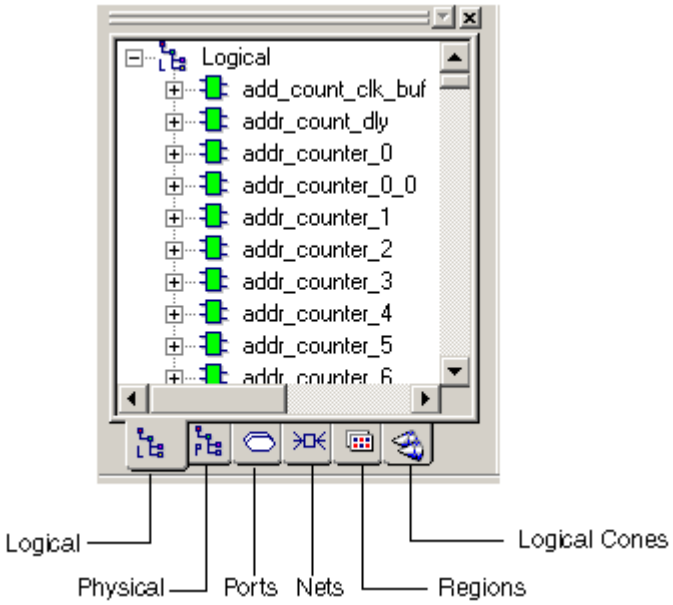
Overview of the Hierarchy Window

Hierarchy Window

Overview of Hierarchy Window

The Hierarchy window (as shown in the figure below) provides easy navigation through the Hierarchy. The Logical tab in this window provides a hierarchical overview of the design.

Click the tabs at the bottom of this window to view macros, instances, ports, nets, regions, and logical cones in your design. Additionally, a Block tab will appear in the Hierarchy window if the design contains Blocks.



Hierarchy Window

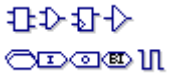
You can use these tabs to explore each level of the hierarchy and to trace signals. You use the Hierarchy window tabs with ChipPlanner, NetlistViewer, PinEditor, and I/O Attribute Editor to help identify critical paths.

Tip: Tip: Right-click an object to use its context-sensitive menu.

In all Hierarchy views, you can right-click an object, and select **Properties** to display its properties.

Each view contains color-coded icons to indicate its logic type and state. These icons are explained in the following table:

Table 1 · Icons in Hierarchy View

Icon	Color	What it Represents
	White	The logic or I/O is unassigned.
	Green	The logic or I/O is assigned.

Icon	Color	What it Represents
	Hashed green	Some instances in the block of logic are assigned.
	Red and blue grid	The region is either inclusive or LocalClock.
	Blue grid	The region is exclusive.
	White	The region is empty.
	Black icon	The logic is handled as one unit and cannot be expanded. This icon appears next to the ARM core logic.
	Cone icon	The object is a Logical Cone.
	Blue checkmark	The logic is assigned to a region.
	Gray checkmark	Some instances in the block of logic are assigned to a region.
	Blue lock	The entire block of assigned logic is locked to a location.
	Gray lock	Some instances in the block of assigned logic are locked to a location.
	Yellow cube	Indicates a block flow.
	Blue	Indicates this macro, net, or port only exists in the pre-optimized view.

The Logical tab shown below illustrates that the selected logic is assigned to a region and locked. Only the Logical tab shows the logical hierarchy of the design. The Physical tab shows the physical hierarchy. The other tabs are not hierarchical.

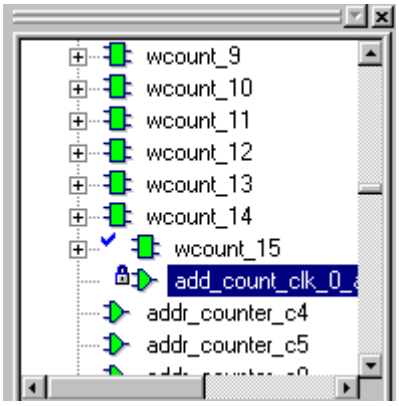


Figure 3 · Logical Tab - Checkmark and Lock Icons

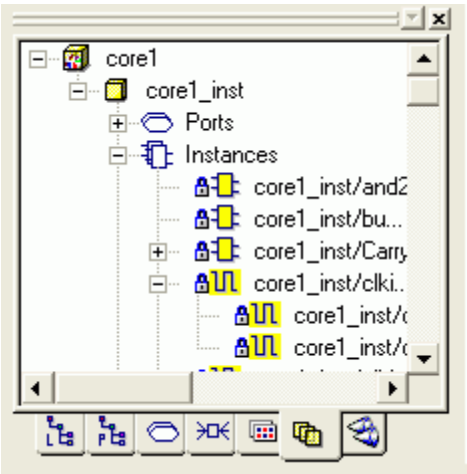


Figure 4 · Block Tab - Locked instances and nets are highlighted

See Also

Logical Tab

Physical Tab

Ports Tab

Nets Tab

Regions Tab

Logical Cones Tab

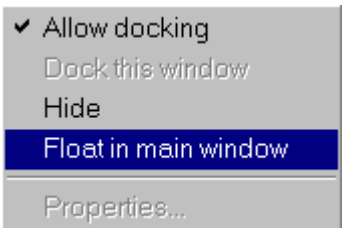
Block Tab

Floating and Docking Windows

You can rearrange or hide the Hierarchy window, World window, and Log window within MultiView Navigator. These windows are referred to as "floating" because you can move them within the Tools window. You can also "dock" or anchor them in place.

To move a window:

1. Select the window to move.
2. Right-click anywhere on the window except on a macro or within the display area of the Log window, and then choose **Float in main window** from the right-click menu.
3. Click and drag the title bar of the window to its new location.
4. Release the mouse button.



To return the floating window to its docked location:

1. Select the floating window to dock.
2. Right-click and choose **Dock this window** from the right-click menu. To dock the Log window, unselect **Float in main window** from the right-click menu.

The window returns to its original location in the MultiView Navigator interface.

Tip: Tip: You can also dock and undock a floating window by double-clicking the window frame.

To hide a window:

1. Select the window to hide.
2. Right-click and choose **Hide** from the right-click menu.

To show a hidden window:

1. From the **View** menu, choose **Windows.**
2. Select the name of the window to display (Hierarchy Window, Log Window, or World Window).

Selecting Objects

Before you can highlight, assign, unassign, configure, or otherwise manipulate an object, you must first select it by clicking it.

From the Hierarchy window, you can also select groups of objects. The procedure for selecting more than one object in the Tools window depends on which tool you are using. See the documentation for your tool.

To select a group of objects in the Hierarchy window:

- To select consecutive objects, click the first object, press and hold down **SHIFT**, and then click the last object.
- To select objects that are not consecutive, press and hold down **CTRL**, and then click each object.

To unselect specific selected objects:

- To unselect one or more consecutive objects, press and hold down **SHIFT**, and then click the last object to include in the selection. The objects below it are unselected.
- To unselect objects that are not consecutive, press and hold down **CTRL**, and then click each object to unselect.

To unselect all selected objects:

- Click on a clear spot in either the **Hierarchy** or **Tools** window.

Highlighting and Unhighlighting Objects

Highlight objects or groups of objects for easy reference. You can change the default highlight color.

To highlight an object:

1. Select the object to highlight in the **Tools** window.
2. From the **Edit** menu, choose **Highlight** or click the **Highlight** toolbar button. The color of the object changes to the default highlight color. In the following illustration, the objects are highlighted in red.

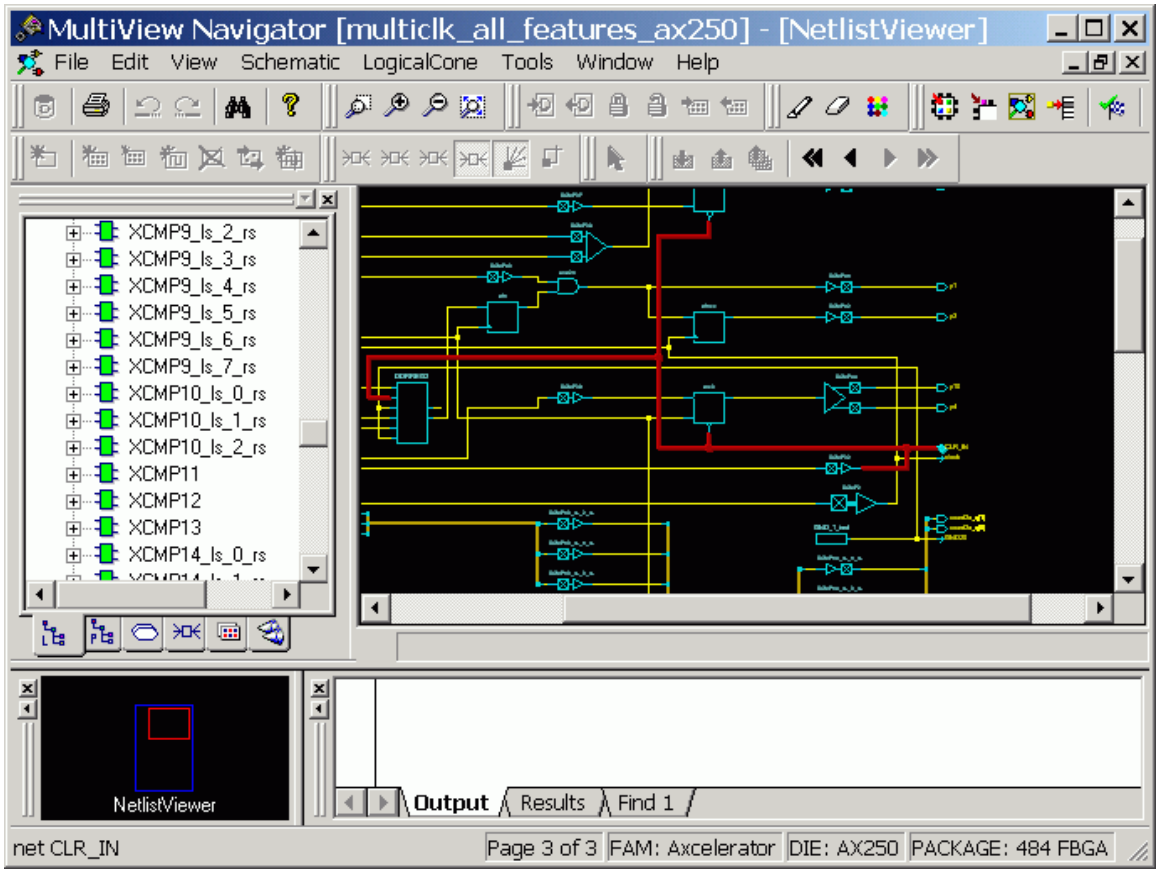


Figure 5 · Objects Highlighted in Red

To highlight a group of objects:

Highlighting a group of objects is useful for tracing a net.

1. From the **Edit** menu, choose **Highlight**,or click the **Highlight**toolbar button. The cursor turns into a pen icon.
2. Press and hold down the **CTRL** key, and then click each object to highlight.

To unhighlight a group of objects:

1. Select the highlighted group of objects.
2. From the **Edit** menu, choose **Unhighlight All**,or click its equivalent toolbar button.

See Also

Selecting Objects

Changing the Highlight Color

Changing the Highlight Color

To change the highlight color:

1. From the **Edit** menu, choose **Highlight Color.**
2. Select the new highlight color from the **Color palette** that appears.
3. Click **OK**.

All objects that you choose to highlight will appear in the new highlight color. However, objects previously highlighted will not change to the new color.

See Also

Selecting Objects

Highlighting and Unhighlighting Objects

Finding Objects

Use the Find command from any tool in MultiView Navigator to locate instances, nets, ports, and regions.

To find instances:

1. From the **Edit** menu, choose **Find**. The **Find** dialog box appears.

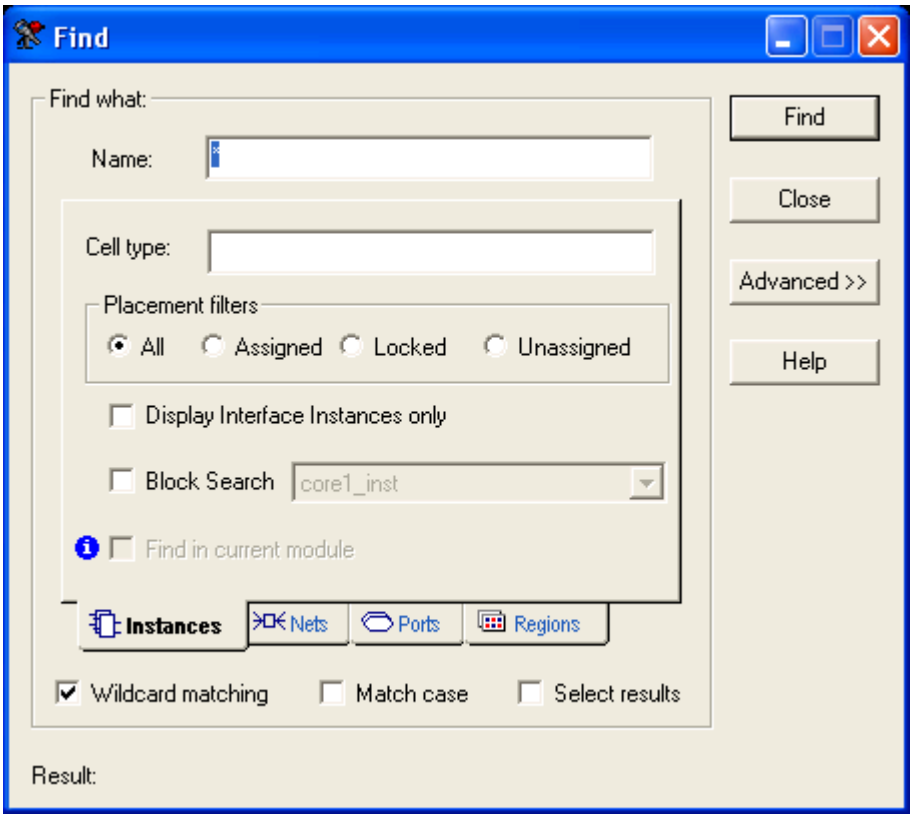


Figure 6 · Find Instances Dialog Box

2. Make sure the **Instances** tab is selected.
3. To search by name, type the name and Cell Type in the **Name** and **Cell Type** fields. Name is the name of the instance. Cell Type refers to the macro type. For example, you can search for all macros of type AND by typing *AND* in the Cell Type field. Likewise, you can search for *OR2A* to list all the ORs used in the design. Usually cell types are prefixed with "ADLIB." When searching for instances, Instance Name or Cell Type can be blank, but not both. These fields accept wildcards. Wildcard characters include:

Wildcard	What It Does
?	Matches any single character
*	Matches any string

Wildcard	What It Does
/	This is the level-bordering symbol. “A/B” designates “object B, which is part of instance A.”

4. For Placement filters, select one of the following:
   All – Find all instances
   Assigned – Find only instances assigned to a location
   Locked – Find only locked instances
   Unassigned - Find only instances that are not assigned to a location
5. To find only macros connected to ports, select **Display Interface Instances only**.
6. To find only instances in the current module, select **Find in current module**. This option is only available when NetlistViewer is the active view and is displaying the pre-optimized netlist.
7. To find only instances in a specific user block or in all user blocks, select **Block search**, and then select the block from the drop-down list.
8. Select **Wildcard matching** to search using wildcards.
9. Select **Matchcase** to make the search case sensitive.
10. Select **Select Results** to select the results of your find.
11. Click to specify how you want to display your results.
12. Click **Find**. The located instances, if any, appear in the Find pane in the Log window.

Instances, ports, and nets found in the current module but which only exist in the pre-optimized netlist have a special icon next to them in the Find pane:  See the Find pane in the illustration below for an example:

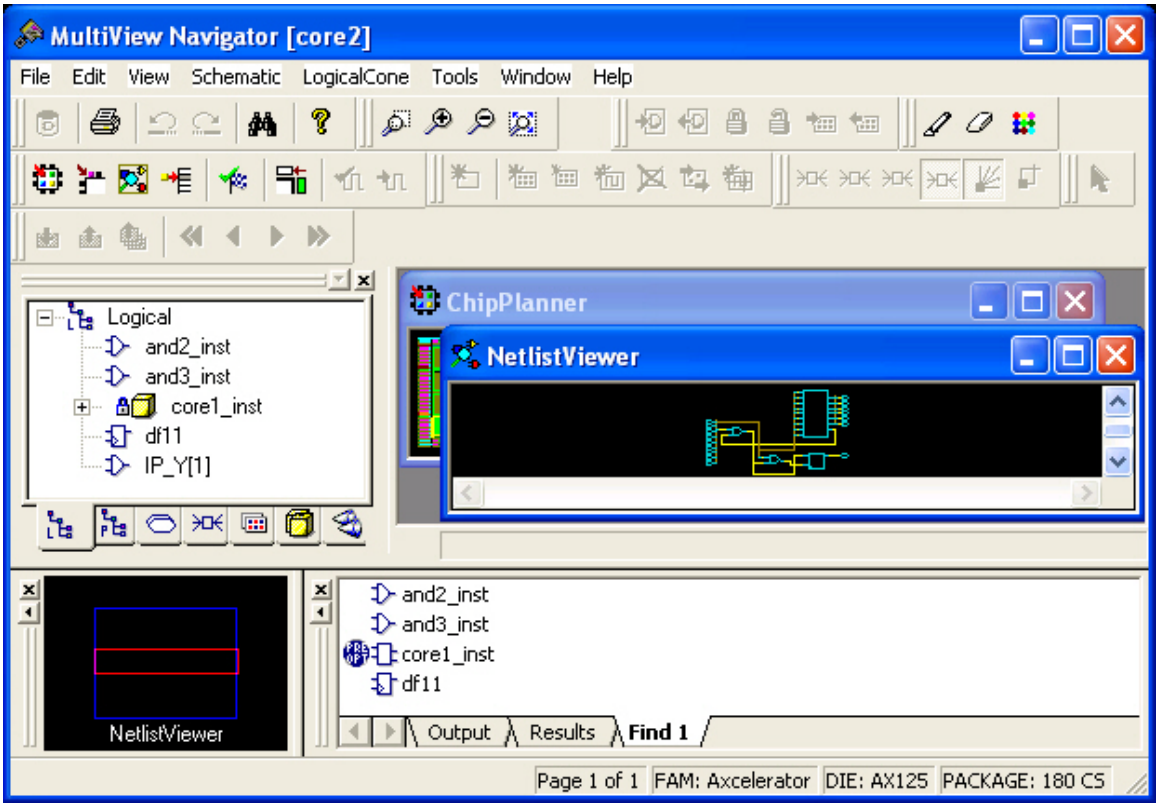


Figure 7 · Instances That Exist Only in the Pre-optimized Netlist

To find a net:

1. From the **Edit** menu, choose **Find**. The **Find** dialog box appears.
2. Click the **Nets** tab.

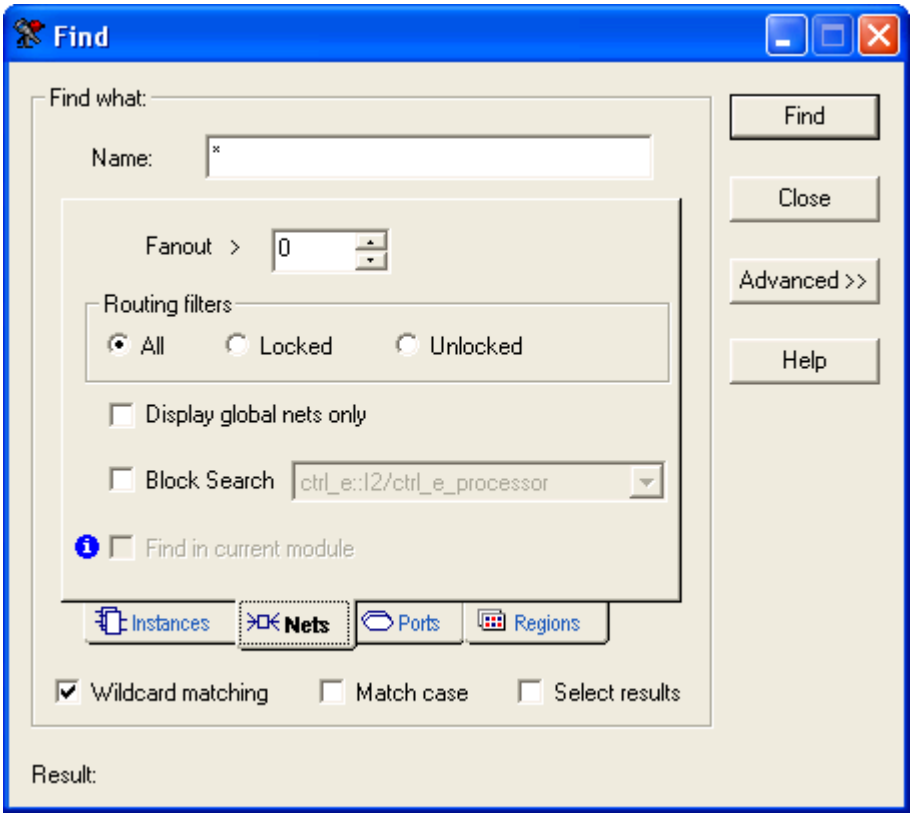


Figure 8 · Find Nets Dialog Box

3. Type the **name** of the net. This field accepts .
4. To find nets with a specific fanout value, click the up and down arrows next to **Fanout** to set the fanout value.
5. For Routing filters, select one of the following:
   All – Find all nets
   Locked – Find only locked nets
   Unlocked – Find only unlocked nets
6. To find only clock nets in your active list, select **Display global nets only**.
7. To find only nets in the current module, select **Find in current module**. This option is only available when NetlistViewer is the active view and is displaying the pre-optimized netlist.
8. To find only nets in a specific block, select **Block search** box, and then select the block from the drop-down list.
9. Select **Wildcard matching** to search using wildcards.
10. Select **Matchcase** to make the search case sensitive.
11. Click **Select Results** to select the results of your find.
12. Click to specify how you want to display your results.
13. Click **Find**. The located nets, if any, appear in the **Find** pane in the **Log** window.

To find ports:

1. From the **Edit** menu, choose **Find**. The **Find** dialog box appears.
2. Click the **Ports** tab.

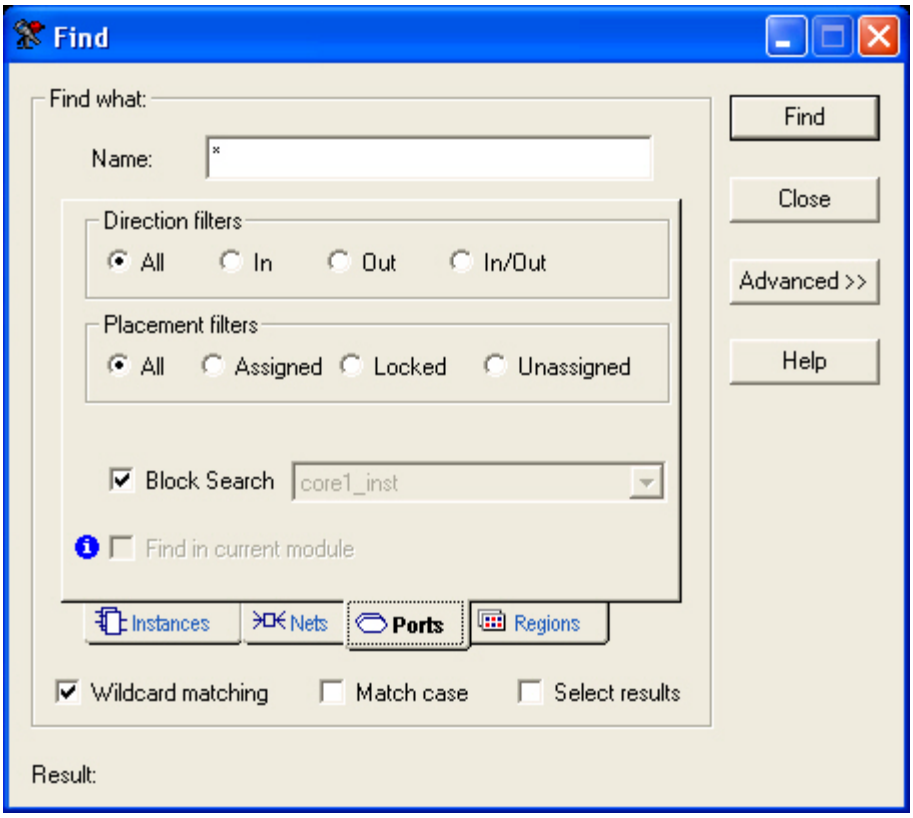


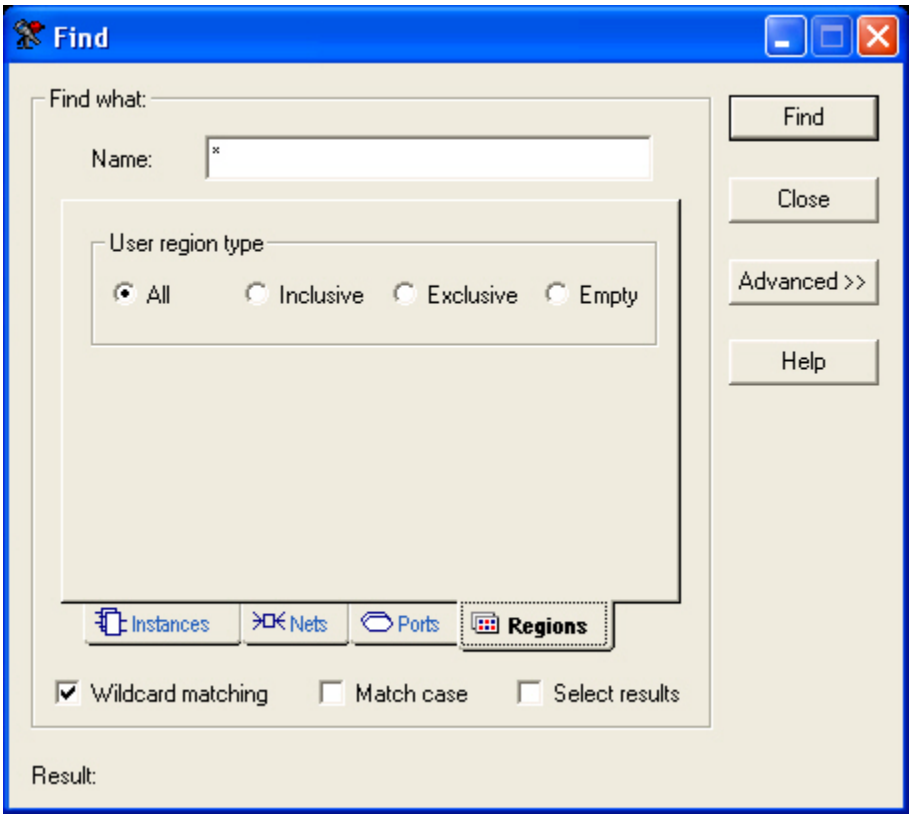
Figure 9 · Find Ports Dialog Box

3. To search by name, type the **Name** of the port to be located. This field accepts wildcards.
4. To find a port by type, select **All**, **In**, **Out**, or **In/Out.**
5. To find only ports in the current module, select **Find in current module**. This option is only available when NetlistViewer is the active view and is displaying the pre-optimized netlist.
6. To find only ports in a specific block, select **Block search** box, and then select the block from the drop-down list.
7. For Placement filters, select one of the following:
   All – Find all ports (input ports, outputs, and ports you can use for both input and output)
   Assigned – Find only assigned ports
   Locked – Find only locked ports
   Unassigned – Find only unassigned ports
8. Select **Wildcard matching** to search using .
9. Select **Matchcase** to limit the search to items with the exact characters specified.
10. Click **Select Results** to select the results of your search.

11. Click to specify how you want to display your results.
12. Click **Find**. The located ports, if any, appear in the **Find** pane in the **Log** window.

To find regions:

1. From the **Edit** menu, choose **Find**. The **Find** dialog box appears.
2. Click **Regions**.



Find Regions Dialog Box

3. To search by name, in the **Name** field, type the name of the region you want to find. This field accepts wildcards. Wildcard characters include:

Wildcard	What It Does
?	Matches any single character
*	Matches any string

4. To search by type of region, select **All**, **Inclusive**, **Exclusive**, or **Empty**.
5. Click to specify how you want to display your results.
6. Click **Find**. The located regions, if any, appear in the **Find** pane in the **Log** window.

To use the advanced features:

- Click **Advanced** to specify where you want your results to appear. Your options appear below the **Result** area of the **Find** dialog box.

Creating Multiple Searches

You can create multiple types of searches and save the results by creating panes. A pane contains the results of a Find operation and appears in the Log window.

To create a new pane in the Log window:

1. Click **Advanced** to display more options.
2. Select the **New pane** option in the dialog box, and then type a name for it in the text box below it.
3. Perform your search. The results of your search appear in the new pane in the Log window. Also, the name of the new pane appears in the drop-down list below the **Pane** option.
4. Before you use a saved search, select whether you want to overwrite your previous results or append the new results to the previous one.

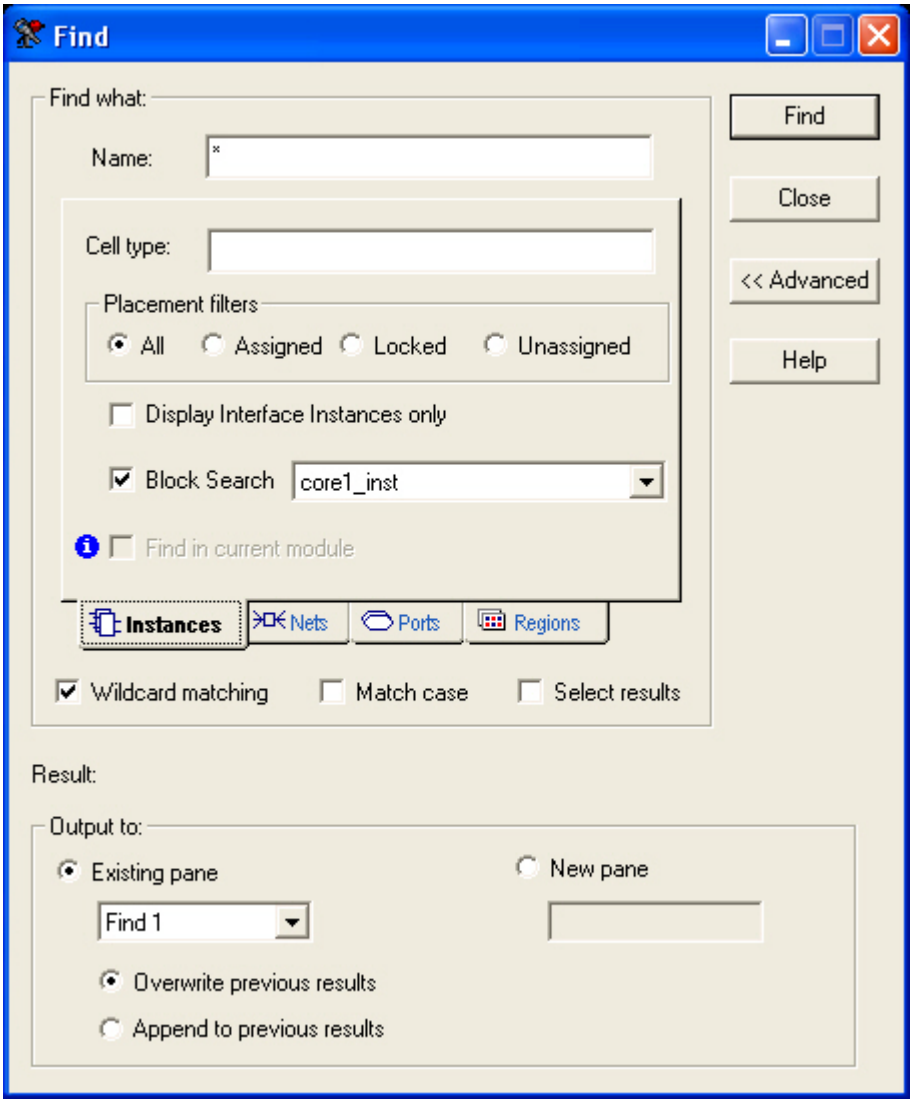


Figure 10 · Find Instances/Advanced Dialog Box

Using the Prelayout Checker

The Prelayout Checker checks your design for possible error conditions before you place-and-route. Prelayout checks are a subset of the Design Rule Check (DRC). If the Prelayout Checker finds potential errors, it displays warning and error messages in MultiView Navigator's Log window.

To run the Prelayout Checker, from the **Tools** menu, choose **DRC**. Use the DRC command to check for errors before you use the Layout command.

Selecting DRC performs the following checks:

- Validates common macros in overlapping regions against the overlap capacity
- Checks placement of I/Os against the banks' voltage settings

When you choose **Commit and Check** from the **File** menu in the MultiView Navigator, it automatically performs comprehensive checking in addition to committing the changes to your design.

See Also

About I/O banks

Automatically assigning technologies to I/O banks

Using the Global Checker

The Global Checker only checks the validity of the current global net assignments. Global net checks are a subset of the Design Rule Check (DRC). If the Global Checker finds potential errors, it displays warning and error messages in MultiView Navigator's Log window.

To run the Global Checker, from the **Tools** menu, choose **Global Planner>Run Global Checker**. From the **Tools** menu, choose **DRC** to check for errors before running Layout in the Designer software. You can also click the Global Checker toolbar button:

In MVN, when you choose **Commit and Check** from the **File** menu, the Global Checker automatically performs comprehensive checking in addition to committing the changes to your design.

See Also

Using the Local Clock Assigner

Using the Prelayout Checker

Using the Global Planner

The Global Planner runs automatically when you run Layout. The Global Planner automatically assigns global nets to clock conditioning circuit (CCC) locations on the chip in the design. You can also use the Global Planner tool from within the MultiView Navigator (MVN) to assign global nets in the design.

The Global Planner tool is available in MVN when at least one net is unassigned. In MVN, you can use the Global Planner tool either to assign all global nets in the design or to run the Global Checker.

Note: Note: The Global Planner is only available for Fusion, IGLOO, and ProASIC3 families.

If the Global Planner assigns a net to any of the four corners of the floorplan, a QuadrantClock region is automatically created for that area. You can lock this region to prevent the Global Planner tool from removing it during consecutive runs.

To automatically assign global nets:

- From the **Tools** window, choose **Global Planner>Assign All Nets**, orclick the **Global Planner** toolbar button:

Messages appear in the Output window informing you when the automatic global net assignment begins and ends. If the assignment is successful, "Global assigner completed successfully" appears in the Output window as shown below:

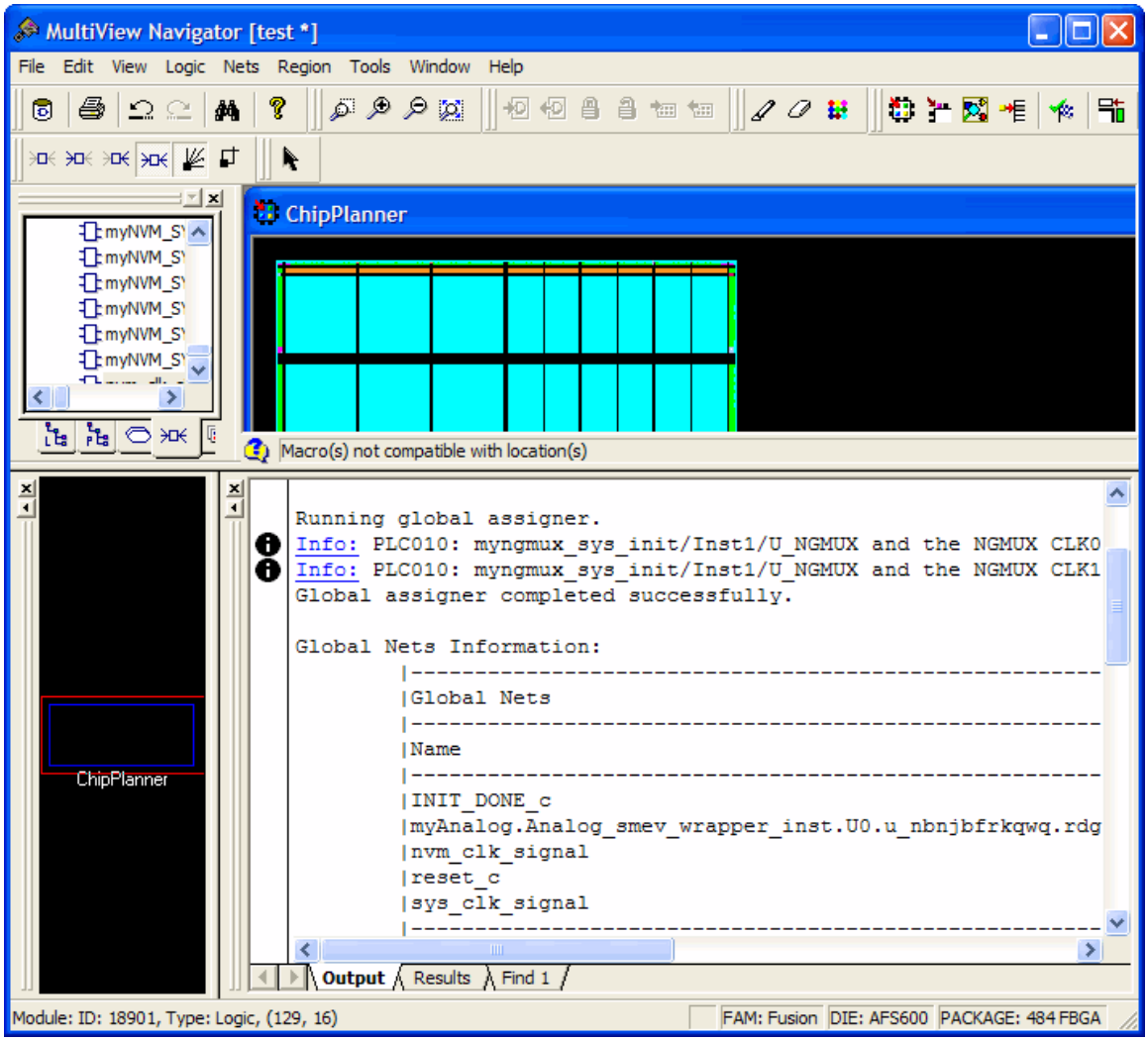


Figure 11 · Global Planner Displays Messages in Output Window

Tip: Tip: Click an underlined "Error" or "Info" message to display more information.

To undo the global net assignments, choose **Undo** from the **Edit** menu. Undo unassigns the global nets assigned by the Global Planner. It does not unassign the global nets previously assigned manually.

To redo the changes undone by the Undo command, choose **Redo** from the **Edit** menu.

If you need to clear global net assignments made before using the **Undo** command, you can manually unassign or re-assign clocks to nets.

When you choose **Commit and Check** from the **File** menu in the MultiView Navigator, it automatically performs comprehensive checking in addition to committing the changes to your design.

See Also

Using the Global Net Checker

Using the Prelayout Checker

Flash*Freeze Pins

The Flash*Freeze pin is a dedicated pin used to enter or exit Flash*Freeze mode; the pin can also be routed internally to the FPGA core to allow your logic to decide if it is safe to transition to this mode. If you do not use Flash*Freeze technology, you can use the Flash*Freeze pin as a regular I/O to take advantage of the low power consumption of IGLOOe, IGLOO, and ProASIC3L devices.

In PinEditor, the package pin assigned as a Flash*Freeze pin displays "FF/.." preceding the pin name, for example, FF/GEB2/IO108PDC4B0 but only when no I/O sits on the same location.

The Flash*Freeze port is displayed as a locked port in both ChipPlanner and the Hierarchy window's Ports tab. You cannot move or unassign it. The "FF/.." label is not visible in ChipPlanner.

You can assign only one Flash*Freeze pin per IGLOOe, IGLOO, IGLOO PLUS, or ProASIC3L device.

The Flash*Freeze pin is specific to a die-package combination. See the *IGLOO and IGLOOe Low Power Flash FPGAs with Flash*Freeze Technology* Application Notes. Refer to the tables in the Application Notes to see which pin to use as the Flash*Freeze pin.

Reserving Pins for Device Migration

With this feature, you can begin a design with a larger device that you intend to implement later with a smaller device. Because there might be some pins on the smaller device that are not bonded, you want to make sure that the pin assignments created on the larger device are compatible with the pins on the smaller device. This feature reserves the pins on the larger device that are not bonded on the smaller device.

Pins in the current device that are not bonded in the target device will be marked as "reserved."

You can explicitly reserve a pin in PinEditor or I/O Attribute Editor (Package Pins view). You can also reserve a pin by importing a PDC constraint file with the `reserve` PDC command.

To explicitly reserve a pin in PinEditor:

- Select the pin to reserve, right-click it, and choose **Reserve Pin** from the right-click menu. (See screen below.) Repeat for each pin to reserve.

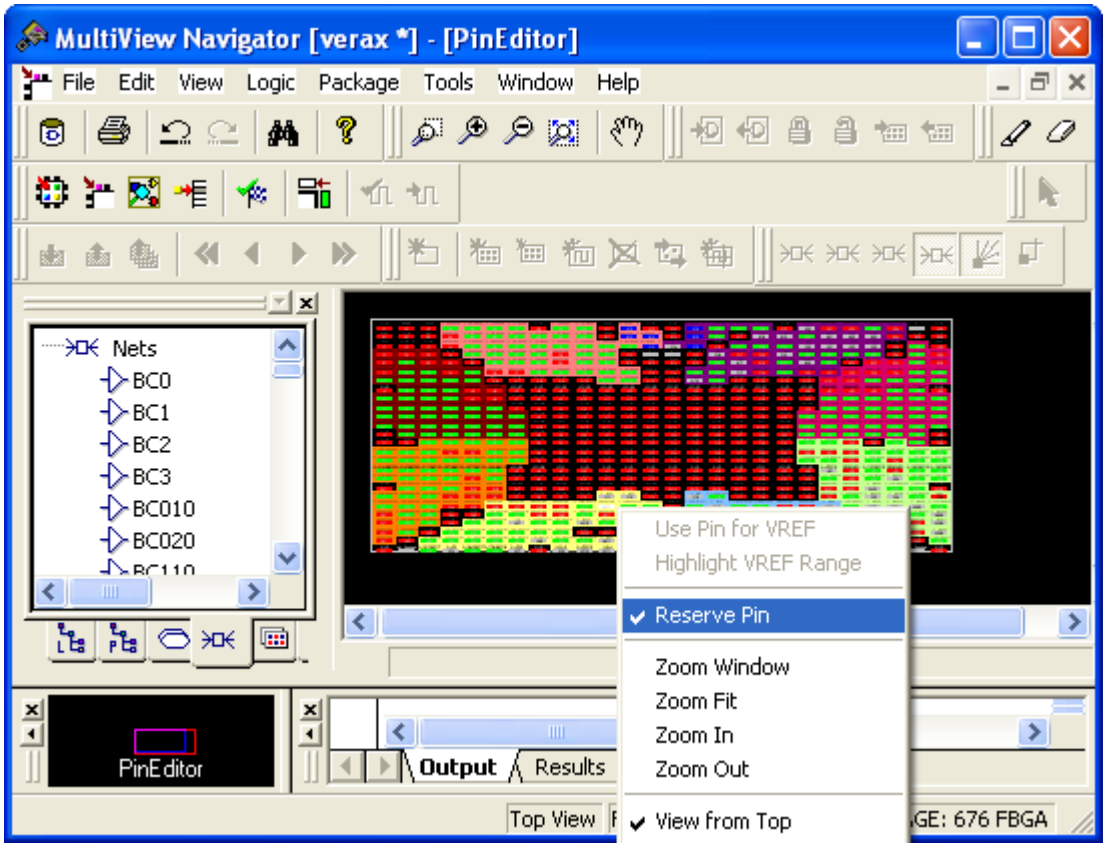


Figure 12 · Figure 13 · Reserve Pins from Right-click Menu in PinEditor

Note: To unreserve a reserved pin from the right-click menu in PinEditor, select the pin to unreserve, right-click it, and choose Reserve Pin to remove the checkmark.

To explicitly reserve a pin in I/O Attribute Editor:

- In **Package Pins** view, select the **User Reserved** check box associated with the pin to reserve. (See screen below.) Repeat for each pin to reserve.

To automatically reserve pins that are not bonded in a destination device for migration, follow these steps:

1. In PinEditor, from the **Edit** menu, choose **Reserve Pins for Migration**. The **Reserve Pins for Migration** dialog box appears. The current device for which the pins will be reserved appears in the **Reserve pins in the current device** text box.
2. From the **"that are not bonded in the target device"** drop-down list, select the target device to which you will be migrating your design.
3. Unselect the **Keep explicitly-reserved pins** check box if you do not want to save the pins that are currently explicitly reserved.

Choose **Undo Reserve Package Pin** from the **Edit** menu to unreserve the last pin you reserved.

To reserve pins with a PDC file:

1. Open the PDC file to edit.
2. Use the `reserve` command to specify the names of the pins to reserve.

To unreserve pins with a PDC file:

1. Open the PDC file to edit.
2. Use the `unreserve` command to specify the names of the pins to unreserve.

Note: Note: SX-A devices do not support the reserved pins feature.

See Also

`reserve`
`unreserve`

Committing Changes in MVN

Changes you make are not permanent until you use the **Commit** command. The Commit command saves your changes to your design session. Changes are not reversible. To commit your changes but not run the Prelayout Checker, from the **File** menu, choose **Commit**.

To commit your changes and run both the Prelayout Checker and the Global Net Checker, from the **File** menu, choose **Commit and Check**.

NetlistViewer

The NetlistViewer tool displays the contents of the design as a schematic, making it easier for you to debug. Use NetlistViewer to view nets, ports, and instances in the schematic view. You can start NetlistViewer only after the design is compiled.

Note: Note: This version of NetlistViewer supports only the IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, Axcelerator, SX-A, and eX families. If you are designing for other families, use the non-MVN version of NetlistViewer.

Starting NetlistViewer in MultiView Navigator

NetlistViewer requires a compiled design. If you start NetlistViewer before compiling your design, Designer guides you through the compile process before opening NetlistViewer.

To start NetlistViewer from Designer, either click the **NetlistViewer** icon in the Designer Design Flow window, or from the **Tools** menu, choose **NetlistViewer**.

To start NetlistViewer from within MVN, either click the **NetlistViewer** button in the MVN toolbar, or from the **Tools** menu, choose **NetlistViewer**.

NetlistViewer opens in the Tools window of MultiView Navigator. After reading your netlist design, NetlistViewer generates a clearly laid out schematic view as shown below.

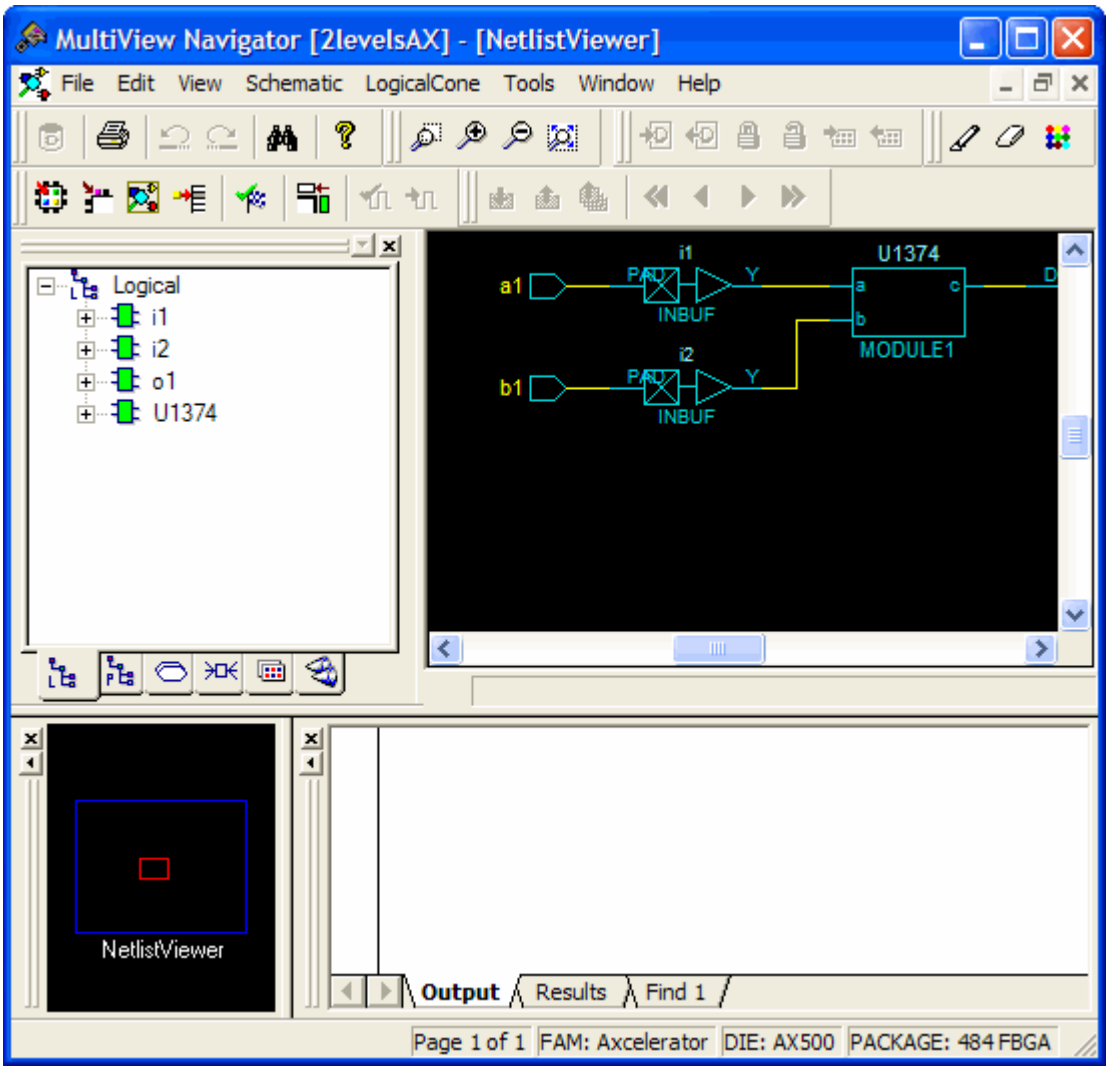


Figure 14 · NetlistViewer in MultiView Navigator

Displaying Your Netlist

The NetlistViewer window displays your netlist in graphical format. When you open an IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, Axcelerator, SX-A, or eX design, and click **NetlistViewer**, it automatically starts MultiView Navigator and displays your design in the NetlistViewer window.

To view your netlist using NetlistViewer:

- After NetlistViewer starts and displays your netlist in MultiView Navigator, you can view the optimized flattened netlist or the pre-optimized hierarchical netlist.
- The optimized flattened netlist is a non-hierarchical view. Use the optimized flattened netlist when cross-probing with other tools, such as PinEditor or ChipPlanner.
- The pre-optimized netlist is your original netlist, as passed to the Designer software. The hierarchical structure is useful for navigating. The pre-optimized netlist is the default.

To switch between views, from the **Schematic** menu, click **Show Pre-optimized Netlist** or **Show Optimized Netlist**.

See Also

Navigating Through Your Netlist

Identifying Paths

Bundling Nets

A netBundle is a group of nets with names that have the same pattern. For example, nets with names such as `N_357_0`, `N_357_1`, and `N_357` are bundled together as are `crc_100_`, `crc_200_`, and `crc_300_`.

A netBundle represents all nets in the group as a bus. In NetlistViewer, lines representing netBundles are brown and thicker than single nets. NetlistViewer automatically generates netBundles whenever possible. You cannot create, expand, or unbundle a netBundle.

Nets are bundled into a netBundle if the net names match one of the following patterns:

```
*(..)
*[..]
*{..}
*<..>
*_..._
*_..
```

where "`*`" stands for any character string and "`..`" must consist of digits only.

Note: Note: Pins are connected to the net, not the netBundle.

Navigating Through Your Netlist

You can navigate in the logical view of the design vertically and horizontally.

Vertical Navigation

Navigate vertically through your hierarchical design using the **Push**, **Pop**, and **Top** commands. These commands are available from the **Schematic** menu, the right-click menu, and the toolbar.

To go one level deeper in a design:

Note: Note: This feature is only available for hierarchical instances (that is, instances that contain logic).

1. Select an instance.
2. From the **Schematic** menu, choose **Push**, or from the right-click menu, choose **Push instance<name of instance>.**

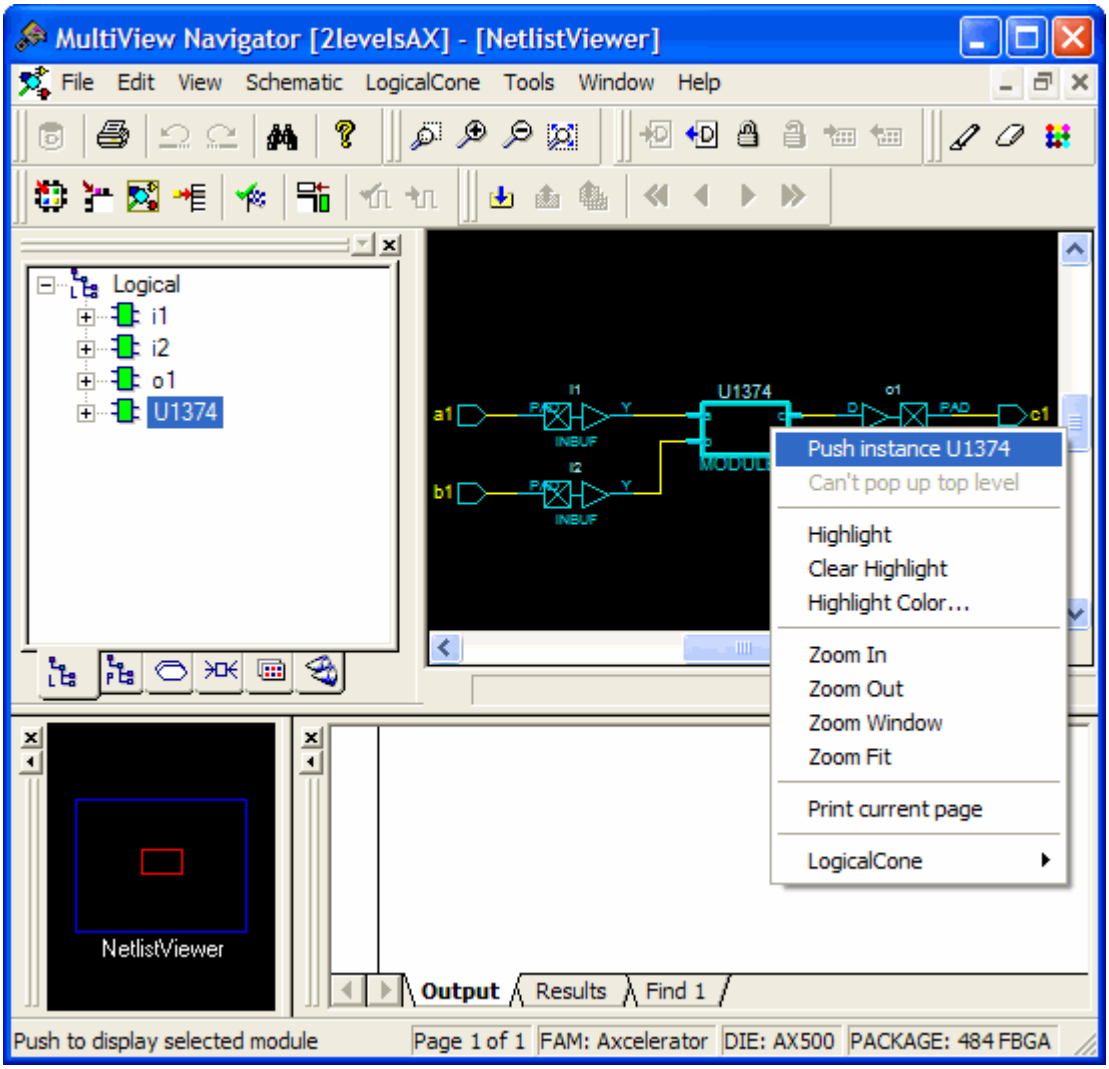


Figure 15 · Pushing Instance U1374

You can also select one pin of an instance, and then choose **Push** from the right-click menu to move the focus to that pin. For example, if you select pin C of block U1374, and then choose **Push** from the right-click menu (as shown below), NetlistViewer centers on the port corresponding to the pin you selected (as shown below):

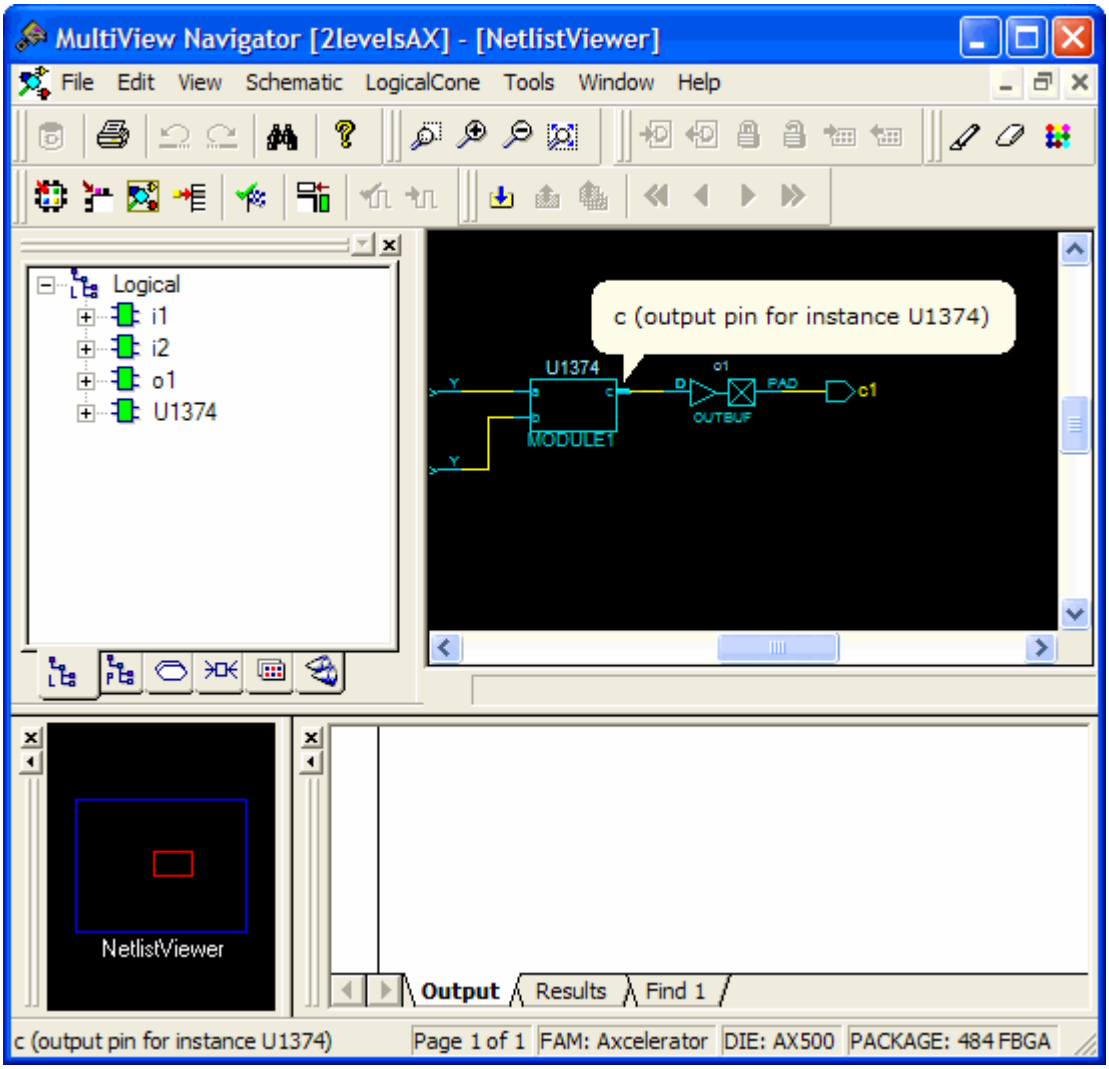


Figure 16 · Pushing Only Pin C

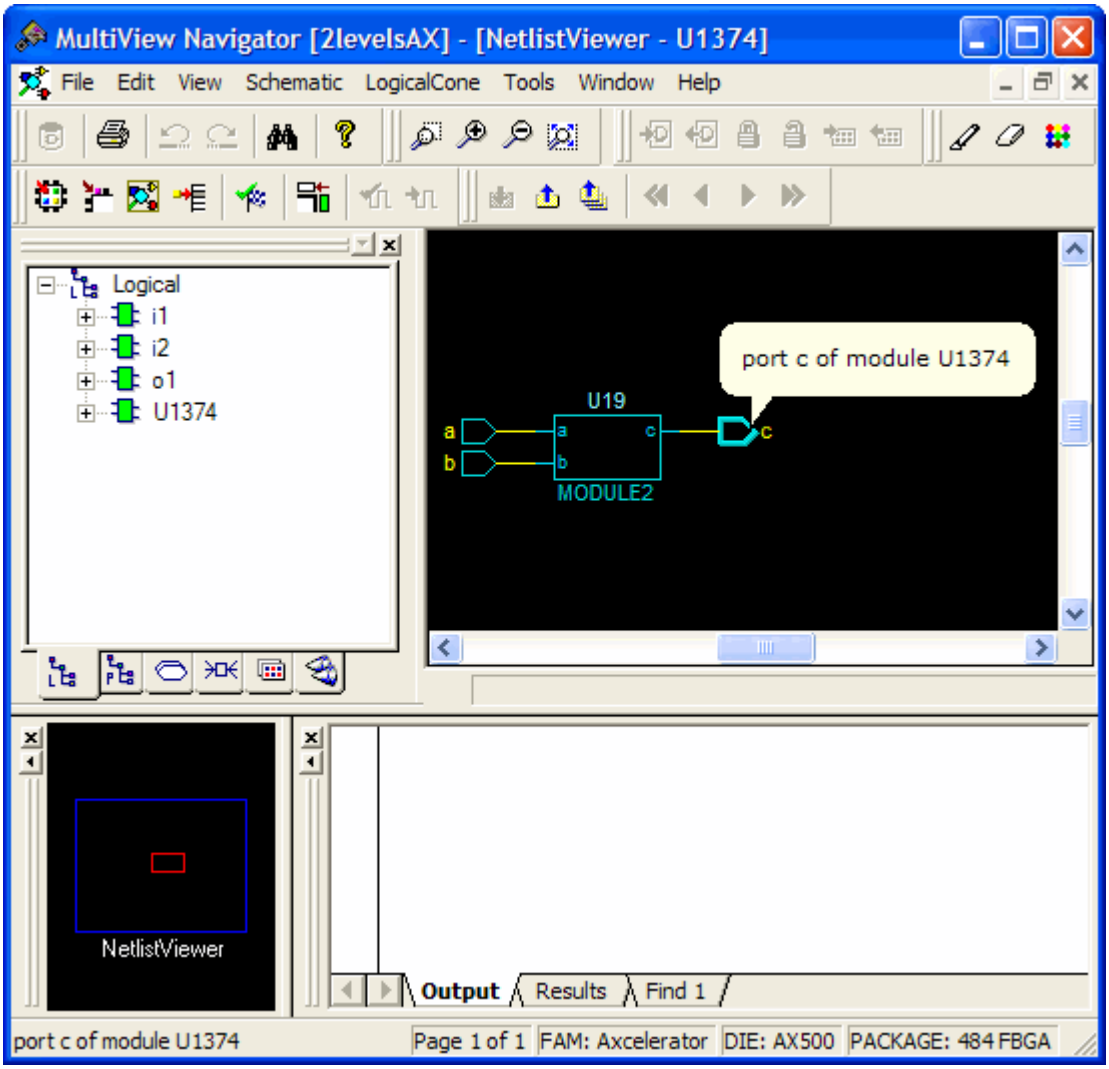


Figure 17 · Result of Pushing Pin C

To go one level higher in a design:

1. Select an instance.
2. From the **Schematic** menu, choose **Pop**, or from the right-click menu, choose **Pop up current level.** You can also select a port and click the **Pop** toolbar button to go up one level and center on the pin corresponding to the port you selected.

To go to the top level, from the **Schematic** menu, choose **Top**, or click the **Top** toolbar button.

Horizontal Navigation

When large designs do not fit in the Schematic View window, NetlistViewer splits the design into multiple pages. Page splitting enables you to quickly compute and display the schematic. You can also turn off page splitting to view your

entire design on a single page. For larger designs, when this option is turned off, it may take NetlistViewer significantly longer to display the schematic. To turn page splittingon or off, from the **Schematic** menu, choose **Allow Page Splitting**.

To navigate to the next page in a design, from the **Schematic** Menu, choose **Go to Next Page**, orclick the **Next Page** button in the toolbar.

To navigate to the previous page, from the **Schematic** Menu, choose **Go to Previous Page**, or click the **Previous Page** button in the toolbar.

To navigate to the first page, from the **Schematic** menu, choose **Go to First Page**, or click the **First Page** toolbar button.

To navigate to the last page, from the **Schematic** menu, choose **Go to Last Page**, or click the **Last Page** toolbar button.

Following Nets

Following a net might take you to another page or another level in your design. Following nets is useful when your design is split into several pages or if it includes some hierarchical logic. Nets that continue on other pages are terminated by a page connector symbol (>). Note that a net can continue on many pages.

	Indicates the net ends on another page
	Indicates the net begins on another page

The illustrations below show two pages that include the pin labeled "data_6." On both pages, the net ends with the page connector symbol (>), indicating the net continues on another page. (Nets can continue on many pages.)

Figure 18 · Symbols for a Continuing Net

Nets that cross a hierarchical boundary are inside a hierarchical instance and connected to a port of the instance or those connected to a pin of a hierarchical instance.

To follow a net:

1. Select a net in NetlistViewer.
2. From either the **Schematic menu** or right-click menu,choose **Follow Net Into**. NetlistViewer displays a list of all pages or modules to which your net is connected. Choose one item in the list. If the item you chose is a page, NetlistViewer displays the corresponding page and centers to the page connector (the -> or >- symbol ending a split net) ending the selected net. If you chose a module, NetlistViewer does the corresponding Push or Pop operation to display it, and selects the net connected to the one initially selected.

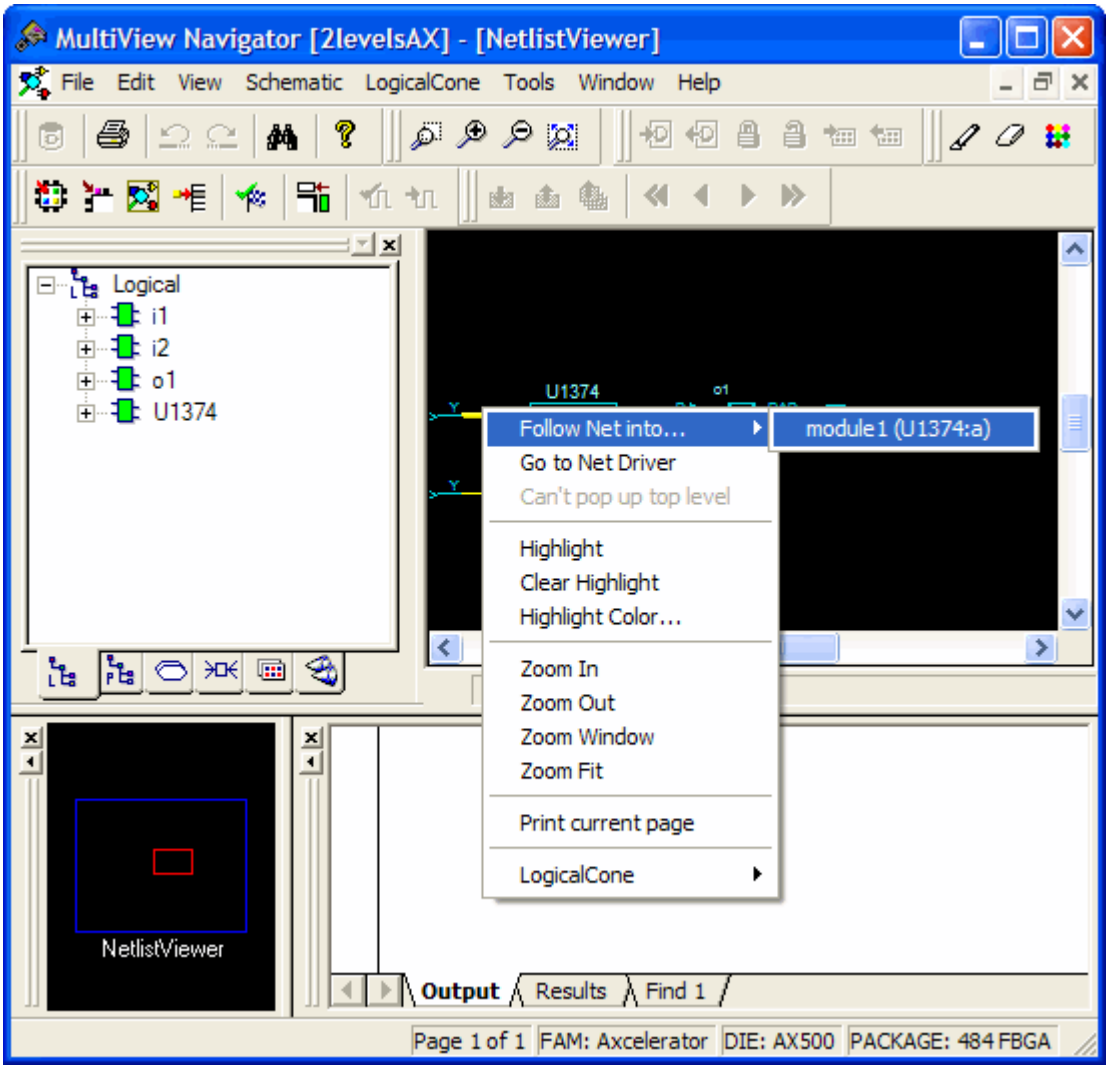


Figure 19 · Page and Module Option

Center to Net Driver

This feature allows you to easily retrieve the driver of a net.

To go to the net driver:

1. Select a net in NetlistViewer.
2. From either the **Schematic menu** or right-click menu,choose **Go to Net Driver**.

NetlistViewer displays the actual driver of the net. For example, in the sample design shown below, U1374 is a hierarchical block. Selecting the net connected to its output pin, and then choosing **Go to Net Driver** from the right-click menu displays instance U19 inside of block U1374 because instance U1374/U19 is the actual driver of the net.

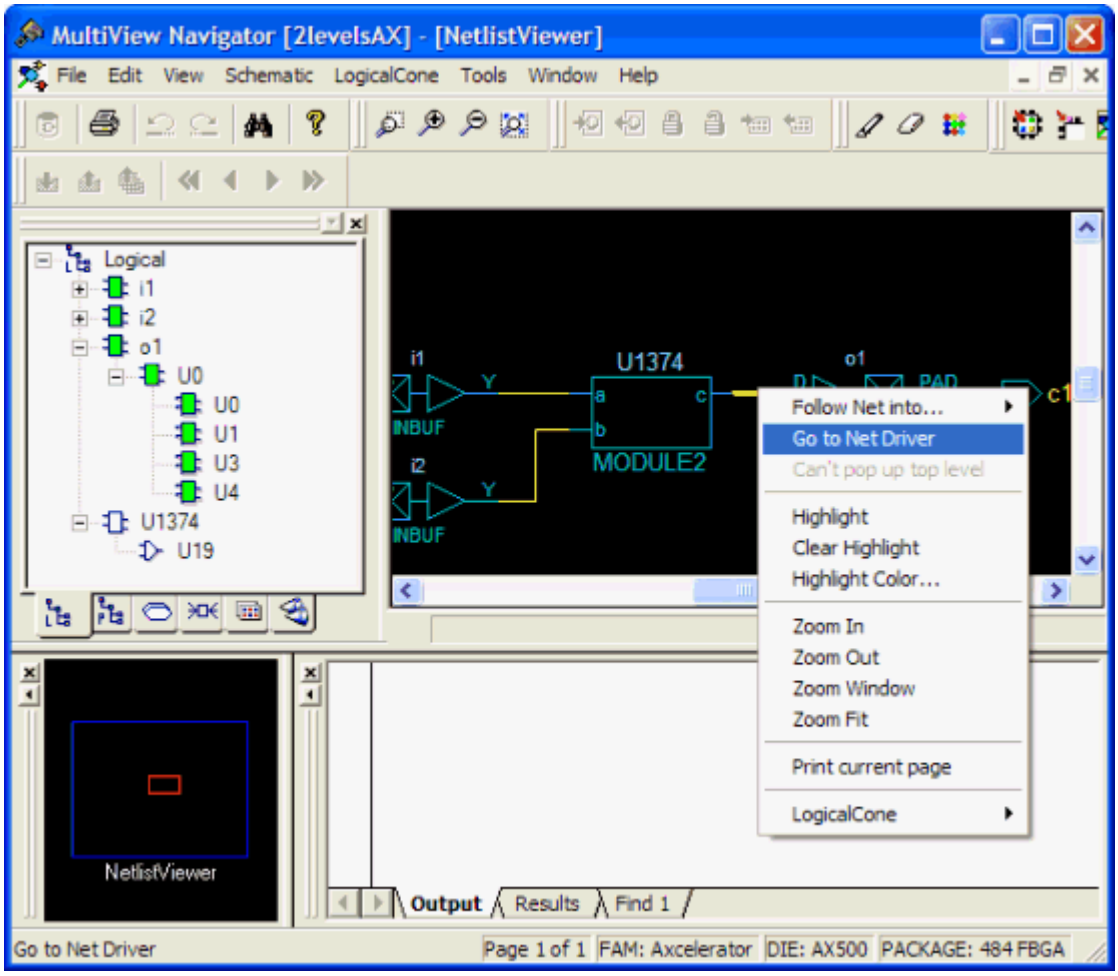


Figure 20 · Go to Net Driver

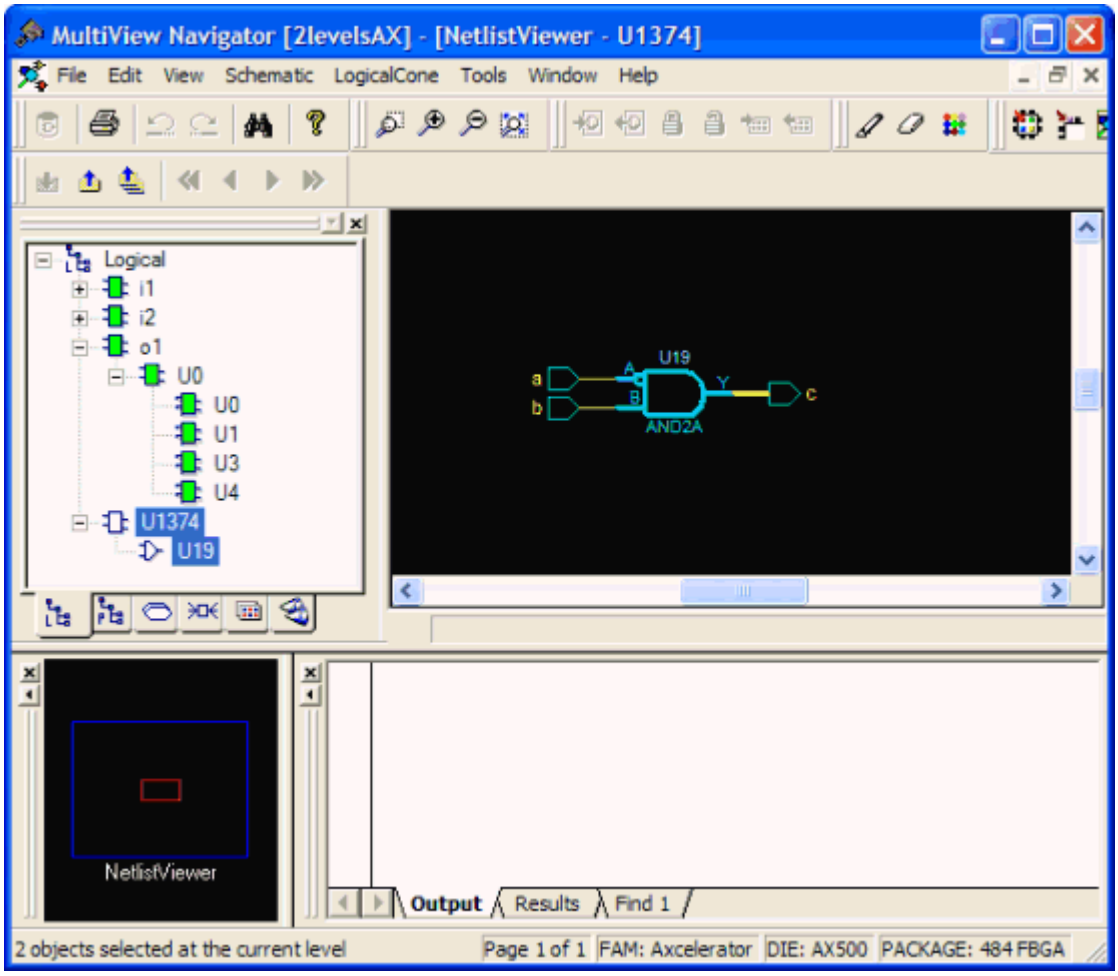


Figure 21 · Zooms to and Selects Actual Driver of the Net (U19)

Note: Note: When you choose Go to Net Driver, NetlistViewer selects the driver of the net to help you find it easily.

Selecting Objects in NetlistViewer (MVN)

Before you can highlight an object, you must first select it. Selecting objects in NetlistViewer is similar to selecting objects in other MultiView Navigator tools. The main difference is that you use the **SHIFT** key instead of the **CTRL** key when selecting and unselecting more than one object in NetlistViewer.

To select a group of objects in the NetlistViewer window:

1. Click an object.
2. Press and hold down the **SHIFT** key while you click each object to select.

To unselect specific selected objects:

- Press and hold down the **SHIFT** key, and then click on a selected object to unselect it. You can also hold down the left mouse button and drag and draw a rectangle toward the bottom-right corner. Release the mouse button when all items you want to unselect are included in the rectangle.

To unselect all selected objects:

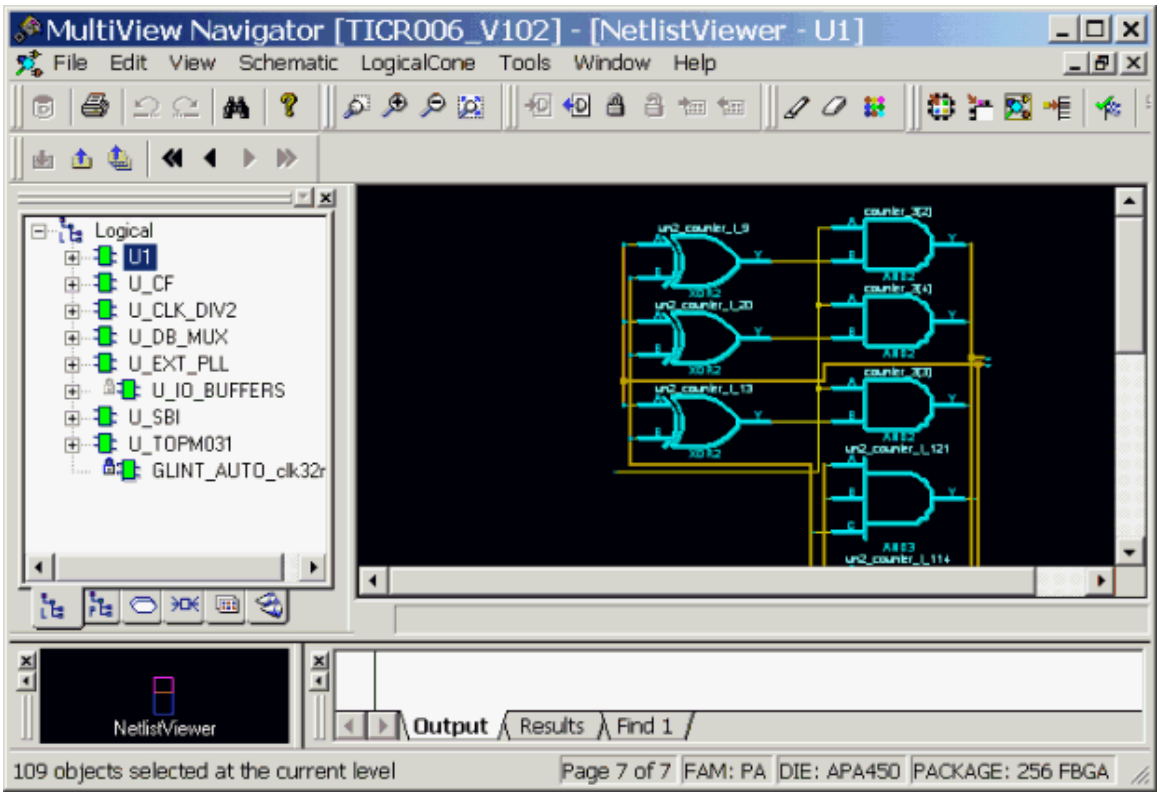
- Click a clear spot within NetlistViewer to unselect all objects.

Identifying Paths

You can use NetlistViewer with SmartTime to identify the signal path or individual instances. For more information about SmartTime, see the SmartTime online help. For more information about SmartTime, see the *SmartTime User's Guide*.

To identify paths:

1. In the **Design Flow** window, click **NetlistViewer** to display your netlist.



D>isplay the Netlist in NetlistViewer

2. In the Design Flow window, click **Timing Analyzer** to display the **SmartTime Timing Analyzer**.
3. In the **SmartTimeTiming Analyzer**, select the clock domain in the **Domain Browser**.
4. Select a set in the Paths List and the paths within that set are displayed in the Path Details (lower table). The Paths List displays timing information for various categories.

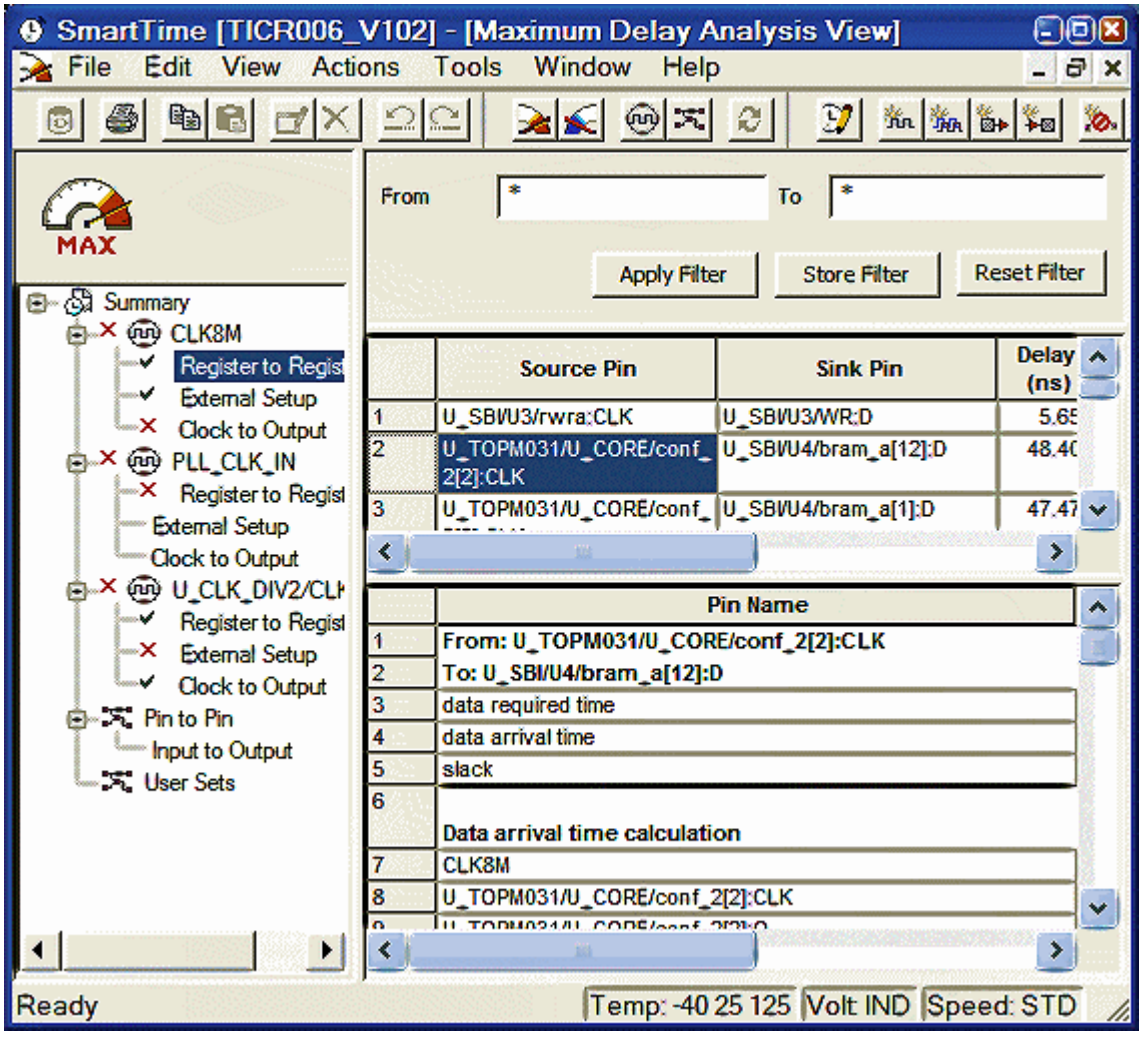


Figure 22 · Select a Clock Domain and a Set of Paths

5. Select the path to cross probe.
6. Right-click on the selected path, and choose **Cross-probe selected paths** from the right-click menu.

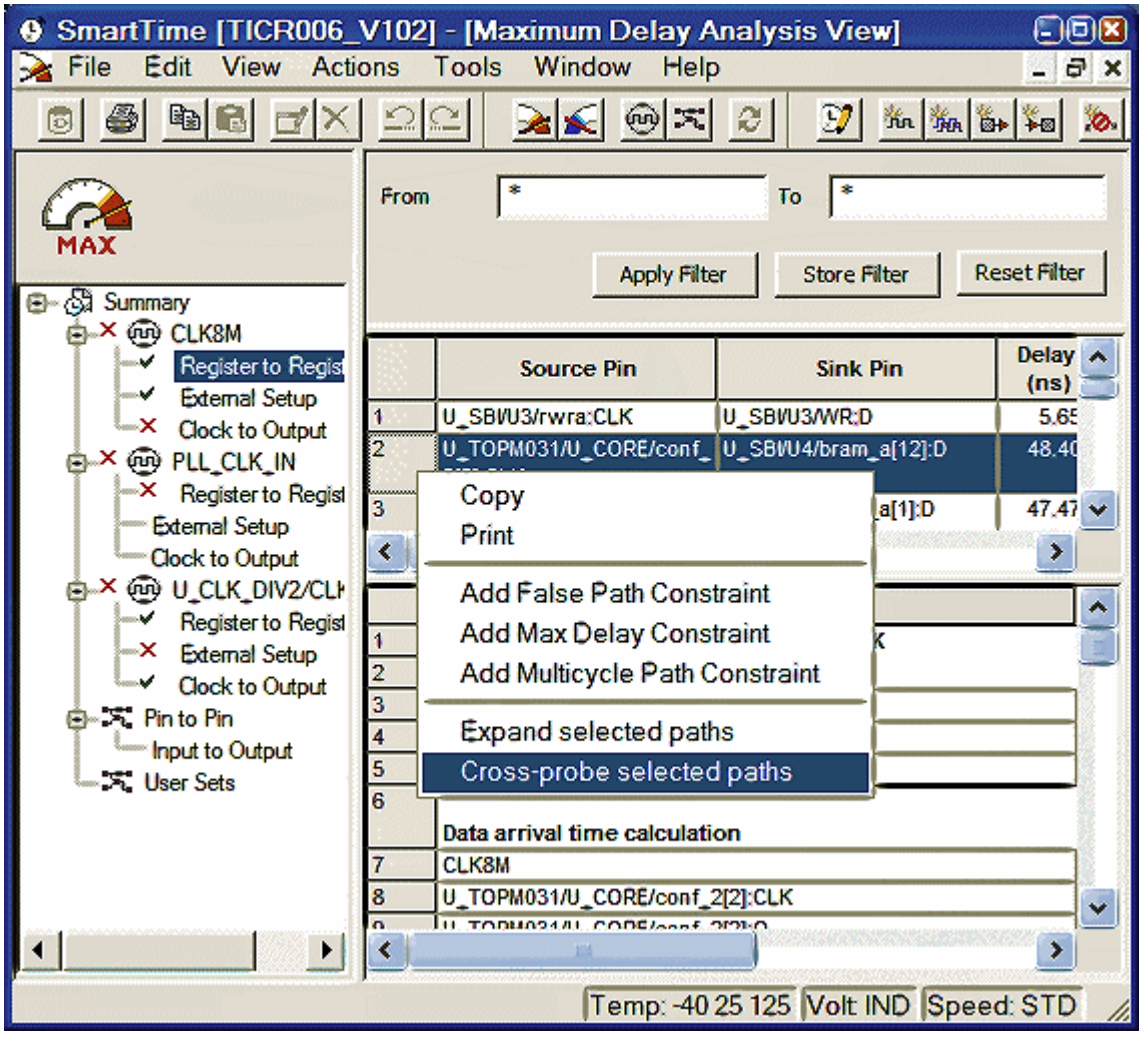


Figure 23 · Cross-probe the Selected Paths

All objects in the selected path appear highlighted in NetlistViewer.

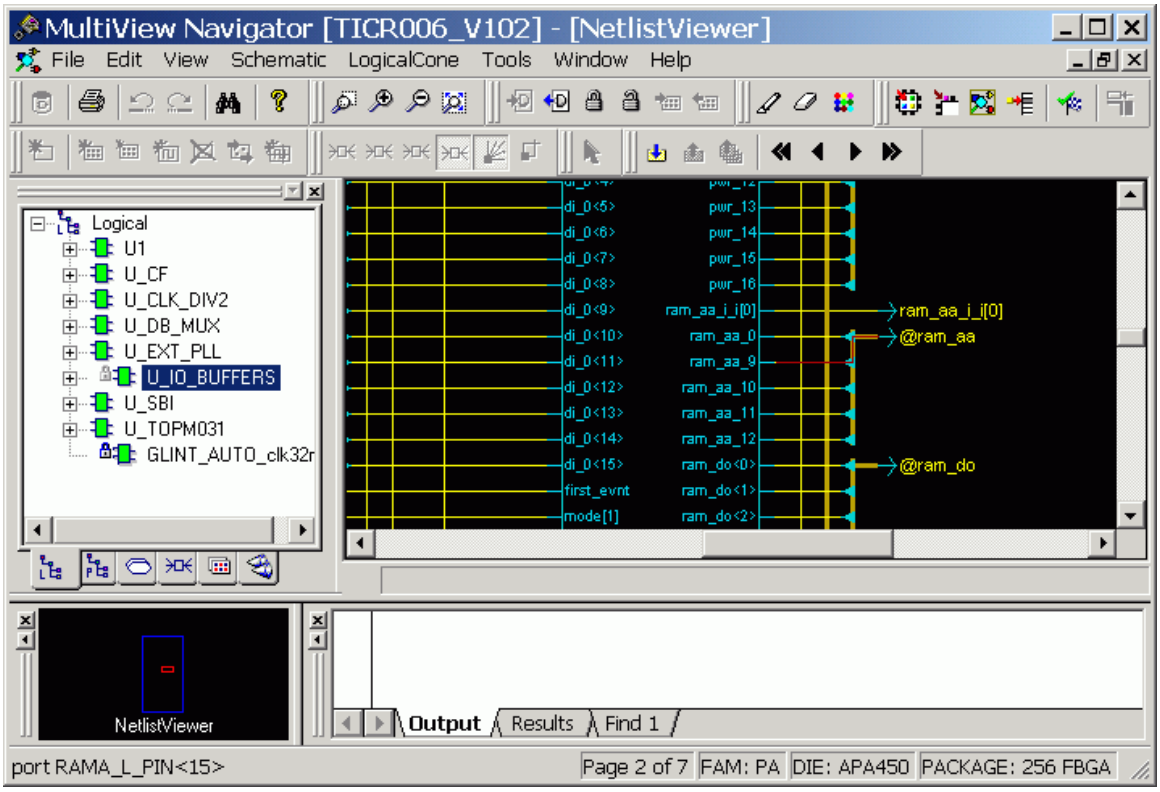


Figure 24 · Cross-probed Paths Appear Highlighted in NetlistViewer

Note: Note: You can create a Logical Cone window to view a specific path. A logical cone is a view of a specific part of your design. See "Managing Logical Cones" and "Creating a Logical Cone" in this guide.

See Also

What is a Logical Cone?

Creating a Logical Cone

SmartTime User's Guide

What is a Logical Cone?

A logical cone is a window that displays only a portion of a netlist. You create this window in NetlistViewer and simply select the objects that you want to appear in this separate view. You can add individual instances, blocks, and ports to a logical cone. You can also remove objects from this cone.

Logical cones help you navigate and analyze a specific part of the design. A Logical Cone view is very similar to the NetlistViewer view. The main differences between the Logical Cone and NetlistViewer views are:

- In a logical cone, you see only the pieces of the design that you want to focus on (for example, path analysis), whereas in NetlistViewer, you see the entire netlist.
- In a logical cone, a net appears as a dashed line unless all instances that are connected to that net in the netlist are also present in the Logical Cone view. These nets are designated as partially connected, as opposed to fully connected nets.
- In a logical cone, all objects of the netlist appear on a single sheet, with hierarchical boundaries still visible. This is a trade-off between the classical hierarchical view, where you must use Push and Pop commands to navigate in the netlist, and the flattened view, where hierarchy is simply ignored.

Logical cones support cross-probing. Therefore, you highlight and select objects the same way you do in the NetlistViewer. See “Selecting Objects” and “Highlighting and Unhighlighting Objects” in this guide.

All Logical Cone commands are available from the LogicalCone menu in MultiView Navigator, and most Logical Cone commands are also available from the right-click menu in both the NetlistViewer and Logical Cone windows.

Creating a Logical Cone

Use logical cones to view, highlight, and cross-probe a selected subset of your netlist.

You can create as many logical cones as you want. A logical cone displays only the objects you add to it. Initially, the cone does not contain objects.

To create a logical cone:

1. In NetlistViewer, from the **LogicalCone** menu, choose **Create New Cone**.

A new window appears in which you can add logic to the cone. The name of the new cone appears in the **Logical Cones** tab of the **Hierarchy** window.

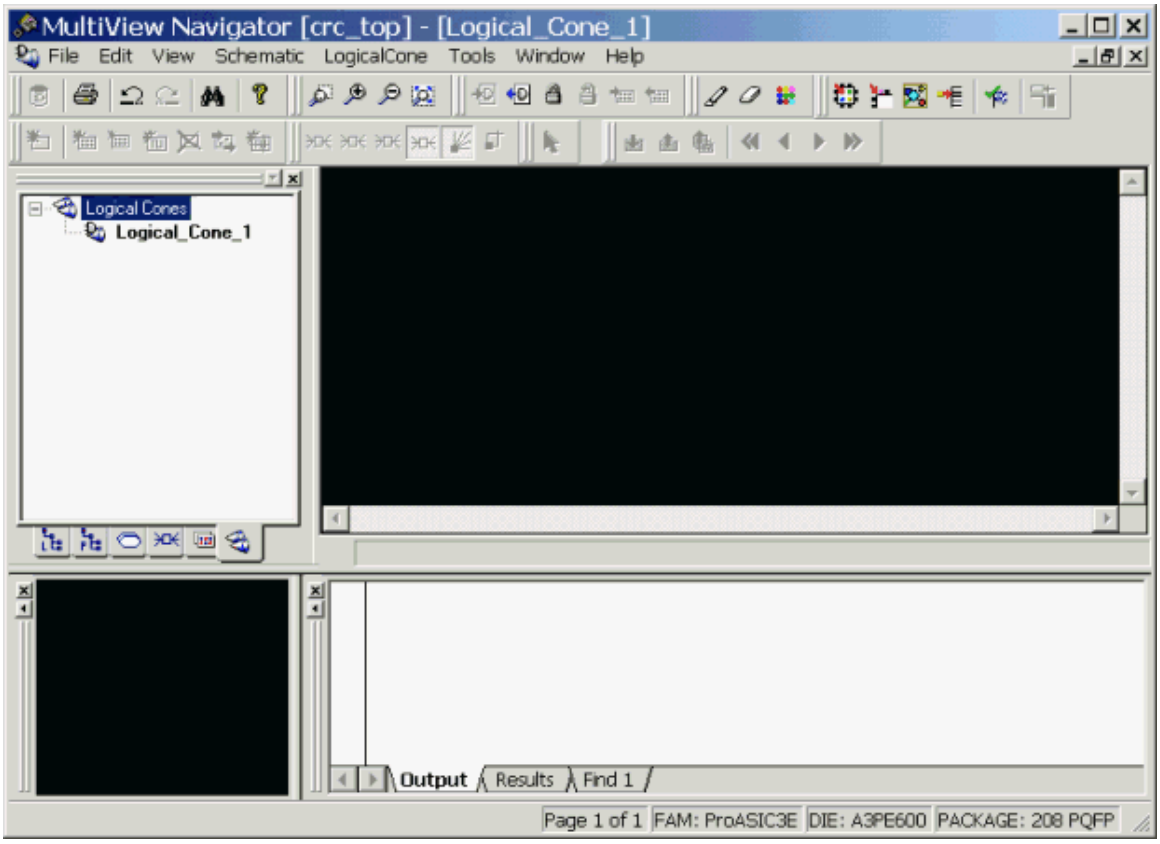


Figure 25 · New Logical Cone Window Added

2. In NetlistViewer, select one or more objects.
3. Right-click the selected object(s).
4. From the right-click menu, choose **LogicalCone** > **Add To Active Cone** > **Selection**.

A Logical Cone window containing only the selected object(s) appears as shown in the following example. You can add and delete objects from a logical cone window.

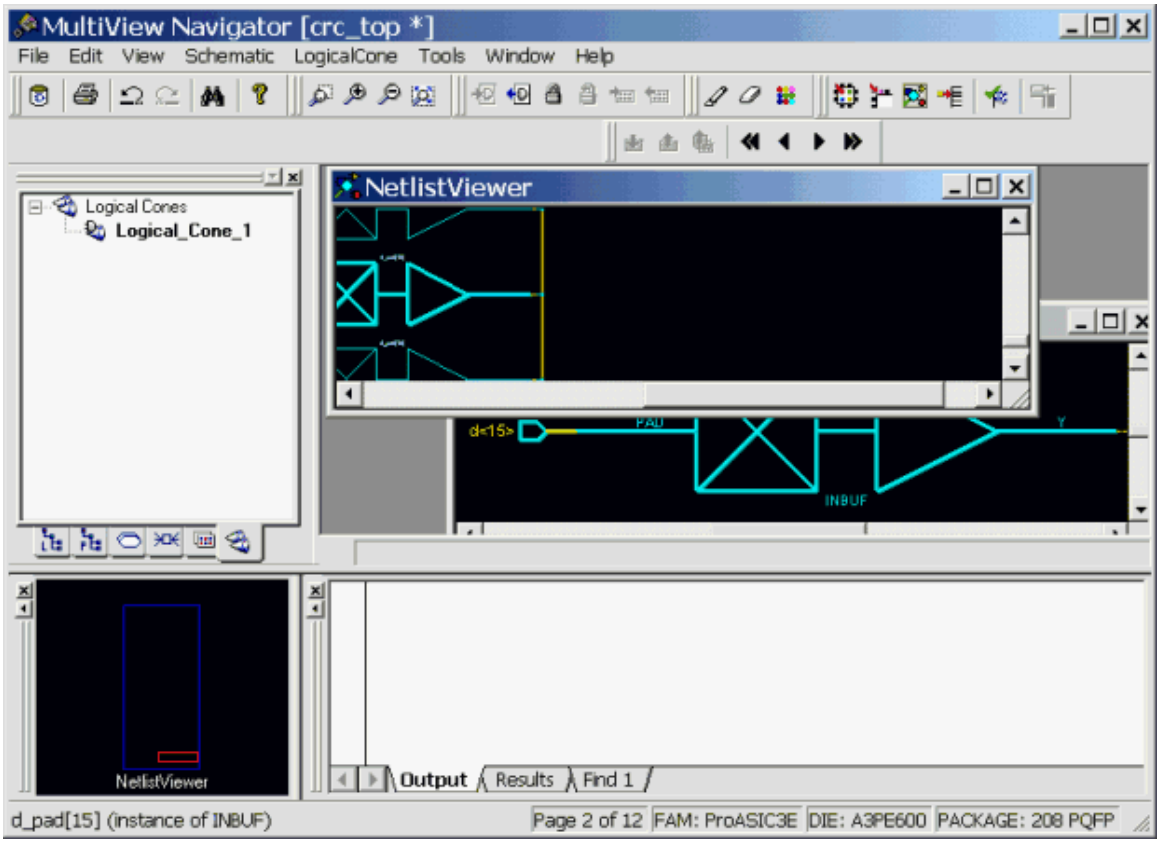


Figure 26 · Selected Objects Added to the Logical Cone

Tip: Tip: If no cones exist in the current design, you can skip a step. Just select one or more objects, right-click, and then choose **LogicalCone > Add To Active Cone > Selection** from the right-click menu.

See Also

Changing the Name of a Cone

Deleting a Logical Cone

Setting the Active Cone

Changing the Name of a Cone

You can modify the name of any Logical Cone view. The new name appears in the title bar of the cone window as well as in the Logical Cones tab of the Hierarchy window.

To change the name of a cone:

1. Select a Logical Cone view.
2. From the **LogicalCone** menu, choose **Rename Cone**.
3. In the Rename Cone dialog box, type the new name over the existing one.
4. Click **OK**.

Note: Note: The Rename Cone command is available only when the current window is a Logical Cone view.

Tip: Tip: You can also rename a cone from the **Logical Cones** tab in the **Hierarchy** window. Click once on the cone name to select it, and click again to edit it. When you see an outline around the highlighted name, type the new name in place of the old one.

Deleting a Logical Cone

To delete a Logical Cone:

1. In the **Logical Cones** tab of the **Hierarchy** window, click the **plus sign (+)** to the left of Logical Cones to display the names of the cone views.
2. Right-click the cone to delete, and choose **Delete** from the right-click menu.

Setting the Active Cone

The active or current cone is the one in which you can add or remove logic. Before you can add or remove objects from a cone, you must select the cone you want to modify.

To set the active cone, right-click the cone in the **Logical Cones** tab of the **Hierarchy** window, and choose **Set Active**.

Hiding Logic in a Hierarchical Instance

To hide logic within a hierarchical instance in a cone view:

1. Click the Logical Cone containing the logic to hide.
2. Select the instance to hide from view.
3. From the **LogicalCone** menu, choose **Fold Selection**.

All the logic inside the selected hierarchical instance disappears from the cone. Hiding the logic inside an instance reduces the size of the logic, providing you with a better global view of the cone content.

Displaying Logic Hidden Within a Hierarchical Instance

To display logic that was added to a hierarchical instance in a cone view:

1. Click the Cone view containing the logic to show.
2. Select the instance containing hidden logic.
3. From the **LogicalCone** menu, choose **Unfold Selection**.

All the logic previously hidden inside of the selected hierarchical instance reappears in the cone. If the selected instance does not contain logic, nothing happens.

Adding Selected Objects to a Cone

You can add only instances and pins to a cone. (Nets and ports, if required, are automatically added to the cone.)

To add objects to a cone:

1. Make sure the cone to which you want to add objects is the active cone.
2. In NetlistViewer or a Logical Cone view, select the instances and pins to add to the cone.
3. From the **LogicalCone** menu, choose **Add To Active Cone > Selection**.

All the objects appear in the active cone view. If the objects can be connected to other objects already present in the active cone, the command also connects those objects. If some of the selected objects are pins, the corresponding instances are added.

See Also

Adding a Group of Highlighted Objects

Adding a Group of Highlighted Objects to a Cone

You can add a group of highlighted instances and pins to the active cone. (Nets and ports, if required, are automatically added to the cone.)

To add a group of highlighted objects to a cone:

1. Highlight the objects you want to add to a cone.
2. Click the cone to which you want to add your highlighted objects.
3. From the **LogicalCone** menu, choose **Add To Active Cone > Highlighted Group**.
4. Click a highlighted object. All objects with the same highlight color are added to the active cone.

All the highlighted objects appear in the active cone view. If the highlighted objects can be connected to other objects already present in the active cone, the command also connects those objects. If some of the highlighted objects are pins, the corresponding instances are added.

Tip: Tip: Click outside a highlighted object, or press **Esc** to terminate the command.

See Also

Adding Selected Objects to a Cone

Clearing All Objects from a Cone

You can clear the entire contents of a cone with one command.

To remove all objects from a cone:

1. Make sure the cone you want to remove all objects from is the active cone.
2. From the **LogicalCone** menu, choose **Remove From Active Cone > All Logic**.

The active window is now empty.

See Also

Removing Selected Objects from a Cone

Removing a Group of Highlighted Objects from a Cone

Removing Selected Objects from a Cone

You can remove specific instances and pins from the active cone. You cannot remove nets and ports from a Logical cone.

To remove only selected objects from a cone:

1. Make sure the cone you want to remove objects from is the active cone.
2. Select the object(s) you want to remove from the cone.
3. From the **LogicalCone** menu, choose **Remove From Active Cone > Selection**.

The selected objects no longer appear in the active cone. If some of the selected objects are pins, their corresponding instances are removed as well.

See Also

Clearing All Objects from a Cone

Removing a Group of Highlighted Objects from a Cone

Removing a Group of Highlighted Objects from a Cone

You can remove a group of highlighted instances and pins from the active cone. You cannot remove nets and ports from a Logical cone.

To remove only highlighted objects from a cone:

1. Make sure the cone you want to remove objects from is the active cone.
2. From the **LogicalCone** menu, choose **Remove From Active Cone > Highlighted Group**. The cursor turns into a color picker pointer.
3. Click a highlighted object. All objects with the same highlight color are removed from the active cone.

The highlighted objects you selected no longer appear in the active cone view. If some of the highlighted objects are pins, their corresponding instances are removed.

Tip: Tip: Click outside a highlighted object, or press **Esc** to terminate the command.

See Also

Removing Selected Objects from a Cone

Clearing All Objects from a Cone

Adding Drivers to a Cone

You can add the driving instance(s) for an instance, a net, or an input pin to a cone.

To add the driver of an instance to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select the instance, net, or input pin whose driver you want to add to the cone.
2. Right-click the selected instance, and choose **Add To Active Cone > Driver**.

The driver for the selected instance appears in the active cone. For input pins, this command adds the connected net and driving instance to the active cone. For nets, this command adds the driving instance to the active cone. For each instance, this command adds the driver for each of the instance's input pins to the active cone.

If the added objects can be connected to other objects already present in the active cone, this command also connects those objects.

See Also

Adding Driven Instances to a Cone

Adding Adjacent Objects to a Cone

Adding Driven Instances to a Cone

You can add all of the logic driven by an instance, a net, or an output pin to a cone at the same time.

To add a driven instance to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select the output pin, net, or instance for which you want to add the driven logic to the cone.
2. Right-click the instance, and choose **Add To Active Cone > All Driven Logic**.

All instances driven by the selected object(s) appear in the active cone. For each selected net, it adds all the driven instances to the active cone. For each selected output pin, this command adds the connected net and all the instances connected to it. For each selected instance, this command adds the driven logic for each output pin.

If the added objects can be connected to other objects already present in the active cone, the command also connects those objects.

See Also

Adding Drivers to a Cone

Adding Adjacent Objects to a Cone

Adding Adjacent Objects to a Cone

You can add some of the objects that are connected to a net, pin, or instance to the active cone. These objects include the ones that have a pin driven by the selected net, output pin, or instance.

To add an adjacent object to a cone:

1. In the **NetlistViewer** or a **Logical Cone** window, select a pin, net, or instance connected to objects that you want to add to a cone.
2. Right-click the selected object, and choose **Add To Active Cone > Adjacent Logic**. The **Add Adjacent Logic** dialog box displays all instances connected to your selection.
3. Select one or several instances from the list.
4. Click **OK**.

The selected instance(s) are added to the active cone. If the added instances can be connected to other objects already present in the active cone, this command also connects those objects.

See Also

Adding Drivers to a Cone

Adding Driven Instances to a Cone

Cross-probing Between NetlistViewer and ChipPlanner

If both NetlistViewer and ChipPlanner are open, items selected in either tool are selected and highlighted in the other. ChipPlanner is Actel's floorplanning tool, which you use to create and edit regions on your chip and assign logic to those regions.

To use NetlistViewer with ChipPlanner:

1. Click **NetlistViewer** in the Designer Design Flow window. NetlistViewer starts and displays your netlist.
2. From the **Tools** menu, choose **ChipPlanner**. ChipPlanner opens in a separate window in the MultiView Navigator and displays the logic and I/O modules on the device as shown below.

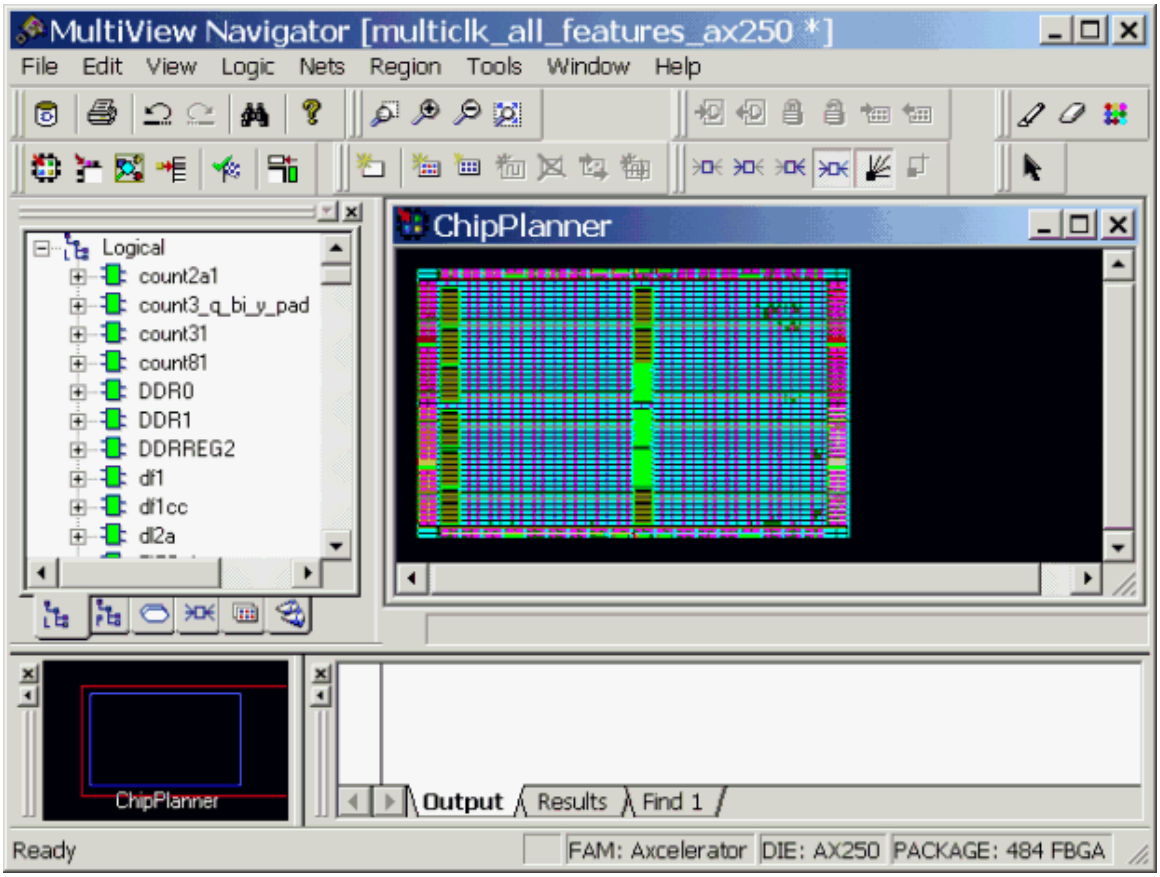


Figure 27 · ChipPlanner window

3. Select a macro or instance in either ChipPlanner or NetlistViewer. The selected item appears selected in both tools. The following example shows the selected item highlighted in both NetlistViewer and ChipPlanner.

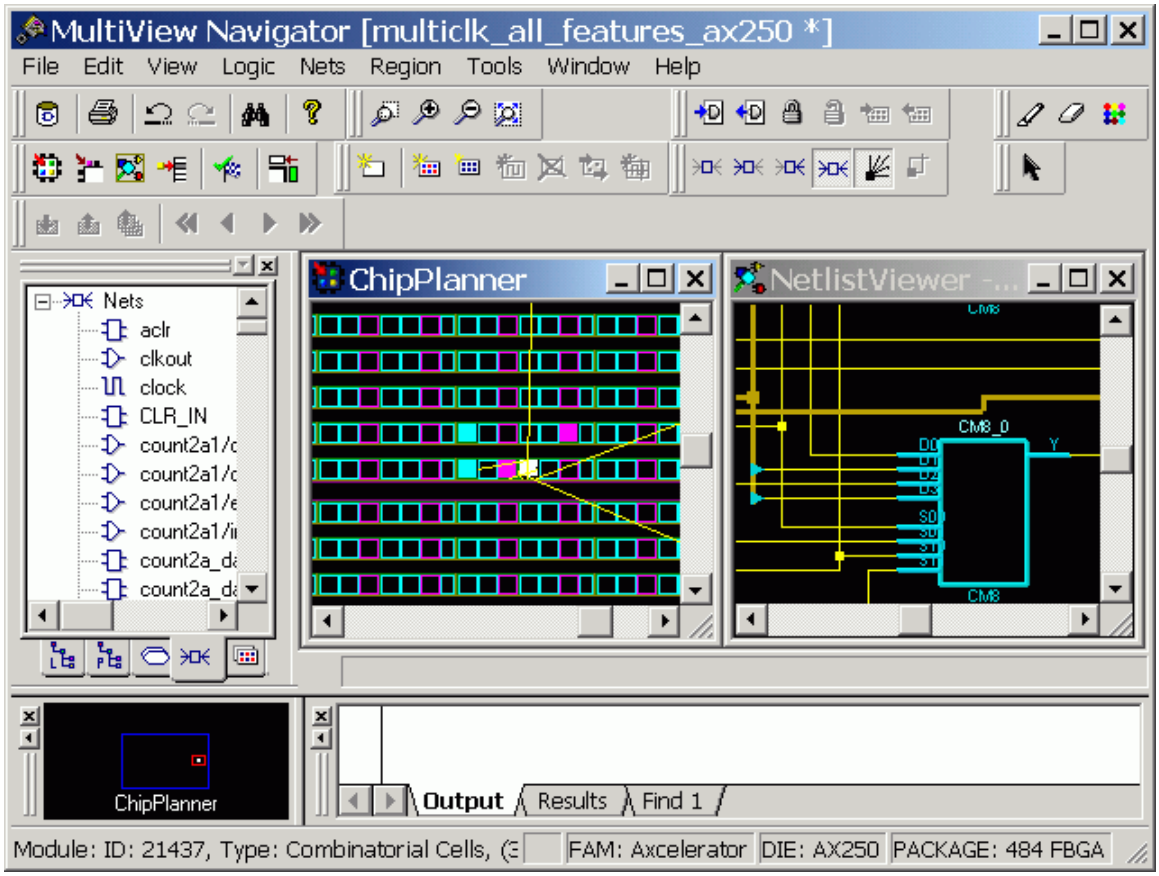


Figure 28 · Item Selected in NetlistViewer and ChipPlanner

See Also

Identifying Paths

Cross-probing Between NetlistViewer and SmartTime

Use NetlistViewer with SmartTime to view and trace entire Timing paths and to cross-probe one or more objects.

Note: Note: Your design must be compiled to start NetlistViewer. If it is not compiled, Designer prompts you to compile your design. After you compile it, NetlistViewer opens and displays the netlist.

To cross-probe an object using NetlistViewer and SmartTime:

1. In the **Design Flow** window, click **NetlistViewer** to display your netlist, and then click **Timing Analyzer** to display the **SmartTime Timing Analyzer**.
2. In the **SmartTimeTiming Analyzer**, select the clock domain in the **Domain Browser**.
3. Select a path in the **Paths List**, right-click it, and choose **Expand selected paths** from the right-click menu.
4. Select any instance in the **SmartTime Expanded Path View**. The instance appears highlighted in both SmartTime and NetlistViewer as shown in the following example.

Tip: Tip: To select multiple instances, hold down the Shift key as you click each instance.

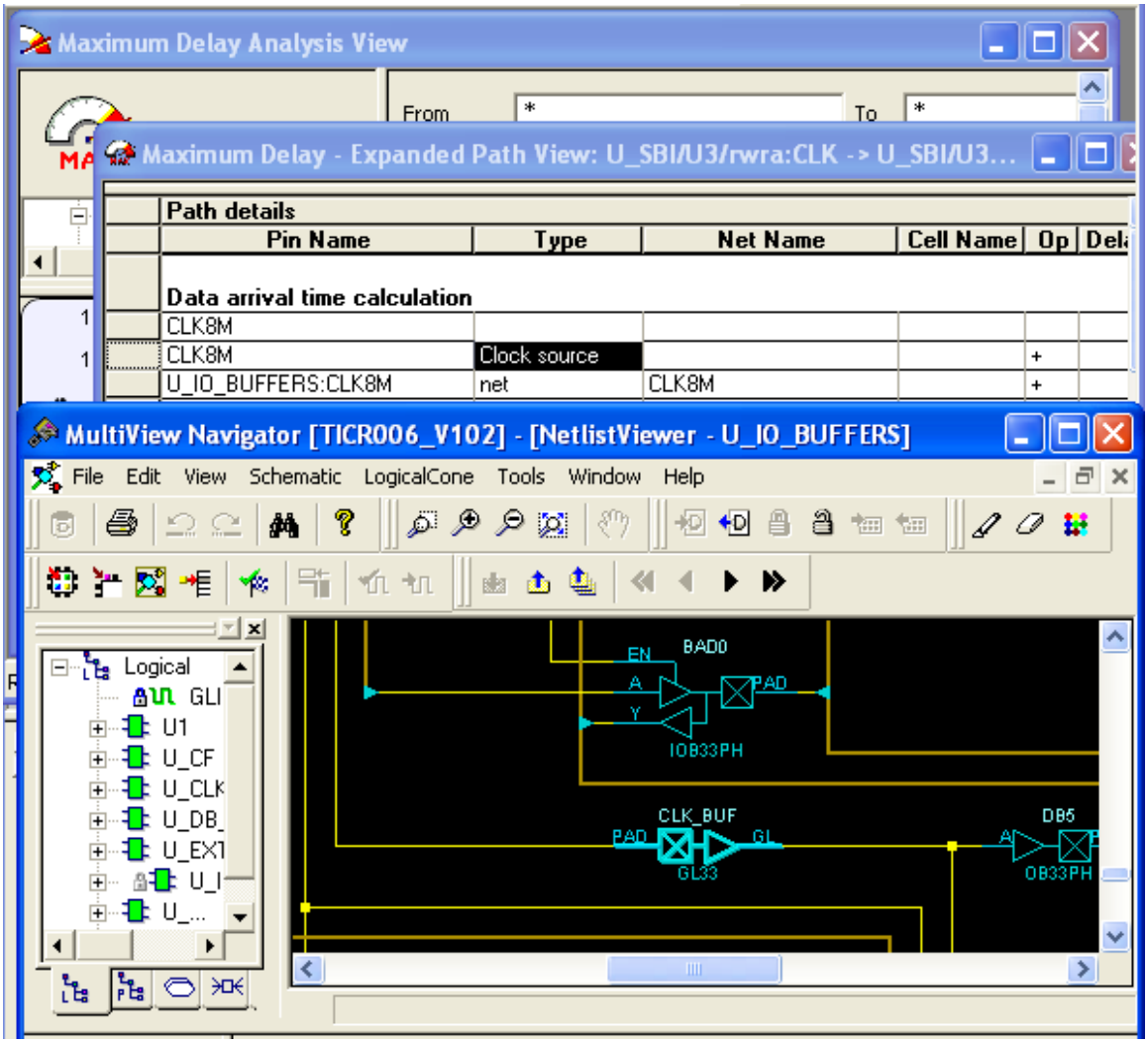


Figure 29 · Selected Instance Appears Highlighted in Both SmartTime and NetlistViewer

5. To cross-probe a path, right-click the path, and choose **Cross-probe Path** from the right-click menu (as shown in the following example).

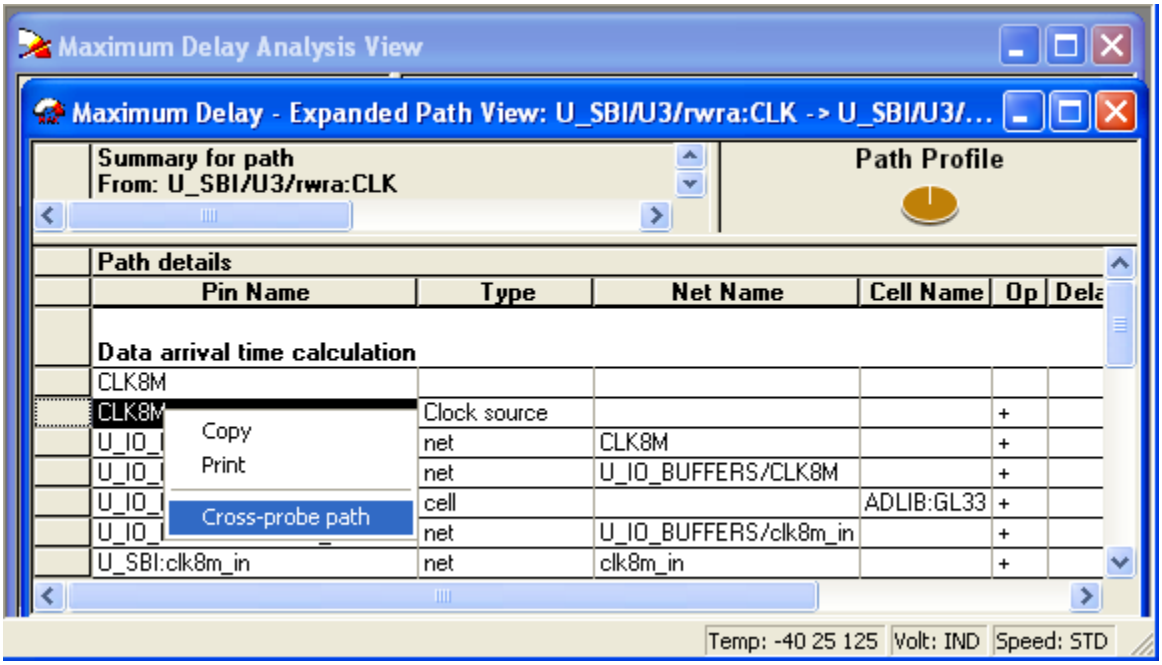


Figure 30 · Cross-probe Path Using Right-click Menu

All objects in the selected path appear highlighted in NetlistViewer as shown below.

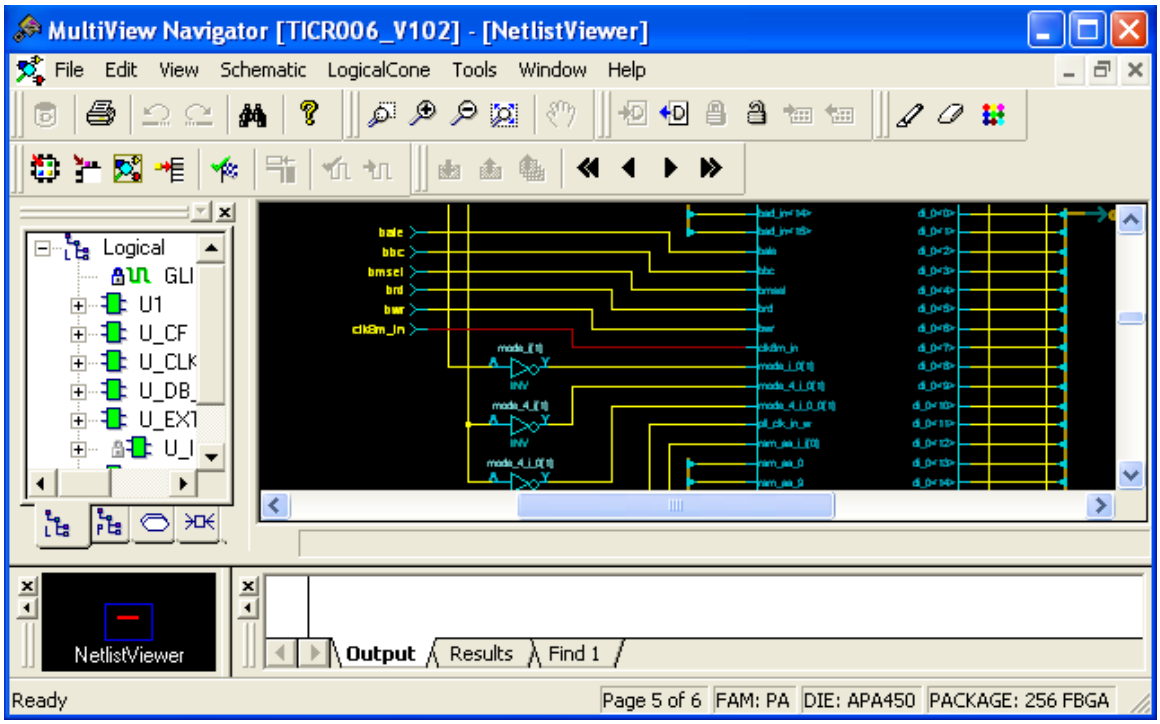


Figure 31 · All Objects in the Cross-probed Path Appear Highlighted in NetlistViewer

Tip: Tip: Changing the highlight color does not change the color of all cross-probed paths in NetlistViewer. To change the color of a cross-probed path, from the Edit menu, choose Highlight Color and select a different color. Then cross-probe the path again in SmartTime. The cross-probed path will appear in the new highlight color.

See the *SmartTime User's Guide* for more information.

See Also

Identifying Paths

Cross-probing between NetlistViewer and ChipPlanner

Viewing Buffers

You can use NetlistViewer to see buffers inserted by your synthesis tool due to the high-fanout number of some signals.

To view inserted buffers, click **NetlistViewer** in the Design Flow window. NetlistViewer starts and displays your netlist.

In the following example, the fanout of the DATAIN and RESET inputs of the design exceeds the specified value in the Synplify synthesis tool. To reduce the number of fanout for these signals, Synplify inserts two buffers in their path. You can use NetlistViewer to see these inserted buffers.

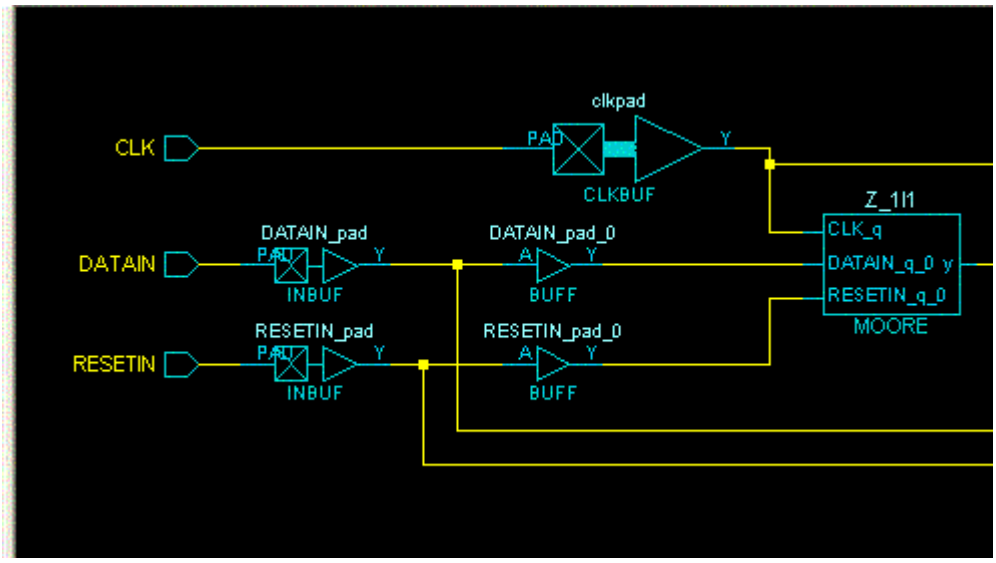


Figure 32 · Inserted Buffers

PinEditor

About PinEditor in MultiView Navigator

PinEditor is the package layout interface you use to assign I/O ports to package pins.

Note: This version of PinEditor supports only the IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, Axcelerator, SX-A, and eX families. If you are designing for other families, use the non-MVN version of PinEditor. See the PinEditor (non-MVN) online help or the *PinEditor (non-MVN) User's Guide* for more information.

Use PinEditor to:

- Assign I/O macros to pins
- Lock pin assignments that have automatically been assigned during layout
- View and print pin assignments
- Assign I/O standards to banks (for families that use I/O banks)
- Assign VREF pins (for I/O standards that require an input reference voltage)

Scripting Commands

You can make pin assignments, lock and unlock pins, commit pin assignments, and edit I/O attributes by running Tool Command Language (Tcl) scripts. You can run scripts from the Windows or UNIX command line or store and run a series of commands in a .tcl batch file.

See Also

Overview (MultiView Navigator)

Introduction to Tcl scripting in the Designer Users Guide

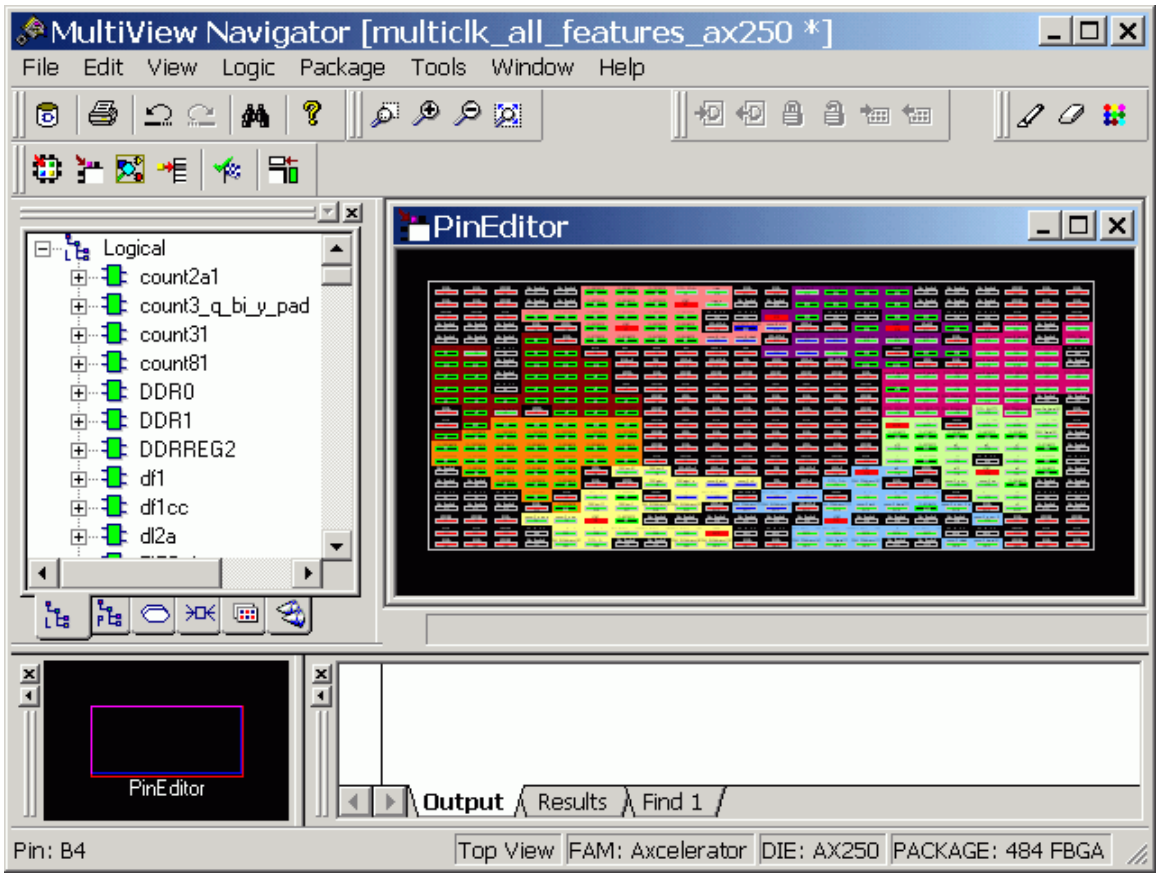
About Designer Tcl commands in the Designer Users Guide

Starting PinEditor in MultiView Navigator (MVN)

To start PinEditor from Designer, either click the **PinEditor** icon in the Designer Design Flow window, or from the **Tools** menu, choose **PinEditor**.

To start PinEditor from within MVN, either click the **PinEditor** button in the MVN toolbar, or from the **Tools** menu, choose **PinEditor**.

PinEditor opens in the Tools window of the MultiView Navigator interface and displays the pins and I/O macro assignments in your design. It also displays I/O banks for IGLOO, Fusion, ProASIC3, and Axcelerator families.



PinEditor in MultiView Navigator

When you select an assigned pin, the pin location appears selected in the World View window, and the I/O macro name is selected in the and hierarchy tabs.

You can display a top-down or bottom-up view of the package. To display a top-down view, from the **Package** menu, choose **View From Top**. To display a bottom-up view, from the **Package** menu, choose **View From Bottom**.

Colors and Symbols

Colors and symbols differentiate the pin and logic I/O macro assignments in PinEditor. The following table indicates the default colors assigned to pins.

Color	Definition
White border	A white border denotes a selected pin.
Green	A green border with a black center denotes a regular, unassigned pin. A pin with a grey or yellow border and a green center denotes a regular, assigned pin.
Blue	A blue border with a black center denotes a special, unassigned pin. A pin with a grey or yellow border and a blue center denotes a special, assigned pin. Special pins are pins that have some additional meaning to them. For example, pins used for JTAG are blue. When unassigned, special pins have additional descriptive text next to the pin number.
Grey with red center	Reserved pin. You use this pin for some specific purpose on the package, and you cannot assign it an I/O macro. Examples of such pins are ground and power.
Yellow	Yellow denotes *locked* assignments. If the assignment is selected, the symbol appears yellow. If the assignment is unselected, the border appears yellow.
Grey/black	A pin with a grey border and a black center denotes a pin that is not connected. You cannot use these pins, and they have no meaning.

Assigning Pins

Edits you make to pin assignments in PinEditor are permanent provided that they are locked and have been committed.

To assign an I/O macro to a pin:

1. Select the instance in the **Ports** tab of the **Hierarchy** window.
2. Drag the instance to the pin location. If the location is valid, the macro is assigned and automatically locked.

Note: If you assign a macro to a pin that has already been assigned a macro, the previously assigned macro becomes unassigned if it was not locked.

To assign multiple I/Os:

1. Select the I/Os from the **Ports** tab of the **Hierarchy** window.
2. From the **Logic** menu, choose **Assign to Location**.
3. In the **PinEditor** window, click each I/O location to which you want to assign the I/Os.

See Also

Unassigning Pins

Locking and Unlocking Pin Assignments

Closing and Committing Pin Assignments

Unassigning Pins

To unassign a macro from a pin:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Location**. This command is available only if the macro has been assigned to a location.

To unassign a macro from a region:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Region**. This command is available only if the macro has been assigned to a region.

Tip: You can also right-click the macro, and choose **Unassign From Region** or **Unassign From Location**.

To unassign all I/Os from a location, choose **Unassign All From Location** from the **Logic** menu. To unassign all I/Os from the selected region, choose **Unassign All From Region** from the **Logic** menu.

See Also

Assigning Pins

Locking and Unlocking Pin Assignments

Closing and Committing Pin Assignments

Locking and Unlocking Pin Assignments

Designer does not alter locked pins during Layout. Designer recognizes pins as locked when they are assigned in one of the following ways:

- Manually using PinEditor in a design schematic
- Using a PIN file (all Antifuse families except Axcelerator)
- Using a PDC file (IGLOO, Fusion, ProASIC3, and Axcelerator families only)
- Using a GCF file (ProASIC and ProASIC Plus families only)

Locked pins are permanent, provided you commit locked pins to your design before you exit PinEditor. To save changes to disk (in your ADB file), use the Save command in Designer before exiting PinEditor.

To lock pins:

1. Select the instance to lock in the **Ports** tab or in the **PinEditor** window. To select multiple pins, hold down the **CTRL** key and select multiple pins with your mouse.
2. From the **Logic** menu, choose **Lock**.

To lock all pins, from the Logic menu, choose Lock All.

Note: You can also lock pins in the I/O Attribute Editor by selecting the Locked check box. To lock all pins, select the entire column, hold the CTRL key, and click an empty checkbox to lock all pins in the selected column.

To unlock a pin:

1. Select the instance(s) to unlock in the Ports tab of the **Hierarchy** window or in the **PinEditor** window. To select multiple pins, hold down the **CTRL** key and select multiple pins with your mouse.
2. From the **Logic** menu, choose **Unlock**.

To unlock all pins, from the Logic menu, choose Unlock All.

Note: If you are using the I/O Attribute editor, clear a locked checkbox to unlock a pin.

See Also

Assigning Pins

Unassigning Pins

Closing and Committing Pin Assignments

Closing and Committing Pin Assignments

The changes you make to your pin assignments and I/O attributes in PinEditor are temporary until you commit them.

- To commit your pin assignments at any time, from the **File** menu, choose **Commit**. To run the Prelayout Checker in addition to committing your assignments, from the **File** menu, choose **Commit and Check**.
- To commit your pin assignments when closing PinEditor, click **Yes** when prompted.

Committing your changes saves them to the "working" design for this Designer session only.

To save changes made in PinEditor to disk, you must save your design by choosing **Save** from the **File** menu in Designer.

See Also

Assigning Pins

Unassigning Pins

Locking and Unlocking Pin Assignments

Setting PinEditor Properties

You can bring the selected macro into view in PinEditor by setting the **Move the display to show Selected Macro or Module** property.

This property brings the selected macro or module into view in the PinEditor window. By default, this property is selected. If you don't want to change your viewing area each time you select a macro or module, clear this check box.

To set PinEditor properties:

1. From the **View** menu, choose **Properties**.
2. In the PinEditor **Properties** dialog box, select the check box if you want to bring a macro or module into view when you select it, or clear the check box if you do not.
3. Click **OK**.

See Also

Colors and symbols

Changing an object's color

Changing an Object's Color

You can control the objects visible in your design and their displayed color.

To set display properties:

1. From the **View** menu, choose **Display Settings**. The **Display Settings** dialog box displays a list of all the architectural features you can turn on and off in PinEditor.

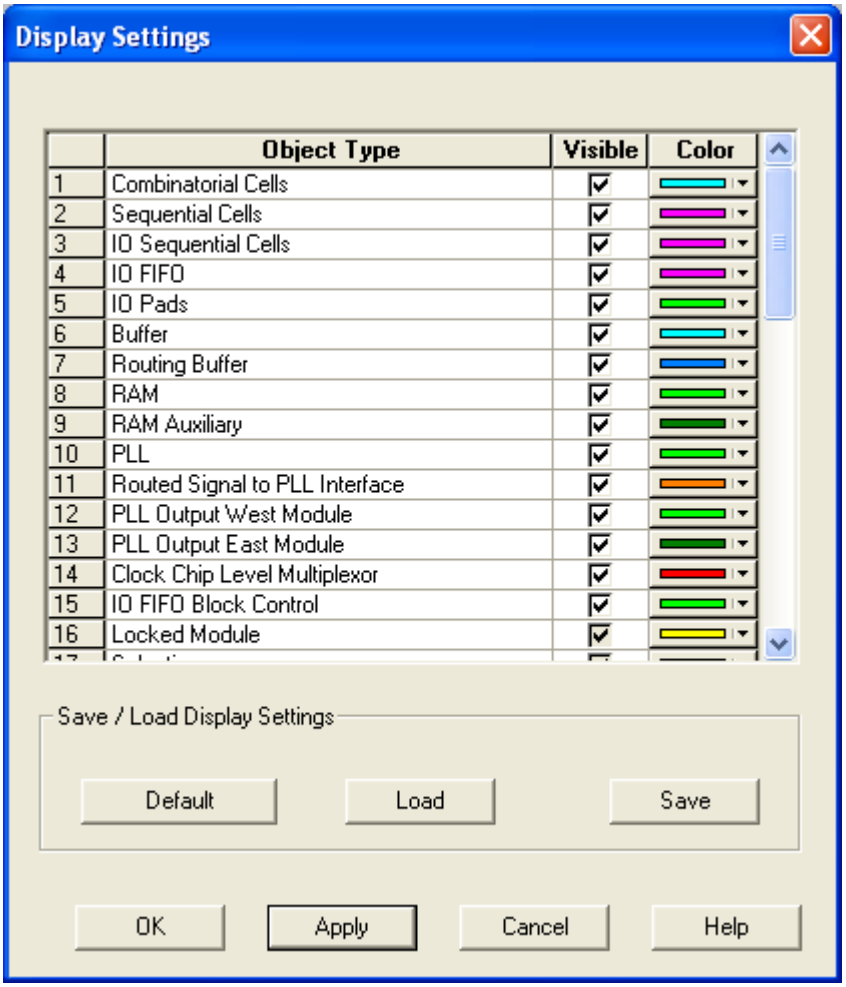


Figure 33 · Display Settings Dialog Box in ChipPlanner

2. To make an object visible, select the **Visible** check box
3. To change the color used to display the object, click its color bar and select another color.
4. To save or open previously saved Display Settings, click:

- Save to save your display settings to a file.
- Load to open a saved display settings file.

- Default to load the default display settings.

5. Click **Apply** to see your changes.
6. Click **OK** to dismiss the dialog box.

To change the color of an individual region:

1. Select the region.
2. Right-click the region, and choose **Properties.**
3. Select a different color from the **Color** drop-down list.

See Also

Colors and Symbols

Setting PinEditor Properties

Editing I/O Attributes

You edit I/O attributes using the I/O Attribute Editor tool. This tool displays all assigned and unassigned I/O macros and their attributes in a tabular format.

Use the I/O Attribute Editor tool to view, sort, select, and edit common and device-specific I/O attributes.

From the **Tools** menu, choose **I/O Attribute Editor**.

For descriptions of individual I/O attributes and support by family, refer to the I/O Attributes Reference section of the *Designer User's Guide*.

See Also

About I/O Attribute Editor

Specifying an I/O Standard

Common I/O Attributes (All Families)

I/O Attributes by Family

I/O Attribute Editor

About I/O Attribute Editor

Note: This version of I/O Attribute Editor supports only the IGLOO, Fusion, ProASIC3, ProASIC PLUS, ProASIC, Axcelerator, SX-A, and eX families. If you are designing for other families, use the non-MVN version of PinEditor, which includes an embedded I/O attribute editor. See the PinEditor (non-MVN) online help or the *PinEditor (non-MVN) User's Guide* for more information.

The I/O Attribute Editor opens within the Tools window of the MultiView Navigator. It displays all assigned and unassigned I/O macros and their attributes in a spreadsheet format.

Use I/O Attribute Editor to:

- View, sort, select, and edit common and device-specific I/O attributes
- Lock and unlock assigned attributes

See Also

Overview (MultiView Navigator)

Introduction to Tcl Scriptingin the Designer Users Guide

About Designer Tcl commandsin the Designer Users Guide

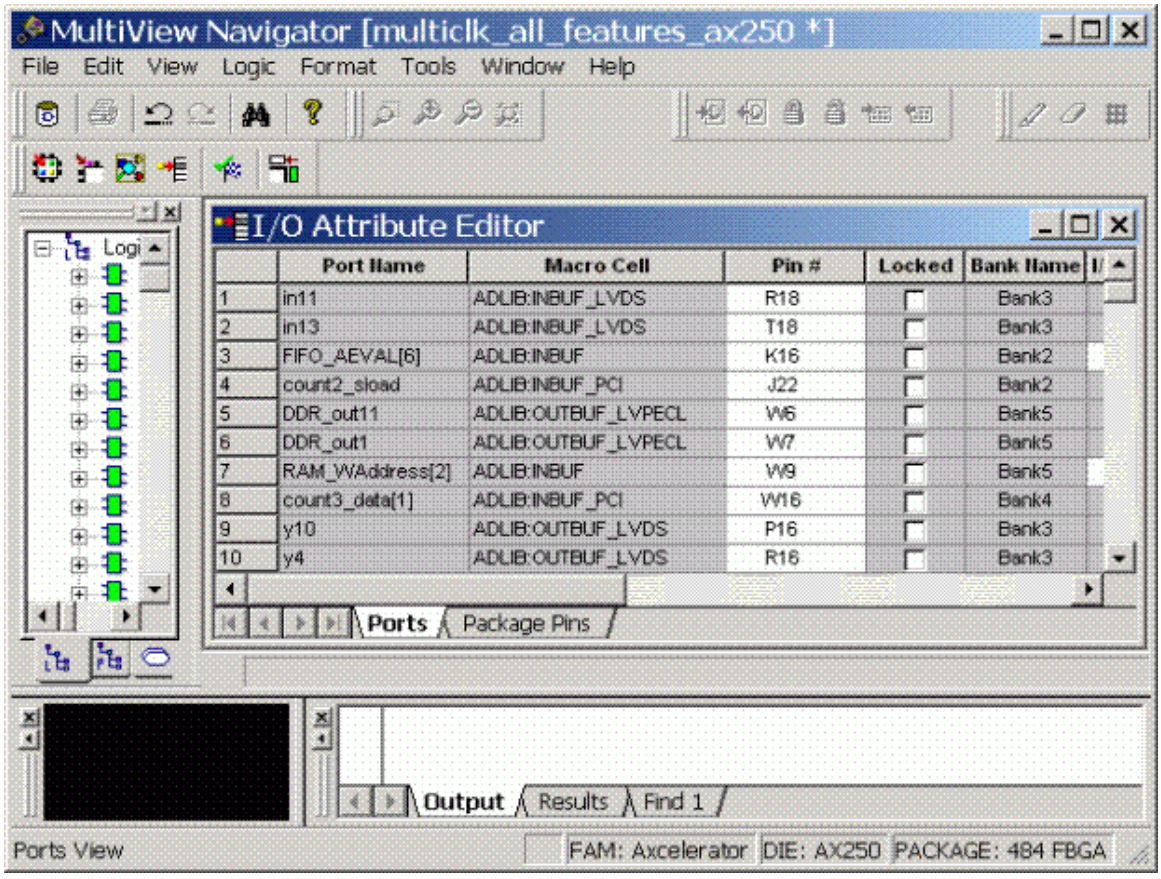
Starting I/O Attribute Editor

I/O Attribute Editor requires a compiled design. If you start I/O Attribute Editor before compiling your design, Designer compiles your design before opening I/O Attribute Editor.

To start I/O Attribute Editor from Designer, either click the **I/O Attribute Editor** icon in the Designer Design Flow window, or from the **Tools** menu, choose **I/O Attribute Editor**.

To start I/O Attribute Editor from within MVN, either click the **I/O Attribute Editor** button in the MVN toolbar, or from the **Tools** menu, choose **I/O Attribute Editor**.

The I/O Attribute Editor appears in the Tools window inside the MultiView Navigator and displays all assigned and unassigned I/O ports and their attributes in a tabular format. It functions much like a spreadsheet with sort, copy, and paste capabilities. Each row corresponds to either a port or a pin in the design, depending on which view you chose.



I/O Attribute Editor in MultiView Navigator

When you select a port name within the table, it also appears selected in the Logical, Physical, and Ports tabs of the Hierarchy window.

You can also start I/O Attribute Editor from Libero IDE. See Opening an Existing PDC File.

Assigning pins in Package Pins View

I/O Attribute Editor (v6.2 and higher) includes a Package Pins view in addition to its Ports view. Click the **Package Pins** tab to display your I/O attributes by package pin number. This view makes it much easier to assign address/data ports to adjacent pins. Additionally, it enables you to assign VREF pins (which you cannot do in Ports view) and to sort on banks.

Package Pins View

The Package Pins View displays all columns shown in the Ports view plus the following additional columns:

- Function
- Dedicated
- VREF
- User Reserved

Function is the functionality of the I/O (for example, GND or ground). See the datasheet for your device for details about each function.

Dedicated determines whether the pin is reserved for some special functionality, such as UJTAG / Analog Block / XTL pads inputs.

VREF (Voltage referenced), if checked, assigns the selected pin as a VREF. This column only appears for devices that support VREF (IGLOOe, Fusion, ProASIC3L A3PE3000L, ProASIC3E, and Axcelerator). A device supports VREF if one or more of its I/O banks support VREF. IGLOO (excluding IGLOOe) and ProASIC3 (excluding ProASIC3L A3PE3000L and ProASIC3E) devices are not supported.

User Reserved, if checked, reserves the pin for use in another design. When a pin is reserved, you cannot assign it to a port. To unreserve the pin, deselect the **User Reserved** check box.

Editing I/O Attributes

You edit I/O attributes using the I/O Attribute Editor. It displays all assigned and unassigned I/O macros and their attributes in tabular format.

Use the I/O Attribute Editor to view, sort, select, and edit common and device-specific I/O attributes.

You can view the I/O attributes by port or by package pin. Click the **Ports** tab to view I/O attributes by port name. Click the **Package Pins** tab to view I/O attributes by pin number.

Each row corresponds to an I/O macro (port) or a pin in the design, depending on the view displayed. The column headings specify the names of the I/O attributes in your design. The first four column headings are standard for all families so they will not change. However, the other column headings will change depending on the family you are designing for. For some I/O attributes, you will choose from a drop-down menu; for others, you might enter a value.

To edit I/O attributes:

1. Select an I/O standard for each I/O macro in your device.
2. Select I/O attributes that are available for your selected I/O standard.

For descriptions of individual I/O attributes and support by family, refer to the I/O Attributes Reference section of the *Design Constraints Guide*.

See Also

Editing Multiple Rows

Formatting Rows and Columns

Specifying an I/O Standard

Common I/O Attributes (All Families)

I/O Attributes by Family

Editing Multiple Rows

To edit multiple rows:

1. Select the rows to edit. To select consecutive rows, click the first row, press and hold down the **SHIFT** key, and then click the last row. To select rows that are not consecutive, press and hold down the **CTRL** key, and then click each row to select. Continue to hold down the **SHIFT** or **CTRL** key.
2. While still holding down the **SHIFT** or **CTRL** key, click in the cell containing the value you want to change. Release the **SHIFT** or **CTRL** key, and then release the mouse button.

The change occurs in all selected rows.

Note: Note: You can also select an entire column, which enables you to edit all rows in that column.

See Also

Editing I/O Attributes

Sorting Attributes

Formatting Rows and Columns

Common I/O attributes (All Families)

I/O Attributes by Family

Sorting Attributes

You can sort rows by column in either ascending or descending order.

To sort I/O macros by attributes:

- Double-click a column heading to sort the table rows in ascending order.
- Double-click the column again to sort the table rows in descending order.

When sorted, an arrowhead appears in the column header to indicate the sort order.

See Also

Formatting Rows and Columns

Editing Multiple Rows

Formatting Rows and Columns

When viewing and editing your input/output attributes, you can format the table to display only the attributes you want to see.

Note: Note: Clicking the top-left cell selects all rows in the I/O Attribute Editor.

To hide one or more rows or columns:

1. Select the row(s) or column(s) you want to hide from view.
2. From the **Format** menu, choose **Row > Hide** or **Column > Hide**, or right-click the row or column header and choose **Hide** from the right-click menu.

To show a hidden row or column:

1. Select a range of rows or columns that span one or more hidden rows or columns.
2. From the menu, choose **Row > Unhide** or **Column > Unhide**, or right-click the row or column header and choose **Unhide** from the right-click menu.

Note: Note: Unhide also works for a selected column that has a hidden column to its immediate left or right (or both).

You can "freeze" (or lock) one or more columns so they remain visible on the screen as you scroll horizontally.

To freeze or lock one or more columns:

1. Select the column to the right of the last column to freeze.
2. From the **Format** menu, choose **Column > Freeze Pane**, or right-click the column and choose **Freeze Pane** from the right-click menu.

To unfreeze one or more frozen columns, from the **Format** menu, choose **Column > Unfreeze Pane**, or right-click any column header and choose **Unfreeze Pane** from the right-click menu. All frozen columns are unfrozen.

You can also resize all the columns and rows at once so their entire contents are visible.

Note: Note: You must unfreeze the current locked group before you can freeze another group.

To display a column's entire contents within it:

1. Select the column(s) you want to display.
2. From the**Format** menu, choose **Column >AutoFit**. The width of the column either expands or contracts to fit only the cell heading and cell contents.

See Also

Sorting Attributes

Specifying an I/O Standard

Use the I/O Standard column to select an I/O specification for each pin.

If required to match the I/O standard, other I/O attributes, such as I/O threshold, slew, and loading, are automatically set to their default settings; you cannot edit these defaults.

You can change the I/O standards only for a generic I/O buffer to any of the legal I/O standards.

To specify an I/O standard:

1. Click the **I/O Standard** cell in the desired macro row.
2. Type or select a supported I/O standard from the drop-down list.

For devices that support I/O banks (for example, Axcelerator devices), the list is restricted to legal choices only. When an I/O is assigned, the I/O standards available for that I/O are limited to what the I/O bank location can support.

Note: Changing an I/O standard may also unassign existing I/Os. In addition, when a macro is assigned an I/O standard, the I/O bank is automatically assigned the voltages VCCI and VREF, if necessary. Unassigning this macro will undo these assignments as well.

See Also

I/O Attributes by Family

Common I/O Attributes (All Families)

The I/O Attribute Editor displays four common attributes for all I/O macros:

- **Port Name** indicates the I/O macro name.
- **Macro Cell** indicates the type of I/O macro.
- **Pin #** indicates the current pin assignment.
- **Locked**, if checked, indicates that you cannot change the current pin assignment during layout.

Besides the common I/O attributes, the I/O Attribute Editor displays device-specific attributes such as I/O Standard, Skew, and Output Load. Only attributes applicable to a specific device appear in the I/O Attribute Editor table.

I/O Attributes by Family (in MVN)

The following table displays the attributes supported for each family.

Attribute	Family							
	IGLOO	Fusion	ProASIC3	ProASIC PLUS	ProASIC	Axcelerator	SX-A	eX
Bank Name	X	X	X			X		
I/O Standard	X	X	X			X	X	X
I/O Threshold	X, IGLOO PLUS only						X	X
Output Drive	X	X	X			X		
Slew	X	X	X			X	X	X
Power Up State							X	X
Resistor Pull	X	X	X			X		
Schmitt Trigger	X, IGLOOe and IGLOO PLUS only	X	X, ProASIC3e and ProASIC3L only					
Input Delay	X, IGLOOe and IGLOO PLUS only	X	X, ProASIC3e and ProASIC3L only			X		
Skew	X	X	X					

Attribute	Family							
	IGLOO	Fusion	ProASIC3	ProASIC PLUS	ProASIC	Axcelerator	SX-A	eX
Output Load	X	X	X	X	X	X	X	X
Use Register	X	X	X			X		
Hot Swappable	X	X	X			X		X
Hold State	X, IGLOO PLUS only							
User_Reserved	X	X	X, ProASIC3e and ProASIC3L only			X		

Refer to the appropriate datasheet for information about I/O standards for different families.

Note: For Fusion and ProASIC3L devices, not all attributes apply to all banks for a given I/O standard. Refer to the Fusion and ProASIC3L datasheets for details.

See Also

Common I/O attributes (all families)

Design Constraints Guide: I/O AttributesI/O Attributes by Family (all families)

ChipPlanner

About ChipPlanner in MultiView Navigator

ChipPlanner is the floorplanning tool you use to create and edit regions on your chip and assign logic to these regions. You can also use it to view routing information and influence place-and-route for more optimal results. This tool is particularly useful when you need maximum control over your design placement.

Note: ChipPlanner supports only the IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, Axcelerator, SX-A, and eX families. If you are designing for other families, use ChipEditor. See the ChipEditor online help or the *ChipEditor User's Guide* for more information.

Use ChipPlanner to:

- View macro assignments made during layout
- Assign, unassign, or move macros
- Lock macro assignments
- View net connections using a ratsnest or route view
- View architectural boundaries
- View and edit silicon features, such as I/O banks
- Create Regions and assign macros or nets to regions (floorplanning)
- View placement and routing of paths when used with SmartTime

Using PDC Files (IGLOO, Fusion, ProASIC3, and Axcelerator only)

Any constraint that you can enter using ChipPlanner, you can also enter using a Physical Design Constraint (PDC) file. A PDC file is a Tool Command Language (Tcl) script file specifying physical constraints. This file can be imported and exported from Designer. PDC files replace the PIN file for the Axcelerator family.

Using GCF Files (ProASIC and ProASIC Plus only)

Any constraint that you can enter using ChipPlanner, you can also enter using a GCF file. A GCF file is a constraint file specifying placement or timing constraints. This file can be imported and exported from Designer.

See the *Designer User's Guide* for more information about PDC and GCF files.

See Also

Overview (MultiView Navigator)

Starting ChipPlanner

Starting ChipPlanner

ChipPlanner requires a compiled design. If you start ChipPlanner before compiling your design, Designer guides you through the compile process before opening ChipPlanner.

To start ChipPlanner from Designer, either click the **ChipPlanner** icon in the Designer Design Flow window, or from the **Tools** menu, choose **ChipPlanner**.

To start ChipPlanner from within MVN, either click the **ChipPlanner** button in the MVN toolbar, or from the **Tools** menu, choose **ChipPlanner**.

ChipPlanner opens in the Tools window of the MultiView Navigator interface and displays pins and I/O macro assignments. For IGLOO, Fusion, ProASIC3, Axcelerator, eX, and SX-A families, it also displays I/O banks.

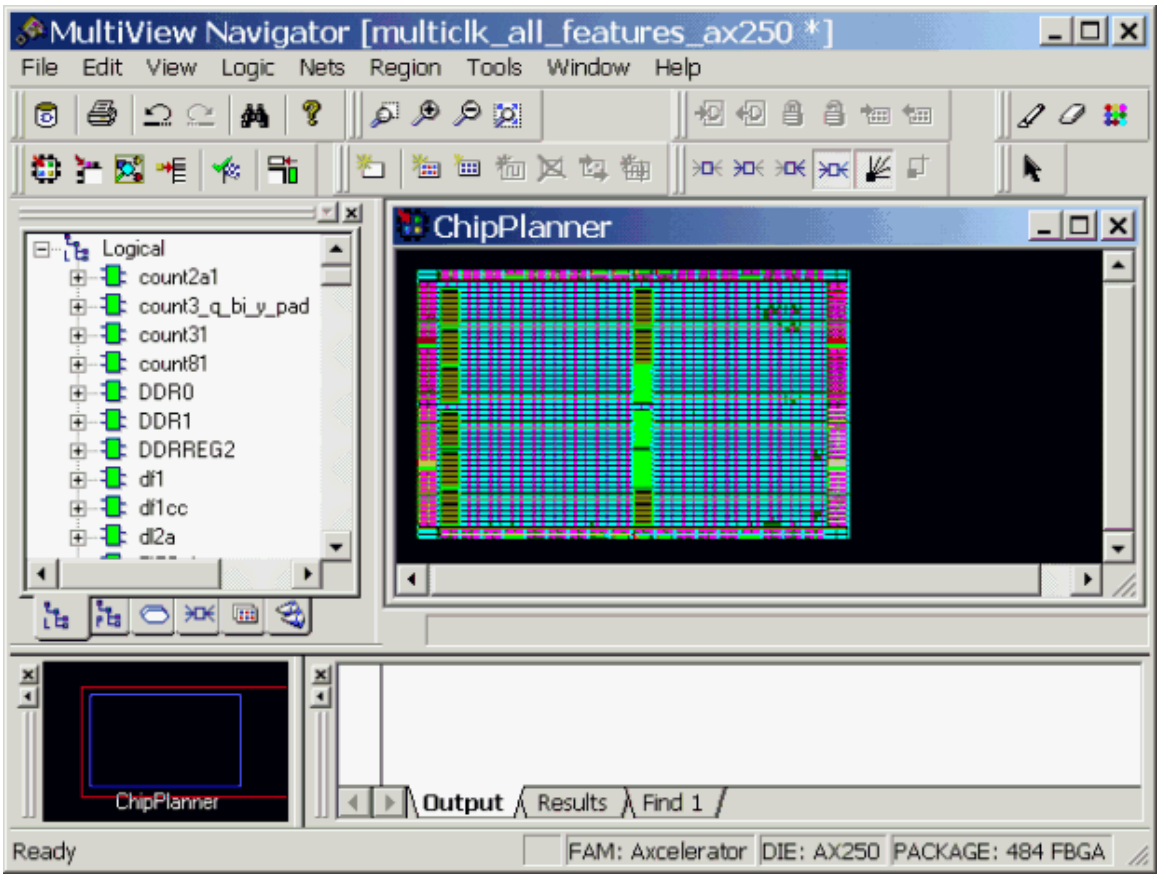


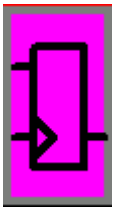
Figure 34 · ChipPlanner in MultiView Navigator

When you select an assigned macro, the macro location appears selected in the World window, and the I/O macro name is selected in the Logical and Physical hierarchy tabs.

Colors and Symbols

Colors and symbols differentiate the I/O and logic macros in ChipPlanner. The following table defines the default colors assigned to symbols. You can change these colors per design.

Color	Definition
White Border	A white border denotes a selected object.
Black Background	A black background denotes an unused or unassigned module.
Blue	Blue denotes a combinatorial module.
Yellow	Yellow denotes *locked* logic modules. If the module is selected, the symbol appears yellow. If the module is unselected, the border appears yellow.
Green	Green denotes I/O modules.
Red	Red denotes clock modules.
Magenta	Magenta denotes sequential modules.
	Reserved modules that are not user definable are gray, crossed-out symbols on a black background.
	Clock modules are red. Unused/unassigned modules are red symbols on a black background. Used/assigned modules are black symbols on a red background.
	Input/Output modules are green. Unused/unassigned modules are green symbols on a black background. Used/assigned modules are black symbols on a green background.
	Combinatorial modules are blue. Unused/unassigned modules are blue symbols on a black background. Used/assigned modules are black symbols on a blue background.

Color	Definition
	Sequential modules are magenta. Unused/unassigned modules are magenta symbols on a black background. Used/assigned modules are black symbols on a magenta background.
	Buffer modules are blue.
	RAM modules are green. Unused/unassigned modules are green symbols (RAM) on a black background. Used/assigned modules are black on a green background.
	PLL modules are green. Unused/unassigned modules are green symbols (PLL) on a black background. Used/assigned modules are black on a green background.
	I/O Inbuff modules are pink on a black background. Used/assigned modules are black on a pink background.

Setting ChipPlanner Properties

You can bring the selected macro or net into view in ChipPlanner by setting the **Move the display to show Selected Macro** and **Center display around Selected Net** properties.

The first property brings the selected macro into view in the ChipPlanner window. Likewise, the second one brings the selected net into view and zooms into the selected net. By default, both properties are selected. If you do not want your viewing area to change when you select a macro or net, you can clear these check boxes.

To set ChipPlanner properties:

1. From the **View** menu, choose **Properties**.
   Note: You can also right-click anywhere in the **ChipPlanner** window, except on a region, and choose **Properties** from the right-click menu.
2. In the **ChipPlanner Properties** dialog box, clear one or both check boxes.
3. Click **OK**.

Changing Colors

You can control which objects are visible in your design and what color they are.

To set display properties:

1. From the **View** menu, choose **DisplaySettings**. The Display Settings dialog box displays a list of all the architectural features you can turn on and off in your tool.
2. To make an object visible, select the **Visible** check box.
3. To change the color used to display the object, click its color bar and select another color.

To save or open previously saved display settings, click:

1. **Save** to save your display settings to a file.
2. **Load** to open a saved display settings file.
3. **Default** to load the default display settings.
4. Click **Apply** to see your changes.
5. Click **OK** to dismiss the dialog box.

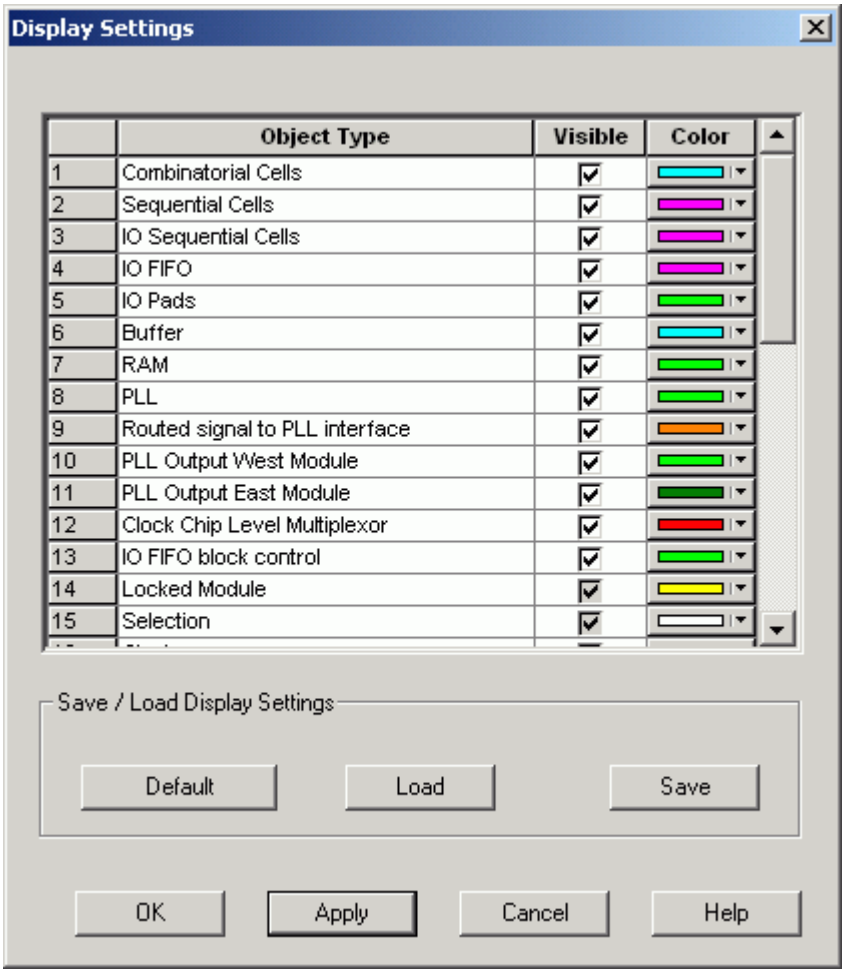


Figure 35 · Display Settings Dialog Box in ChipPlanner

Floorplanning

About Floorplanning

Floorplanning includes creating regions and making logic assignments to those regions. It is an optional methodology you can use to improve the performance and routability of your design. The objective in floorplanning is to assign logic to specific regions on the chip to enhance performance and routability.

When floorplanning, you analyze your design to see if certain logic can be clustered within regions. Clustering is especially helpful for hierarchical designs with plenty of local connectivity within a block. If your timing analysis indicates several paths with negative slack, try clustering the logic included in these paths into their own regions. This forces the placement of logic within the path closer together and may improve timing.

Use ChipPlanner before and after running Layout to help you floorplan.

See Also

Creating Regions

Assigning a Macro to a Region

Assigning a Net to a Region

Floorplanning a Designer Block

Actel recommends that you floorplan your Designer Block component (in MVN or with PDC commands) to ensure that your Designer Block is placed in a specific region. If you do not restrict your Designer Block placement, it may be placed anywhere on your die; see the define_region PDC command.

It is also important to consider the placement of all interface macros in the boundaries of these regions. This facilitates the interconnection of the Designer Block to the top-level design. If the Designer Block is highly optimized (densely packed) there may be no routing channels available to connect to any internal Designer Block interface macro. Placing all interfaces at Designer Block boundaries helps you eliminate routability issues, routing congestion, and failure.

Designer-Block specific features in MVN are:

- Block Ports tab - Lists all the ports in a Designer Block even if they are not connected to I/Os.
- Interface Instances in Designer Block creation (in the Active Lists) - Lists all macros connected to ports. These macros must be placed on the boundary of your Designer Block region, since they will be connected to the <top> design.
- Designer Block content available when you instantiate a Designer Block in the <top> design (in Active Lists) - Lists all macros in the Designer Block.
- A block tab that lists all the blocks in your design.
- Search support that enables you to find a specific block in your design.
- Show the routing of locked nets from the Designer Blocks immediately after compile is complete; no need to wait until layout is finished since the routing is locked and will not be changed.

About Regions

A region is a user-defined area on the device. When floorplanning, you can assign logic to regions to improve the design performance. You can use ChipPlanner to create regions or create them with PDC or GCF commands.

Note: You cannot create regions for ex and SX-A families.

ChipPlanner supports the following types of regions:

Logic Region (Inclusive/Exclusive)

A logic region is a region that has logic assigned to it. Logic can include core logic, memory, and I/O modules. The place-and-route tool will place all the logic assigned to a logic region inside that region. The floorplanning process usually requires you to create several regions and assign logic to them.

Logic regions can either be inclusive or exclusive. If a logic region is exclusive, it means that the place-and-route tool cannot place any logic within the region other than what you have previously assigned to it. If a logic region is inclusive, the place-and-route tool can place any logic within the region. Exclusive regions are not supported for ProASIC and ProASIC PLUS devices. However, exclusive regions are supported for IGLOO, Fusion, and ProASIC3 devices.

Empty Region

To prevent logic from being placed within a predefined area in the device, you can create an empty region. The place-and-route tool will not place any logic within an empty region; however, the routing resources within the region can be used.

Local Clock Regions

A local clock is a portion of the global clock network on the device. Local clock regions are inclusive by default and cannot be changed. Each family has different local clock capabilities. For specific details, see the datasheet for your device.

Quadrant Clock Regions

A quadrant clock is a portion of the global clock network on the device. Each family has different quadrant clock capabilities. For specific details, see the datasheet for your device. You create and delete a quadrant clock in the same way that you create a local clock in IGLOO and ProASIC3 devices.

Overlapping Regions

If you create Logic regions whose areas intersect, the regions are defined to be overlapping. The place-and-route tool will detect the area where these regions intersect and try to place logic common to both of them within this area.

Blocks and Regions

Nets driving a block can be assigned to regions, local clocks, and quadrant clocks. VREF I/Os are not supported in the top design if the block has I/Os.

See Also

Creating Regions

Using Empty Regions

Using Logic Regions

Using Local Clock and Quadrant Clock Regions

Editing Regions

Creating Regions

With ChipPlanner, you can create empty, exclusive, inclusive, QuadrantClock and LocalClock regions under certain conditions:

Table 2 · Types of Regions

Region Type	Conditions
Empty	• Cannot assign macros to an empty region • Cannot create empty regions in areas that contain locked macros
Exclusive	• Only contains macros assigned to the region • Not supported in ProASIC and ProASIC PLUS
Inclusive	• Contains all macros, both assigned and unassigned to the region
LocalClock	• Can create LocalClock regions for ProASIC and ProASIC PLUS devices either in ChipPlanner or in a GCF file • Can create LocalClock regions for IGLOO, ProASIC3, and Axcelerator devices in a PDC file • Cannot resize or move a LocalClock region • Cannot assign logic to a LocalClock region
QuadrantClock	• Can assign CORE, RAM, and I/Os to QuadrantClock regions that are inclusive • Can create QuadrantClock regions only for IGLOO and ProASIC3 devices

Note: To create an empty or logic region:

1. From the **Region** menu, choose **CreateEmpty, Create Exclusive,** or **Create Inclusive**.
2. Click and drag the mouse over the area where you want the region to be placed. As you drag out the region, a tooltip appears in its lower-right corner, showing you how many tiles, RAMs, and I/Os are in the region.

To create a LocalClock region:

1. In the **Net** tab of the Hierarchy window, select a clock net. Clock nets have a clock icon next to them in the Net view.
2. From the **Region** menu, choose **Create LocalClock**,or click its icon in the toolbar.
3. Click and drag a rectangle from the top-left corner of the new LocalClock region to its bottom-right corner. As you drag out the region, a tooltip appears in its lower-right corner, showing you how many tiles, RAMs, and I/Os are in the region.

To create a QuadrantClock region:

1. In the **Net** tab of the Hierarchy window, select a clock net. Clock nets have a clock icon next to them in the Net view.
2. From the **Region** menu, choose **Create QuadrantClock**,or click its icon in the toolbar. “Select a point in the Chip...” appears in the status bar.
3. Select a point in the chip that is driven by QCLK. ChipPlanner creates a QuadrantClock region for the given net. The region name is Qclock_<netname> and appears in the **Regions** tab of the Hierarchy View window. A tickmark appears next to the net in the Net tab and next to all the macros driven by it.

See Also

Creating LocalClock Regions

Creating QuadrantClock regions

Using Empty Regions

Empty regions allow you to create exclusive areas on the device where no logic placement can occur. Empty regions help guide the placer to pack your logic closer together and thereby use more local routing resources to connect it. You cannot create empty regions in areas that contain locked macros. Use the following guidelines for empty regions.

Use Empty Regions to Guide the Place-and-Route Process

If your design does not completely use up your target device (for example 60% utilization or lower), use empty regions to cluster your logic placement into specific subareas of the chip. This helps when you have originally placed-and-routed the design into a smaller device but want to fit it to a larger part while still preserving the performance you have achieved in the smaller device.

Use Empty Regions to Reduce Routing Congestion

Creating empty regions next to the congested area(s) of your design helps reduce congestion. When you place an empty region next to congested logic blocks or regions, the placer cannot place any logic next to your region or logic block. Logic, which would normally be placed there, is forced to be placed somewhere else. Routing resources next to the congested area are, therefore, freed up and provide the router more options to route signals into the congested block.

Before deciding to place empty region(s), analyze your design for congestion areas. Use the **Ratsnest** view in ChipPlanner to see dense areas of connectivity into and out of your logic blocks or regions. Create empty regions in these congested areas and see it if improves the routability of your logic.

Use Empty Regions to Reserve Device Resources

If you want to preserve the placement of your existing design but plan additional modifications in the future, create empty regions in the areas of the chip where you plan to add additional logic. As you add new logic, remove or resize your empty regions accordingly to fit your new logic. Empty regions placed over I/O pins reserve them for future use as the I/O needs of your design changes. There are some restrictions for using empty regions in this manner. See the *Floorplanning ProASIC/ProASIC PLUS Devices for Increased Performance* application note for more details.

See Also

Creating Regions

Using Logic Regions

Using LocalClock and QuadrantClock Regions

Editing Regions

Using Logic Regions

Use Logic regions to condense the placement of certain logic blocks in your design. This allows you to control logic placement at the region or block level. This may simplify your floorplanning task, since you might not have to place logic instances individually on the device. The following sections contain guidelines for using Logic regions.

Use Logic Regions to Localize Placement of Logic Blocks

If you partitioned your design into several modules, and some of these modules contain regular structures (such as arithmetic logic, register arrays, counters, or multiplexors), place these modules into Logic regions. These logic functions have a good amount of both local connectivity and regularity to their structure, which makes them good candidates for regions. Interconnects between your regions now become interconnects between hierarchical blocks in your design. Floorplan your regions so there is a smooth horizontal or vertical data flow between each Logic region.

For Pipelined Logic, Place Registers on Region Boundaries

If you assigned logic to a region so its inputs and outputs are bounded by a register array (pipeline registers), it is a good idea to place these pipeline registers close to the boundary of the region. If you plan to manually fix the placement of your pipeline registers, make sure you orient them in the correct direction to assure a smooth data flow between them and their interfacing logic.

Aligning RAM I/O with Placement

Before placing your memory blocks, review your design and understand how data is flowing into and out of them. Determine what logic blocks are driving the memory inputs (for example, address line, control signals) and what logic is driven by the memory outputs (for example, databus lines). Follow these guidelines:

- Place pins that drive or are driven by your memory blocks close to where your memory blocks are placed.
- Create an empty region next to your memory block to free up local routing resources that may need to be used to connect to the memory blocks.
- If you are driving high fan-in memory inputs such as read/write clocks or read/write enables, try using low-skew routing resources such as global nets or clock spines to connect them. Make sure your clock spine assignments are aligned with your RAM placement.

See Also

Creating Regions

Using Empty Regions

Using LocalClock and QuadrantClock Regions

Editing Regions

Using Local Clock and Quadrant Clock Regions

Use a quadrant clock when you want to drive all instances within one quadrant. Use a local clock when you want to drive instances within the entire chip.

Table 3 · Local Clock and Quadrant Clock Regions by Family

Families	Create Local Clock Region in ChipPlanner?	Create Local Clock Region using PDC or GCF file?	Create Quadrant Clock Region in ChipPlanner?	Create Quadrant Clock Region using PDC or GCF
IGLOO	No	Yes, PDC file	Yes	Yes, PDC file
Fusion	No	Yes, PDC file	Yes	Yes, PDC file
ProASIC3	No	Yes, PDC file	Yes	Yes, PDC file
ProASIC PLUS	Yes	Yes, GCF file	No	No
Axcelerator	Yes	Yes, PDC file	No	No

Note: The IGLOO family includes IGLOOe, IGLOO PLUS, and IGLOO devices. The ProASIC3 family includes ProASIC3L, ProASIC3E, and ProASIC3 devices.

See the *Floorplanning ProASIC/ProASIC PLUS Devices for Increased Performance* application note for more information about assigning LocalClocks.

See Also

Creating Regions

Using Empty Regions

Using Logic Regions

Editing Regions

Editing Regions

After creating regions, with the exception of LocalClock regions, you can rename, delete, move, and re-size them. LocalClock regions can only be renamed or deleted.

Regions must have unique names. Two regions cannot have the same name.

To change the name of a region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the region with the name you want to change.
3. From the **Region** menu, choose **Properties**.
4. In the **Properties** dialog box, type the new region name over the existing one.

Tip: Tip: You can also right-click a region, choose **Properties**, and type a new region name in the **Properties** dialog box.

To delete a region:

- Right-click the region, and chose **Delete**.

To move a region:

- Select the region and drag it to a new location.

Note: Note: You cannot move the region if a macro assigned to the region is locked.

To re-size a region:

1. Select the region.
2. Grab and drag the sides and corners to re-size the region. You cannot resize a region smaller than the logic it already contains.

To merge a region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the regions you want to merge.
3. Right-click any selected region and choose **Merge**.

The merge operation:

- Creates a new region with rectangles of all selected regions
- Assigns logic and nets that were assigned to the selected region to the new region
- Removes the selected regions

See Also

Creating Regions

Using Empty Regions

Using Logic Regions

Using Local Clock and Quadrant Clock regions

Locking Regions

Assigning a Macro to a Region

During floorplanning, you can improve design performance by assigning macros to regions.

Note: Note: You can use the Logical or Physical tab right-click menus to bypass the Assign Instances to Region dialog box and assign instances to regions directly. To do so, in the Hierarchy window, Logical/Physical tab, select one or more instances, right-click and choose Assign to Region.

Note: You can also use the right-click menu to assign instances in the results from the ActiveLists and in results from the Find command (in the Log window).

To assign a macro to a region:

1. In the Regions tab of the Hierarchy window, right-click a region and choose **Assign/Unassign Instance**from the right-click menu. The **Assign Instances to Region** dialog box appears with the name of the selected region in the **Region name** field. The dialog box displays all the macros that you can assign to the selected region.

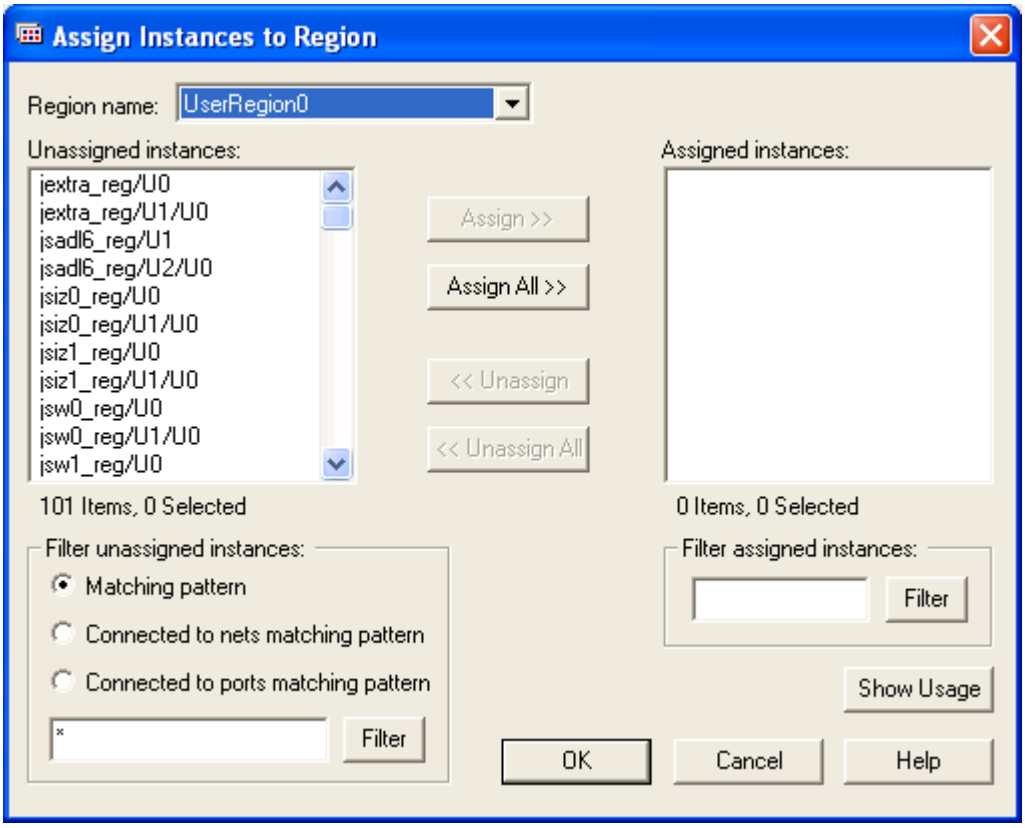


Figure 36 · Assign Instances to Region Dialog Box

2. To display a subset of the unassigned instances, you can create and apply filters. To filter the unassigned instances list by a pattern, enter the pattern (string) in the text box to the left of the Filter button, select **Matching pattern**, and then click **Filter**. Only the instances that match the pattern appear in the **Unassigned**

Instances list. For example, enter *U18* to display only unassigned instances containing the characters U18. You can also display only instances connected to net or port names matching the specified pattern. These filters are valid for both regular and Block flows. In regular flows, each port is connected to only one instance, which is an I/O.

3. To assign specific instances to the region, select one or more instances in the **Assignable Instances** list box, and then click **Assign**. To assign all instances to the region, click **Assign All.**
4. Click **OK**.

The total number of instances that you can assign as well as the number of currently selected unassigned instances appears under the list box.

Tip: Tip: You can also assign logic to regions from the Hierarchy window. To do so, drag and drop the logic from the Hierarchy window to the region.

See Also

Unassigning a Macro from a Region

Assigning a Net to a Region

Assigning a net to a region results in assigning all instances connected by the net to the specified region. The assignment of all instances of a net to a region packs logic more closely together, which improves (reduces) net delays.

Assigning nets to regions also enables you to apply floorplanning constraints correctly over design iterations. During design iterations you may change your design, causing a change in the instances connected by a particular net. The assignment of a net to a region assigns all instances connected by that net in the current design iteration, enabling your constraints to be applied correctly.

Note: Note: You can use the right-click menu to assign a net to a region. To do so, select one or more nets in the Nets tab of the Hierarchy menu, right-click, and choose Assign to Region. Using the right-click menu assigns all instances except the driver macro.

Note: You can also use the right-click menu to assign nets in the ActiveList, and in the results from the Find command (in the Log window).

To assign a net to a region:

1. In the Regions tab of the Hierarchy window, right-click a region and choose **Assign/Unassign Net** from the right-click menu.

The **Assign Nets to Region** dialog box appears with the name of the selected region in the **Region name** field. The dialog box displays all the nets that you can assign to the selected region (as shown in the figure below).

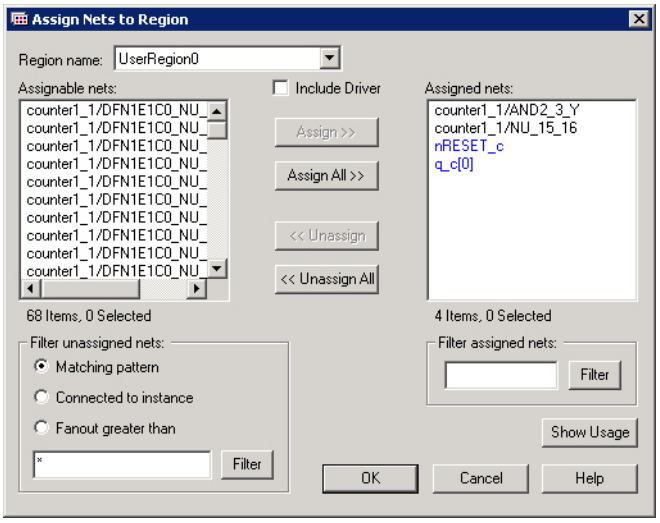


Figure 37 · Assign Nets to Region Dialog Box

To display a subset of the unassigned nets, you can create and apply filters.

2. To filter the unassigned nets list by a pattern, enter it in the text box to the left of the Filter button, select **Matching pattern**, and then click **Filter**. Only the nets that match the pattern appear in the Assignable nets list. For example, enter *INV* to display only unassigned nets containing the characters INV.

3. To assign specific nets, select one or more nets in the **Assignable nets** list box, and click **Assign**.

To select all nets, click **Assign All**.

Check the Include Driver checkbox to assign all instances, including the driver connected by the selected net, to the region.

3. Click **OK** to continue.

The total number of nets that you can assign, as well as the number of currently selected unassigned nets, appears in the list box.

Tip: Tip: You can assign nets from the Hierarchy window. To do so, drag and drop the nets from the Hierarchy window to the region in ChipPlanner.

See Also

Editing Regions

Assigning a Macro to a Region

Assigning Nets to Regions Dialog Box

Unassigning a Macro from a Region

To unassign a macro from a region:

1. In the **Hierarchy** window (Logical or Physical tab), select the macro to unassign.
2. From the **Logic** menu, choose **Unassign From Region**.

Tip: Tip: You can also right-click the macro, and choose **Unassign From Region**.

You can also unassign all macros from a specific region.

To unassign all macros from a region:

1. Select the region from which to unassign all macros.
2. From the **Logic** menu, choose **Unassign All From Region**.

See Also

Assigning a Macro to a Region

Creating Local Clock Regions

For **IGLOO, Fusion, ProASIC3**, and **Axcelerator** families, you can use a PDC file to create local clock regions.

For **ProASIC** PLUS and **ProASIC** families, you can create local clock regions in ChipPlanner or define them in a GCF file. See the *Floorplanning ProASIC/ProASIC* PLUS *Devices for Increased Performance* application note for more information.

For Axcelerator, you can create local clock regions in ChipPlanner or define them in a PDC file.

When you create a local clock region, the selected net and all the macros driven by that net are assigned to the local clock region.

To create a local clock region from the MVN Hierarchy window:

1. In the **Net** tab of the **Hierarchy** window, select a clock net.
   Clock nets have a clock icon next to them in the **Net** view.
2. From the **Region** menu, choose **Create LocalClock**.

- ProASIC PLUS or ProASIC - choose **Spine**
- Axcelerator- Choose one of the following: **RCLK Tile**; **RCLK Row**; **HCLK Tile**; **HCLK Column**

3. Drag a rectangle from the top-left corner of the new local clock region to its bottom-right corner. As you drag out the region, the rectangle snaps to the spine, tile, row or column based on the type of local clock you chose and a tooltip appears in its lower-right corner, showing how much logic, RAM blocks, and I/Os are in the region.

Note: A net that is already assigned to a local clock region cannot be assigned to another non-overlapping region.

For ProASIC and ProASIC PLUS families, the RAM blocks and I/Os are assigned to the local clock region unless the Compile option “Include RAM and I/O in Spine and Net Regions” is cleared. See "Compile Options" in the online help for more information. For Axcelerator, the RAM blocks and I/Os are always included in the local clock region.

The default name of the local clock region is LocalClock_<netname> (for example, LocalClock_exl_d_0), and its type is inclusive.

Designer does not support exclusive local clock regions. Local clock regions are inclusive by default, and you cannot change their type.

Note: Note: ProASIC and ProASIC PLUS - To assign a signal to a spine, the spine itself and the entry MUX must be free. However, this does NOT necessarily require the corresponding global network to be unused.

Note: For example, you can assign non-global signals to spines when four global networks are used by other high fan-out nets. For more information, refer to the application note *Optimal Usage of Global Network Spines in ProASIC* PLUS *Devices,* which is available from the Actel web site.

For more information on creating and using local clock regions for Axcelerator, see the *RTAX-S/SL Clocking Resource and Implementation* application note, which is available from the Actel web site.

See Also

Renaming a Local Clock Region

Using Local Clock and Quadrant Clock Regions

Locking Regions

Editing Regions

set_io

set_location

Renaming a Local Clock Region

To change the name of a local clock region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the local clock region with the name you want to change.
3. From the **Region** menu, choose **Properties**.
4. In the **Properties** dialog box, type the new region name over the existing one.

Tip: Tip: You can also right-click on the region name, and choose **Properties** to display the region's properties. Type the new name over the old one in the **Properties** dialog box.

See Also

Using Local Clock and Quadrant Clock regions

Editing Regions

About Quadrant Clocks

A clock conditioning circuit (CCC) can include any of the following functional block cores: CLKBUF, CLKINT, PLL, and CLKDLY. All of the CCCs include the quadrant clock feature.

You can use both CLKBUF and CLKINT as a quadrant clock driver. They can be placed in either a global or quadrant clock location.

The PLL and CLKDLY cores are options for a global or quadrant clock location.

You can instantiate as many CCC cores as you want in your design, up to the maximum allowed by the architecture (18).

Synthesis tools can only infer CLKBUF and CLKINT cores up to a total of six clocks in the design. The six clocks include any clock you instantiated using CCC cores. There is no user variable to control the maximum number of clocks available to the synthesis engines for inferring purposes.

Physical Constraints for Quadrant Clocks

If quadrant clocks are present in a design or if it is necessary to "promote" global clocks (CLKBUF, CLKINT, PLL, CLKDLY) to quadrant clocks to satisfy the clock network resource constraints, you must define physical design constraints to execute the promotion. You may choose to create physical design constraints using PDC commands (pre-compile) or the MVN interface (post-compile).

The advantage of using the PDC flow over the MVN flow is that Compile is able to automatically promote any regular net to a global net before assigning it to a quadrant.

Prelayout Physical Constraint Verification

The prelayout checker performs the following DRC (Design Rule Checker) checks:

- The remaining clocks, which need to be assigned to a global clock resource, need to be less than 6. For example:

```
Resource Limit
The number of chip globals in your design exceeded the maximum number
available in the device.
```

- The checker verifies that the total number of clock resources assigned to the given quadrant does not exceed 3. For example:

```
PRL09: The number of clocks assigned (4) to the Upper Left quadrant exceeds the maximum
number available (3) in the device.
```

- If a clock is placed and assigned to a quadrant clock region, the checker verifies that the clock is placed in the given quadrant clock region. For example:

```
PRL11: Cannot assign net:net_out2 to the Upper Right quadrant and its driver
macro:clkbibuf1 to Upper Left quadrant which is outside the quadrant.
```

See Also

Creating QuadrantClock regions

Assigning a Clock to a QuadrantClock Region

Editing Regions

Using the Prelayout Checker

Creating Quadrant Clock Regions

You can create QuadrantClock regions only for IGLOO, Fusion, and ProASIC3 devices.

To create a QuadrantClock region:

1. In the **Net** tab of the **Hierarchy** window, select a clock net.
   Clock nets have a clock icon next to them in the Net view.
2. From the **Region** menu, choose **Create QuadrantClock**,or click its icon in the toolbar. "Select a point in the Chip..." appears in the status bar.
3. Select a point in the chip that is driven by QCLK. ChipPlanner creates a QuadrantClock region for the given net. The region name is Qclock_<netname> and appears in the **Regions** tab of the Hierarchy window. A tickmark appears next to the net in the **Net** tab and next to all the macros driven by it.

Under the following conditions, ChipPlanner does not create a QuadrantClock region and displays an error message in the Log window:

- A net is not selected or more than one net is selected.
- The selected net is already assigned to a QuadrantClock region.
- Any macros connected to the selected net are locked outside of the region.
- Any macros connected to the selected net are assigned to a region that does not overlap the QuadrantClock region.
- The macros connected to the net exceed the capacity of the quadrant clock.

Note: You can also create a QuadrantClock using the assign_quadrant_clock command in a PDC file.

See Also

Creating a quadrant clock

Assigning a Clock to a QuadrantClock Region

Locking QuadrantClock Regions

Editing Regions

Design Constraints Guide: assign_quadrant_clock

Assigning a Clock to a QuadrantClock Region

You can assign a clock to a QuadrantClock region either using the ChipPlanner tool in the MultiView Navigator or using a PDC file.

In ChipPlanner, you can assign a clock to a quadrant clock in one of the following ways:

- Assign a clock macro (not hardwired to an I/O) to a QuadrantClock region using the ChipPlanner tool
- Assign a clock macro (hardwired to an I/O) to an I/O location using either the PinEditor or I/O Attribute Editor tool, or to an I/O module location that drives a QuadrantClock region using the ChipPlanner tool
- Assign a regular net to a QuadrantClock region

Using a PDC file, you can assign a clock to a QuadrantClock in one of the following ways:

- Assign a clock macro (not hardwired to an I/O) to a QuadrantClock region using the `assign_quadrant_clock` command
- Assign a clock macro (hardwired to an I/O) to an I/O location (`set_io`) or to an I/O module location (`set_location`) that drives a QuadrantClock region
- Assign a net driven by a regular net or a clock net to a specific QuadrantClock region using the following command:

  ```
  assign_quadrant_clock -net <net name> -quadrant <QuadranClock region>
  ```

  where

  `<net name>` is the name of the net assigned to the QuadrantClock region

  `<QuadrantClock region>` is the QuadrantClock region to which the net should be assigned. QuadrantClock regions are defined as UL (upper left), UR (upper right), LL (lower left), and LR (lower right)

  Example: **assign_quadrant_clock -net FRAMEN_in -quadrant UL**

Note: If the net assigned to the QuadrantClock is a regular net, Designer inserts a QCLKINT on the net.

See Also

About Quadrant Clocks

Creating QuadrantClock Regions

Locking QuadrantClock Regions

Editing Regions

Design Constraints Guide: assign_quadrant_clock

Design Constraints Guide: set_io

Design Constraints Guide :set_location

Locking Quadrant Clock Regions

You can lock and unlock quadrant clock regions only in IGLOO, Fusion, and ProASIC3 devices.

Running the Global Planner automatically deletes all unlocked quadrant clock regions and re-assigns them. To prevent the Global Planner from deleting a quadrant clock region, you must lock it.

To lock a quadrant clock region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the Qclock region to lock.
3. Right-click and choose **Lock**, or from the **Region** menu, choose **Lock**.
4. From the **File** menu, choose **Commit**.

To unlock a quadrant clock region:

1. In the **Hierarchy** window, click the **Regions** tab.
2. Select the region to unlock.
3. Right-click and choose **Unlock**, or from the **Region** menu, choose **Unlock**.
4. From the **File** menu, choose **Commit**.

Tip: Tip: You can also lock or unlock a Qclock region in the Find panel select the region, right-click, and choose **Lock** or **Unlock**.

Note: Notes:

- When you create quadrant clock regions in MVN, the regions are automatically locked. Running the Global Planner tool will not delete locked quadrant clock regions.
- When you lock a net driver in a quadrant clock region, running the Global Planner will not unlock nor delete the net driver.
- When you explicitly lock quadrant clock regions in MVN, running the Global Planner in MVN will not unlock nor delete them.
- In MVN, when you place the driver of a global net in a quadrant location, MVN automatically creates the quadrant clock region.

See Also

Creating Quadrant Clock Regions

Assigning a Clock to a Quadrant Clock Region

Using the Global Planner

Assigning Logic to Locations

Manually assigning logic is an optional methodology to help you improve the performance and density of your design.

You do not need to manually assign logic to particular locations in your design. However, should you have specific design requirements, ChipPlanner allows you to have maximum control over your design.

To assign logic to specific locations:

1. Select the logic in the **Physical** tab of the **Hierarchy** window or in an Active List.
2. Drag the logic to the desired location. As you drag, valid assignment locations are highlighted. To remove the assignment, from the **Edit** menu, choose **Undo**.

If the logic assignment is valid, the logic is assigned and locked. To save changes for this design session, commit your changes when exiting the MultiView Navigator.

To assign logic to multiple locations:

1. While holding down the **CTRL** or **SHIFT** key, select the logic in the order you want it placed.
2. From the **Logic** menu, choose **Assign To Location**.
3. One by one, select the desired locations. The macros are placed in the order selected.

To unassign logic from a location:

1. Select the logic.
2. From the **Logic** menu, choose **Unassign From Location.**

To unassign logic from multiple locations:

1. While holding down the **CTRL** or **SHIFT** key, select the logic you want to unassign.
2. From the **Logic** menu, choose **Unassign From Location**.

To unassign logic from all locations:

- From the **Logic** menu, choose **Unassign All From Location.**

See Also

Moving Logic to Other Locations

Locking Logic to Locations

Unassigning All Logic from a Location

To unassign all logic from a location:

- From the **Logic** menu, choose **Unassign All From Location.**

Moving Logic to Other Locations

You can move logic that was assigned manually or automatically during Layout.

To move logic:

1. Select the logic to move.
2. Drag the logic to the new location.

Tip: Tip: To remove the assigned macro, from the **Edit** menu, choose **Undo**.

See Also

Assigning Logic to Locations

Locking Logic to Locations

Locking Logic to Locations

Locked logic is not moved during Layout. Locked logic only becomes permanent if you commit the changes to your design before exiting.

To lock macros:

1. Select the macro to lock. To select multiple macros, hold down the **CTRL** key and select multiple macros with your mouse. To select all macros, from the **Edit** menu,choose **Select All**.
2. From the **Logic** menu, choose **Lock**.
3. From the **File** menu, choose **Commit** to save your changes in this session. To save your changes in the design file (.ADB), you must save your design in Designer as well.

To unlock a macro:

1. Select the macro. To select multiple macros, hold down the **CTRL** key and select multiple macros. To select all macros, from the **Edit** menu,choose **Select All**.
2. From the **Logic** menu, choose **Unlock**.

See Also

Assigning Logic to Locations

Moving Logic to Other Locations

Block Ports

About Block Ports

You can see Block ports in the Ports tab of the Hierarchy window. Unlike regular I/O ports, Block ports have a plus sign (+) in front of them to indicate that they can be expanded to show connected ports and instances (as shown below):

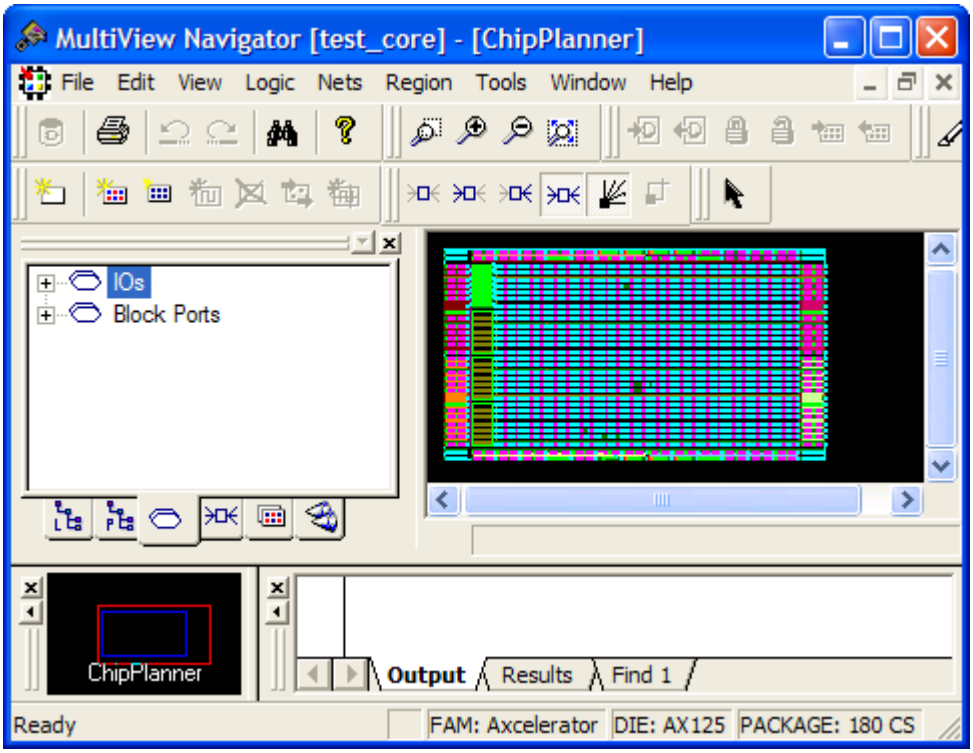


Figure 38 · Block Ports Include a Plus sign (+) in the Hierarchy Window

When you expand a Block port, you see the macros and blocks connected to the Block port under the expanded node:

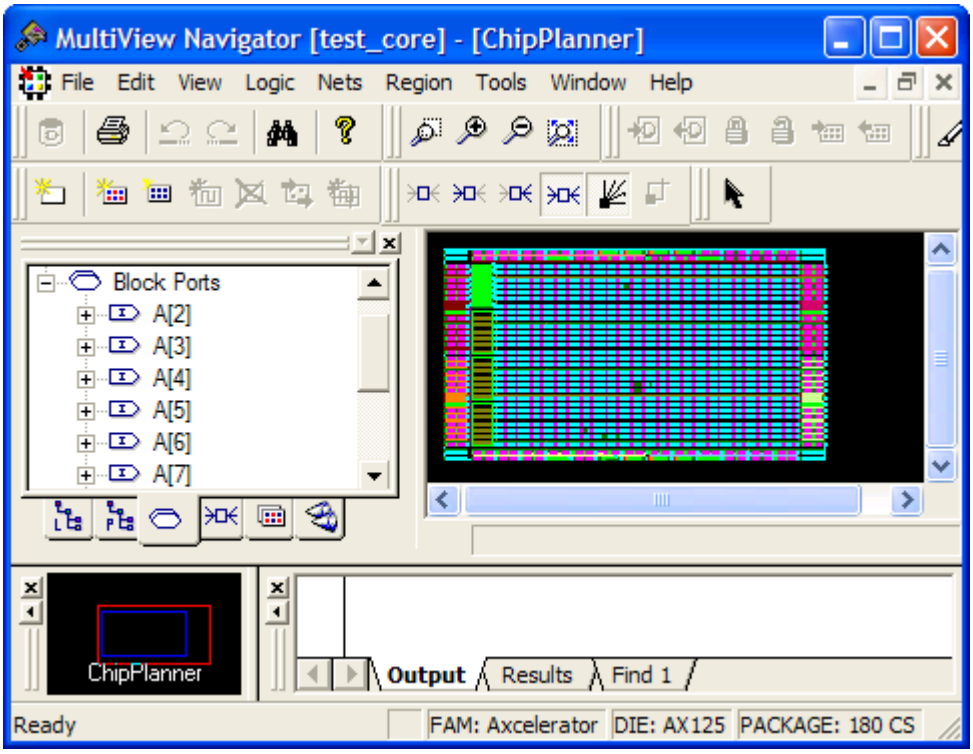


Figure 39 · Block Ports Expanded

Note: Block ports are not displayed in the I/O Attribute Editor but are visible in NetlistViewer.

Block ports have features similar to other MVN objects, such as a tooltip, a context menu, and a properties dialog box. You cannot drag and drop block ports. The symbols used in the Ports tab for Block ports are the same for regular I/O ports. The symbol is dependent on the direction: Input, Output, or InOut.

Selecting Connected Ports

When you right-click on a Block port in the Ports tab of the Hierarchy window, the right-click menu displays two commands: **Select Connected Ports** and **Properties**.

To select all ports connected to a macro:

1. Select the macro.
2. Right-click and choose **Select Connected Ports** from the right-click menu.

Figure 40 ·

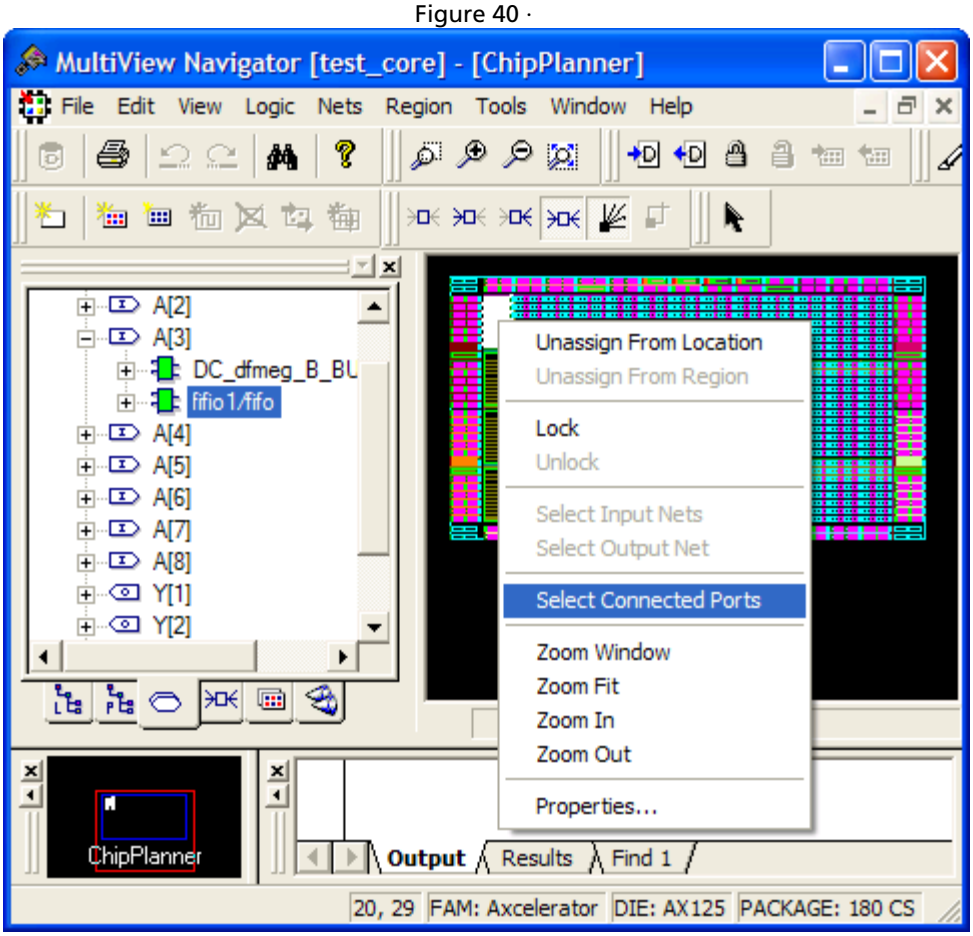


Figure 41 · Block Right-click Menu

All ports to which the macro is connected will be selected.

Note: The Select Connected Ports command appears grayed if the macro you selected is not connected to any ports.

Viewing Resources

Ratsnest View

The Ratsnest view displays net connectivity between assigned logic macros by connecting lines from all output pins to all input pins. Use the Ratsnest view to understand how logic macros are connected to each other. The Ratsnest view is activated by default, showing all input and output nets for the selected macro.

To display the Ratsnest view:

1. From the **Nets** menu, choose **Show Input Only**, **ShowOutput Only**, or **Show Input & Output**, or click the corresponding Net toolbar button, to indicate which nets you want to see.
2. From the **Nets** menu, choose **Show Ratsnest**, or click the **Ratsnest** button in the toolbar.
3. Select the assigned macro in the ChipPlanner window. ChipPlanner displays all nets connected to the assigned macro. See nets assigned to multiple macros by holding down the **CTRL** key while you click on each assigned macro.

Here is an example of a Ratsnest view in a ProASIC3E design. Note that the module icons look different from the way they appear in the Route view.

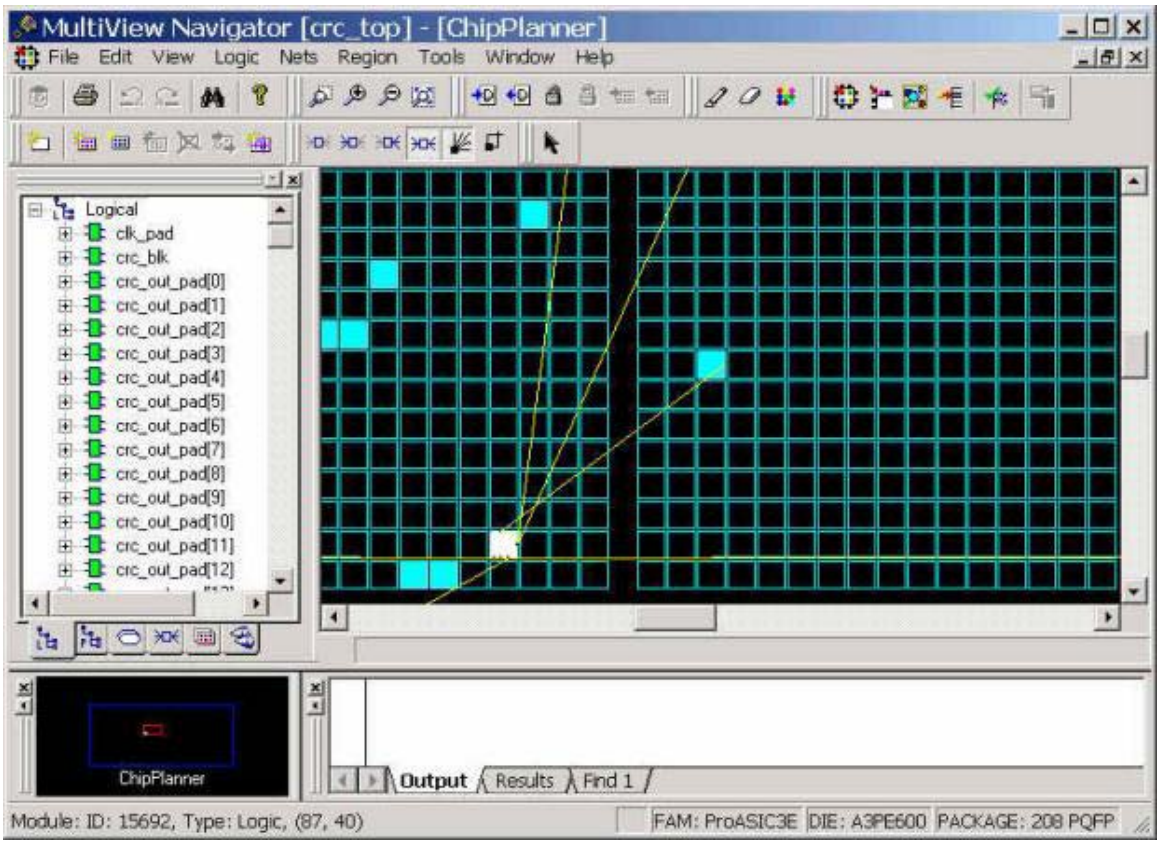


Figure 42 · Ratsnest View in ChipPlanner

Route View

Note: This feature is available only for IGLOO, Fusion, ProASIC3, ProASIC Plus, ProASIC, and Axcelerator devices.

The Route view displays a representation of the routes. This feature shows the general location of routing segments used by the design.

To activate the route view in ChipPlanner:

1. Complete **Layout**. To display routes, Layout must be completed before running ChipPlanner.
2. Select the assigned macro in either the **ChipPlanner** window or the **Physical** tab of the **Hierarchy** window. Select multiple macros by holding down the **CTRL** key.
3. From the **Nets** menu, choose **Show Routes**, or click the **Show Routes** toolbar button.

The following screen shows a route view for a ProASIC3E design followed by a route view for an Axcelerator design. Note that the module icons look different from the way they appear in the Ratsnest view. Also, notice how the routing views for Flash families differ from those for Axcelerator.

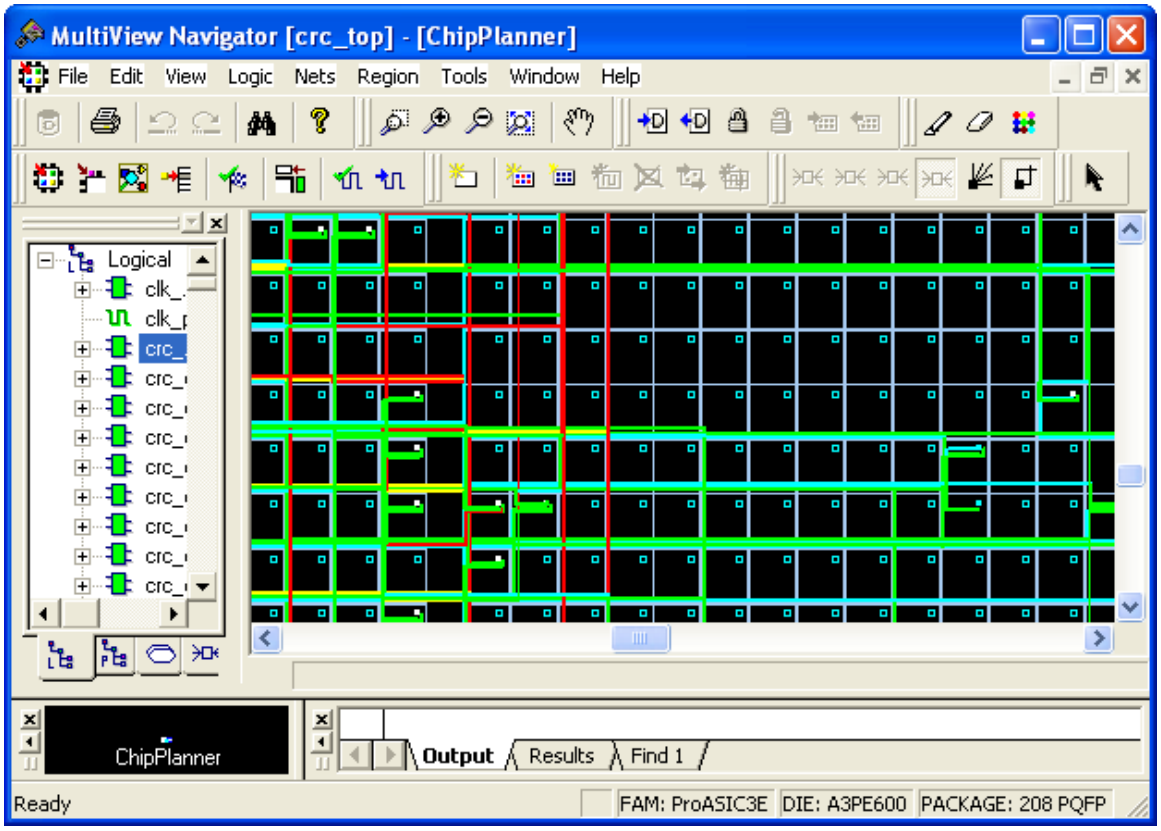


Figure 43 · Route View for a ProASIC3E design in ChipPlanner

Axcelerator designs include routing buffers and "clusters." Clusters include one SEQ, two COMB, and one buffer. Routing buffers are used to redirect traffic. Axcelerator designs can include many extra routing buffers.

You can use the **Display Settings** dialog box to change the color schemes used in routing. The default colors are red for clocks, yellow for locked modules, and green for RAM.

To display routes for one or more nets, select at least one net form the **Nets** tab in the **Hierarchy** view window when in Route view. When you select one or more macros, the connected nets are also selected. When in Route view, you can see the routing tree for the selected nets (see screen shown above).

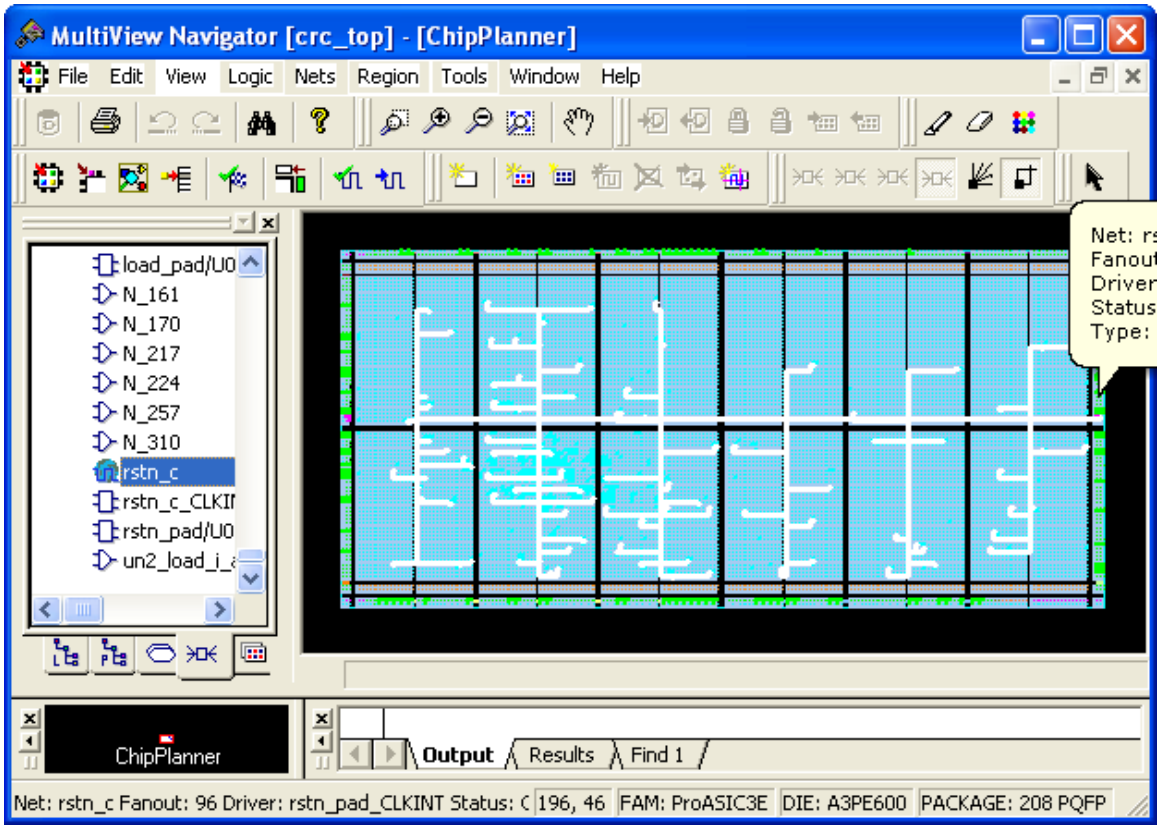


Figure 44 · Routing Tree with Nets Selected

To display the Ratsnest view, select **Show Ratsnest** from the **Nets** menu or click the **Ratsnest** button.

If any nets are selected, switching from Ratsnest view to Route view displays the routing tree.

See Also

Ratsnest View

Clusters and Super Clusters

Clusters and Super Clusters

Note: This feature is only available for the Axcelerator, eX. SX-A, and SX families.

A cluster is a group of logic elements. The type of elements that make up the cluster is determined by the device type.

A super cluster is two clusters and a buffer. Modules in a cluster can be connected by fast or direct connects.

Use these areas as guides to ensure that specific nets can be implemented using fast or direct connects. Nets that connect within a rectangle can be implemented as fast or direct connects, depending on availability. For details about fast connects and direct connects, please see the FPGA datasheet for your device on the Actel web site.

To view clusters or super clusters:

1. From the **View** menu, choose **Display Settings**.

The **Display Settings** dialog box appears.

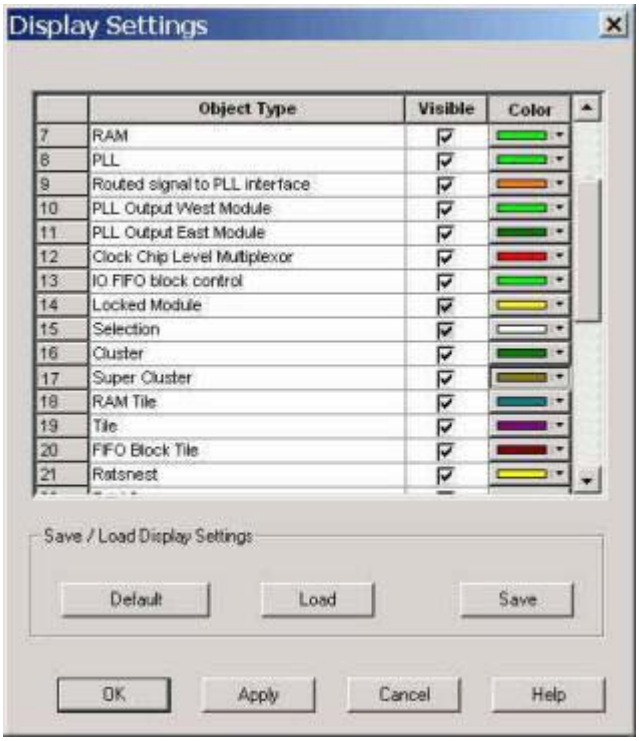


Figure 45 · Display Settings Dialog Box

2. Select the **Visible** check box for **Cluster** or **Super Cluster**.
3. Click the **color bar** and select a color to change its display color.
4. Click **OK**.

Cross-probing between ChipPlanner and SmartTime

Use ChipPlanner with SmartTime to identify the signal path or individual instances in ChipPlanner.

To identify paths in ChipPlanner:

1. In the **Design Flow** window, click **ChipPlanner** to display the chip view, and then click **Timing Analyzer** to display the **SmartTime Timing Analyzer**.
2. In the **SmartTimeTiming Analyzer**, select the clock domain in the **Domain Browser**.
3. Select a set in the Path list (as shown below) and the paths within that set are displayed in the **Path Details** (lower table). The **Paths List** displays timing information for various categories.

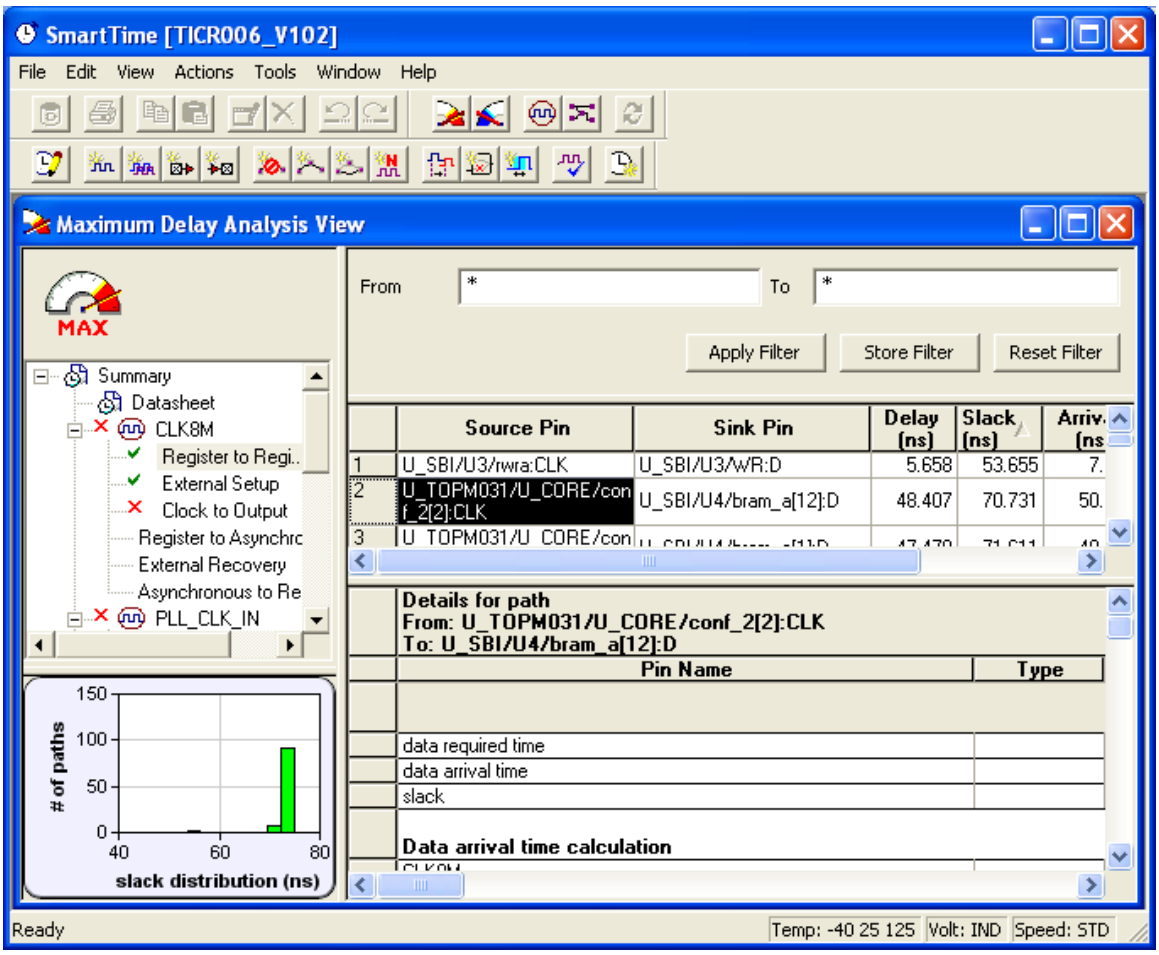


Figure 46 · Path Details of Selected Path Highlighted

4. Select the path to cross-probe.
5. Right-click the selected path, and choose **Cross-probe selected paths** from the right-click menu. All objects in the selected path appear highlighted in ChipPlanner (as shown below).

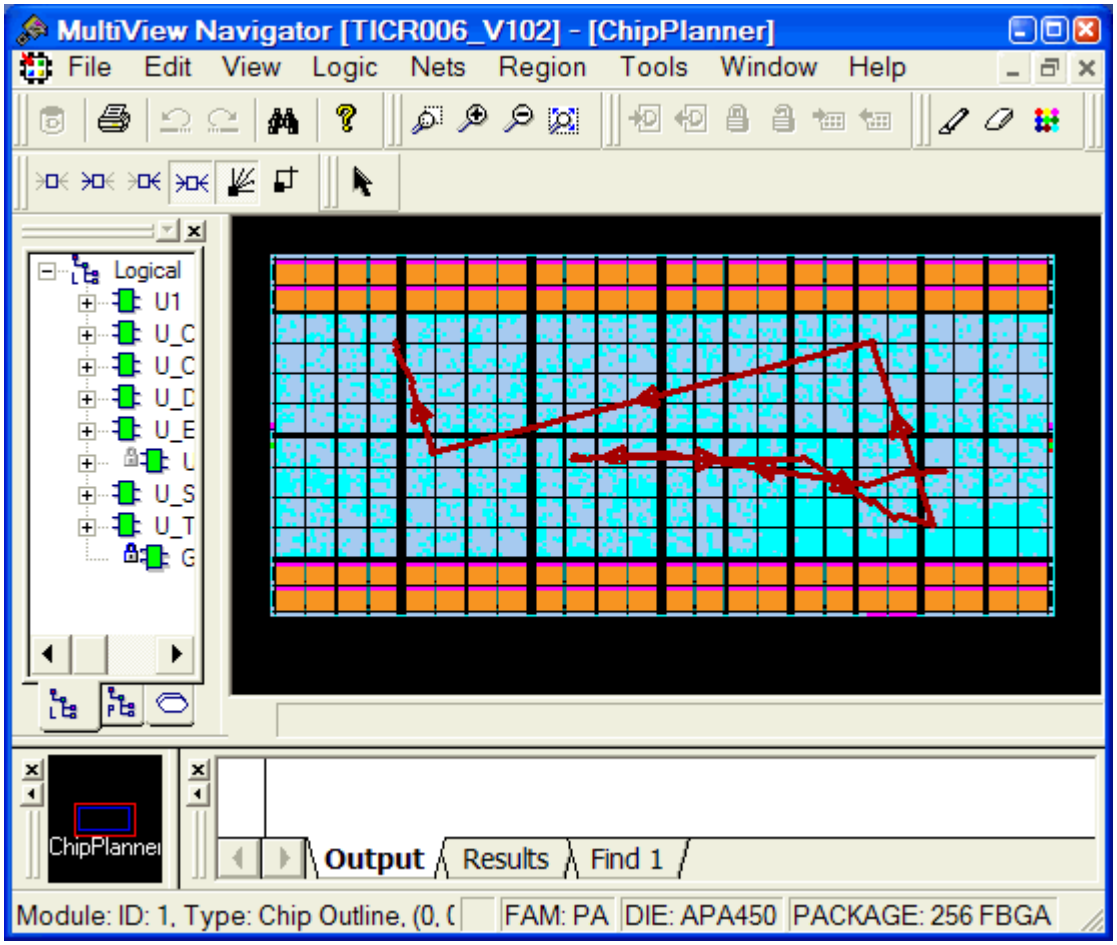


Figure 47 · Objects in Selected Path Appear Highlighted in ChipPlanner

Note: Note: Logic must be either placed or placed-and-routed before you can cross-probe paths.

Tip: Tip: From the **Edit** menu, choose **Unhighlight All** to remove the highlighting from the cross-probed paths in ChipPlanner.

To cross-probe an object with ChipPlanner:

1. In the **Design Flow** window, click **ChipPlanner** to display the chip view, and then click **Timing Analyzer** to display the **SmartTime Timing Analyzer**.
2. In the **SmartTimeTiming Analyzer**, select the clock domain in the **Domain Browser**.
3. Select a path in the **Paths List**, right-click it, and choose **Expand selected paths** from the right-click menu.
4. Select any instance in the SmartTime **Expanded Path View**. The instance appears highlighted in both SmartTime and ChipPlanner.
5. To cross-probe the path of the selected object, right-click the instance, and choose **Cross-probe Path** from the right-click menu. All objects in the selected path appear highlighted in ChipPlanner.

When you cross-probe a path in ChipPlanner, the default view is the Ratsnest view, shown in the following example.

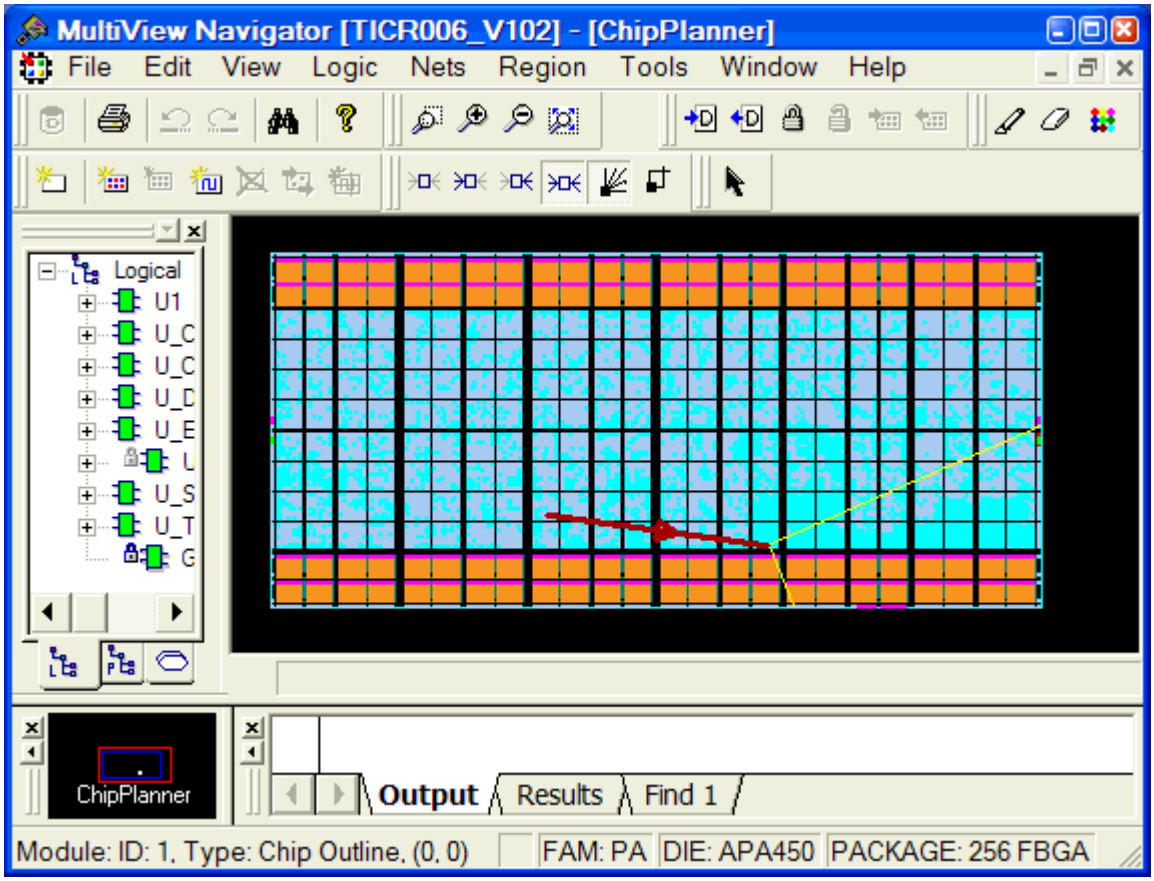


Figure 48 · Ratsnest view in ChipPlanner showing cross-probed path

Tip: Tip: To select multiple instances, hold down the Shift key as you click each instance.

The critical cross-probed path appears highlighted in ChipPlanner as a solid line with arrows indicating the direction of the path. The color of the line is the color you selected for the highlight color.

You can right-click a selected cross-probed path, choose **Properties** to display the **Path Properties** dialog box, and do one of the following:

- Rename the cross-probed path
- Assign a different color to the cross-probed path

You can create more than one cross-probed path in ChipPlanner, building one path on top of another. ChipPlanner does not delete paths you have cross-probed. When you save your design, the cross-probed paths are also saved in your design (.ADB) file.

Tip: Tip: In SmartTime, you can select several paths at one time by clicking the top-left corner square in the Maximum Delay Analysis View window.

See the *SmartTime User's Guide* for more information.

Using I/O Banks

About I/O Banks

For devices that support multiple I/O standards, I/Os are grouped into I/O banks around the chip.

The I/O Bank Assigner runs in the background when you run Layout and automatically assigns technologies to all I/O banks that have not been assigned a technology. You can also choose to manually run the I/O Bank Assigner.

To run the I/O Bank Assigner, from the **I/O Attribute Editor** menu, choose **Tools**, and then **Auto-Assign I/O Banks**.

I/O banks are visible in both ChipPlanner and PinEditor. Information about I/O banks appears in the MultiView Navigator's status bar.

Note: Note: The I/O Bank Assigner runs only for those families that have multiple I/O banks: IGLOO, Fusion, ProASIC3, and Axcelerator.

Fusion

Fusion devices have digital I/Os that are grouped into I/O voltage banks. There are three digital I/O banks on the AFS090 and AFS250 devices and four digital I/O banks on the AFS600 and AFS1500 devices. The north side of I/O in the AFS600 and AFS1500 devices is comprised of two banks of Actel Pro I/Os.

The Actel Pro I/Os support a wide number of voltage referenced I/O standards in addition to the multitude of single-ended and differential I/O standards common throughout all of the Actel digital I/Os. Each I/O voltage bank has dedicated input/output supply and ground voltages (VMV/GNDQ for input buffers and VCCI/GND for output buffers). Because of these dedicated supplies, only I/Os with compatible standards can be assigned to the same I/O voltage bank. The required voltage values and their compatible I/O standards for IGLOOe, Fusion, and ProASIC3E devices are the same (see the "Compatible I/O Standards" table for ProASIC3E devices below).

For more information about Fusion devices, see the *"Fusion Family of Mixed-Signal Flash FPGAs"* datasheet on the Actel web site.

IGLOOe, Fusion, ProASIC3E, and Axcelerator

IGLOOe, Fusion, ProASIC3L (A3PE3000L) devices, ProASIC3E, and Axcelerator devices have eight I/O banks surrounding the chip, two per side, numbered 0-7. The I/O banks are color-coded for quick identification. You can change the default colors through the Display Settings dialog box.

Each I/O bank has a common:

- VCCI, the supply voltage for its I/Os
- VREF, the reference voltage (for voltage-referenced I/O standards)

Each VREF pin assigned to the same I/O bank must have the same value. For example, you cannot assign a VREF with a VCCI of 1.5 and another with a VCCI of 1.8 V to the same I/O bank.

Only I/O standards compatible with the same VCCI and VREF standards can be assigned to the same bank.

The following table shows the required voltage values and their compatible I/O standards for and IGLOOe, Fusion, ProASIC3L (A3PE3000L), and ProASIC3E devices.

VCCI	Compatible I/O Standards
3.3 V	LVTTL, LVCMOS 3.3, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, GTL 3.3, LVPECL
2.5 V	LVCMOS 2.5, LVCMOS 2.5/5.0, GTL+ 2.5, GTL 2.5, SSTL2 (Class I & II), LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I), HSTL (Class II)
1.2 V	LVCMOS 1.2 (see Note below)

Note: Note: The low-power mode and input delay attributes are not available in the I/O Bank Settings dialog box for IGLOOe, Fusion, ProASIC3L (A3PE3000L), and ProASIC3 devices. Because these attributes are not available, the More Attributes button is also not available. Also, the 1.2 voltage is supported for ProASIC3 (A3PL), IGLOOe V2 only, IGLOO V2, and IGLOO PLUS.

The following table shows the required voltage values and their compatible I/O standards for **Axcelerator** devices.

VCCI	Compatible I/O Standards
3.3 V	LVTTL, PCI 3.3, SSTL3 (Class I & II), GTL+ 3.3, LVPECL
2.5 V	LVCMOS 2.5, GTL+ 2.5, SSTL2 (Class I & II), LVDS
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5, HSTL (Class I)

IGLOO and ProASIC3

IGLOO (excluding IGLOOe) and ProASIC3 (excluding) devices have two, four, or eight I/O banks surrounding the chip, one per side, numbered 0-1, 0-3, or 0-7, respectively. Each I/O bank has dedicated resources for an input/output supply voltage (VCCI). Because of these dedicated resources, you can assign only I/Os with compatible standards to the same I/O bank. The following table shows the required voltage values and their compatible I/O standards.

VCCI	Compatible I/O Standards
3.3 V	LVTTL, PCI 3.3, LVPECL, LVCMOS
2.5 V	LVCMOS 2.5/5.0, LVDS

VCCI	Compatible I/O Standards
1.8 V	LVCMOS 1.8
1.5 V	LVCMOS 1.5
1. 2 V	LVCMOS 1.2

Note: Note: Only ProASIC3 (A3PL), IGLOOe V2 only, IGLOO V2, and IGLOO PLUS support 1.2 voltage.

On some dies, the left and right side of the chip have a different selection of I/O standards (LVDS/LVPECL). Because the dies do not need an input referenced voltage (VREF), the **Use Pin for VREF** and **Highlight VREF Range** commands are unavailable from the right-click menu. Also, because the low-power mode and input delay attributes are not available, the **More Attributes** button is not available in the I/O Bank Settings dialog box.

Note: Note: IGLOO and ProASIC3 low-cost devices do not support the Input Delay attribute.

For more about I/O banks, see the datasheet for your device.

See Also

Specifying Technologies for an I/O Bank

Automatically Assigning Technologies to I/O Banks

Manually Assigning Technologies to Banks

Assigning Pins in IGLOOe, Fusion, and ProASIC3E

Assigning VREF Pins

Support for VREF I/Os

VREF I/Os are fully supported in your design. Here are the rules for assigning VREF I/Os in the designer software:

- You cannot unplace I/Os from a block.
- You can change VREF pins in the top of a block only if this will not result in I/Os becoming unplaced from the block.
- If a macro needs a VREF pin, you cannot unset the VREF pin until you first assign a different VREF pin to it.
- If you have I/O Banks with only VCCI set on a block, you can modify those I/O Banks to include VREF technology.
- Setting and unsetting VREF pins on a block must not result in unplacing any I/O from the block.
- You can change the I/O technology to "do not need a VREF" (for example, from SSTL to LVTTL).
- The default VREF pin setting will fail if any I/O from the block becomes unplaced.
- The automatic I/O Bank setting tool will not unplace any I/O from a block.

Specifying Technologies for an I/O Bank

You can specify technologies for each I/O bank by doing one of the following:

- Using the I/O Bank Settings dialog box
- Placing an I/O of a particular technology in an I/O bank that has not been assigned a voltage
- Running the I/O Bank Assigner
- Using the command set_iobankin a PDCfile

You cannot change the I/O technology of an assigned I/O to an I/O technology that is incompatible with the bank. If you need to assign the I/O technology to a new technology, first unassign the I/O.

See Also

Manually Assigning Technologies to Banks

Automatically assigning voltages to I/O banks

Assigning Pins in IGLOOe, Fusion, ProASIC3L, and ProASIC3E

Assigning VREF Pins

Displaying VREF Pins

Automatically Assigning Technologies to I/O Banks

The I/O Bank Assigner (IOBA) tool runs automatically when you run Layout. You can also use this tool from within the MultiView Navigator or from within Libero Project Manager. The I/O Bank Assigner tool automatically assign technologies and VREF pins (if required) to every I/O bank that does not currently have any technologies assigned to it. This tool is available when at least one I/O bank is unassigned.

Each time you run the I/O Bank Assigner, it unassigns all technologies from all I/O banks and then re-assigns them when it finds a feasible solution. To prevent I/O Bank Assigner from unassigning and re-assigning I/O technologies each time you run it, lock the I/O banks by selecting **Locked** in the I/O Bank Settings dialog box or by importing the `set_iobanks` PDC command with its `-fixed` argument set to "yes".

To automatically assign technologies to I/O banks:

- In Project Manager, from the **I/O Attribute Editor** menu, choose **Tools>Auto-Assign I/O Banks**.
- In MultiView Navigator, from the **Tools** menu, choose **Auto-Assign I/O Banks**. You can also click the I/O Bank Assigner's toolbar button shown below.

Messages appear in the Output window informing you when the automatic I/O bank assignment begins and ends. If the assignment is successful, "I/O Bank Assigner completed successfully" appears in the Output window.

If the assignment is not successful, an error message appears in the Output window.

Tip: Tip: Click an underlined "Error" or "Info" message to display more information.

Note: Note: All I/O technologies assigned to I/O banks by the I/O Bank Assigner in Layout are unlocked.

To undo the I/O bank assignments, choose **Undo** from the **Edit** menu. Undo removes the I/O technologies assigned by the I/O Bank Assigner. It does not remove the I/O technologies previously assigned.

To redo the changes undone by the Undo command, choose **Redo** from the **Edit** menu.

If you need to clear I/O bank assignments made before using the Undo command, you can manually unassign or re-assign I/O technologies to banks. To do so, choose **I/O Bank Settings** from the **Edit** menu to display the **I/O Bank Settings** dialog box.

See Also

About I/O Banks

Specifying Technologies for an I/O Bank

Manually Assigning Technologies to Banks

Using the Prelayout Checker

Manually Assigning Technologies to I/O Banks

The procedure for manually assigning technologies to I/O banks differs depending on whether you are designing for IGLOO, Fusion, ProASIC3, or Axcelerator devices.

To assign technologies to I/O banks in IGLOOe, Fusion, ProASIC3L, ProASIC3E, and Axcelerator devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Edit** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further, selecting GTLP (3.3 V) disables SSTL3 as an option because the VREFs of the two are not the same. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Click **More Attributes** to set the low-power mode and input delay. (These attributes are supported in Axcelerator devices only.)
5. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
6. Leave the **Use default pins for VREFs** option selected to set default VREF pins and unset non-default VREF pins. If you unselect this option when setting a new VREF technology, no VREF pins are set. If you unselect this option when default VREF pins are already set, it unsets them.

   If the **Use default pins for VREFs** option is selected when you click **OK** or **Apply**, the software: 1) determines if setting default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, 2) determines if unsetting non-default VREF pins causes any I/O macros to become unassigned, and if so, displays a warning message enabling you to cancel this operation, and 3) sets default VREF pins and unsets non-default VREF pins.
7. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.

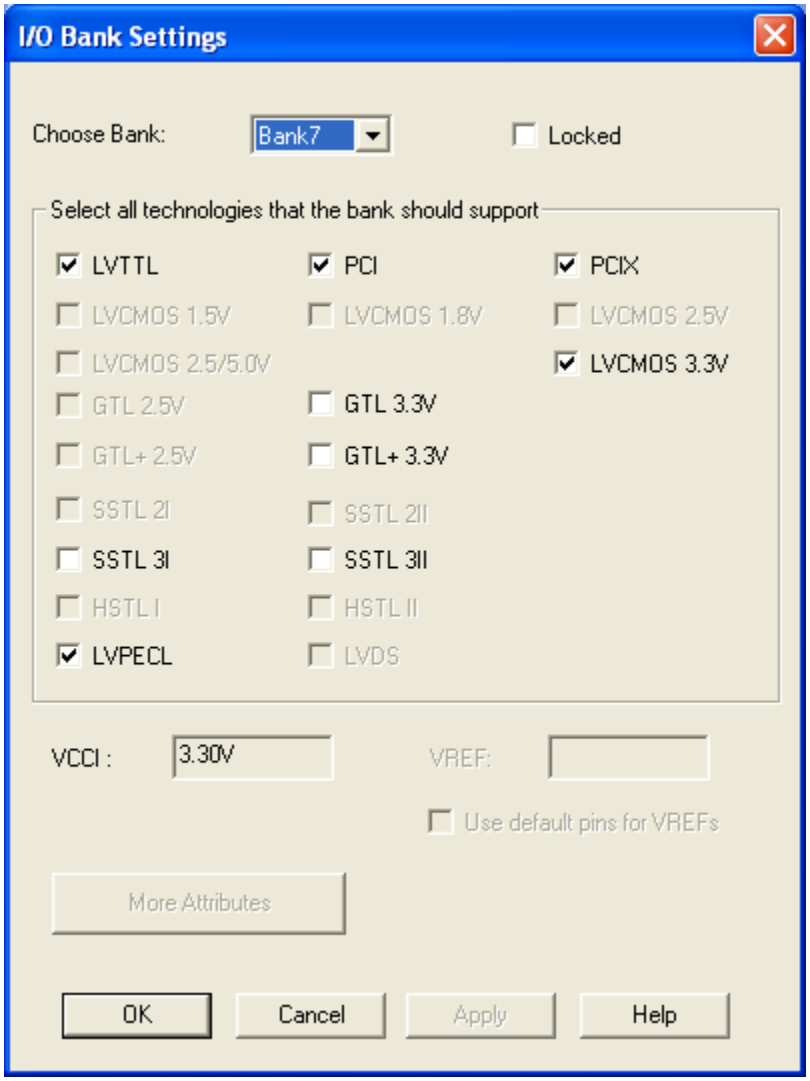


Figure 49 · I/O Bank Settings Dialog Box for IGLOOe, Fusion, ProASIC3L, ProASIC3E, and Axcelerator Devices

If VREF pins can be assigned, you must assign at least one VREF pin before running Layout. See "Assigning VREF Pins" in this guide for more information.

Note: If you use I/O standards that need reference voltage, make sure to assign VREF pins. Actel strongly recommends you use the defaults. VREF pins appear in red in ChipPlanner and are labeled VREF in PinEditor.

To set the low-power mode and input delay (for Axcelerator devices only):

1. Click **More Attributes** in the **I/O Bank Settings** dialog box.
2. Drag the slider bar to the desired delay. The delay is bank specific.
3. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. You must select a technology to see the input delays.

4. Click **OK**.

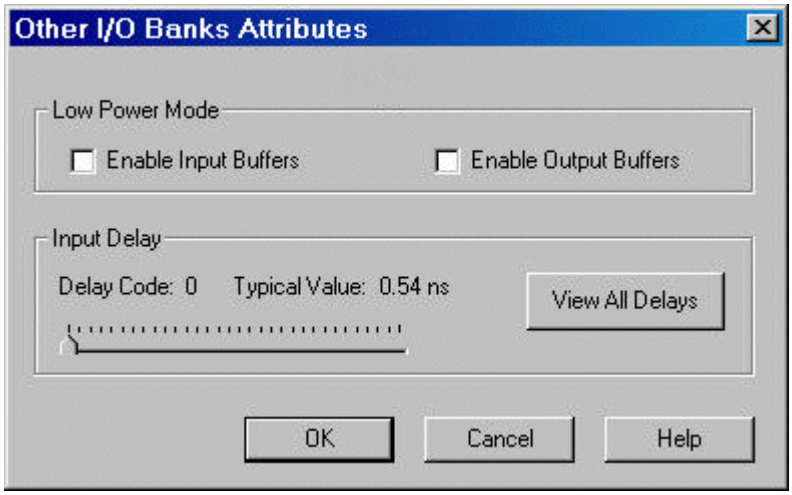


Figure 50 · Other I/O Bank Attributes Dialog Box

Note: To assign technologies to I/O banks in ProASIC3 and IGLOO devices:

1. Select an I/O bank in either ChipPlanner or PinEditor.
2. From the **Edit** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select the technologies, and click **Apply**.
   Selecting a standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Note that LVDS is available only for banks 1 and 3. Once you click **Apply**, the I/O bank is assigned the selected standards. Any I/O of the selected types can now be assigned to that I/O bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.
4. Assign I/O standards to other banks by selecting the banks from the list and assigning standards. Any banks not assigned I/O standards use the default standard selected in the Device Selection Wizard.
5. Click **OK**. Using PinEditor, proceed to assign I/Os with the same standards to the appropriate banks.

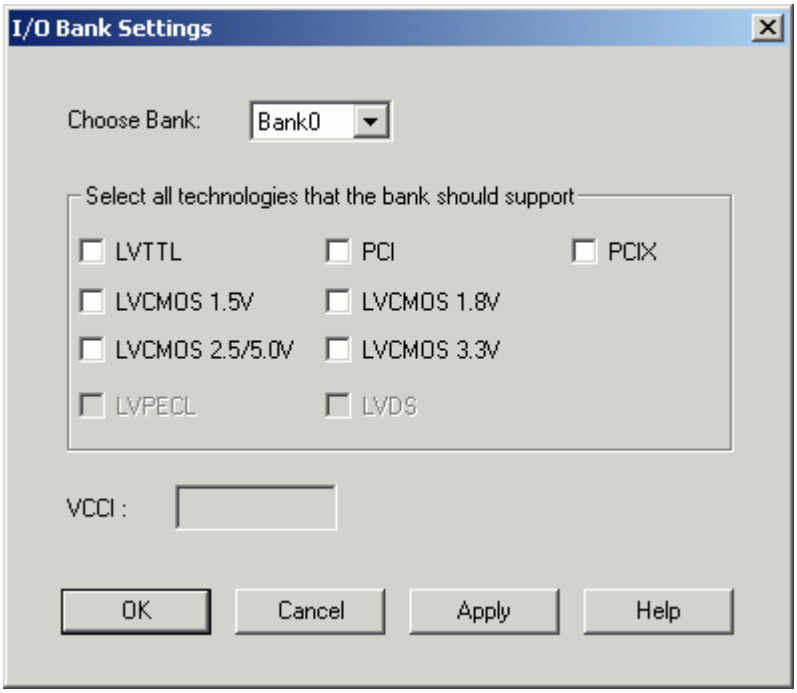


Figure 51 · I/O Bank Settings Dialog Box for IGLOO and ProASIC3 Devices

Note: You cannot assign VREF pins in ProASIC3 and IGLOO devices. You can assign VREF pins only to IGLOOe, Fusion, ProASIC3L (A3PE3000L die only), and ProASIC3E devices.

See Also

Specifying Technologies for an I/O Bank

Automatically Assigning Technologies to I/O Banks

Assigning Pins in ProASIC3E

Assigning VREF Pins

Displaying VREF Pins

Assigning Pins in IGLOOe, Fusion, ProASIC3L, and ProASIC3E

To assign I/O in the IGLOOe, Fusion, ProASIC3L, and ProASIC3E devices

1. From Designer's **Tools** menu, choose **Device Selection**. Select a die, package, speed, and die voltage, and click **Next**.
2. In the **Device Selection Wizard-Variations** dialog box, from the Default I/O Standard drop-down list, select the default I/O standard for all generic I/O macros. This action sets the same VCCI for each bank. You cannot choose LVDS or LVPECL as the default I/O standard. If your design has only one single-ended I/O and one VCCI requirement, go to step 8. Otherwise, in the next step you will specify the I/O standards for each I/O bank.
3. Start either **ChipPlanner** or **PinEditor**.
4. From the **Edit** menu, choose **I/O Bank Settings**.
5. In the **I/O Bank Settings** dialog box, choose anI/O standard for each I/O bank. (I/O technologies that are not allowed for the given VCCI are grayed out.)
6. In ChipPlanner or PinEditor, assign VREF pins, if the standard requires VREF voltage. See Assigning VREF pins. In IGLOOe, ProASIC3L, and ProASIC3E, you can use any I/O as a VREF pin. The default VREFs setting may create more VREF pins than needed and may result in a loss of usable user I/Os. If that happens, you can choose the custom VREF setting. You must create enough VREF pins to allow a legal placement of the compatible user-voltage-referenced I/O macros. After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin.
7. After assigning VREF pins, from the **Tools** menu, choose **DRC** to check the I/O voltage assignment and to generate an I/O bank report. The I/O voltage Usage section in this report shows whether you have enough I/Os available for each voltage. Any infeasible voltage requirements appear as an asterisk (*) in the I/O voltage Usage report. If asterisks appear in your report, you should resolve the problem before continuing.
8. Once you have completed the I/O bank assignments, you can assign I/O macros to individual pad locations using either the MultiView Navigator or a PDC file.

Note: Note: Choosing Commit from the File menu also performs the DRC check.

See Also

Specifying Technologies for an I/O Bank

Automatically Assigning Technologies to I/O Banks

Manually Assigning Technologies to Banks

Assigning VREF Pins

Displaying VREF Pins

Assigning VREF Pins

Voltage referenced I/O inputs (VREF) require an input referenced voltage. You must assign VREF pins to IGLOO, Fusion, and ProASIC3 families, excluding ProASIC3 devices, and Axelerator devices before running Layout.

Before assigning a VREF pin, you must set a VREF technology for the bank to which the pin belongs.

To set a VREF technology for a bank:

1. Select a bank in ChipPlanner.
2. From the **Edit** menu, choose **I/O Bank Settings**.
3. In the **I/O Bank Settings** dialog box, select a technology such as GTL+ 3.3 V so the VREF field displays a non-zero value.
4. Click **OK**. Now when you right-click on pins in this I/O bank, the VREF commands on the menu are enabled.

In either the PinEditor or ChipPlanner window, you can change a regular pin into a VREF pin from the right-click menu.

To assign a pin as a VREF pin:

1. In either PinEditor or ChipPlanner, select the pin to set as a VREF pin.
2. Right-click and choose **Use Pin for VREF**.

A check mark appears next to the **Use Pin for VREF** command in the right-click menu.

Note: Note: The Use Pin for VREF command appears on the right-click menu only if you selected a pin in an I/O bank that supports VREF pins and for package pins or I/O modules that can become VREF pins.

Setting a pin as a VREF may result in I/O macros becoming unassigned, even if they are locked. In this case, a warning message appears so you can cancel this operation.

To unassign a VREF pin:

1. Select the pin to unassign.
2. Right-click and choose **Use Pin for VREF**.Thecheck mark next to the command disappears. The VREF pin is now a regular pin.

Resetting the pin may result in unassigning I/O macros, even if they are locked. In this case, a warning message appears so you can cancel this operation.

Tip: Tip: You can also reset the **Use Pin for VREF** command by choosing **Undo** from the **Edit** menu.

After you assign the VREF pins, right-click a VREF pin and choose **Highlight VREF Range** to see how many I/Os are covered by this pin. To unhighlight the range, choose **Unhighlight All** from the **Edit** menu.

See Also

Specifying Technologies for an I/O Bank

Automatically Assigning Technologies to I/O Banks

Assigning Technologies to I/O Banks

Assigning Pins in IGLOOe, Fusion, and ProASIC3E

Displaying VREF Pins

Displaying Pins in a VREF Range

You can see which pins in an I/O bank are serviced by a VREF pin. Use the right-click menu's **Highlight VREF Range** command while in PinEditor or ChipPlanner to see these pins.

To display pins in a VREF range:

1. Right-click a VREF pin in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight VREF Range.**

When using PinEditor, all pins serviced by the selected VREF pin appear highlighted.

When using ChipPlanner, all I/O modules serviced by the selected VREF pin appear highlighted.

To highlight all pins in a VREF range:

1. Right-click an I/O bank in either PinEditor or ChipPlanner.
2. From the right-click menu, choose **Highlight All Pins in a VREF Range.**

The **HighlightAll Pins in a VREF Range** command appears in the right-click menu for all I/O banks that include a VREF pin.

All of the pins in the I/O bank that are serviced by a VREF appear highlighted. If the I/O bank does not contain a VREF pin, nothing is highlighted when you select this command.

To unhighlight all pins in a VREF range:

1. Select the highlighted range.
2. From the **Edit** menu, choose **Unhighlight All**.

See Also

Assigning Pins in IGLOOe, Fusion, and ProASIC3E

Assigning VREF Pins

Using Active Lists

What are Active Lists?

An active list is a list of macros, ports (I/Os), nets, or regions. Active lists enable you to focus on specific areas of your design.

You can display multiple active lists on the screen at the same time. The lists are updated dynamically when the design objects state changes. For example, when you unassign an instance, it automatically appears in the Unassigned Instances active list.

The Active Lists submenu contains the following predefined lists:

- Clock nets
- Interface Instances
- Unassigned Ports
- Unassigned Instances
- Designer Block Content

For example, to display a list containing only the clock nets in the design, from the **Tools** menu, choose **Active List>Clock Nets**, to display a list containing only macros connected to ports, choose **Interface Instances**,to display all unassigned I/Os, choose **Unassigned I/Os**, and to display all unassigned instances, choose **Unassigned Instances**.

In addition to the predefined lists, you can create your own active lists as well as modify and delete user-defined active lists. However, you cannot edit or delete the predefined active lists.

You can drag and drop items from an active list into ChipPlanner or PinEditor.

Using the Right-click Menu in an Active List Window with No Item Selected

You can use the right-click menu within an active list window to switch between active lists, display the More Active Lists dialog box, edit user-defined active lists, and enable or disable the **Pan to Selection** option.

With the **Pan to Selection** option enabled in an active list window, when you select an object in ChipPlanner or PinEditor, then it becomes visible in the active list window too. Of course, if the selected object does not exist in an active list, you will not see it selected in any active list window.

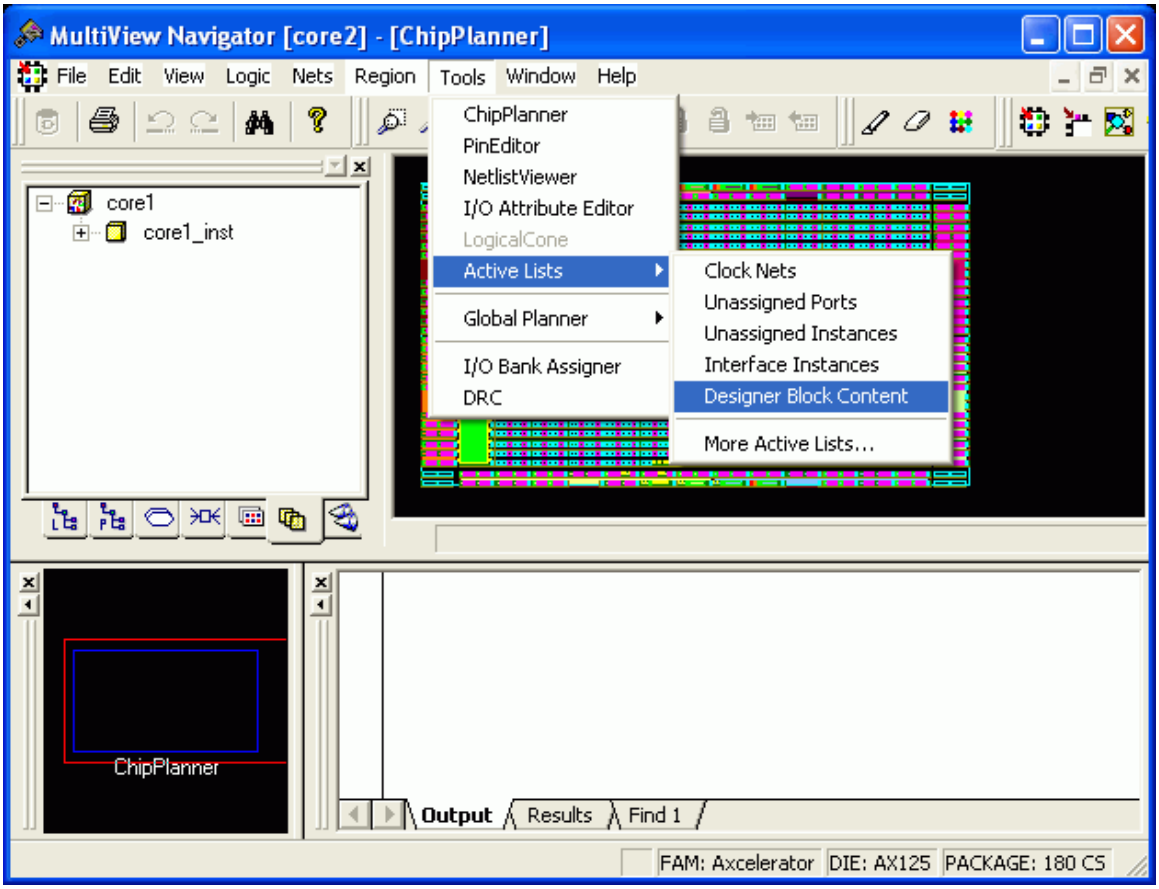


Figure 52 · Right-click Menu in an Active List Window

Using the Right-click Menu in an Active List Window with an Item Selected

To manipulate a specific instance in an active list, select it, and then choose from the options on its right-click menu. For example, you can display the instance's properties, and for user-defined active lists, you can also assign or unassign it from its location or region, lock or unlock it, and select its input or output nets.

See Also

Displaying Active Lists

Creating Active Lists

Copying Active Lists

Editing Active Lists

Deleting Active Lists

Displaying Active Lists

You can display more than one active list on your screen at the same time. All existing active lists appear on both the Tools and View menus.

To display an active list, simply choose it from the **Tools** or **View** menu. If the selected list is already open, choosing it from the Tools menu makes it the active list.

You can close an Active List window, and then re-open it by choosing it again from either the **Tools** or **View** menu.

Note: The Active List submenu in the View menu is enabled only if an Active List window is currently selected.

See Also

What are Active Lists?

Creating Active Lists

Copying Active Lists

Editing Active Lists

Deleting Active Lists

Creating Active Lists

You can create your own active lists. An active list can contain either macros, ports (I/Os), nets, or regions. You can use filters to determine which types of macros, ports, nets, or regions to include in your list. For example, you can create a list of all of the outgoing ports or all of the nets with a fan-out greater than six. You can also filter your list to include only instances, nets, or ports found within a specific block flow.

To create an Active List:

1. From either the **Tools or View** menu, choose **Active Lists > More Active Lists**.
2. In the **More Active Lists** dialog box, click **New**.
3. In the **Create Active List** dialog box, use the filter to specify the types of objects you want to include in your Active List. For example, to include only unassigned instances that begin with the letters "clk," enter **clk*** in the Name filter, and select **Unassigned** in the Instances tab. These fields accept wildcards. Wildcard characters include:

Wildcard	What It Does
?	Matches any single character
*	Matches any string
/	This is the level-bordering symbol. “A/B” designates “object B, which is part of instance A.”

4. Optionally, select Match case to filter on case-sensitive occurrences of a name. This limits the filter to include only text that matches the upper- and lowercase letters you enter.
5. Enter a name for your new active list.
6. Click **OK**.

The newly created Active List now appears on both the **Tools** and **View** menus.

Creating an Active List of Macros

You can create an active list containing macros (instances) filtered by name, cell type, and placement and lock status. Cell Type refers to the macro type. For example, you can include all macros of type AND by typing *AND* in the Cell Type field. Likewise, you can enter *OR2A* to list all the ORs used in the design. Usually cell types are prefixed with "ADLIB." When filtering on instances, Name or Cell Type can be blank, but not both.

Note: To see the cell types for your design, open the I/O Attribute editor. The Macro Cell column displays all of the cell types for your design.

For example, to create a list of unassigned, unlocked, global input buffers (GL*), enter the properties shown in the following filter:

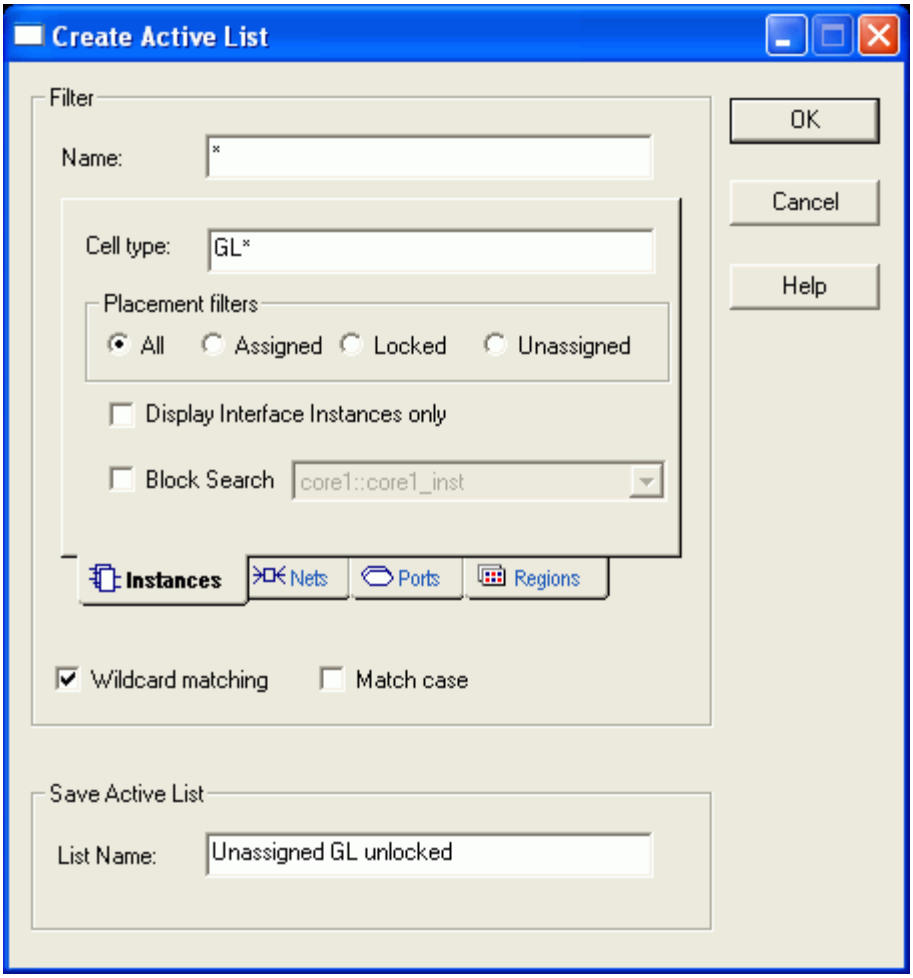


Figure 53 · Create Active List Dialog Box - Instances Tab

To find only macros connected to ports, select the **Display Interface Instances only** check box.

To find only instances in a specific user block or in all user blocks, select **Block search**, and then select the block from the drop-down list.

Creating an Active List of Nets

You can create an active list containing nets filtered by name and number of fan-outs. For example, to create a list of all nets with a fan-out greater than 4, enter the properties shown in the following filter:

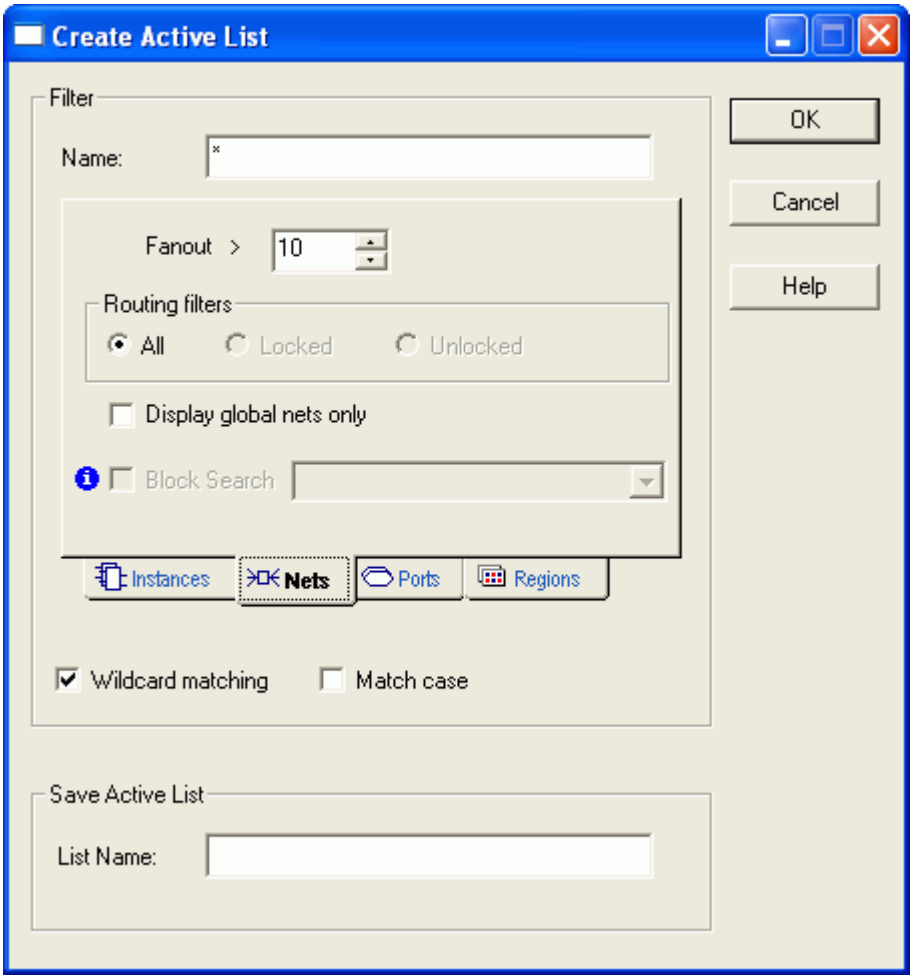


Figure 54 · Create Active List Dialog Box - Nets Tab

Select the **Display global nets only** check box to include only clock nets in your active list.

Creating an Active List of Ports

You can create an active list of ports filtered by name, direction (all ports, input ports, output ports, and ports you can use for both input and output), and placement and locked status. For example, to create a list of all assigned input ports, enter the properties shown in the following filter:

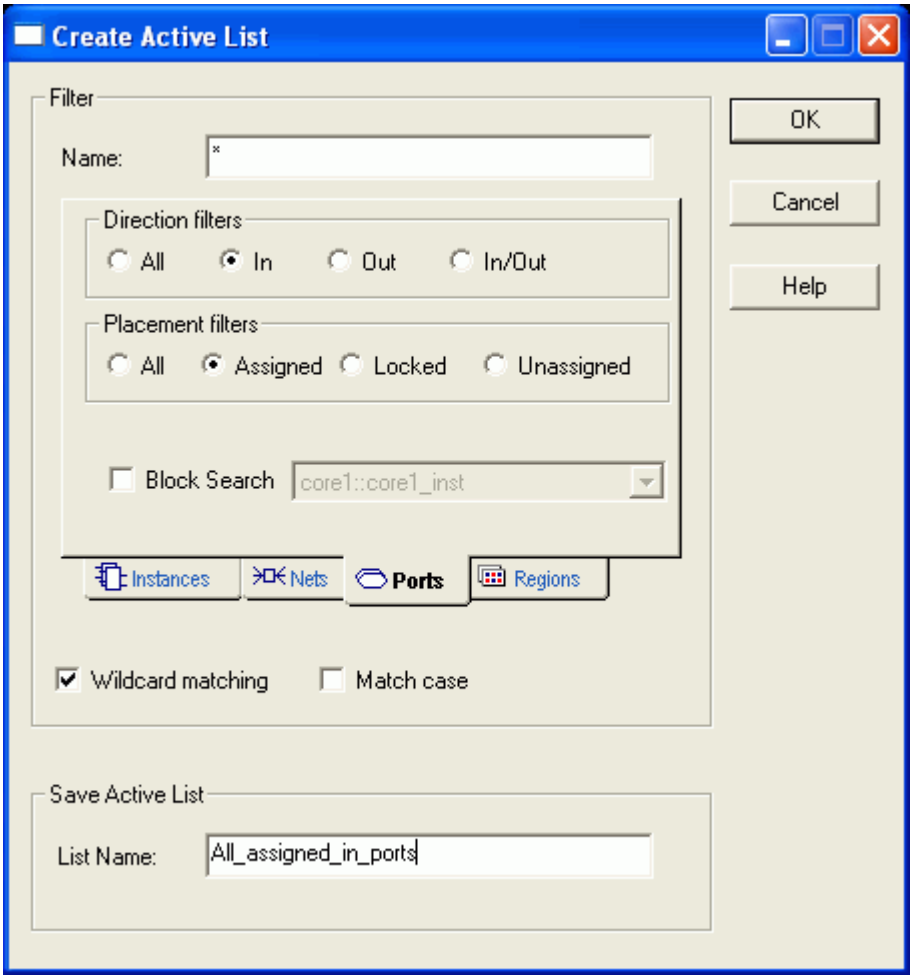


Figure 55 · Create Active List Dialog Box - Ports Tab

Creating an Active List of Regions

You can create an active list of regions filtered by name and type. For example, to create a list of all empty regions, enter the properties shown in the following filter:

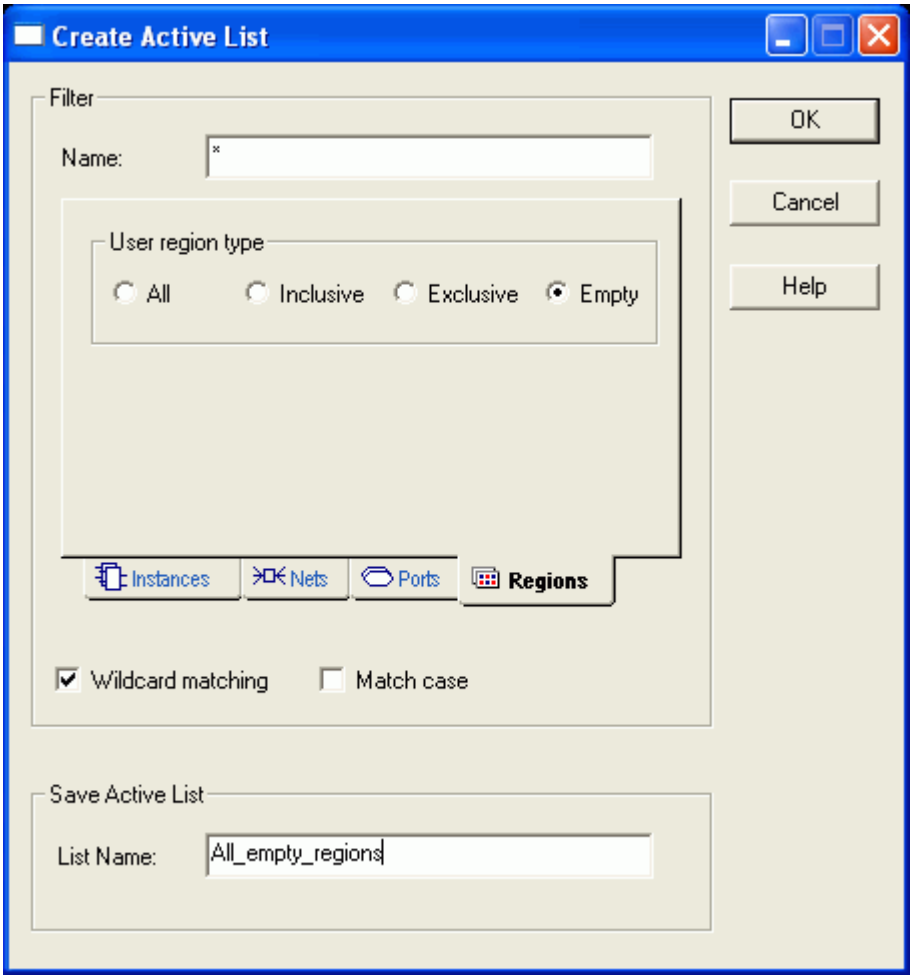


Figure 56 · Create Active List Dialog Box - Regions Tab

See Also

What are Active Lists?

Displaying Active Lists

Copying Active Lists

Editing Active Lists

Deleting Active Lists

Copying Active Lists

You can copy and modify existing active lists. This feature is useful if you want to create a new list that is similar to but not exactly the same as an existing active list.

To copy an Active List:

1. From either the **Tools or View** menu, choose **Active Lists > More Active Lists**.
2. In the **More Active Lists** dialog box, select the list to copy, and click **Copy**.
3. In the **Save List Copy As** dialog box, enter a name for your new active list. This list will contain the same properties as the one being copied.
4. Click **OK**. Your new list now appears in the **More Active Lists** dialog box.
5. Click **Edit** to display the **Edit Active Lists** dialog box in which you can modify the properties of the list.
6. Click **OK** to save your changes.
7. Click **Close** to close the **More Active Lists** dialog box.

The newly created active list now appears on both the **Tools** and **View** menus.

See Also

What are Active Lists?

Displaying Active Lists

Creating Active Lists

Editing Active Lists

Deleting Active Lists

Editing Active Lists

You can change the name of an existing active list as well as modify its contents.

To edit an Active List:

1. Select the active list to edit.
2. From the **View** menu, choose **Edit Current Active List**.

The **Edit Active List** dialog box appears with the properties of the selected active list.

3. In the **Edit Active List** dialog box, modify the properties you want to change.
4. Click **OK**.

See Also

What are Active Lists?

Displaying Active Lists

Creating Active Lists

Copying Active Lists

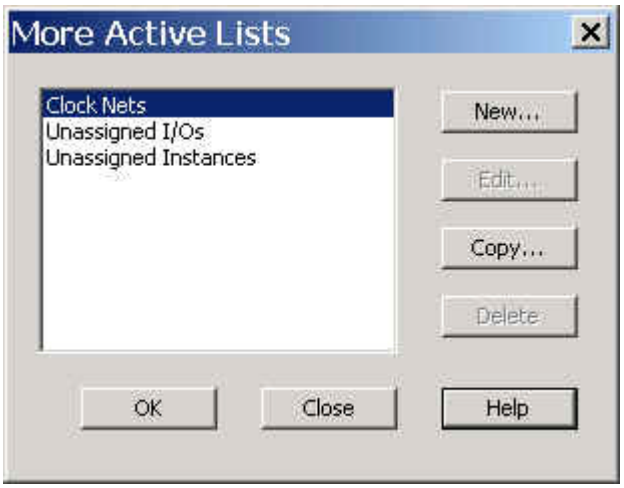
Deleting Active Lists

Deleting Active Lists

Use the **Delete** command in the Active List menu to delete the selected active list.

1. From either the **Tools** or **View** menu, choose **Active Lists** > **More Active Lists**.

The More Active Lists dialog box appears.



2. In the **More Active Lists** dialog box, select the active list to delete, and click **Delete**. You cannot delete a predefined active list.

A verification message appears asking you to verify that you want to delete the active list.

3. Click **Yes** to delete the active list.
4. Click **OK** to close the **More Active Lists** dialog box.

See Also

[What are Active Lists?]

[Displaying Active Lists]

[Creating Active Lists]

[Copying Active Lists]

[Editing Active Lists]

Reference

Tools Window

In the MultiView Navigator interface, the Tools window is the area in which you view and edit your designs. Within this window, you can open a window for each tool: ChipPlanner, PinEditor, I/O Attribute Editor, and NetlistViewer. Logical Cone and Active List windows also appear in this window.

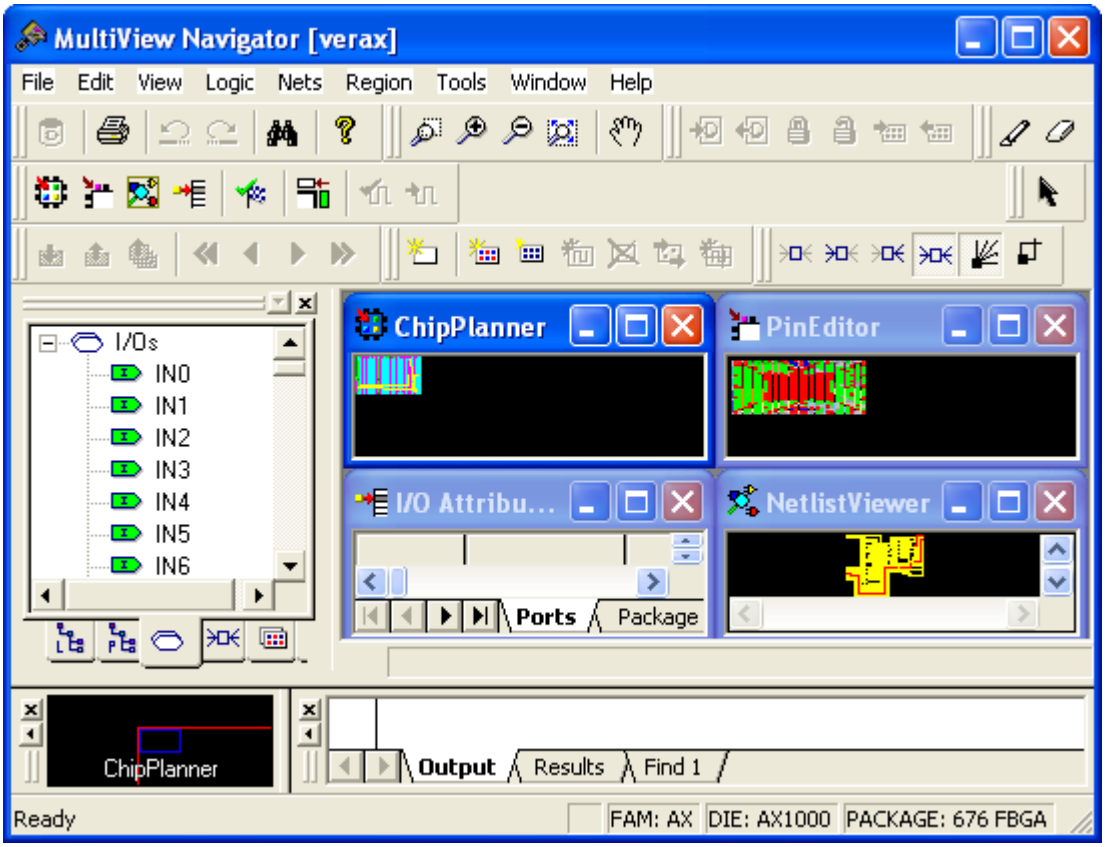


Figure 57 · PinEditor, NetlistViewer, I/O Attribute, Editor, and ChipPlanner in the Tools Window

World Window

Use the World window to control which portion of the design appears in the active window of MultiView Navigator's Tools window. The blue rectangle represents the area of the chip. The red rectangle (known as the Viewing rectangle) represents the part of the design you see in a tool window.

To move the displayed area to another part of the design, click and drag the red rectangle to the area on the blue rectangle you want to see. To specify a new display area, right-click and drag out a new Viewing rectangle on the blue rectangle.

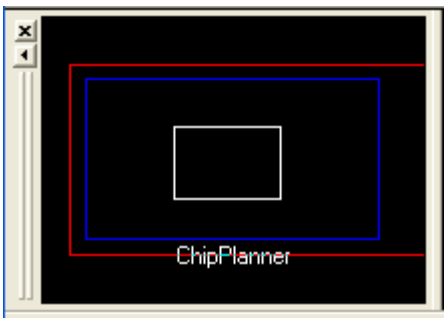


Figure 58 · World window in ChipPlanner

Log Window

The Log window displays information about your tool. This area also displays the results of any search that you perform. Click the tabs at the bottom of the window to view additional information. You can choose:

- **Output** (contains errors, warnings, and other information)
- **Results** (contains information about a message in the message bar)
- **Find1** (default, contains the results of a search)

Colors and Symbols

Messages are color-coded and represented by symbols. The default colors are:

Type	Color
Errors	Red
Warnings	Blue
Information	Black

You can change the colors in the Designer Preferences dialog box. However, you will not see your changes until you restart MultiView Navigator.

Output Tab

The Output tab displays all errors, warnings, and informational messages. It contains a complete history of your design session. Error and warning messages that are dark blue and underlined are linked to online help to provide details or helpful workarounds. Clicking an underlined message displays online help.

Results Tab

The Results tab displays the results of a command or other action. Clicking a message in the message bar displays more information in this tab. The view within this tab is reset when you execute a new command or open a new design. To see a complete history of your design session, click the **Output** tab.

Find Tab

The Find tab displays the results of a search performed with the **Find** command. You can create several Find tabs, one for each search (for example, Find1, Find2, or Find3). You can also drag and drop instances and ports from a **Find** output pane to the **ChipPlanner** window.

Tip: Tip: The right-click menu available from the **Hierarchy** window is also available from the Find tab.

Message Bar

The message bar displays errors, warnings, and other informational messages.

Clicking the icon to the left of the message in the message bar displays more information about the message in the **Results** tab of the **Log** window.

Tip: Tip: You can copy, show more information about, and clear a message from the right-click menu. Choosing **Copy** copies the message to the Clipboard, so you can paste it in another application. Choosing **Show More Info** displays more details about the message in the **Log** window. Choosing **Clear** erases the message from the Message bar.

Status Bar

Family, die, and package information appears in the right side of the status bar of the MultiView Navigator interface as shown in the example below:

To see other information in the status bar:

- Hold your mouse over an assigned macro to see the pin number, instance name, net name, macro cell, and locked or unlocked status bar.
- Hold your mouse over a module, instance, or bank in ChipPlanner to see information about it.
- Select a macro, zoom in, and click one of the ratsnest lines to see information about nets.
- Hold your mouse over a toolbar button or a menu command to see a short description of that command.

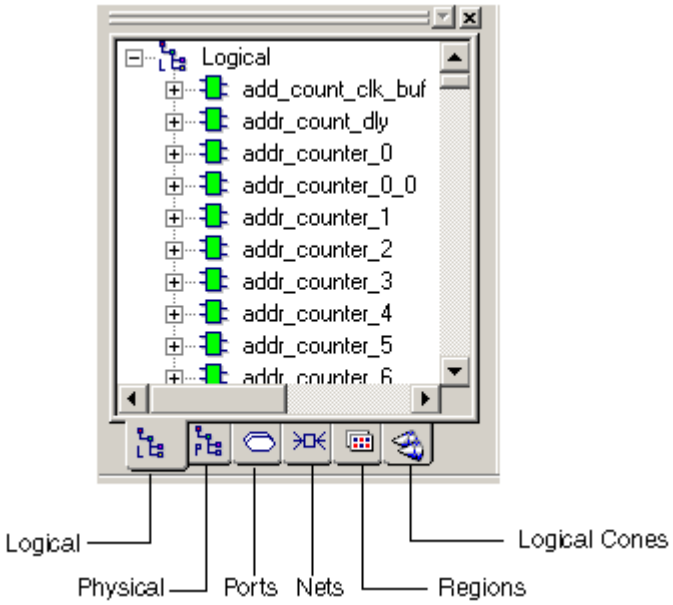
Note: For NetlistViewer, the current page number and the total number of pages also appear in the status bar.

Hierarchy Window

Overview of Hierarchy Window

The Hierarchy window (as shown in the figure below) provides easy navigation through the Hierarchy. The Logical tab in this window provides a hierarchical overview of the design.

Click the tabs at the bottom of this window to view macros, instances, ports, nets, regions, and logical cones in your design. Additionally, a Block tab will appear in the Hierarchy window if the design contains Blocks.



Hierarchy Window

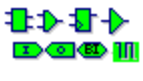
You can use these tabs to explore each level of the hierarchy and to trace signals. You use the Hierarchy window tabs with ChipPlanner, NetlistViewer, PinEditor, and I/O Attribute Editor to help identify critical paths.

Tip: Tip: Right-click an object to use its context-sensitive menu.

In all Hierarchy views, you can right-click an object, and select **Properties** to display its properties.

Each view contains color-coded icons to indicate its logic type and state. These icons are explained in the following table:

Table 4 · Icons in Hierarchy View

Icon	Color	What it Represents
	White	The logic or I/O is unassigned.
	Green	The logic or I/O is assigned.

Icon	Color	What it Represents
	Hashed green	Some instances in the block of logic are assigned.
	Red and blue grid	The region is either inclusive or LocalClock.
	Blue grid	The region is exclusive.
	White	The region is empty.
	Black icon	The logic is handled as one unit and cannot be expanded. This icon appears next to the ARM core logic.
	Cone icon	The object is a Logical Cone.
	Blue checkmark	The logic is assigned to a region.
	Gray checkmark	Some instances in the block of logic are assigned to a region.
	Blue lock	The entire block of assigned logic is locked to a location.
	Gray lock	Some instances in the block of assigned logic are locked to a location.
	Yellow cube	Indicates a block flow.
	Blue	Indicates this macro, net, or port only exists in the pre-optimized view.

The Logical tab shown below illustrates that the selected logic is assigned to a region and locked. Only the Logical tab shows the logical hierarchy of the design. The Physical tab shows the physical hierarchy. The other tabs are not hierarchical.

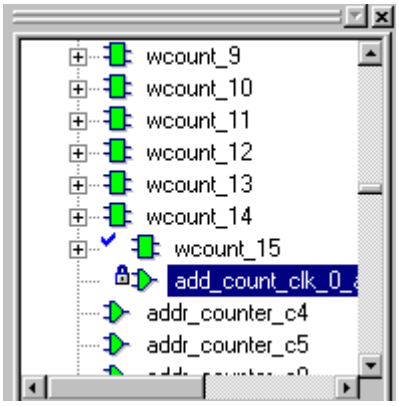


Figure 59 · Logical Tab - Checkmark and Lock Icons

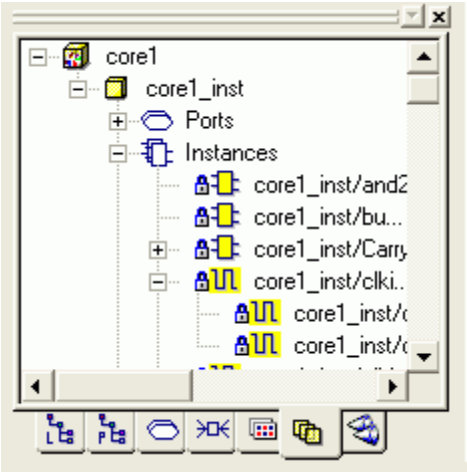


Figure 60 · Block Tab - Locked instances and nets are highlighted

See Also

Logical Tab

Physical Tab

Ports Tab

Nets Tab

Regions Tab

Logical Cones Tab

Block Tab

Logical Tab

The Logical tab displays the logic in your design.

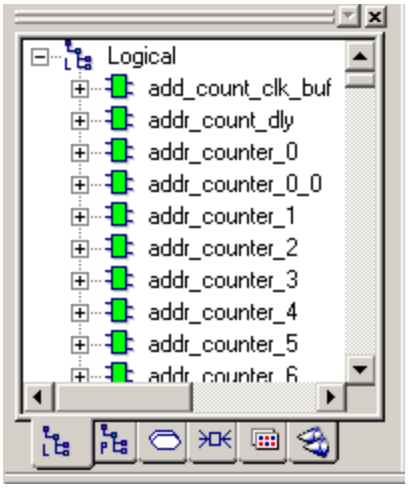


Figure 61 · Hierarchy Window - Logical Tab

When you select a macro in this view, the macro and all of its instances are selected in all other views where it appears.

In this view, you can assign or unassign a macro to a region or location from the right-click menu or drag a macro from this view to the ChipPlanner or PinEditor window.

You can also lock an assigned macro or unlock a locked macro in this view.

Note: You can only lock macros that are currently assigned to a location.

Physical Tab

The Physical tab shows the hard macros and all of its instances in your design with their full hierarchical names. This tab provides you with more detail than the Logical tab.

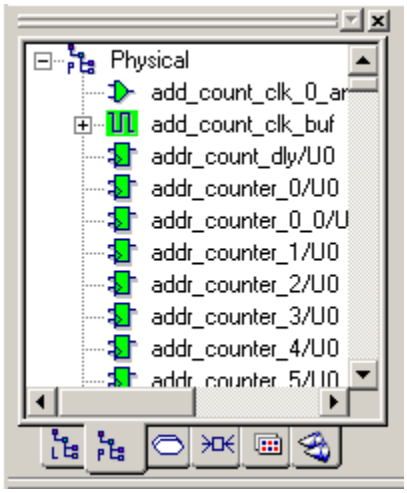


Figure 62 · Hierarchy Window - Physical Tab

When you select a macro in this tab, the macro and all of its instances are selected in all other views where it appears.

In this view, you can assign or unassign an instance to a region or location from the right-click menu or drag an instance from this view to the ChipPlanner or PinEditor window.

You can also lock an assigned instance or unlock a locked instance in this view.

Note: You can only lock macros or instances that are currently assigned to a location.

Ports Tab

The Ports tab shows all the input, output, and bidirectional ports in your design.

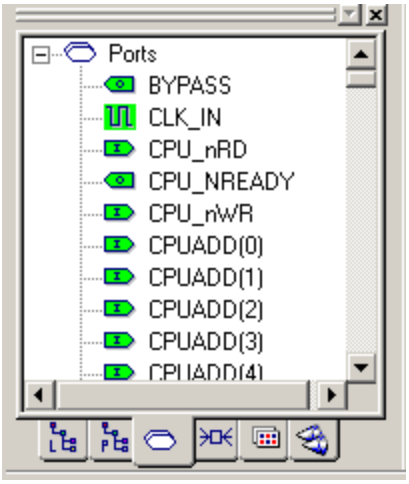


Figure 63 · Hierarchy Window - Ports Tab

When you select a port in this view, the port is selected in all other views where it appears.

In this view, you can assign a port to an I/O region or location, lock an assigned port, and unlock a locked port.

Note: You can only lock ports that are currently assigned to a location. Block ports have a plus sign (+) in front of them to indicate that they can be expanded to show connected ports and instances.

Nets Tab

The Nets tab displays the nets that connect two or more nodes in your design. The symbol to the left of the net indicates the type of driver. A checkmark appears next to a net that is assigned to a LocalClock region.

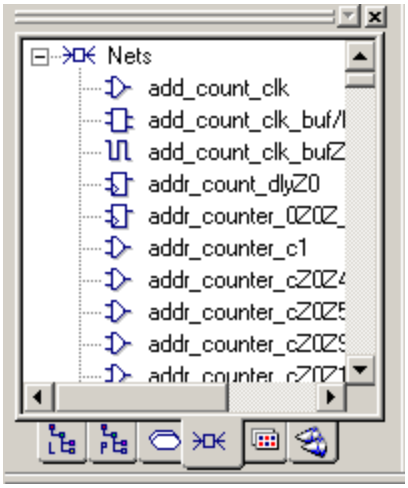


Figure 64 · Hierarchy Window - Nets Tab

When you select a net in this view, the net is selected in all other views where it appears.

In this view, you can right-click a net and select **Properties** to display its properties (name, type, location, status, and PinList).

To display a net's properties:

1. Click the **Nets** tab in the **Hierarchy** window.
2. Select a net, right-click, and then choose **Properties** from the right-click menu.
3. In the **Net Properties** dialog box, click **Routing** to see routing details or **PinList** to see the names and locations of the pins.
4. Click **Close** to close the dialog box.

Regions Tab

The Regions tab shows regions you defined in your design. It also shows instances assigned to that region.

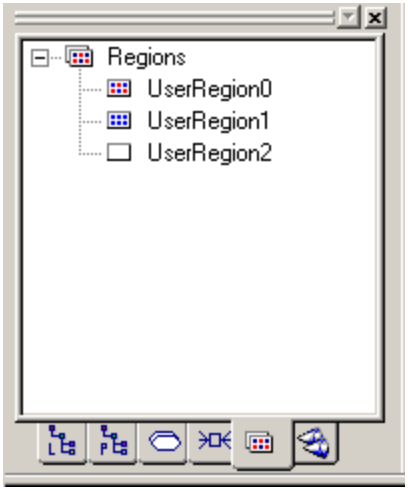


Figure 65 · Hierarchy Window - Regions Tab

In this view, you can right-click a region and select **Properties** to display its properties (name, type, extents, and resource usage). You can also change a region's color in its Properties dialog box.

Additionally, from this view, you can assign an instance to a region, unassign instances from a region, and delete a region.

Note: To assign an instance to more than one region, those regions must be overlapping.

Logical Cones Tab

The Logical Cones tab displays a list of all Logical Cones that you created in your design

A Logical Cone is a netlist view you create to contain only the objects you want to see, such as part of the netlist. You can create Logical Cones to help you navigate and analyze a specific part of the design.

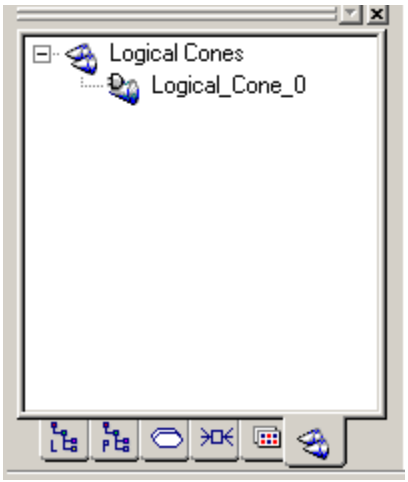


Figure 66 · Hierarchy Window - Logical Cones Tab

Use this view to display only a specific portion of the netlist. Select the objects of interest from the netlist in NetlistViewer and add them to a specific cone view.

Note: The Logical Cones view supports cross-probing. All commands for creating a Logical Cone view are available from the LogicalCone menu in NetlistViewer and from the NetlistViewer right-click menu.

Block Tab

The Block tab shows the blocks in your design. This tab appears only when your design contains blocks.

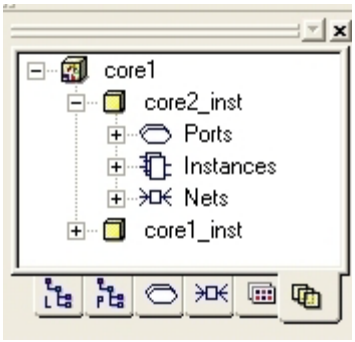


Figure 67 · Hierarchy Window - Block Tab

Instances and nets that are locked (fixed) in the block appear highlighted in yellow. You cannot change the placement or routing constraints in a locked block.

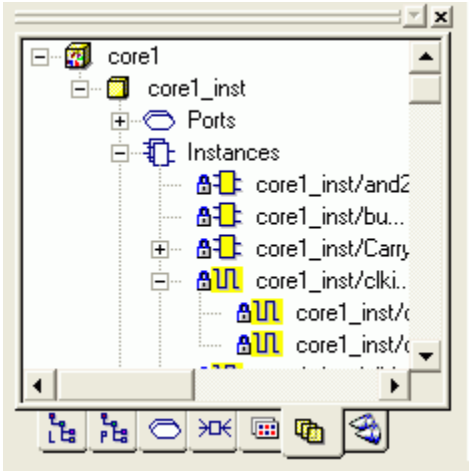


Figure 68 · Locked Instances and Nets Appear Highlighted

In the Block tab, you can right-click a block and select **Properties** to display its properties.

See Also

Designer Block Properties dialog box

Menus, Toolbar Buttons, and Shortcut Keys

Command Overview

The File, Edit, View, Tools, Windows, and Help menus appear in all four tools available from the MultiView Navigator: ChipPlanner, PinEditor, NetlistViewer, and I/O Attribute Editor. Other menus are specific to the tool you are using.

File Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Commit		CTRL + S	Saves changes to the working design for this Designer session only **To save changes to disk, you must also save your file in Designer.**
Commit and Check		CTRL + H	Saves changes to the working design for this Designer session and runs the Prelayout Checker.
Print Preview			Displays the active design in a Preview window
Print		CTRL + P	Displays the Print dialog box from which you can print your active design
Exit			Closes the MultiView Navigator

Edit Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Undo		CTRL + Z	Reverses your last action If you previously reserved a pin, **Undo Reserve Package Pin** appears instead.
Redo		CTRL + Y	Reverses the action of your last Undo command If you previously unreserved a reserved pin, **Redo Reserve Package Pin** appears instead.
Cut		CTRL + X	Removes the selection from your design
Copy		CTRL + C	Copies the selection to the Clipboard
Paste		CTRL + V	Pastes the selection from the Clipboard
Select All		CTRL + A	Selects all rows in I/O Attribute Editor. Not available for other MVN tools.
Find		CTRL + F	Displays the Find dialog box, which you use to locate instances, nets, ports, and regions
Highlight		CTRL + B	Changes the pointer into the highlighter tool, which you can use to highlight objects. Clicking an object changes it to the selected highlight color
Unhighlight All		CTRL + SHIFT + B	Removes highlighting from all highlighted objects, changing them to their original colors
Highlight Color		CTRL + R	Displays the Color palette so you can select a highlight color
I/O Bank Settings		CTRL + I	Displays the I/O Bank Settings dialog box, in which you can assign technologies and VREF pins to your I/O banks
Reserve Pins		CTRL + M	Displays the Reserve Pins for Migration dialog box.

Command	Icon	Shortcut	Function
for Migration			This dialog box enables you to automatically reserve pins that are not bonded in the destination device that you select.

View Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Zoom In		CTRL + +	Magnifies the view by a factor of 2 (scale = 2x) **If using the keyboard shortcut, use the + on the numeric keypad only**.
Zoom Out		CTRL + -	Reduces the view by a factor of 2 (scale = .5x) **If using the keyboard shortcut, use the - on the numeric keypad only**.
Zoom Window		CTRL + W	Drag out an area to enlarge
Zoom Fit		CTRL + 0	Fits the entire design within the active Tools window
Redraw			Redraws the screen
Active List			Displays a submenu of choices: **<User-defined lists>** - displays user-defined lists **<Pre-defined lists>** - displays any pre-defined lists such as Unassigned Macros, Unassigned I/Os, etc. **Edit Current Active List** - displays the Edit Active List dialog box with the settings for the current Active List. **More Lists** - displays a dialog box in which you can choose to create a new list, edit a list, copy a list, or delete a list.
Toolbars			Hides or displays groups of toolbar buttons
Windows			Hides or displays the Hierarchy window, Log window, Status Bar, or World window
Display Settings		CTRL + D	Displays the Display Settings dialog box, which provides a list of all the architectural features you can turn on and off in your tool
Properties			Displays the ChipPlanner Properties dialog box, which enables you tochoosewhether you want to bring a macro or net into view after you select it

Logic Menu

This menu is available only for the ChipPlanner, PinEditor, and I/O Attribute Editor tools in the MultiView Navigator.

Command	Icon	Shortcut	Function
Assign To Location		CTRL + K	Assigns the selected object to the selected location
Unassign From Location		CTRL + SHIFT + K	Unassigns the selected object from its current location
Unassign All From Location			Unassigns all instances from their location
Lock		CTRL + L	Locks the selected instance
Unlock		CTRL + SHIFT + L	Unlocks the selected locked instance
Lock All			Locks all I/Os in PinEditor or all instances in ChipPlanner
Unlock All			Unlocks all I/Os in PinEditor or all instances in ChipPlanner
Assign To Region		CTRL + N	Assigns the selected I/O or instance to the selected region
Unassign From Region		CTRL + SHIFT + N	Unassigns the selected I/O or instance from its current region
Unassign All From Region			Unassigns all I/Os and instances from the selected region
Properties			Displays the Logic Properties dialog box, in which you can change the properties of the selected logic

Nets Menu

This menu is available only for the ChipPlanner tool in the MultiView Navigator.

Command	Icon	Function
Show Input Only		Shows all input nets for the selected macro
Show Output Only		Shows all output nets for the selected macro
Show Input & Output		Shows all input and output nets for the selected macro
Hide All		Hides all input and output nets for the selected macro
Show Ratsnest		Displays net connectivity between assigned macros by connecting lines from the output pins to all input pins
Show Routes		Displays a representation of the routes
Properties		Displays the Net Properties dialog box

Region Menu

This menu is available only for the ChipPlanner tool in the MultiView Navigator.

Command	Icon	Shortcut	Function
Create Inclusive			Use to create an inclusive region in your design
Create LocalClock			Use to create a local clock region for the selected net
Create QuadrantClock			Use to create a quadrant clock region for the selected clock net
Create Exclusive			Use to create an exclusive region in your design
Create Empty			Use to create an empty region in your design
Lock			Locks the selected region
Unlock			Unlocks the selected region
Delete		Del key	Deletes the selected region from your design
Assign/Unassign Logic			Assign or unassign instances to the selected region
Properties			Displays the Region Properties dialog box, in which you can change the properties of the selected region

Package Menu

This menu is available only for the PinEditor tool in the MultiView Navigator.

Command	Shortcut	Function
View From Top		Displays a top-down view of the package
View From Bottom		Displays a bottom-up view of the package

Schematic Menu

This menu is available only for the NetlistViewer tool and Logical Cone windows in the MultiView Navigator.

Command	Shortcut	Function
Pop		Displays the next higher level in the Hierarchy
Push		Displays the next lower level in the Hierarchy
Top		Displays the top level of the Hierarchy
Go to First Page		Displays the first page of the current level of the design
Go to Previous Page		Displays the previous page of the current level of the design
Go to Next Page		Displays the next page of the current level of the design
Go to Last Page		Displays the last page of the current level of the design
Follow Net Into		Displays a dialog box in which you select the next page or instance of the net you want to see
Go to Net Driver		Jumps to the Net Driver
Allow Page Splitting		Enables or disables page splitting in your view
Show Pre-optimized Netlist		Displays the pre-optimized netlist (This is the default view.)
Show Optimized Netlist		Displays the optimized, flattened netlist
Fit to Page		Adjusts each page of the schematic so that its parts will fit neatly on each printed page (Allow Page Splitting must be enabled)

LogicalCone Menu

This menu is available only for the NetlistViewer tool and Logical Cone windows in the MultiView Navigator.

Command	Shortcut	Function
Create New Cone		Opens a new Logical Cone window, which is set as the active cone
Rename Cone		Displays a dialog box, in which you can change the name of the active cone
Fold Selection		Hides all the logic inside the selected hierarchical instance in the cone view
Unfold Selection		Shows the logic that was added into the selected hierarchical instance in the cone view
Add to Active Cone		Displays a submenu of choices: **Selection** - adds selected objects to the active cone **Highlighted Group** - adds a group of highlighted objects to the active cone **Driver** - adds the instances which have a pin driving the selected net, input pin, or instance to the active cone **All Driven Logic** - adds all instances which have a pin driven by the selected net, output pin, or instance to the active cone **Adjacent Logic** - displays a dialog box in which you select instances to add to the active cone
Remove From Active Cone		Displays a submenu of choices: **All Logic** - removes all objects from the active cone **Selection** - removes the selected object from the active cone **Highlighted Group** - removes the selected group of objects from the active cone

Format Menu

This menu is available only for the I/O Attribute Editor tool in the MultiView Navigator.

Command	Icon	Shortcut	Function
Row > Hide			Hide the selected row(s)
Row > Unhide			Show all hidden rows between the selected rows
Column > Hide			Hide the selected column(s)
Column > Unhide			Show all hidden columns between the selected columns
Column > Freeze Pane			Freeze the selected columns(s)
Column > Unfreeze Pane			Unfreeze the selected columns(s)
Column > Autofit			Sets the width of columns within the table to accommodate all the text for any given row in those columns, including the column headings

Note: If no rows or columns are selected and you choose Unhide, all hidden rows or columns are displayed.

Tools Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Function
ChipPlanner		Displays the placement of I/O and logic macros in your chip in the Tools window
PinEditor		Displays the pin out in the Tools window
NetlistViewer		Displays the netlist in the Tools window
I/O Attribute Editor		Displays the attributes in your design in the Tools window
LogicalCone		Displays the last created Logical cone in the Tools window
Active Lists		Displays a submenu of choices: **Clock Nets** - displays a list of all clock nets in the design **Interface Instances** - displays a list of all macros connected to ports in the design **Unassigned I/Os** - displays a list of all unassigned I/Os in the design **Unassigned Instances** - displays a list of all unassigned I/Os in the design **More Active Lists** - displays a dialog box in which you can choose to create a new list, edit a list, copy a list, or delete a list
Global Planner		Displays a submenu of choices: **Assign All Nets** - assign all global nets in the design **Run Global Checker** - checks the validity of the current global net assignments
I/O Bank Assigner		Assigns a voltage to every I/O bank that does not have a voltage assigned to it and if required, a VREF pin
DRC		Runs the Prelayout Checker to ensure that the design can be placed and routed

Window Menu

This menu is available for all tools in the MultiView Navigator.

Command	Function
Close Window	Closes the currently active tool window within the Tools window If the tool has more than one window open, this command closes all the windows for that tool.
Cascade	Arranges windows so you can see the title bar of each window
Tile Horizontally	Arranges windows side-by-side in a horizontal pattern
Tile Vertically	Arranges windows side-by-side in a vertical pattern
Arrange Icons	Arranges minimized windows left-to-right across the bottom of the Tool window
<*Tool name*>	Makes the selected tool active

Help Menu

This menu is available for all tools in the MultiView Navigator.

Command	Icon	Shortcut
<*Tool name*> Help		Displays the first Help topic for the active tool
MultiView Navigator Help		Displays the first Help topic for the MultiView Navigator, which provides an overview of the MVN interface
About the MultiView Navigator		Displays the current version number and copyright information for the MultiView Navigator

Dialog Boxes

Assign Instances to Regions Dialog Box

Use this dialog box to assign or unassign:

- Instances to regions
- Instances associated with a net to a region

Region Name

Select the region to which to assign instances. Only logic that can be assigned to the region appears in the Unassigned instances list box.

Unassigned Instances

Select one or more instances to assign, click **Assign**, and then click **OK**. To assign all unassigned instances shown in the list box (ignores any instances currently selected), click **Assign All**, and then click **OK**.

Note: The total number of instances that you can assign as well as the number of currently selected unassigned instances appears under the list box.

Filter Unassigned Instances

To display a subset of the unassigned instances, you can create and apply filters.

- To filter the list box by a pattern, select **Matching pattern**, enter the string to match, and then click **Filter**. For example, enter *U18* to display only unassigned instances containing the characters U18.
- To filter by a net name, select **Connected to nets matching pattern**, enter the name of the net to match, and then click **Filter**. The Unassigned instances list will display only macros assigned to the net name you specified. For example, enter add_count_clk to display only macros assigned to the net named add_count_clk.
- To filter by a port name, select **Connected to ports matching pattern**, enter the name of the port to match, and then click **Filter**. The Unassigned instances list will display only macros assigned to the port name you specified.
- Filters are valid for both regular and Block flows. Note that in regular flows, each port is connected to only one instance, which is an I/O.

Assigned Instances

Select one or more instances to unassign, click **Unassign**, and then click **OK**. To unassign all assigned instances shown in the list box (ignores any instances currently selected), click **Unassign All**, and then click **OK.** The list box displays prefixes to macro names (components) in blue text.

The list box displays the total number of instances/components that you can unassign as well as the number of currently selected assigned instances/components.

Filter Assigned Instances

To display a subset of the assigned instances, you can also create and apply filters. Type a pattern or net name you want to match, and then click **OK**. Only instances that match your criteria appear in the Assigned instances list box.

Show Usage

Click to display region usage information, which includes resource types, resources assigned, and resources that can be assigned.

See Also

Assigning a Net to a Region

Assigning a Macro to a Region

Assign Nets to Regions Dialog Box

Use this dialog box to assign or unassign nets to regions.

Region Name

Select the region to which to assign nets. Only nets that can be assigned to the region appear in the Assignable nets list box.

Assignable Nets

Select one or more nets to assign, click **Assign**, and then click **OK**. To assign all unassigned nets shown in the list box, click **Assign All**, and then click **OK**.

The list box displays the total number of nets that you can assign as well as the number of currently selected unassigned nets.

Filter Unassigned Nets

To display a subset of the unassigned nets, you can create and apply filters.

- To filter the list box by a pattern, select **Matching pattern**, enter the string to match, and then click **Filter**. For example, enter *U18* to display only unassigned nets containing the characters U18.
- To filter by instance connection, select **Connected to instance**, enter the name of the instance to match, and then click **Filter**. The Assignable nets list will display only nets connected to the instance you specified. For example, enter add_count_clk to display only nets connected to the instance named add_count_clk.
- To filter by fanout, select **Fanout greater than**, enter the fanout limit, and then click **Filter**. The Assignable Nets list displays only nets with fanouts greater than the value you specified.

Include Driver

The Include Driver checkbox enables you to assign all instances connected by a net, including the driver macro. Check the Include Driver checkbox when assigning a net to a region to include the driver. The Include Driver checkbox is unchecked by default.

The Include Driver checkbox has no effect when you unassign a net.

Assigned Nets

Select one or more nets to unassign, click **Unassign**, and then click **OK**. To unassign all assigned nets shown in the list box, click **Unassign All**, and then click **OK.**

The list box displays the total number of nets that you can unassign as well as the number of currently selected assigned nets.

Nets that include driver macros when assigned to a region are listed in blue text.

Assigned nets that do not include a driver macro are shown in black text.

Filter Assigned Nets

You can create and apply filters to display a subset of the assigned nets. Type a pattern or net name you want to match, and then click **Filter**. Only nets that match your criteria appear in the Assigned Nets list box.

Show Usage

Click to display region usage information, which includes resource types, resources assigned, and resources that can be assigned.

See Also

Assigning a Net to a Region

Assigning a Macro to a Region

ChipPlanner Properties Dialog Box

Use this dialog box to view:

- The selected macro
- The selected net

Move the Display to Show Selected Macro

Check this box to bring a macro into view when you select it in the ChipPlanner window. Uncheck this box if you do not want ChipPlanner to change your viewing area each time you select a macro.

Center Display Around Selected Net

Check this box to bring a net into view and zoom into it when you select it in the ChipPlanner window. Uncheck this box if you do not want ChipPlanner to change your viewing area each time you select a net.

Create or Edit Active Lists Dialog Box

Use this dialog box to either create an active list or edit the properties of one.

Name

Type a partial name for the objects to include. This field accepts wildcards.

Cell Type

Enter a few letters representing the type of macro to add to the active list. For example, type GL* to add all global input buffers.

Placement Filters

Select one of the following.

- **All** - Include all instances, regardless of status
- **Assigned** - Include only instances assigned to a location
- **Locked** - Include only locked instances
- **Unassigned** - Include only instances that are not assigned to a location

Display Interface Instances only

Select this box to include only macros connected to ports.

Block Search

Select this box to include only instances in a specific Block flow. Then select the Block to find from the drop-down list.

Fanout

Click the up and down arrows to select the minimum number of fan-outs the selected nets must contain to be included in the active list.

Display clock nets only

Select this box to include only clock nets in your active list.

Direction

Select the type of ports to include.

- **All** - Include all ports, regardless of type
- Input - Include only input ports
- Output - Include only output ports
- In/Out- Include only ports that accept both inputs and outputs

User Region Type

Select the type of region to include.

- **All** - Include all regions, regardless of type
- Inclusive - Include only regions assigned as Inclusive, which means that the place-and-route tool can place logic within the region
- Exclusive - Include only regions assigned as Exclusive, which means that the place-and-route tool cannot place logic within the region (supported only for ProASIC3 families)
- Empty - Include only regions assigned as Empty, which means that the place-and-route tool cannot place logic within the region but that the routing resources within the region can be used

Wildcard Matching

Wildcard characters include:

Wildcard	What It Does
?	Matches any single character
*	Matches any string
/	This is the level-bordering symbol. “A/B” designates “object B, which is part of instance A.”

Match Case

Select to search for case-sensitive occurrences of a word or phrase. This limits the active list to only the names that match the upper- and lowercase characters you enter.

List Name

Type a name for this active list.

I/O Bank Settings Dialog Box (IGLOO and ProASIC3 only)

To access this dialog, from the **Edit** menu, choose **I/O Bank Settings**.

Use this dialog box to assign I/O technologies to I/O banks in IGLOO (excluding IGLOOe) and ProASIC3 (excluding ProASIC3L and ProASIC3E) devices.

Choose Bank

Choose a bank from the drop-down list. If you do not assign I/O standards to a bank, that bank uses the default standard selected in the Device Selection Wizard.

Locked

Select this option to lock all I/O banks, so the I/O Bank Assigner cannot unassign and re-assign the technologies in your design.

Select All Technologies That the Bank Should Support

Selecting an I/O standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further, selecting GTLP (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.

VCCI

Each I/O bank has a common supply voltage, VCCI, for the I/Os within that bank.

Click **Apply** to assign the selected I/O standards to the selected bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.

See Also

Manually Assigning Technologies to I/O Banks

Assigning VREF Pins

I/O Bank Settings Dialog Box

To access this dialog, from the **Edit** menu, choose **I/O Bank Settings**.

Use this dialog box to assign I/O technologies to I/O banks in IGLOOe, Fusion, ProASIC3L, ProASIC3E, and Axcelerator devices.

Choose Bank

Choose a bank from the drop-down list. If you do not assign I/O standards to a bank, that bank uses the default standard selected in the Device Selection Wizard.

Locked

Select this option to lock all I/O banks, so the I/O Bank Assigner cannot unassign and re-assign the technologies in your design.

Select All Technologies That the Bank Should Support

Selecting an I/O standard selects all compatible standards and grays out incompatible ones. For example, selecting LVTTL also selects PCI, PCIX, and LVPECL, since they all have the same VCCI. Further, selecting GTLP (3.3V) disables SSTL3 as an option because the VREFs of the two are not the same.

VCCI

Each I/O bank has a common supply voltage, VCCI, for the I/Os within that bank. (Technologies not allowed for the selected VCCI appear grayed out.)

VREF

A voltage referenced I/O input (VREF) requires an input referenced voltage. You must assign VREF pins to IGLOOe, Fusion, ProASIC3L (A3PE3000L only), ProASIC3E, and Axcelerator devices before running Layout.

Note: You cannot assign VREF pins in IGLOO or ProASIC3 low-cost devices.

Use Default Pins for VREFs

Select this check box to set default VREF pins and unset non-default VREF pins. If you unselect this option when setting a new VREF technology, no VREF pins are set. If you unselect this option when default VREF pins are already set, it unsets them.

Click **More Attributes**to set the low-power mode and input delay. (These attributes are not supported in IGLOOe, Fusion, ProASIC3E, or RTAXS devices.)

Click **Apply** to assign the selected I/O standards to the selected bank. Any previously assigned I/Os in the bank that are no longer compatible with the standards applied are unassigned.

See Also

Manually Assigning Technologies to I/O Banks

Assigning Pins in IGLOOe, Fusion, and ProASIC3E

More I/O Bank Attributes Dialog Box

To access this dialog, from the **Edit** menu, choose **I/O Bank Settings**, and then click **More Attributes.**

Use this dialog box to configure these low-power mode settings:

- Enable/disable input/output buffers
- Input delay for a bank

Although designed for high performance, the Axcelerator architecture also allows you to place the device into a low-power (LP) mode via a dedicated LP pin. Asserting the LP pin, which is grounded in normal operation, activates LP mode on all the I/O banks. When LP mode is activated, I/O banks are disabled (inputs disabled, outputs tristated), and PLLs are placed in a power-down mode. All internal register states are maintained in this mode. Furthermore, you can configure individual I/O banks to opt out of the LP mode, giving you access to critical signals while the rest of the chip is in LP mode.

Using the following options in the **More Attributes** dialog box, you can individually configure each I/O bank in an Axcelerator device when in low-power mode:

Low-Power Mode

- **Enable Input Buffers**- Select to enable input buffers. If this option is selected, all used input buffers within this bank will remain enabled whether or not the LP pin is asserted.
- **Enable Output Buffers** - Select to enable output buffers. If this option is selected, all used output buffers within this bank will remain enabled whether or not the LP pin is asserted.

Input Delay

Drag the slider bar to your desired delay. The delay is bank-specific. The delay code and typical value appear. Click **View All Delays** to see all the delay values (Best, Worst, Typical, Rise-Rise, Fall-Fall) for the input delay selected. You must select a technology to see the input delays.

Note: The Low-Power mode option is not supported in the IGLOO (all devices), ProASIC3 nano, ProASIC3L, Fusion and RTAX-S families.

For more information, refer to the datasheet for your device. Datasheets are available from the Actel web site.

Logic Instance Properties Dialog Box

Use this dialog box to display the properties assigned to the selected instance.

Name

Displays the name of the selected logic instance.

Location

Displays the x and y coordinates of the location of the instance.

Region Constraints

Displays the names of the regions to which the selected logic instance is constrained. NONE means the instance is not constrained to a region.

Cell Name

Displays the name of the associated cell.

Netlist

Displays the name of each pin, net, and instance in the netlist to which the logic instance belongs.

More Active Lists Dialog Box

Use this dialog box to open, create, copy, edit, or delete an active list.

Note: You cannot edit or delete the Actel-predefined active lists.

New

Displays the Create or Edit Active Lists dialog box in which you can create a new active list.

Edit

Displays the Create or Edit Active Lists dialog box in which you can modify the properties of an existing active list.

Copy

Displays the **Save List Copy As** dialog box, in which you enter a name for your new active list. This list will contain the same properties as the active list being copied. You can then create a new active list by modifying the properties of the existing one.

Delete

Deletes the selected active list.

Net Properties Dialog Box

Use this dialog box to display the properties assigned to the selected net.

Name

Displays the name of the selected net

Type

Displays the type of the selected net

Location

Displays the x and y coordinates of the location of the net

Status

Displays whether the selected net is connected

Click the **Routing** button to display the Routing Details dialog box.

Click the **PinList** button to see to display the PinList dialog box, which displays a list of pin assignments with their locations.

Path Properties Dialog Box

Use this dialog box to display the properties assigned to the selected net.

Name

Displays the name of the selected path. You can change the name of this path by typing a new name over the existing one in this field.

Delay

Displays the maximum number of milliseconds between the specified ports on a path

Connections

Displays the instances and pins that exist in the selected path

Block Port Properties Dialog Box

Use this dialog box to display the properties assigned to the selected block port.

Name

Displays the name of the selected block port

Net

Displays the net to which the block port is connected

Direction

Indicates whether the block port is an input, output, or InOut port

Fanout

Displays the fanout value of the net

Connections

Displays the names of instances assigned to the block port

PinEditor Properties Dialog Box

Use this dialog box to bring the selected macro or module into view in the PinEditor window.

Move the Display to Show Selected Macro or Module

Check this box to bring a macro or module into view when you select it in the PinEditor window. Uncheck this box if you do not want PinEditor to change your viewing area each time you select a macro or module.

Pin List Dialog Box

Use this dialog box to display the names and locations of pins assigned to the selected net.

Net

The name assigned to the selected net.

Pin

The name of each pin assigned to the selected net.

Location

The x and y coordinates of the current location of the pin on the selected net.

In the following example, the net usw1/U0/NET1 includes two unassigned pins.

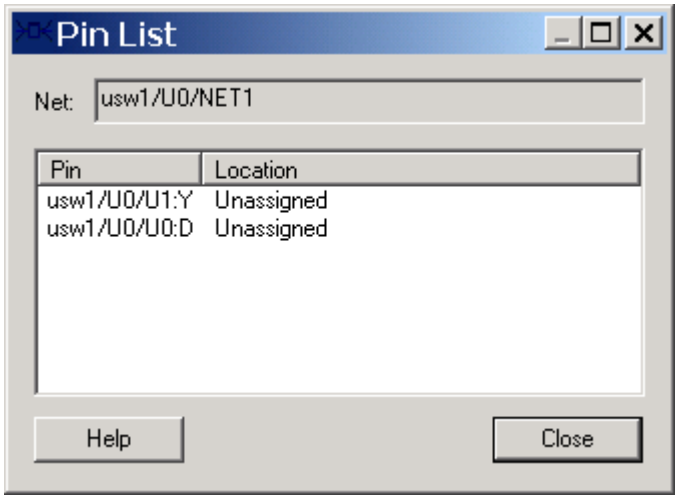


Figure 69 · Pin List Dialog Box

Region Properties Dialog Box

Use this dialog box to display the properties assigned to the selected net.

Region Name

Displays the user-defined name of the selected region

Region Type

Displays the selected region's type

- Inclusive - the place-and-route tool can place logic within the region
- Exclusive - the place-and-route tool cannot place logic within the region (supported only for IGLOO, Fusion, and ProASIC3 families)
- Empty - the place-and-route tool will not place any logic within an empty region; however, the routing resources within the region can be used

Constrain Routing

Note: Note: This option only applies to IGLOO, Fusion, and ProASIC3 families.

Selecting the **Constrain routing** option specifies that routing will be constrained, in addition to the placement. The constrain routing behavior is further influenced by the selected Region type.

Region Type	Conditions
Inclusive	An inclusive routing region is an inclusive placement region (rectilinear area with assigned macros) along with the following additional constraints: • For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resource which is outside the region or crosses the region boundaries). • Nets not internal to the region can be assigned routing resources within the region.
Exclusive	An exclusive routing region is an exclusive placement region (rectilinear area with assigned macros) along with the following additional constraints: • For all nets internal to the region (the source and all destinations belong to the region), routing must be inside the region (that is, such nets cannot be assigned any routing resource which is outside the region or crosses the

Region Type	Conditions
	region boundaries). • Nets without pins inside the region cannot be assigned any routing resource which is inside the region or crosses any region boundaries.
Empty	An empty routing region is an empty placement region, and no routing is allowed inside the empty region. However, local clocks and globals can cross empty regions.

Over-constrain Placement for Routability

When **Constrain routing** is selected, an additional option to **Over-constrain placement for routability** becomes available. Selecting this option contracts or expands the size of a placement region, depending on the region's type. This usually creates a tighter placement region. For example, a normal MxN Inclusive placement region would shrink to (M-2)x(N-2). On the other hand, the prohibited region for external nets of Exclusive and Empty Region types would expand to (M+2)x(N+2).

Region Color

Displays the color assigned to the selected region. You can change this color by choosing a different color from the drop-down color box. You can also create a custom color by choosing **Other** from the drop-down color box. Changing a region's color does not change the color of existing regions of that type. It only changes the color of newly created regions of the selected type.

Region Extents

Displays the location and size of the selected region on the chip.

- Origin - The x and y coordinates of the region's location
- Width - The number of pixels extending horizontally from one end of the region to the other
- Height - The number of pixels extending vertically from one end of the region to the other

Note: You cannot use this dialog box to change a region's size. To change a region's size, select the region in the ChipPlanner window, and then drag a corner of it to the right or left to change its width. Drag a corner of the region up or down to change its height.

Resource Usage

Displays a table indicating the number of the resource, an icon depicting its graphical representation, its name, and the percentage of the regions placed in the design (for example, if a region has 100 core cells and 50 of them are placed, then the resource usage is 50% for the core cells).

Click the **Assignment** button to display the **Assign Instances to Region** dialog box.

Reserve Pins for Migration Dialog Box

Use this dialog box to automatically reserve all the pins that are not bonded in a destination device for migration.

Reserve Pins in the Current Device

Displays the name of the device that you are currently targeting for your design that are not bounded in the Target Device. Displays a drop-down list with the names of the available destination devices to which you intend to migrate.

Keep Explicitly-reserved Pins

Select this check box to preserve all pins that you have entered either using PinEditor, I/O Attribute Editor, or a previous PDC file.

The **Keep explicitly-reserved pins** option is ON by default. When this option is OFF, all the explicitly reserved pins are lost. When this option is ON, the pins that you explicitly reserved are merged with the existing pin reservations.

Note: A warning message appears if reserving pins results in unsetting at least one VREF pin or unplacing at least one I/O.

Routing Details Dialog Box

Use this dialog box to display routing information.

Net

The name of the selected net.

See the datasheet for your device for more information.

Designer Block Properties Dialog Box

Use this dialog box to display the properties assigned to the selected block .

Designer Block Name

Displays the block name of the selected instance.

Instance of

Displays the name of the selected block.

Statistics

Displays the total number of locked instances and nets inside of the block. These instances and nets are preserved by Layout. If these instances or nets are modified, a message appears in the Log window.

Product Support

Actel backs its products with various support services including Customer Service, a Customer Technical Support Center, a web site, an FTP site, electronic mail, and worldwide sales offices. This appendix contains information about contacting Actel and using these support services.

Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From Northeast and North Central U.S.A., call **650.318.4480**
From Southeast and Southwest U.S.A., call **650. 318.4480**
From South Central U.S.A., call **650.318.4434**
From Northwest U.S.A., call **650.318.4434**
From Canada, call **650.318.4480**
From Europe, call **650.318.4252** or **+44 (0) 1276 401 500**
From Japan, call **650.318.4743**
From the rest of the world, call **650.318.4743**
Fax, from anywhere in the world **650. 318.8044**

Actel Customer Technical Support Center

Actel staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions. The Customer Technical Support Center spends a great deal of time creating application notes and answers to FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

Actel Technical Support

Visit the Actel Customer Support website (http://www.actel.com/support/search/default.aspx) for more information and support. Many answers available on the searchable web resource include diagrams, illustrations, and links to other resources on the Actel web site.

Website

You can browse a variety of technical and non-technical information on Actel's home page, at http://www.actel.com/.

Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. Several ways of contacting the Center follow:

Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is tech@actel.com.

Phone

Our Technical Support Center answers all calls. The center retrieves information, such as your name, company name, phone number and your question, and then issues a case number. The Center then forwards the information to a queue where the first available application engineer receives the data and returns your call. The phone hours are from 7:00 A.M. to 6:00 P.M., Pacific Time, Monday through Friday. The Technical Support numbers are:

650.318.4460
800.262.1060

Customers needing assistance outside the US time zones can either contact technical support via email (tech@actel.com) or contact a local sales office. Sales office listings can be found at www.actel.com/company/contact/default.aspx.

Actel is the leader in low-power and mixed-signal FPGAs and offers the most comprehensive portfolio of system and power management solutions. Power Matters. Learn more at http://www.actel.com .

Actel Corporation *• 2061 Stierlin Court • Mountain View, CA 94043 • USA*
Phone 650.318.4200 • Fax 650.318.4600 • Customer Service: 650.318.1010 • Customer Applications Center: 800.262.1060

Actel Europe Ltd*. • River Court, Meadows Business Park • Station Approach, Blackwater • Camberley Surrey GU17 9AB • United Kingdom*
Phone +44 (0) 1276 609 300 • Fax +44 (0) 1276 607 540

Actel Japan *• EXOS Ebisu Building 4F • 1-24-14 Ebisu Shibuya-ku • Tokyo 150 • Japan*
Phone +81.03.3445.7671 • Fax +81.03.3445.7668 • http://jp.actel.com

Actel Hong Kong *• Room 2107, China Resources Building • 26 Harbour Road • Wanchai • Hong Kong*
Phone +852 2185 6460 • Fax +852 2185 6488 • www.actel.com.cn

5-02-0003-17/11.10