Designing Clean Analog PLL Power Supply in a Mixed-Signal Environment

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Introduction

Majority of the system-level designs involve a mix of both analog and digital circuit components. In some systems, a single integrated circuit may contain both analog and digital circuit components. For instance, Microsemi's Axcelerator family of FPGA devices contains analog clock-conditioning circuits such as Phase Locked Loops (PLLs) in addition to the digital circuits. In general, analog components operate in the transistor's active region and are very sensitive to disturbances in their supply voltage. Thus, a low-noise analog power supply network is a stringent requirement for the proper operation of these components. Noise caused due to variations in the power supply voltage, can be coupled into the analog portion of the chip and may become amplified along with the desired signal. This can result in processing errors and affect the functionality of the system. This application note discusses some of the issues related to noise contamination of the analog components in a mixed signal environment and provides useful suggestions for designing a clean analog supply to minimize the effects. All suggestions in this document are applicable to both Flash and Axcelerator devices with the exception of "Technique 1: Use of Power Supply Filters" on page 2. The application for Axcelerator and Flash devices in "Technique 1: Use of Power Supply Filters" are slightly different and are described below.

Sources of Power Supply Noise

Digital CMOS circuits consume dynamic switching power. The dynamic current drawn from the power supply leads to frequency-dependent IR (voltage) drops in the V_{DD} and VSS traces of the printed circuit board (PCB). This phenomenon is called ground bounce on the VSS side. The ground bounce is related to the parasitic inductance of the package pins of the integrated circuit (IC), device ground, and system ground. The dynamic current can transform into noise by contributing an amount of voltage equal to V, as per the following equation.

$$V = L\frac{di}{dt}$$

EQ 1

between the system ground and device ground (Figure 1). Since various components may share the V_{DD} and VSS planes or buses as a source of power, any large voltage fluctuations on the PCB may violate the voltage noise rating of these components. Such noise, if not reduced, can produce logical errors and other undesirable effects. The problem is more pronounced if the noise is coupled to the analog portion of a mixed-signal integrated circuit as it can lead to jitter, distortion, and reduced performance of the analog components. It is important to properly separate the digital and analog powers supplies to minimize the noise levels as much as possible in a mixed-signal environment.

Techniques to Reduce Analog Power Supply Noise

Technique 1: Use of Power Supply Filters

For Flash devices, a noise filter between the power supply and the device power pins, as shown in Figure 2 on page 3, can be used to filter out low and/or high frequency differential noise between AVCC and ground that might couple into the device from the digital power pin. This can be implemented by using an inductor, L1, and a large polarized capacitor C3 in parallel with a set of two small ceramic high frequency capacitors C1 and C2.The impedance of inductor L1 is selected to be much greater than that of the analog component, in order to isolate the analog domain from the digital domain at low, medium and high frequencies. This is because L1 is seen as an open circuit at these frequencies. The two small ceramic capacitors need to be placed near the device power pins (less than one inch from PLL power and ground pins). The purpose of the smaller capacitors is to filter the high frequency switching noise, while the purpose of the larger capacitor is to filter out low frequency supply ripple noise. This technique can be combined with "Technique 3: Use Wide Traces for Analog Power" on page 3. Please refer to "Appendix" on page 6 for a sample implementation of such a filter. The analog power supply for Axcelerator devices uses a “floating ground” approach to eliminate noise.Therefore the suggested filter in this section is implemented differently. Please refer to the *Axcelerator data sheet* for the recommended implementation.

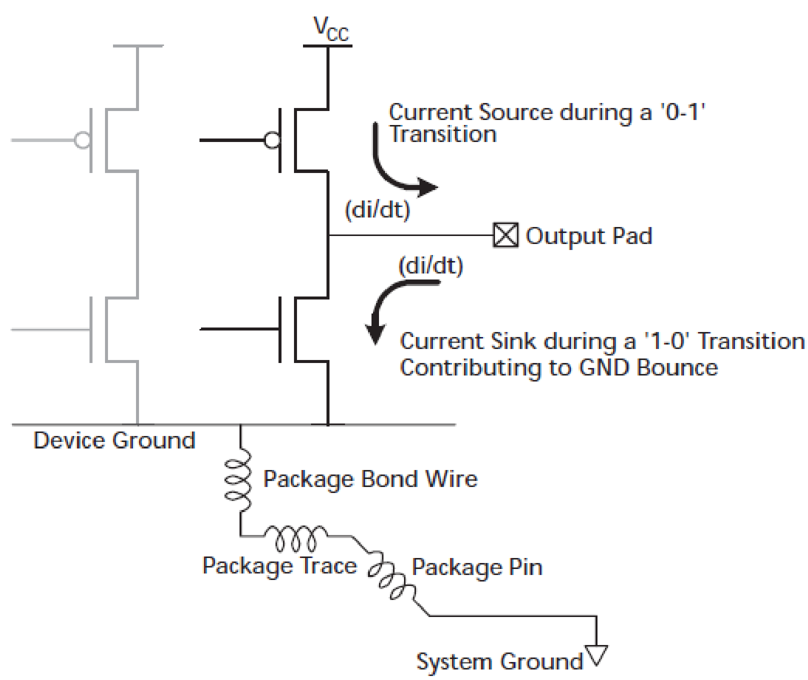

***Figure 1* • Sources of Parasitic Inductance Causing Ground Bounce**

Sample Filter

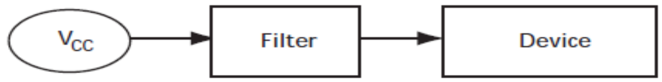

Figure 2 • **Sample Filter**

Contents of the Filter

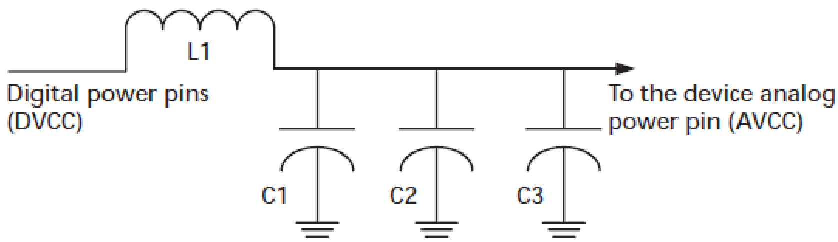

Figure 3 • **Power Supply Filter and Possible Implementation**

Technique 2: Separation of Digital and Analog Supplies with Regulators

'Individual supply outputs must be implemented to supply power to the digital and analog power pins of the device. User can benefit from the inherent higher noise rejection characteristics of the voltage regulators, but it must be verified whether or not the selected regulators provide sufficient rejection. Additionally, the insertion of voltage regulators before the filter can provide isolation of the power between the analog and digital supplies (Figure 2 on page 3), which minimizes the switching noise produced by the digital electronics from interfering with the analog components.

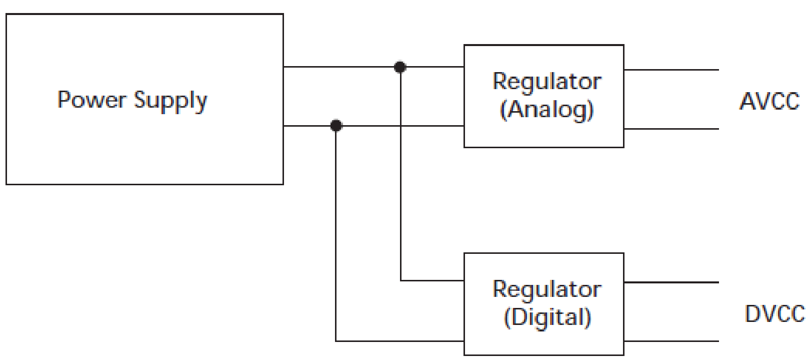

Figure 4 • **Separation of AVCC and DVCC by Means of Power Regulators**

Technique 3: Use Wide Traces for Analog Power

The use of separate planes on the PCB must be implemented for DVCC, DGND, AVCC, and AGND. For the optimum solution, the AGND and the DGND planes must be connected together at the power supply source. This ensures that both planes are at the same potential, and the transfer of noise from the digital to the analog domain is minimized.

This power and ground planes approach allows the use of vias to directly connect the component pins to the GND or V_{CC} planes instead of using traces. As traces become longer, parasitic capacitance, inductance, and coupling noise between neighboring traces increase.

Adding extra layers on the PCB may not always be possible due to cost and other design constraints. For example if the number of analog components is small compared to digital components, it may not be reasonable to dedicate an entire power and ground plane just for the analog components. Instead, a wide trace can be implemented on a signal plane to serve as the analog supply for the analog parts (See Figure 5). This trace is made many times wider than the regular signal traces to minimize the amount of resistance and to have it large enough to be considered a "plane". The same concept can be applied to the analog ground. Another wide trace or island of conducting material positioned close to the analog device in another signal layer can provide the ground "plane". The AGND "plane" must be connected to DGND at the power source to minimize the noise transfer. This approach still allows the use of vias to connect surface-mounted components to the supply and ground.

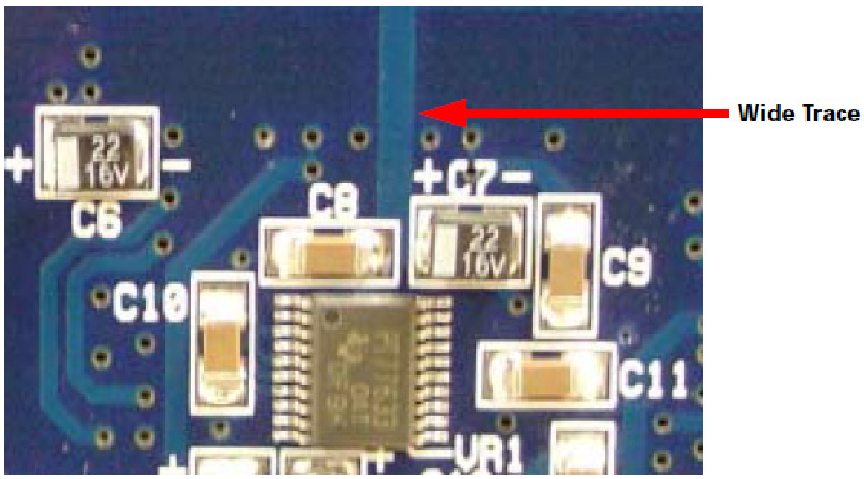

Figure 5 **• Example of Using Wide Traces Instead of an Entire Plane**

Technique 4: Shorten the Current Loops as Much as Possible

In high-speed circuits, the path of the signal current going to ground is always along the path of least inductance. The low inductance path is located directly under the signal's conductor (the PCB trace). Large current loops can increase the signal rise time due to increased parasitic capacitance and contribute to crosstalk or coupling between two conductors.

Adding bypass or decoupling capacitors can shorten the return path from analog and digital V_{CC} to ground and therefore reduce the noise associated with I/O switching. Capacitors with low intrinsic inductance and resistance must be chosen. Place them as close as possible to each of the analog and digital V_{CC} pins to minimize path inductance between the pin and the capacitor. These bypass capacitors provide local energy storage and supply the dynamic current required by the switching circuits. Bypass capacitors must be large enough to supply the required current for a few nanoseconds (ns).

The amount of current the capacitor needs to source depends on the load that the device output is driving and the voltage dips that can be tolerated. EQ 2 shows how to calculate the capacitance required for a device operating at an I/O voltage of 3.3 V with 12 outputs. Each output is driving a 70 Ω load that is assumed to be much greater than the output resistance of the driver.

Total current needed to source is

$$12 \times \frac{3.3V}{70\Omega} = 566mA$$

EQ 2

Assume that, as a requirement of the design, the voltage on the V_{CC} bus cannot drop more than 50 mV, and the capacitor is needed to source this current for 2 ns.

Check the following equation to define current across a capacitor

$$I_c = C\frac{dV}{dT}$$

EQ 3

Where:

I_C = Value of current being sourced by the capacitor (Amperes)

dT = Amount of time the current is sourced for (seconds)

dV = Maximum allowable voltage drop (Volts)

C = Capacitance needed (Farads)

Solving for Capacitance

$$C = I_c\frac{dT}{dV}$$

EQ 4

Substituting the required values into the equation

$$C = (566 \times 10^{-3}s)\frac{2 \times 10^{-9}s}{50 \times 10^{-3}V} = 22.64\mu F = 0.023\mu F$$

EQ 5

Microsemi also recommends using a mix of decoupling capacitors of different sizes to provide proper decoupling across a wide frequency range. For example, 0.1 µF, 0.01 µF, 1000 pF, and 100 pF ceramic capacitors can be scattered throughout to maximize the filtering effects.

Conclusion

Digital systems will continue to run at faster clock speeds which poses a challenge to the system-board designers. Extreme care must be taken in board layouts and filtering circuits to ensure that digital logic does not couple switching noise into the analog domain. The guidelines described in this document, outline some of the areas that board designers need to be aware of while designing a more robust and reliable system, incorporating both analog and digital circuits.

Appendix

The sample scheme presented here uses a 6.8 µH inductor, 10 µF generic electrolytic capacitor, 10 nF and 0.1 µF ceramic high-frequency capacitors to decouple the switching noise. No ground filter is required, since the described LC filter ensures that the voltage difference V(diff) between V(Analog) and V(GND) is constant at any frequency, therefore acting as a filter for both power and ground. In this example, up to three PLLs can be connected to the filtered analog supply as long as the distance of high frequency capacitors can be kept below one inch from each analog supply and ground pin of the device

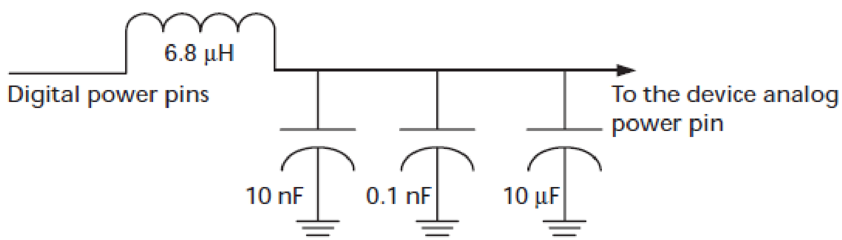

Figure 6 **• Sample Implementation of the Power Supply Filter**

Example of Capacitor and Inductor Selection

Selection for 100 nF Capacitor

- Producer BC components, Type X7R, 100 nF, 16V
- BC components part number: 0603B104K160BT
- Digikey Part number (quantity <10): BC1254CT-ND
- Digikey Part number (quantity >10): BC1254TR-ND

Selection for 10 nF Capacitor

- Surface mount ceramic capacitor
- Producer BC components, Type X7R, 10 nF, 50V
- BC components part number: 0603B103K500BT
- Digikey Part number (quantity <10): BC1252CT-ND
- Digikey Part number (quantity >10): BC1252TR-ND

Selection for 6.8 µH Inductor

- Unshielded surface mount inductor
- Producer Delevan, Q=7.9 at 30 MHz, maximum current
- Delevan components part number: 1210-682J
- Digikey Part number (quantity <500): DN10682JCT-ND
- Digikey Part number (quantity >500): DN10682JTR-ND

List of Changes

The following shows important changes made in this document for each revision

Revision	Changes	Page
Revision 2 (August 2016)	Non-Technical Updates	N/A
Revision 1 (May 2004)	"Technique 1: Use of Power Supply Filters" on page 2 was updated to highlight the differences between Flash and Axcelerator	2
Revision 0 (April 2003)	Initial release	N/A

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