Microsemi SX-A and RTSX-SU Devices in Hot-Swap and Cold-Sparing Applications

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Introduction

Microsemi® Antifuse Field Programmable Gate Array (FPGA)s are nonvolatile, which means that they are live at power-up and do not require a configuration device. This makes the Microsemi chips ideal candidates for hot-swap and cold-sparing applications. With new features suchas pull-up or pull-down resistors, PCI compliance, and slew rate control, the Microsemi's SX-A and RTSX-SU devices are specifically designed to accommodate a variety of power-up and power-down system requirements. These devices are also the first to support both hot-swap and cold sparing. This document discusses in detail the characteristics of these devices during power-up and recommends proper configuration for hot-swap and cold-sparing compliance.

Power-Up Characteristics

Power-Up Sequence

SX-A and RTSX-SU devices by Microsemi can function with any power-up or power-down sequence of power supplies. However, to comply with hot-swap and cold-sparing requirements using SX-A devices, VCCA (array power supply) should come up no less than a diode drop below VCCI (I/O power supply), so deriving the both VCCA and VCCI from the same power supply is recommended.

If VCCA ramps up after VCCI and more than a diode drop below it, outputs may drive to an unknown state for a short period of time during power-up, regardless of power-up resistor settings (Figure 1). This is caused by the propagation delay of an input signal from an input buffer to the output buffer of your design.

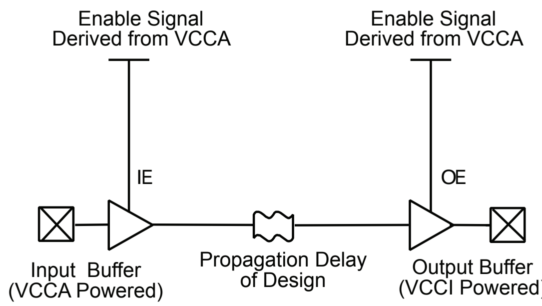


Figure 1 **• SXA Power-Up Circuitry**

RTSX-SU High Standby Current on VCCI

On RTSX-SU devices, if VCC is powered on and VCCA is off, there may be a high standby current on VCCI in the order of 80 mA. This has been closely studied and determined that there are no reliability concerns with this condition. The device can safely remain in this state for 10 years.

I/O State During Power-Up

General Behavior of I/Os

The I/Os of SX-A and RTSX-SU devices are tristated during power-up until the I/Os become active. SX-A requires the recommended power-supply sequencing – VCCA at the same time as or before VCCI. Referto the "Power-Up Sequence" section on page 1 for details. After the I/Os become active, they behave according to your design.

Table 1 summarizes the times at which the I/Os become active during power-up for devices at room temperature with various ramp-up rates. The data assumes a linear voltage ramp up to 2.5 V.

Table 1 • **Power-up Time at which I/Os Become Active**

Ramp Rate	0.25 V/µs	0.025 V/µs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
Units	**µs**	**µs**	**ms**	**ms**	**ms**	**ms**	**ms**	**ms**
A54SX08A	10	96	0.34	0.65	2.7	5.4	12.9	50.8
A54SX16A	10	100	0.36	0.62	2.5	4.7	11	41.6
A54SX32A	10	100	0.46	0.74	2.8	5.2	12.1	47.2
A54SX72A	10	100	0.41	0.67	2.6	5	12.1	47.2
RT54SX32SU	10	100	0.4	0.7	2.8	5.2	13	47
RT54SX72SU	10	100	0.42	0.68	2.6	4.8	11	40

Voltage Spike on RTSX-SU Outputs During VCCI Power-Up

On RTSX-SU devices, the output pin produces an insignificant voltage spike during the VCCI power-up (in between 0 to 650 mV). This voltage spike depends on internal and external pull-up and pull-down conditions. The leakage through the output buffer transistors is very negligible (few micro amps max) due to this spike. Refer to the "Power-Up Resistors" section on page 4 for more information.

RTSX-SU Outputs Driving Low in Certain Configurations

Incase of RTSX-SU devices, Microsemi has observed on certain user designs that outputs without an externally controlled output enable signal may drive low before VCCA and VCCI reach their minimum operational levels.

Note: The internal logic is not guaranteed to be valid under these conditions.

It is good design practice to explicitly disable the outputs until the FPGA completes its power-up initialization with the use of an output enable signal.

The behavior manifests itself as an output that drives low for a period of 400 ns to 500 ns (Figure 2) when the later power supply in the power-up sequence (either VCCA or VCCI) reaches 1.5 V. For logic expected to be high once the power supplies reach their minimum operational levels (on outputs with either internal or external pull-up resistor), the logic module will produce a low signal before it produces the expected signal.

This behavior does not impact the reliability of the RTSX-SU FPGAs.

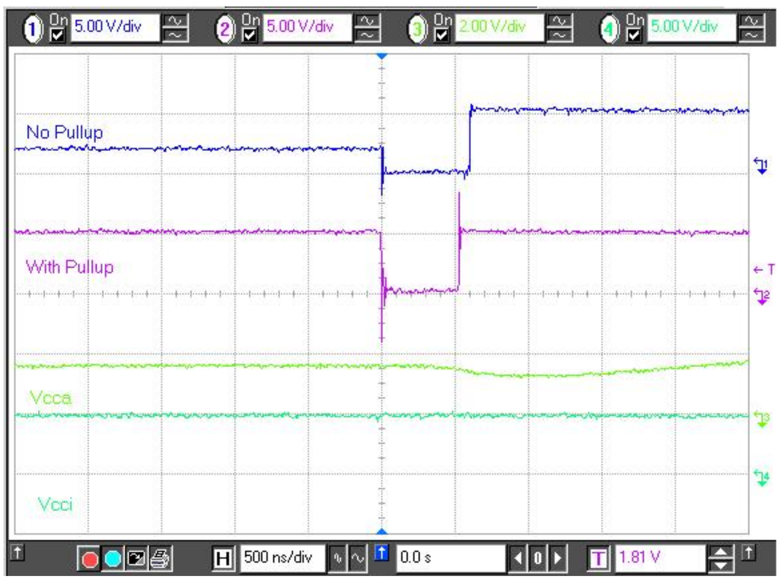


Figure 2 **• Glitch on Outputs with External Pull-up**

Recommended Solution

In order to prevent this behavior during power-up, Microsemi recommends doing either of the following:

- Outputs should be explicitly disabled until the FPGA has completed its power-up initialization. This can be done by using a TRIBUFF macro with its output enable driven low by an input pin.
- Outputs should be pulled low with an external resistor. For outputs configured with internal pull-up which is active during power-up, the external pull-down resistor has to have lower resistance than the internal pull-up (range from 25-35 Kohm) to drive the outputs low.

Note:

- *Using the internal pin to drive enable pin of TRIBUFF is not recommended.*
- *BIBUF can also be used in place of TRIBUFF, if that suites the design requirements. The enable pin of BIBUF should be driven low by the external input pin to make sure that BIBUF is in input mode at power-up.*
- *This power-up glitch is not dependent on VCCA/VCCI power supply sequence.*
- *The current that each I/O sinks is very low because it is on outputs with pull-up transistors, that are in orders of K Ohms. So the current sunk by an I/O is below 5 mA for pull-up resistors higher than 1 Kohm.*

Root Cause of the Low Pulse

The main cause of the glitch is due to the fact that at VCCA/VCCI level of 1.5 V, the functionality of the device is not in a stable condition. Most of the control logic for the device at that level is still being activated. One of the main control logic is the “charge pump” circuit. This circuit generates a signal called “PMPOUT”. This PMPOUT signal drives the isolation transistors for every logic module in the device. Unless these isolation transistors are turned “ON” by the PMPOUT signal, the signal driven by the logic modules will not be able to propagate through the signal path. Both the VCCA and VCCI need to be powered up in order for the charge pump to become activated and output a full level on PMPOUT.

When the supplies are being ramped and below 1.5 V, the PMPOUT level will not be at a high enough level to turn ON the isolation transistors. As a result of this, even if the modules are driving a high signal, that signal will not be at the “Module output” track because the pass devices will not be able to pass the high signal. This results in the outputs driving the “low” signal when a high is expected. When the VCCA/VCCI reach 1.5 V, the PMPOUT becomes high enough to fully turn-on the isolation transistors and drive the expected logic high on the “Module output” track. The duration of the low pulse (glitch) is the time from the outputs becoming active and the PMPOUT reaching a high enough level to enable the isolation transistors. This low pulse (glitch) duration depends on the VCCA/VCCI ramp rate as well as the location of the output with respect to the logic module thatis driving it.

Since the 1.5 V level on VCCA is not at full nominal condition, the logic modules will be slow to produce the expected signal. Figure 4 shows a simplified schematic of the logic modules and the control circuit.

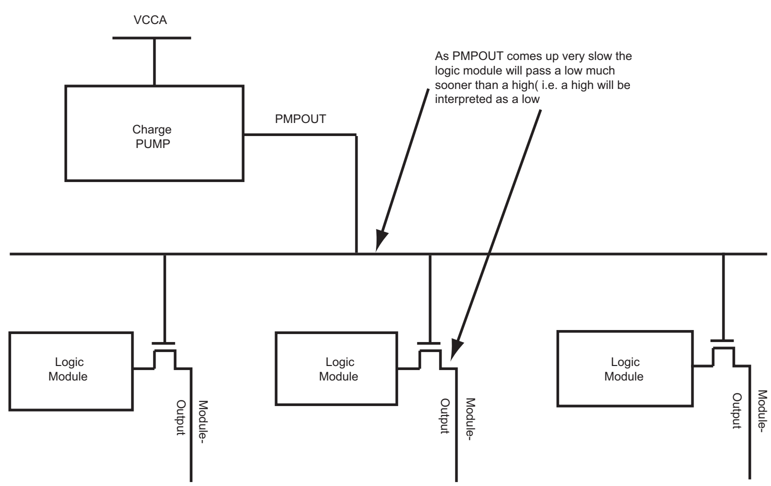


***Figure 3* • Simplified Schematic of the Charge Pump and Isolation Transistors**

HCLK Activation Delay

The RTSX-SU, SX-A, and eX devices contain an HCLK Reset Synchronizer circuit. HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the design software and the pin must be tied to GND on the board. For more information on HCLK Reset Synchronizer circuit, refer to the *Global Clock Networks in Microsemi SoC Products Group Antifuse Devices* application note.

Power-Up Resistors

All SX-A and RTSX-SU devices are equipped with optional pull-up or pull-down resistors of about 50 k that are enabled during power-up. Just slightly before VCCA reaches 2.5 V, these resistors are disabled so the I/Os will behave normally (Figure 3). When using these resistors, consider that on SX-A devices, the risk of an I/O driving a temporary unknown state towards the end of the power-up sequence still remains when VCCI is powered up before VCCA (this glitch is discussed in the "Power-Up Sequence" section on page 1).

The resistors cannot override this phenomenon. When VCCA is powered-up first, outputs will drive according to your design when the resistors are disabled.

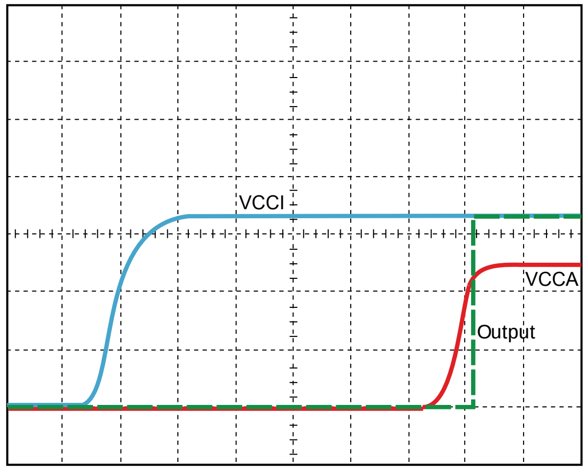


Figure 4 **• SX-A Scope Plot of Actual Output Behavior During Power-Up with Active Pull-Down Resistor**

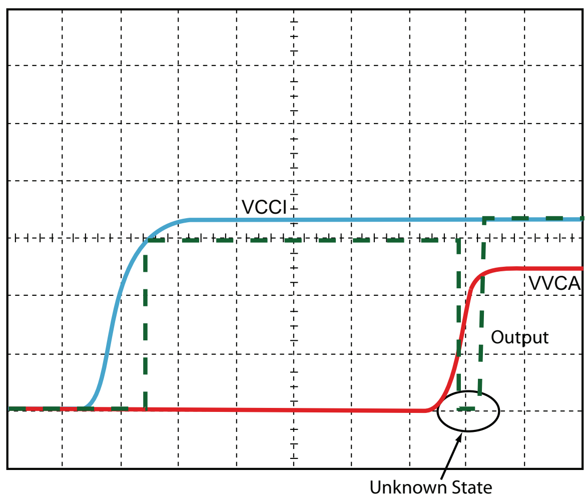


Figure 5 **• SX-A Output Driving to Unknown State with Pull-Up Resistor**

However, as mentioned in "Voltage Spike on RTSX-SU Outputs During VCCI Power-Up" section on page 2 may be observed on the output pin depending on pull-up/down (internal and/or external) resistors. The spike is higher, if the VCCI is ramping up alone and an external resistor (~ 1 MΩ) is used. Table 2 summarizes the voltage spike data.

Table 2 • **RTSX-SU Output Spike Characteristics**

Power Supply Condition		Internal Power-On Resistor Selected		External Resistor 1 M		Voltage Spike on Output Pin (mV)
VCCI[1]	VCCA[2]	Pull-Up	Pull-Down	Pull-Up	Pull-Down	
Ramping	GND	-	Yes	Yes	-	500
Ramping	GND	Yes	-	-	Yes	Output Drops to 2.5 V
Ramping	GND	-	-	-	-	225
Ramping	GND	Yes	-	-	-	Output Drops to 2.5 V
Ramping	GND	-	Yes	-	-	100
Ramping	On	-	-	-	-	200
Ramping	On	-	Yes	-	-	100
Ramping	On	Yes	-	-	-	1200

Note:

1. *VCCI = 3.3 V.*
2. *VCCA = 2.5 V.*
3. *Dash(-) means not used.*

Root Cause of the Spike on RTSX-SU Outputs

The voltage spike in the output pin during power-up can be explained as follows:

The inverted buffer at the output of the pad depends on Pull-Up and Pull-Down transistors driven by the core (Figure 6 on page 6). These transistors are connected to GND and VCCI.

When VCCI starts ramping up, the internal circuitry driving Pull-Up and Pull-Down are still in a floating state until VCCI reaches 650 mV. During this transition, Pull-Up has a dip to ground that produces the voltage spike on the PAD.

The power-up resistors are available for all I/O standards. Microsemi recommends to use this feature only for output signals. You are allowed to assign a power-up state to inputs that will be seen by inputs during, but not after power-up.

Therefore, since the time at which the power-up state becomes disabled is variable, it is difficult to prevent a floating input condition, which can cause unknown values to be input through an I/O.

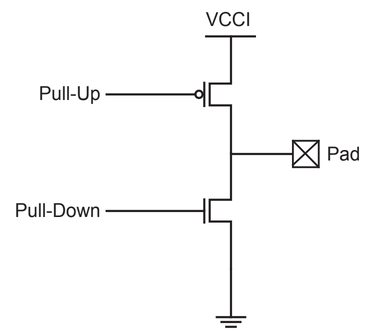
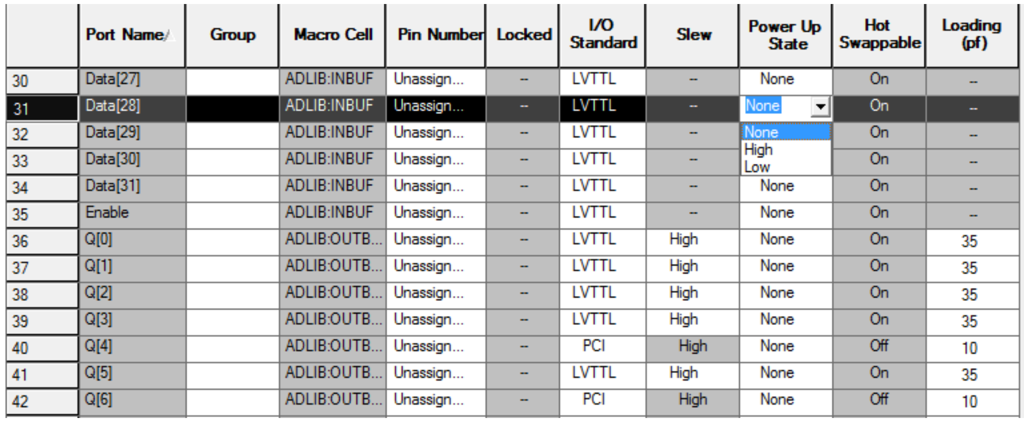


Figure 6 • **Output Pad Buffer Schematic**

The pull-up and pull-down resistors can be enabled in the designer software in the I/O Attribute Editor tool on an individual basis (Figure 7).



	Port Name	Group	Macro Cell	Pin Number	Locked	I/O Standard	Slew	Power Up State	Hot Swappable	Loading (pf)
30	Data[27]		ADLIB:INBUF	Unassign...	--	LVTTL	--	None	On	--
31	Data[28]		ADLIB:INBUF	Unassign...	--	LVTTL	--	None	On	--
32	Data[29]		ADLIB:INBUF	Unassign...	--	LVTTL	--	None	On	--
33	Data[30]		ADLIB:INBUF	Unassign...	--	LVTTL	--	High Low	On	--
34	Data[31]		ADLIB:INBUF	Unassign...	--	LVTTL	--	None	On	--
35	Enable		ADLIB:INBUF	Unassign...	--	LVTTL	--	None	On	--
36	Q[0]		ADLIB:OUTB...	Unassign...	--	LVTTL	High	None	On	35
37	Q[1]		ADLIB:OUTB...	Unassign...	--	LVTTL	High	None	On	35
38	Q[2]		ADLIB:OUTB...	Unassign...	--	LVTTL	High	None	On	35
39	Q[3]		ADLIB:OUTB...	Unassign...	--	LVTTL	High	None	On	35
40	Q[4]		ADLIB:OUTB...	Unassign...	--	PCI	High	None	Off	10
41	Q[5]		ADLIB:OUTB...	Unassign...	--	LVTTL	High	None	On	35
42	Q[6]		ADLIB:OUTB...	Unassign...	--	PCI	High	None	Off	10

***Figure 7* • Setting Power-Up State in the I/O Attribute Editor Tool**

Transient Current

During power-up of the SX-A and RTSX-SU devices, a built-in initialization sequence turns off isolation devices inside the FPGA. These isolation devices are only used during programming to protect the logic array and I/Os from high programming voltages. When the isolation devices are disabled, the array and I/O logic modules are enabled simultaneously, causing a large transient current to exist for approximately 500 ns on the VCCA plane.

The device I/Os will remain tristated during this time. The duration and the time of occurrence of this current pulse will vary depending on the ramp rates of the power supplies as well as the maximum value of this current. Current values have been measured for several different power-up rates under typical operating conditions (room temperature, VCCA at 2.5 V).

The results are summarized in Table 3. The transient current will occur during the ramp up of VCCA just slightly before the point at which the I/Os become active.

***Table 3* • Typical Peak Transient Current on VCCA (mA)**

Ramp Rate	0.25 V/µs	0.025 V/µs	5 V/ms	2.5 V/ms	0.5 V/ms	0.25 V/ms	0.1 V/ms	0.025 V/ms
A54SX08A	162	125	61	51	41	50	46	45
A54SX16A	247	267	159	104	46	34	74	56
A54SX32A	440	430	340	236	116	97	73	72
A54SX72A	557	549	353	232	108	92	73	66
RTSX32-SU	408	310	335	352	228	206	180	144
RTSX72-SU	790	789	544	408	208	224	244	231

Hot-Swap Compliance

Hot-swapping, to quote the PCI Industrial Computer Manufacturers Group, is the "orderly insertion and extraction of boards without adversely affecting system operation." This section summarizes the ability of Microsemi parts to operate in hot-swap environments. Originally the PCI SIG issued a Hot Plug Specification in 1997. This has been largely supplanted by the Compact PCI Hot-Swap Specification (dated August 3, 1998). Version 2.0, dated January 17, 2001 is the latest revision. PCI Industrial

Computer Manufacturers Group (PICMG's) hot-swap is a more comprehensive specification, and the remainder of the document will refer to that specification as the "Hot-Swap Specification." The PCI SIG makes a subtle distinction by saying that software support is standardized for hot-swap but up to the user in hot plug. Silicon requirements are the same for both.

Microsemi's SX-A and RTSX-SU families provide support for hot-swap according to the Compact PCI specification. These FPGAs do not have to be configured as PCI compliant to satisfy these hot-swap requirements.

Hot-Swap Silicon Requirements

The Hot-Swap Specification defines three levels of compatibility that silicon vendors may use to claim compliance:

- Silicon Requirements for hot-swap compliant boards
- Requirements for hot-swap silicon
- Recommended features for hot-swap silicon

Implementation in a Hot-Swap Compliant Board is by far the most important for a programmable-logic device. All of these requirements cannot be met with external circuitry alone. The required features are described in the following subsections. Hot-swap silicon includes all features needed for hot-swap compliant boards plus software registers in PCI configuration space (support for software connection control) and support for device hiding. Although the basic Microsemi silicon does not include such features, Microsemi's CorePCI macros do, as described in detail below.

The final class, Recommended Features, encompasses all requirements for hot-swap silicon plus support circuitry for voltage precharge, early power, and the 64EN# signal. Version 2.0 of the Hot-Swap Specification has also added optional Initially Not Responding silicon support.

Silicon Requirements for Hot-Swap Compliant Boards

The silicon requirements are as follows:

- PCI specification 2.1 (or later) compliant
- Toleration of VCC from early power
- Asynchronous reset
- Precharge voltage toleration
- Modified I/O buffer V/I requirements
- Limited I/O pin leakage

PCI Specification 2.1 (or later) Compliant

The PCI device buffers must meet the AC specifications for 5.0 V or 3.3 V signaling. Input buffers require a clamping diode to ground. The clamp to VCCI is optional in a 5.0 V system, whereas in a 3.3 V only system, the clamp is required (the power supply is the system power supply of 3.3 V). In addition, a clamp diode to a power rail must be able to withstand short-circuit current until the drivers can be tristated

(Figure 8).

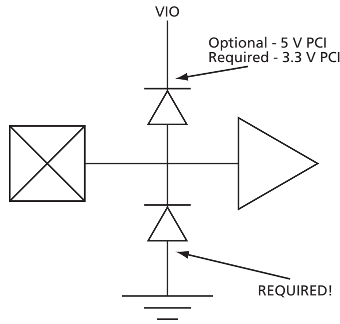


***Figure 8* • Hot-Swap PCI Input Buffer with Clamp Diodes**

In the Microsemi SX-A and RTSX-SU parts, selection of the clamping diode to VCCI is fuse-programmable.

There are additional requirements associated with Revision 2.2 of the PCI Specification. The PCI buffers must be in a high-impedance state when the device reset is asserted. This is required in Revision 2.2 of the spec, but may not be the case in Revision 2.1. The Microsemi devices are compliant with this revision.

In addition, after RST# is released and before the device completely responds to a PCI cycle, Revision 2.2 specifies that the device is either Initially Not Responding or Initially Retrying. The Microsemi devices are in the former category, which is preferred for hot-swap compliance.

The output buffers use a slightly different V/I curve for hot-swap as discussed in the "Modified I/O Buffer V/I Requirements" section on page 11. Microsemi SX-A and RTSX-SU devices fully comply with this requirement.

Toleration of VCC from Early Power

The early power pins supply the power for the I/O circuit during physical insertion. These can be limited using a series register, so the maximum 5.0 V and 3.3 V supply currents during insertion may be somewhat lower than during normal operation of the card. Power-up and power-down are controlled in the Compact PCI environment using boards with unequal-length pins.

The insertion/power-up process consists of the following steps (unimportant steps from a silicon point of view have been eliminated):

- The board is in the "not-installed" state.
- Board installation begins.
- The board's logic ground is discharged to chassis ground through a bleed resistor.
- The bleed resistor breaks contact with chassis ground. Logic ground is again isolated.
- The board contacts long pins on the backplane first. These are for ground, +5.0 V, +3.3 V, and VCCI. The board is in an unstable state when pins are first mated.

  Note:This condition typically lasts less than 4 ns, but could be much longer.
- Enough pins are connected to achieve stable early power. Compact PCI bus interface logic is powered up and decoupling capacitors attached to early power are charged. The device's PCI reset signal is driven active and is asserted throughout the connection process.
  The device asynchronously tristates all PCI signals. Early power stabilizes all of the CompactPCI bus signals to the signal precharge potential.
- The board contacts the medium-length pins on the backplane, which will make contact in a random manner. The board's Compact PCI pins begin to track the levels on the PCI bus. The board now receives the PCI clock. The medium-length power pins contact and short out the current-limiting resistors.

- The board contacts the short BD_SEL# pin. The board is now fully inserted in the backplane. The precharge potential is now (optionally) removed from each signal, and the board enters the "installed" state.

The SX-A devices use a core voltage of 2.5 V and an I/O voltage of either 3.3 V or 5.0 V. CompactPCI provides 3.3 V and 5.0 V power, but not 2.5 V, which must be derived from one of the other two supplies. Therefore, at power-up there are four possibilities:

VCCI = 3.3 V

- 2.5 V derived from 3.3 V supply (VCCI)
- 2.5 V derived from 5.0 V supply

VCCI = 5.0 V

- 2.5 V derived from 3.3 V supply
- 2.5 V derived from 5.0 V supply (VCCI)

If different power supplies are used to derive the I/O and array voltages, the device may not be hot-swap compliant. Also, even if the Microsemi core and I/O voltages are derived from the same supply, the order of supply power-up is less critical, but it is still possible for the I/O voltage to be applied before the core voltage. Powering the SX-A or RTSX-SU core before or at the same time as the I/O ring is required for hot-swap compliance. Additional power-up information is discussed in the "Power-Up Characteristics" section on page 1. Microsemi SX-A and RTSX-SU devices fully comply with this requirement as long as the I/O voltage is not supplied before the core voltage.

Asynchronous Reset

The device must maintain a high-impedance output until reset is released (this is not the master PCI reset). The bus pins will be live when reset is released, and therefore a requirement exists in which state machines must be able to recover from unknown states. Of course, this should not affect the I/O circuits.

Note: Since the local PCI_RESET# signal is stable before the medium pins are contacted, this signal can be used to tristate the PCI bus signals. In other words, the I/O buffers need not power on in a tristated condition.

Microsemi SX-A and RTSX-SU devices fully comply with this requirement.

Precharge Voltage Toleration

The device must tolerate holding I/O pins at the precharge voltage for an unspecified period. This is not a problem for the I/O buffer itself. However, there is an issue associated with power-up and power-down. The combination of precharge and a power rail at 0 V could cause excessive current draw from two sources. One could be the hot-swap monitoring circuitry; the other is the clamp diode required for 3.3 V PCI.

To avoid a potential problem, the power rail for either 5.0 V or 3.3 V devices MUST be no more than a diode drop below the precharge voltage at all times. The orderly power-up/power-down procedure (with early power pins) specified by the Compact PCI Hot-Swap Specification is highly recommended. If the system complies with this, then SX-A and RTSX-SU devices meet the precharge voltage toleration requirement.

Modified I/O Buffer V/I Requirements

The device's output buffer must have the same characteristics as the standard 5 V PCI output buffer with two exceptions. For pull-down, standard PCI allows low-voltage drive to begin at 0.55 V, while hot-swap PCI requires that drive begin at 0 V. On the pull-up side, standard PCI allows voltage drive to begin at 2.4 V, while hot-swap PCI requires that driving begin at 3.3 V. Microsemi SX-A and RTSX-SU devices fully comply with this requirement.

Limited I/O Pin Leakage

Vp at the device must be adjusted so that I/O pin leakage over all operating conditions is limited to 10 µA. It is a recommendation, not required, that the I/O pin leakage is controlled within even tighter limits. I/O pin leakage in the SX-A and RTSX-SU devices be currently specified at a maximum of 10 µA. Microsemi SX-A and RTSX-SU devices fully comply with this requirement.

Summary of Silicon Requirements for Hot-Swap Capable Boards

Microsemi SX-A and RTSX-SU parts meet the Compact PCI requirements (Revision 1.0 or 2.0) for hot-swap capable boards. Microsemi recommends that all designs follow the Compact PCI Hot-Swap Specification.

If a board does not completely conform to the Hot-Swap Specification, it is recommended that at least the power-up and power-down be controlled as specified in the Hot-Swap Specification. Even if power-up and power-down are not controlled, there is never a problem with 3.3 V PCI operations.

Hot-Swap Silicon

Software/Register Requirements

As a minimum, hot-swap silicon requires a hot-swap control and status register mechanism. The Microsemi PCI Target, Target + DMA, and Target/Master macros implement this feature in accordance with the Hot-Swap Specification. A brief description follows.

The Hot Plug System Driver uses a uniform bit assignment ("Not Used" means reads are undefined and writes should always be 0):

Bit 7 – ENUM# Insertion Status

 1 – ENUM# Asserted

 0 – Not Asserted

Bit 6 – ENUM# Insertion Status

 1 – ENUM# Asserted

 0 – Not Asserted

Bit 5 – Not Used

Bit 4 – Not Used

Bit 3 – LED ON/OFF (the "Blue LED" that indicates it is safe to extract the card)

 1 – LED ON

 0 – LED OFF

Bit 2 – Not Used

Bit 1 – ENUM# Signal Mask

 1 – Mask Signal

 0 – Enable Signal

Bit 0 – Not Used

The accessing of the hot-swap control and status register is through two levels of indirection. First, Bit 4 of the regular PCI status register (address 04h) is set to indicate the presence of a capabilities list. If that bit is set, then register 37h in the configuration header indicates the location of the first item in the linked list. The two least significant bits must be zero (the offset is DWORD aligned). This address would point to the hot-swap register block.

In the case of an Microsemi PCI macro, register 37h contains 80h. The macro implements the following register block in configuration space:

80h – Reserved

81h – Hot-Swap Control and Status Register

82h – Next Item in Capabilities List (a dummy location in our case)

83h – 06h (indicates hot-swap capability)

Revision 2.0 of the Hot-Swap Specification includes a provision for device hiding support. This is not yet incorporated in Microsemi's PCI macro.

Summary of Hot-Swap Silicon Features

Although an unprogrammed Microsemi FPGA does not contain hot-swap silicon features, these PCI-specific features are part of the Microsemi PCI macros, so an FPGA that includes the macro will satisfy Revision 1.0 of the Hot-Swap Specification's requirements for hot-swap silicon features. Support for device hiding will be incorporated in a future release of Microsemi's PCI macro.

Recommended Hot-Swap Silicon Features

Microsemi Antifuse devices do not currently support any of the optional hot-swap silicon features. Such circuitry should be implemented outside of the Microsemi Antifuse devices, although a portion of the control circuitry can be done using programmable logic.

Cold Sparing

As discussed in the "Power-Up Sequence" section on page 1, the I/Os of SX-A and RTSX-SU devices can be tristated during power-up. Cold-sparing applications rely on this silicon feature. In cold sparing, voltage may be applied to an I/O before and during power up of a device. When the device is powered off, both VCCA and VCCI must be clamped to the ground. This will prevent the power supplies from experiencing residual voltage when a voltage is applied to the inputs in a cold-sparing condition. The 3.3 V PCI mode can be used provided there is no power present in VCCI. There is a pass transistor which is enabled by VCCI, creates a direct path between clamp diode and VCCI. Then the clamp diode will be forward biased and eventually power up the device.

When these conditions are met, you can safely drive any I/O of an unpowered device, with less than 100 µA of leakage current. It is a good design practice to not use outputs of an unpowered (or partially powered) SXA or RTSX-SU FPGAs to drive other components in the system. Designers should wait for the SXA and RTSX-SU FPGAs to finish their power-up initialization first. Refer to the "Driving an Unpowered Device" section on page 12, for recommended software settings to enable cold sparing.

As in hot-swap applications, there will be a delay from the time at which the I/Os become active during power-up to the time at which data will be valid at the output pins (Figure 1 on page 2). This delay can be determined through timing analysis of the critical path from the input pin to the output pin.

Driving an Unpowered Device

In hot-swap and cold sparing applications, the array can inadvertently consume power even if neither VCCA nor VCCI is powered. This is caused by external driving of a tristated I/O, which can forward-bias the clamp diode and power-up a portion of the array. To avoid this, the clamp diode should always be disabled in Microsemi's Libero software. This means avoiding the choice of PCI for the I/O standard. If high slew is still required, choose the LVTTL I/O standard option and select HIGH for slew.

Note: The hot-swap box will indicate on, that states the clamp diode is not used.

Driving Unused I/Os

If unused I/O pins are connected on the board (for future use) that are driven by another device while the device is in an unpowered state, select Disable Clamping Diode for Unused I/O Pins in the Generate Programming Files dialog box, as shown in Figure 9.

This feature also disables the clamp diodes on the JTAG input pins. This is necessary because in case of VCCI losing power, the clamp diode could affect the system bus operation.

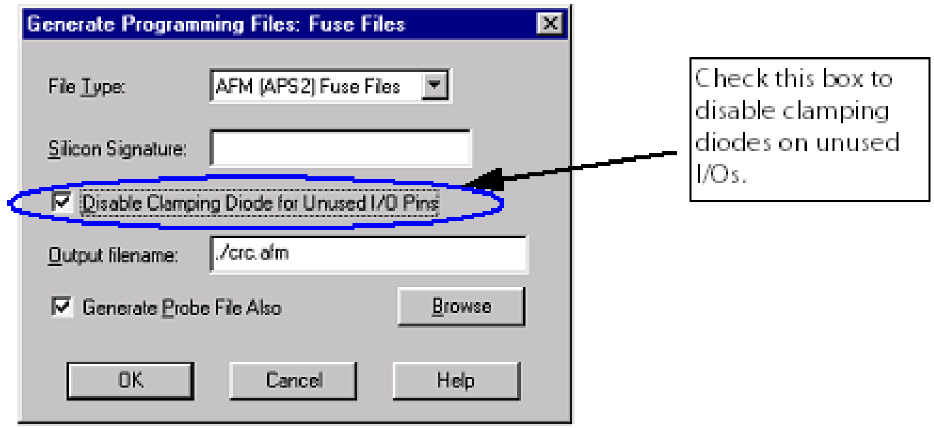


Figure 9 **• Generate Programming Files: Fuse Files (Disable Clamping Diodes on Unused I/Os)**

Conclusion

The Antifuse FPGAs provide an excellent solution for commercial and aerospace applications that require high performance, low power consumption, low cost, and exceptional reliability. The SX-A and RTSX-SU families adds the benefits of power-up friendly silicon that supports both cold sparing and hot-swap.

No power-up or power-down sequence is required for the devices to operate correctly. To take advantage of cold-sparing and hot-swap features, follow the recommendations described in this document.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 3 (September 2012)	Replaced Output with I/O in "Driving an Unpowered Device" section (SAR 38986).	12
Revision 2 (October 2011)	Updated Table 1 (SAR 32793).	2
	Replaced RT54SX-S with RTSX-S, changed the template, added a new Table 2 and Figure 5 (SAR 34148).	6
Revision 1	Initial draft	

Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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