Designing a Web Server System Using CoreMP7

Introduction

The Actel CoreMP7 processor is a soft IP version of the popular ARM7TDMI-S™ that has been optimized to maximize speed and minimize size in Actel Flash-based FPGAs. The combination of the ARM7TDMI-S microprocessor and an FPGA enable the users to quickly design ARM7 systems and add new features to an existing system, without the high cost of the traditional ASICs. One type of application is adding network connectivity to a system. This application brief provides an overview of the web server system that can be created using the CoreMP7 devices.

Overview

The web server system consists of a hardware component and a software component.

Hardware Component

The web server system has the following hardware components:

- M7 device—CoreMP7 microprocessor
- Memory controller
- Ethernet Media Access Controller (MAC)
- 10/100 PHY device
- Flash memory
- SDRAM

M7 Devices

The M7 family of FPGAs is the main engine of the web server. The CoreMP7 microprocessor, the memory controller, and the Ethernet MAC are all programmed into the M7 devices. Because the M7 device is an FPGA, the user can add functions to the device by reprogramming, eliminating the need to re-spin the silicon or the printed circuit board (PCB).

CoreMP7 Microprocessor

CoreMP7 is a soft IP-core implementation of the popular ARM7TDMI-S microprocessor. The CoreMP7 microprocessor has the following features:

- 32-bit ARM instruction set for maximum performance and flexibility
- 16-bit Thumb® instruction set for increase code density
- Unified bus interface
- 3-stage pipeline
- 32-bit ALU
- Fully static operation

More information regarding the CoreMP7 microprocessor can be found in the *CoreMP7* datasheet.

Memory Controller

The memory controller is used to read and write off chip memories.

Core10/100 Ethernet MAC

The Core10/100 Ethernet MAC is a high-speed MAC Ethernet controller. It implements Carrier Sense Multiple Access with Collision Detection defined by IEEE 802.3 for media access control over an Ethernet connection to communicate over the network. Communication with an external host is implemented via a set of Control and Status Registers and the DMA controller for external shared RAM memory. For data transfers, Core10/100 operates as a DMA master. More information regarding the Core10/100 can be found in the *Core10/100* handbook.

10/100 PHY

The 10/100 PHY device provides the physical communication over the network.

Flash Memory

The Flash memory is used to store the web server program and possibly the web pages.

SDRAM

The SDRAM memory is used as the program memory. The components are connected as shown in Figure 1.

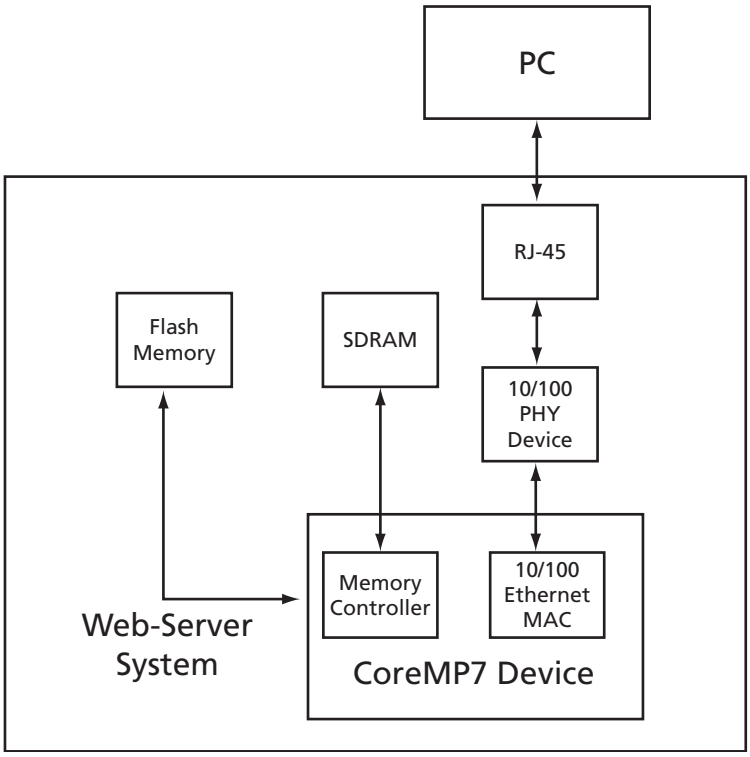

Figure 1 • **Web Server Block Diagram**

Software Component

The software component is a program that runs on CoreMP7. The heart of the program is the Internet Protocol suite, also know as the TCP/IP suite. In a protocol stack, each layer solves a set of problems involving the transmission of data, and provides a well-defined service to the higher layers. Higher layers are logically closer to the user and deal with more abstract data, relying on lower layers to translate the data into forms that can eventually be physically manipulated.

The TCP/IP protocol is normally considered to be a four-layer system as shown in Table 1.

Table 1 • **TCP/IP Protocol System Layers**

Application	HTTP, FTP, Telnet
Transport	TCP, UDP
Network	IP, ICMP
Link	Device drivers, Interface card

Application Layer

The application layer is the layer that most network programs use in order to communicate across a network with other programs. Each network-aware application passes data to each other, using a format that is internal to each application. The data has to be encoded into a standard format before being passed down to the next layer of the stack. The applications in the application layer provide services that directly support user applications.

Transport Layer

The transport layer handles the reliability of the transmission and ensures that the data arrives in the correct order. The transport protocols also determine for which application any given data is intended.

Within the transport layer, there are several protocols:

- TCP is a reliable, connection-orient, transport mechanism providing a reliable byte stream. This protocol ensures data arrives complete, undamaged, and in order.
- UDP is a connectionless datagram protocol. It is an unreliable protocol because it does not verify that packets have reached their destination and does not provide any guarantee that they will arrive in order.

Network Layer

The network layer transports the data (also known as packets) from the source network to the destination network. The most commonly used protocol is the Internet Protocol (IP). IP can carry data for a number of different higher-level protocols.

Link Layer

The link layer specifies the physical characteristics of the communication. The link layer normally includes the device driver. This layer handles the hardware details of physically interfacing with the cable.

Encapsulation

When an application sends data through the network, the data is sent down the protocol stack, through each layer, until it is sent as a stream of bits across the network. Each Layer adds information to the data by adding headers and trailers to the data it receives. Figure 2 shows this process.

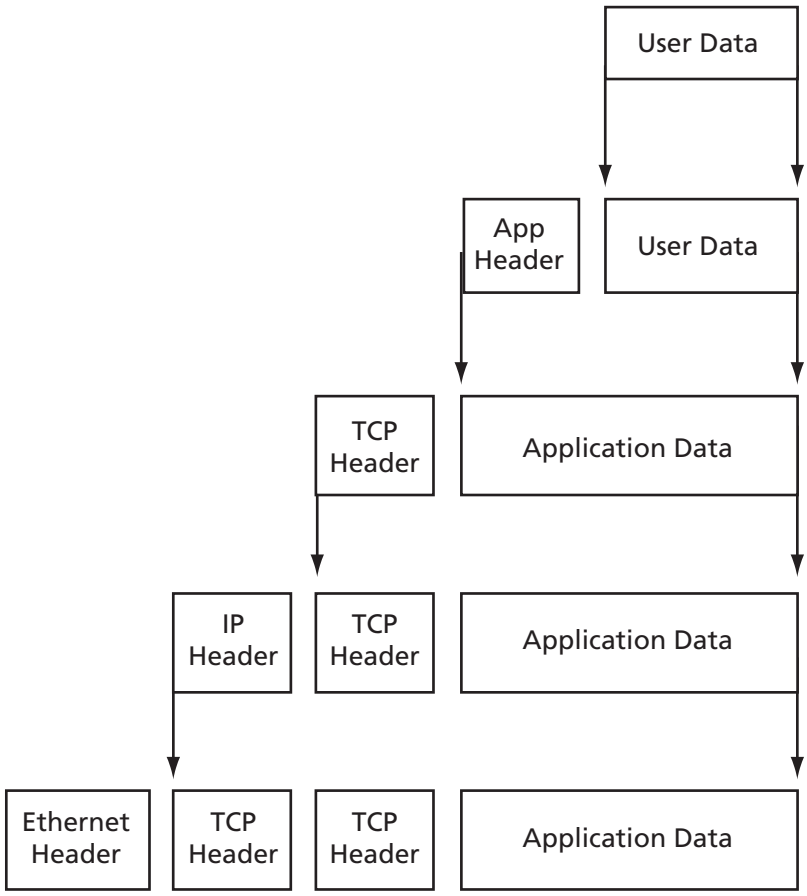

Figure 2 • **TCP/IP Packet Encapsulation**

Security

The M7 devices are based on the ProASIC3 and ProaASIC3E devices, which have been designed with the most comprehensive programming logic design security in the industry. The M7 devices incorporate the Advanced Encryption Standard (AES) decryption core to provide leading-edge security in a programmable logic device. Any M7 configuration data will be automatically encrypted (by Actel's Designer software) and can only be decrypted within M7 device prior to being written to the FPGA core. The AES decryption key is stored in on-chip, nonvolatile Flash memory, and is set by Actel and cannot be changed by the user.

Conclusion

The CoreMP7 processor allows system designers to quickly design and modify ARM7TDMI-S systems at a much lower cost than traditional ASICs. The ability to reprogram the CoreMP7 into an M7 device enables the designer to rapidly prototype, test, and manufacture a system, greatly reducing the time to market. The CoreMP7 and the designer's IP are protected by a 128-bit AES key, ensuring that the design is safe from would be IP thieves.

Related Documents

Datasheets

CoreMP7

http://www.actel.com/ipdocs/CoreMP7_DS.pdf

Handbooks

Core10/100

http://www.actel.com/ipdocs/Core10100_hb.pdf

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