

# Axcelerator I/O Selection Guide

## Introduction and Feature Summary

The Axcelerator family offers I/O features to support a very wide variety of user designs. An outline of the features is as follows:

- Support for multiple I/O specs
- Mixed-voltage operation – 1.5V, 1.8V, 2.5V, 3.3V
- Bank-Selectable I/Os – 8 Banks per Chip
- Registered I/O
- DDR Operation
- Hot-Swap Compliant I/Os
- Programmable Slew Rate, Output Drive, and Input Delay
- Integrated Pull-Up and Pull-Down Circuits
- Boundary-Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)

This I/O Selection Guide is intended to give designers an overview of the supported standards and features as well as performance information. Details on configuration of I/Os are provided in the *I/O Features in Axcelerator Family Devices* application note.

## Supported I/O Standards – A Quick Look

Fourteen different I/O standards are supported in three basic groups:

- Single-ended – LVTTTL, 3.3V PCI/PCI-X, LVC MOS (2.5V, 1.8V, and 1.5V)
- Voltage-referenced – GTL+, SSTL2 Classes I/II, SSTL3 Classes I/II, HSTL Class I
- Differential – LVPECL, low-speed LVDS

### Single-Ended

All of these standards use a push-pull CMOS output stage. The input buffer configuration and default output drive differ, as does the I/O supply voltage  $V_{CCI}$ . The reference voltage,  $V_{REF}$ , and the differential amplifier supply voltage,  $V_{CCDA}$ , are not needed.

### LVTTTL

An LVTTTL input buffer is used to implement this 3.3V standard (JEDEC JESD8-B). The LVTTTL output buffers can have four different drive strengths: 8mA, 12mA, 16mA, and 24mA. Two configuration bits are required to select one of these four strengths. The default strength is 24mA.  $V_{CCI}$  is 3.3V.

### 3.3V PCI/PCI-X

This option uses a 3.3V CMOS input buffer. A clamp diode is used to allow 5V input tolerance (see the “3.3V PCI/PCI-X” section on page 4). Again  $V_{CCI}$  is 3.3V. Like LVTTTL, the output buffer has four different drive strength options. The default for PCI is 16mA and PCI-X has a default of 12mA. Programmable slew rate is also available in the Axcelerator family. The slow option should NOT be used for 3.3V PCI.

### LVC MOS

The Axcelerator family provides three kinds of LVC MOS. 2.5V LVC MOS (LVC MOS2) is compliant with JEDEC standard JESD8-5. 1.8V LVC MOS (LVC MOS3) is compliant with JEDEC standard JESD8-7. 1.5V LVC MOS is the projected extension of these standards to a 1.5V supply voltage.  $V_{CCI}$ , of course, is either 2.5V, 1.8V, or 1.5V depending on the standard.

All versions use a 3.3V-tolerant CMOS input buffer.

## Voltage-Referenced

All of these standards use an external reference voltage ( $V_{REF}$ ).

### GTL+

The GTL+ standard was derived from the JEDEC JESD8-3 GTL standard. Intel extended the standard to define a bus architecture for the Pentium Pro CPU. The bus is an incident-wave-switching, open-drain bus with external pull-up resistors. A differential amplifier input buffer and open-drain CMOS output buffer are used.  $V_{REF}$  is 1.0V.

### SSTL3

SSTL3 is a 2.5V memory bus interface standard sponsored by IBM and Hitachi. There are two classes (I and II) and both are supported in the Actel Axcelerator family. The standard is implemented with a differential amplifier input buffer and a push-pull CMOS output stage. The relevant JEDEC standard is JESD8-8.  $V_{REF}$  is 1.5V.

**SSTL2**

SSTL2 is the 2.5V version of SSTL. There are two classes (I and II) and both are supported in the Actel Axcelerator family. The standard is implemented with a differential amplifier input buffer and a push-pull CMOS output stage. The relevant JEDEC standard is JESD8-9.  $V_{REF}$  is 1.25V.

**HSTL**

This memory bus interface standard is designed for 1.5V operation. The IBM-sponsored standard is defined in JEDEC specification JESD8-6. Like SSTL, it is implemented with a differential amplifier input buffer and a push-pull CMOS output stage. Class I HSTL is supported in the Axcelerator family.  $V_{REF}$  is 0.75V for Class I HSTL.

**Differential**

The differential interface standards offer higher performance and lower power consumption than their single-ended counterparts. Two I/O pads are used for each data-transfer channel. Both standards require resistor termination.

**LVPECL**

Often used for high-speed clock inputs, LVPECL employs a  $V_{CCI}$  of 3.3V and a differential voltage of 300mV.

**Low-Speed LVDS**

LVDS is a low voltage, differential-signal interface standard. The "standard" is really two – IEEE 1596.3 SCI-LVDS and

ANSI/TIA/EIA-644. LVDS uses a differential driver connected to a terminated receiver through a constant-impedance transmission line. The receiver is a wide-common-mode-range differential amplifier. The typical common-mode voltage is 1.25V with a 350mV differential voltage swing.  $V_{CCI}$  is 2.5V.

**I/O Architecture Overview**

Each I/O has an input register, an output register, and an enable register. I/Os are organized into banks, and there are eight banks per device (two per side). Each I/O bank has a common supply voltage,  $V_{CCI}$ , for the I/Os within that bank. For voltage-referenced I/Os, each bank also has a common reference-voltage bus,  $V_{REF}$ . The location of  $V_{REF}$  is user-selectable; any user I/O within the bank can be chosen. If differential I/Os are used, the differential amplifier supply voltage  $V_{CCDA}$  must be connected to 3.3V. Otherwise,  $V_{CCDA}$  must be tied to either 3.3V (3.3V if available in the system) or 2.5V. [Table 1](#) lists the acceptable ranges for all of the supply voltages.

Multiple I/O standards can co-exist within a single I/O bank; the legal combinations are given in [Table 2 on page 3](#). A standard listed in a row in the left column can be used with any of the other standards checked in the same row.

[Table 3 on page 3](#) summarizes DC input and output levels for the supported single-ended and voltage-referenced I/O standards. The AC test conditions for these standards are given in [Table 4 on page 4](#).

**Table 1 • Supply Voltage Ranges**

Supply	Min (V)	Typ (V)	Max (V)	Notes
$V_{CCA}$	1.4	1.5	1.6	
$V_{CCI}$	3.0	3.3	3.6	LVTTTL, 3.3V PCI, LVPECL, GTL+, SSTL3
	2.3	2.5	2.7	LVCMOS 2.5V, GTL+, SSTL2
	1.7	1.8	1.9	LVCMOS 1.8V
	1.4	1.5	1.6	LVCMOS 1.5V
	2.375	2.5	2.625	LVDS only
$V_{CCDA}$	3.0	3.3	3.6	Differential Amplifier in use
	3.0	3.3	3.6	No Differential Amplifier (recommended)
	2.3	2.5	2.7	No Differential Amplifier (also permitted)

Table 2 • Legal I/O Usage Matrix

I/O Standard	LVTTTL 3.3V	LVC MOS 2.5V	LVC MOS 1.8V	LVC MOS 1.5V (JESD8-11)	3.3V PCI 3.3V PCI-X	GTL + (3.3V)	GTL + (2.5V)	HSTL Class I (1.5V)	SSTL2 Class I & II (2.5V)	SSTL3 Class I & II (3.3V)	LVDS (2.5V ±5%)	LVPECL (3.3V)
LVTTTL 3.3V ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
LVTTTL 3.3V ( $V_{REF}=1.5V$ )	✓				✓					✓		✓
LVC MOS 2.5V ( $V_{REF}=1.0V$ )		✓					✓				✓	
LVC MOS 2.5V ( $V_{REF}=1.25V$ )		✓							✓		✓	
LVC MOS 1.8V			✓									
LVC MOS 1.5V ( $V_{REF}=1.75V$ ) (JESD8-11)				✓				✓				
3.3V PCI 3.3V PCI-X ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
3.3V PCI 3.3V PCI-X ( $V_{REF}=1.5V$ )	✓				✓					✓		✓
GTL + (3.3V)	✓				✓	✓						✓
GTL + (2.5V)		✓					✓					
HSTL Class I				✓				✓				
SSTL2 Class I & II		✓							✓		✓	
SSTL3 Class I & II	✓				✓					✓		✓
LVDS ( $V_{REF}=1.0V$ )		✓					✓				✓	
LVDS ( $V_{REF}=1.25V$ )		✓							✓		✓	
LVPECL ( $V_{REF}=1.0V$ )	✓				✓	✓						✓
LVPECL ( $V_{REF}=1.5V$ )	✓				✓					✓		✓

Notes: A "✓" indicates whether standards can be used within a bank at the same time.

Examples:

- a) LVTTTL can be used with 3.3V PCI/PCI-X, and GTL+ (3.3V), when  $V_{REF} = 1.0V$  (GTL+ requirement).
- b) LVTTTL can be used with 3.3V PCI/PCI-X, and SSTL3 Class I & II, when  $V_{REF} = 1.5V$  (SSTL3 requirement).
- c) LVDS  $V_{CCI} = 2.5V \pm 5\%$ .

Table 3 • DC Input and Output Levels

Standard	$V_{IL}$		$V_{IH}$		$V_{OL}$	$V_{OH}$	$I_{OL}$	$I_{OH}$
	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
LVTTTL	-0.3	0.8	2.0	$V_{CCI}+0.3$	0.4	2.4	24	-24
3.3V PCI/PCI-X	-0.5	$0.3 V_{CCI}$	$0.5 V_{CCI}$	$V_{CCI}+0.5$	$0.1 V_{CCI}$	$0.9 V_{CCI}$	*	*
LVC MOS 2.5V	-0.3	0.7	1.7	$V_{CCI}+0.3$	0.4	2.0	12	-12
LVC MOS 1.8V	-0.3	$0.35 V_{CCI}$	$0.65 V_{CCI}$	$V_{CCI}+0.3$	$V_{CCI}-0.45$	$V_{CCI}+0.45$	2	-2
LVC MOS 1.5V	-0.3	$0.35 V_{CCI}$	$0.65 V_{CCI}$	$V_{CCI}+0.3$	0.4	$V_{CCI}+0.4$	8	-8
GTL+	N/A	$V_{REF}-0.05$	$V_{REF}+0.05$	N/A	0.6	N/A	N/A	N/A
SSTL2 I	-0.3	$V_{REF}-0.18$	$V_{REF}+0.18$	$V_{CCI}+0.3$	$V_{REF}-0.57$	$V_{REF}+0.57$	7.6	-7.6
SSTL2 II	-0.3	$V_{REF}-0.18$	$V_{REF}+0.18$	$V_{CCI}+0.3$	$V_{REF}-0.76$	$V_{REF}+0.76$	15.2	-15.2
SSTL3 I	-0.3	$V_{REF}-0.2$	$V_{REF}+0.2$	$V_{CCI}+0.3$	$V_{REF}-0.6$	$V_{REF}+0.6$	8	-8
SSTL3 II	-0.3	$V_{REF}-0.2$	$V_{REF}+0.2$	$V_{CCI}+0.3$	$V_{REF}-0.8$	$V_{REF}+0.8$	16	-16
HSTL I	-0.3	$V_{REF}-0.1$	$V_{REF}+0.1$	$V_{CCI}+0.3$	0.4	$V_{CC}-0.4$	8	-8

Note: \* Current characteristics as specified in PCI Specification Revision 2.2.

**Table 4 • AC Test Conditions**

Standard	Input Waveform Low (V)	Input Waveform High (V)	Measuring Point (V)	V <sub>REF</sub> (typ) (V)	Capacitive Load (pF)
LVTTTL	0	3.0	1.40	N/A	35
3.3V PCI/PCI-X	*	*	*	N/A	10
LVC MOS2.5V	0	2.5	1.125	N/A	35
LVC MOS1.8V	0	1.8	0.8	N/A	35
GTL+	V <sub>REF</sub> -0.2	V <sub>REF</sub> +0.2	V <sub>REF</sub>	1.0	0
SSTL2 I	V <sub>REF</sub> -0.75	V <sub>REF</sub> +0.75	V <sub>REF</sub>	1.25	30
SSTL2 II	V <sub>REF</sub> -0.75	V <sub>REF</sub> +0.75	V <sub>REF</sub>	1.25	30
SSTL3 I	V <sub>REF</sub> -1.0	V <sub>REF</sub> +1.0	V <sub>REF</sub>	1.5	30
SSTL3 II	V <sub>REF</sub> -1.0	V <sub>REF</sub> +1.0	V <sub>REF</sub>	1.5	30
HSTL I	V <sub>REF</sub> -0.5	V <sub>REF</sub> +0.5	V <sub>REF</sub>	0.75	20

*Note:* \*Specified in PCI Specification Revision 2.2 and PCI-X Specification Revision 1.0.

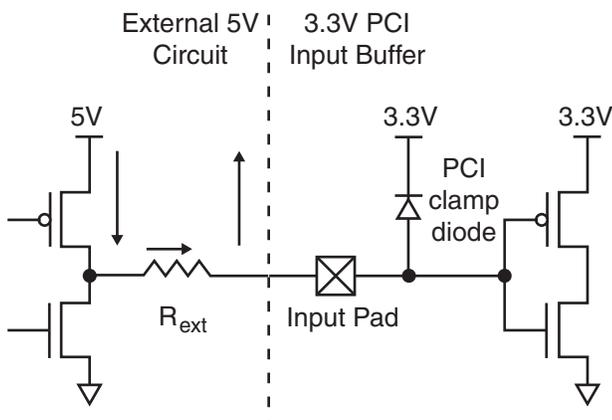
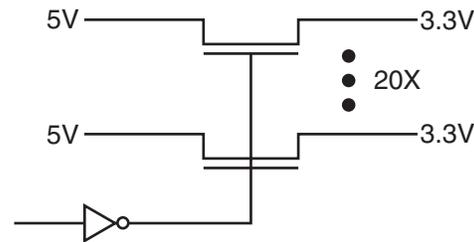
## I/O Details

The following sections provide implementation details on some of the standards.

### Single-Ended Standards

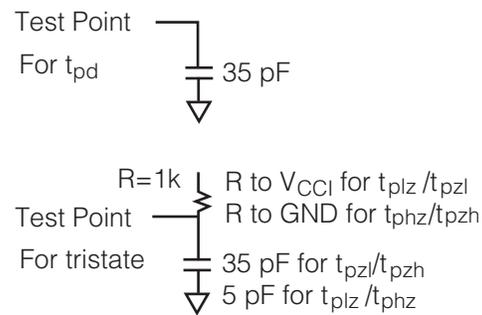
#### 3.3V PCI/PCI-X

5V tolerance is allowed for 3.3V PCI only. In this case, an INTERNAL clamp diode (required for compliance with the 3.3V PCI I/O standard) is enabled between the input pad and the V<sub>CCI</sub> pad. The diode clamps the voltage at the input pin at V<sub>CCI</sub> + V<sub>diode</sub> (3.3V + 0.8V = 4.1V worst-case). An EXTERNAL current-limiting serial resistor (about 100Ω) is required between the input pin and the 5V signal source (Figure 1). An alternative to the external resistor is the bus switch, such as the IDTQS32X2384, shown in Figure 2. Note that hot swapping is NOT available with 3.3V PCI.


**Figure 1 • 5V Tolerance with 3.3V PCI**

**Figure 2 • IDTQS32X2384 Bus Switch**

#### Test Circuit

Parameters for all of the single-ended standards were obtained using the same test circuit (Figure 3).


**Figure 3 • Test Circuit for LVTTTL and LVC MOS**

### Voltage-Referenced

#### HSTL

The Class I V<sub>CCI</sub> range is from 1.4V to 1.6V and the V<sub>REF</sub> range is from 0.68V to 0.9V. The differential amp (both PMOS and NMOS) does not work properly in this range. Even if V<sub>CCI</sub> is equal to 1.8V, the differential amp still will not work very well because of the low end of the V<sub>REF</sub> range (0.68V).

Proper HSTL operation is achieved by having a 3.3V external reference voltage powering all the differential amps. This simplifies circuit design and saves die size, because we can use one differential amp circuit per I/O instead of using multiple differential amps to handle different  $V_{CCI}$  values. This is done by placing eight 3.3V  $V_{CCDA}$  pads around the chip. Internally, they are tied together by metal. If none of the differential amplifiers are used, these eight pads can be

tied to either 2.5V or 3.3V. If one voltage value is applied to one  $V_{CCDA}$  pin, all other  $V_{CCDA}$  pins should have the same value.

### Test Circuits

The test circuits for SSTL2/SSTL3 and HSTL are shown in Figure 4.

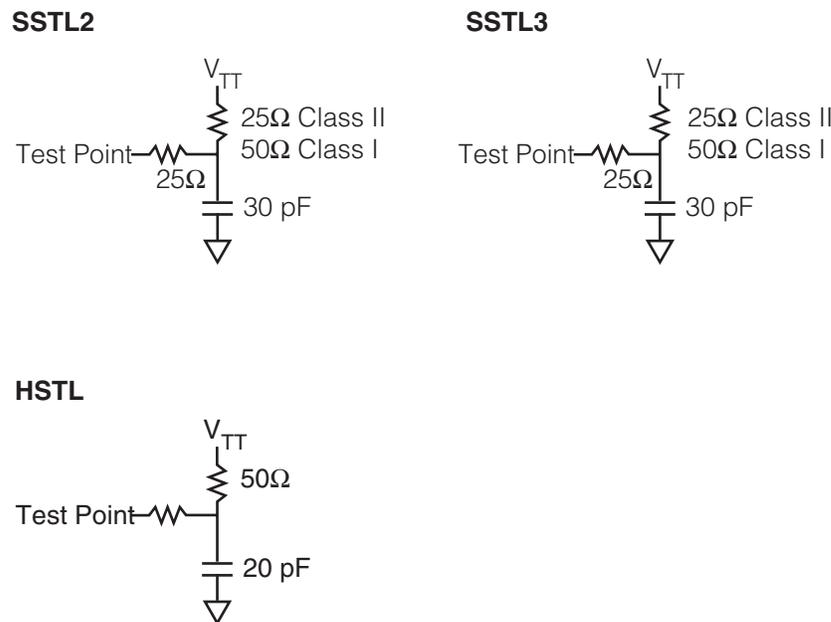


Figure 4 • Test Circuits for SSTL and HSTL

## Differential

### Low-Speed LVDS

In "true" LVDS, a current-mode driver provides a nominal current of 3.5mA. When this current flows through a 100Ω termination resistor on the receiver side, a voltage swing of 350mV is developed across the resistor (Figure 5 on page 6). The direction of the current flow is controlled by the data fed to the driver. In the Accelerator LVDS implementation, the receiver is similar to the "true" LVDS receiver (Figure 5 on page 6). However, the driver is not a current-mode driver. Instead, two CMOS drivers from two adjacent I/O cells are used to generate the differential signals. Two complementary signals have to be routed by software to these two drivers. An external resistor network (three resistors) is needed to reduce the voltage swing to about 350mV. Note that the signal skew of the two adjacent CMOS drivers must be minimized to avoid a loss in performance. Figure 6 on page 6 illustrates the circuit. Therefore, four external resistors are required, three for the driver and the 100Ω termination resistor on the receiver side.

Table 5 on page 6 provides DC parametric data for the LVDS implementation.

### LVPECL

This scheme is similar to the LVDS scheme described above. It also requires four external resistors, three for driver and one for receiver, but the values for the three driver resistors are different from the LVDS resistors above because the output voltage levels are different (Figure 7 on page 6). This LVPECL is different from the standard LVPECL because the  $V_{OH}$  levels are 200mV below standard LVPECL levels. Table 6 on page 6 illustrates the DC parametric data for LVPECL.

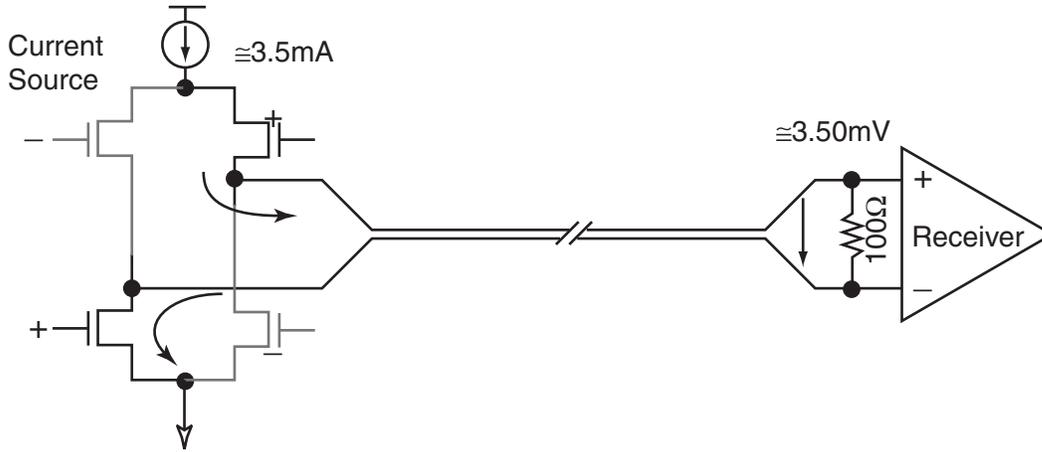


Figure 5 • LVDS Operation

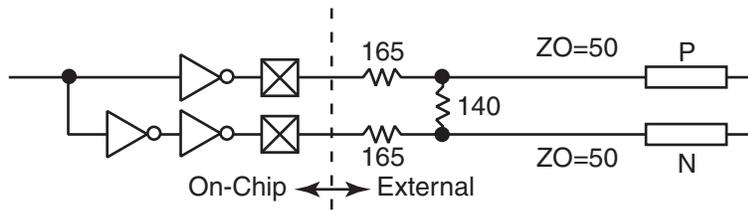


Figure 6 • Accelerator LVDS Driver Circuit

Table 5 • LVDS DC Parameters

Symbol	DC Parameter	Notes	Min	Typ	Max	Units
$V_{CCI}$	Supply Voltage	+/- 5%	2.375	2.5	2.625	V
$V_{OH}$	Output High Voltage		1.25	1.425	1.6	V
$V_{OL}$	Output Low Voltage		0.9	1.075	1.25	V
$V_{ODIFF}$	Differential Output Voltage		250	350	450	mV
$V_{OCM}$	Output Common Mode Voltage		1.125	1.25	1.375	V
$V_{ICM}$	Input Common Mode Voltage	Differential input voltage = +/-350mV	0.2	1.25	2.2	V

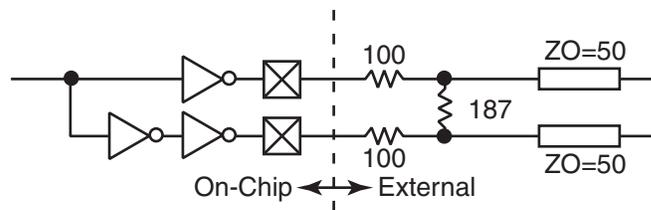
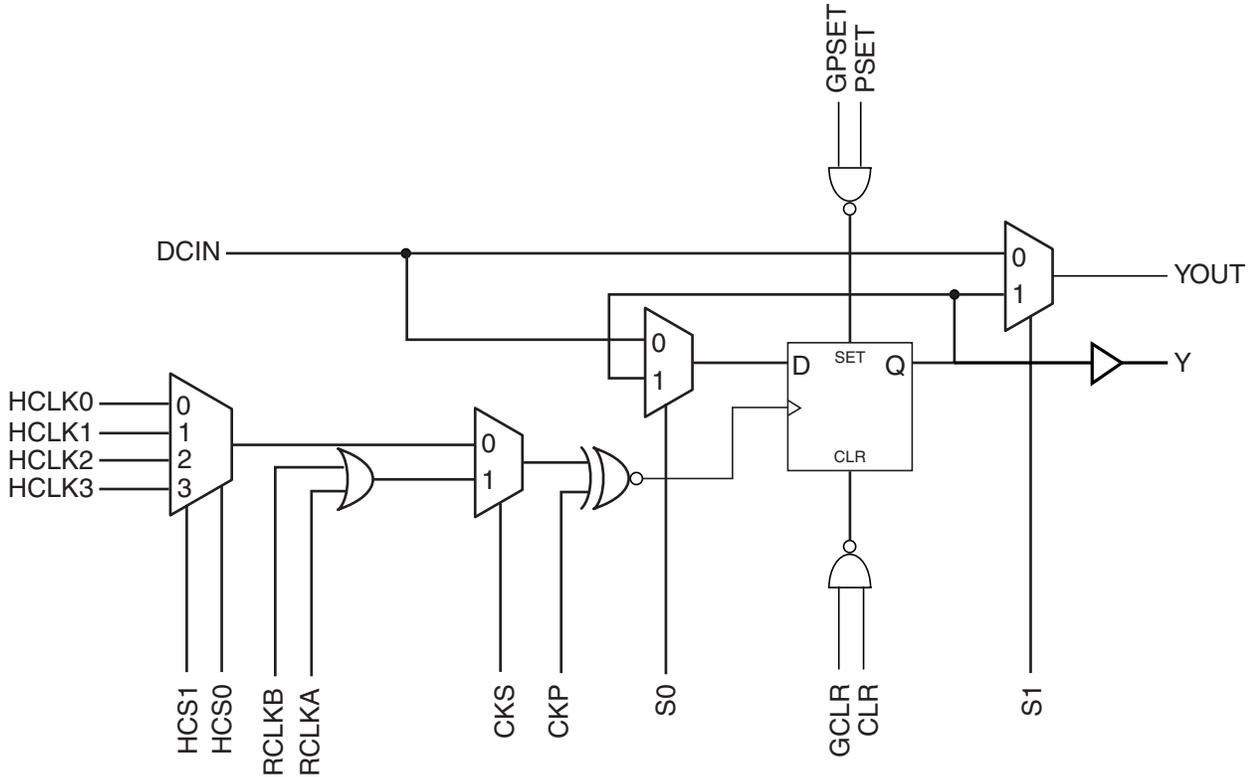


Figure 7 • LVPECL Driver Circuit

Table 6 • LVPECL DC Parameters

DC Parameter	$V_{CCI}=3.0V$		$V_{CCI}=3.3V$		$V_{CCI}=3.6V$		Units
	Min.	Max.	Min.	Max.	Min.	Max.	
$V_{OH}$	1.8	2.11	1.92	2.28	2.13	2.41	V
$V_{OL}$	0.96	1.27	1.06	1.43	1.30	1.57	V
$V_{IH}$	1.49	2.72	1.49	2.72	1.49	2.72	V
$V_{IL}$	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3		0.3		0.3		V




**Figure 9 • Output and Enable Register Configuration**
**Table 7 • Input Buffer Delays (ns)**

I/O Standard	'-3' Speed	'-2' Speed	'-1' Speed	'Std' Speed
<b>LVTTTL</b>				
Low Slew – 8 mA	0.98	1.13	1.28	1.51
– 12 mA	0.96	1.11	1.26	1.48
– 16 mA	0.98	1.13	1.28	1.50
– 24 mA	0.98	1.13	1.28	1.50
High Slew – 8 mA	0.98	1.13	1.28	1.50
– 12 mA	0.98	1.13	1.28	1.50
– 16 mA	0.98	1.13	1.28	1.50
– 24 mA	0.98	1.13	1.28	1.50
LVC MOS25	1.72	1.98	2.25	2.65
LVC MOS18	2.62	3.03	3.43	4.03
LVC MOS15	3.65	4.22	4.78	5.62
3.3V PCI/PCI-X	1.09	1.26	1.43	1.68
GTL+	0.87	1.01	1.14	1.34
HSTL Class I	2.47	2.85	3.23	3.80
SSTL2 Class I	1.04	1.20	1.36	1.60
SSTL2 Class II	1.00	1.16	1.31	1.55
SSTL3 Class I	0.86	0.99	1.12	1.32
SSTL3 Class II	0.83	0.96	1.09	1.28
LVDS	1.68	1.94	2.20	2.59
LVPECL	1.23	1.42	1.61	1.90

Table 8 • Output Buffer Delays (ns)

I/O Standard	'-3' Speed	'-2' Speed	'-1' Speed	'Std' Speed
LVTTTL				
Low Slew – 8 mA	8.80	10.15	11.51	13.54
– 12 mA	6.92	7.98	9.05	10.65
– 16 mA	0.84	0.97	1.10	1.30
– 24 mA	6.64	7.67	8.69	10.22
High Slew – 8 mA	0.84	0.97	1.10	1.30
– 12 mA	0.84	0.97	1.10	1.30
– 16 mA	0.84	0.97	1.10	1.30
– 24 mA	0.84	0.97	1.10	1.30
LVC MOS25	1.12	1.29	1.46	1.72
LVC MOS18	1.73	2.00	2.26	2.66
LVC MOS15	2.35	2.71	3.07	3.61
3.3V PCI/PCI-X	0.96	1.11	1.26	1.48
GTL+	1.13	1.30	1.47	1.73
HSTL Class I	0.99	1.14	1.30	1.53
SSTL2 Class I	1.05	1.21	1.38	1.62
SSTL2 Class II	1.05	1.21	1.38	1.62
SSTL3 Class I	1.11	1.28	1.46	1.71
SSTL3 Class II	1.11	1.28	1.46	1.71
LVDS	1.63	1.88	2.14	2.51
LVPECL	1.41	1.75	1.98	2.33



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