In-System Programming ProASIC Devices

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Introduction

To decrease time-to-market, designers often use in-system programmable (ISP) field programmable gate arrays (FPGAs). Compared to traditional FPGAs, Microsemi's flash-based ProASIC® devices do not require an external boot PROM to support device programming. While on-board security mechanisms prevent all access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades.

This application note describes the requirements for programming a ProASIC device and specific requirements when using Silicon Sculptor I /II and FlashPro.

If you are not sure which method of in-system programming to use, refer to the *Programming Flash Devices* application note, which explains the differences between the various programming solutions Microsemi offers.

ISP Setup

To facilitate the ISP of ProASIC devices, Microsemi provides three solutions: FlashPro or Silicon SculptorI/II with an add-on ISP Kit. Figure 1 on page 2 shows the programming setup with the Silicon Sculptor and FlashPro.

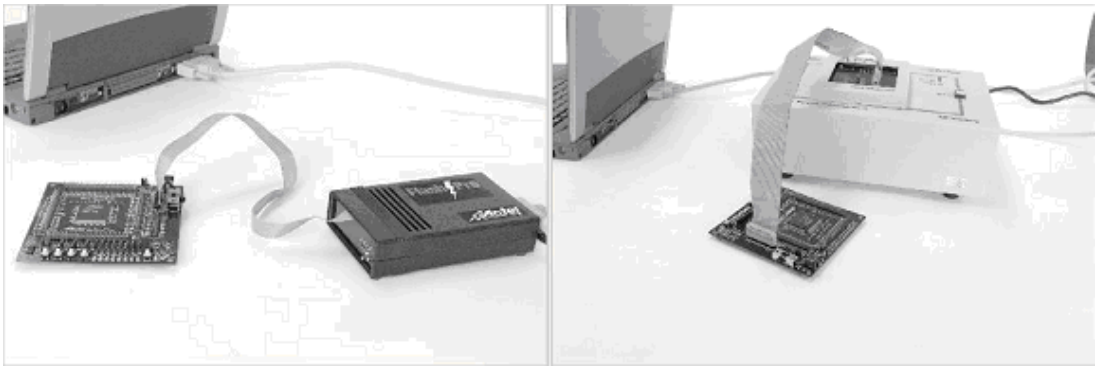


***Figure 1* • Programming Setup**

ProASIC Device Programming Requirements

During programming, all I/O pins, except for JTAG interface pins, are tristated and pulled up to VDDP. This isolates the part and prevents the signals from floating.

Interruptions in the programming sequence may result in unpredictable behavior of a partially programmed device. Additionally, switches that are programmed incorrectly can cause high current flow through the circuitry, resulting in permanent damage to the device.

Power Supply Configurations

Two power supplies, one for the VDDL pins and the other for the VDDP pins, are needed in normal operation. VDD powers the core and VDDP powers the I/O pads. VDD must be set to 2.5 V (±0.2 V), and VDDP can be set to either 2.5 V(±0.2 V) or 3.3 V (±0.3 V) (Table 1).

During programming for ProASIC devices, Microsemi recommends powering down the board and using the FlashPro or Silicon Sculptor I/II programmer to provide the power supply (Table 1).

If you must power up the ProASIC device from the board during programming, you need to deselect the VDDL and VDDP power supplies from the programmer. On the board, the VDDP for the ProASIC device must be set to 2.5 V during programming. The tristated I/Os must not be driven by 3.3 V signals. If this occurs, the pads will latch-up and a high current will flow through the pad cell, which can damage the device.

Programming ProASIC devices also requires that the VDDL be set to 0 V. The board power supply design must allow for this if you use it to power-up the device during programming. The typical current consumption for each programming pin during programming is shown in Table 1.

***Table 1* • ProASIC Voltages and Currents**

Power Supply	Normal Operation	Programming Mode	Current During Programming
VDDL	2.5 V	0 V	IVDDL < 0 mA at VDDL
VDDP	2.5 V or 3.3 V	2.5 V	IVDDP < 20 mA at VDDP
VPP	=VDDP	16.4 V to 16.6 V	IVPP < 35 mA at VPP
VPN	0 V	–12.1 V to -11.9 V	IVPN < 15 mA at VPN

Board Considerations

Microsemi recommends bypass capacitors from VPP to GND and VPN to GND for all ProASIC devices during programming. These bypass capacitors protect the ProASIC devices from voltage spikes that occur on the VPP and VPN power supplies during the erase cycle. Two bypass capacitors are required for each supply.

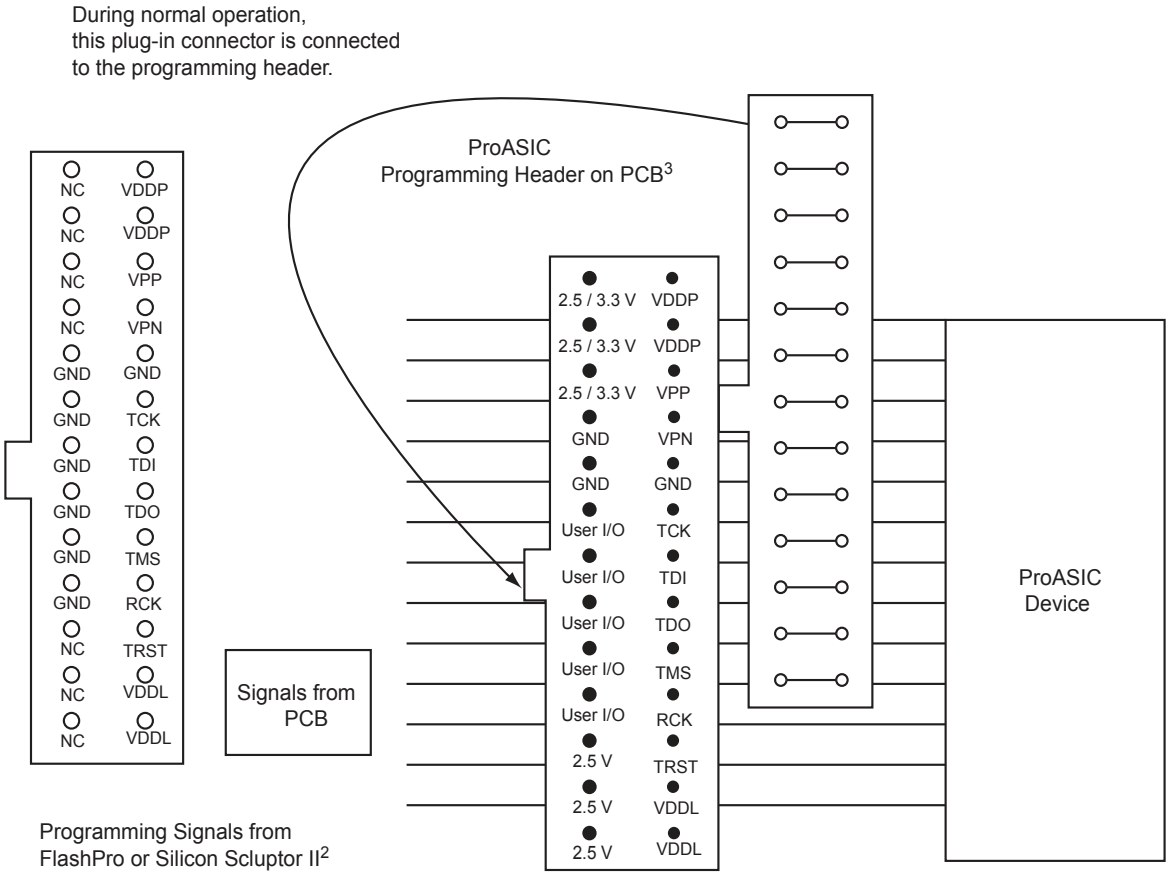
One of the bypass capacitors is a 4.7 µF (low ESR, <1 Ω, tantalum, 25 V or greater rating). The other bypass capacitor is a 0.01 µ ceramic capacitor with a 25 V or grater rating (Figure 6 on page 10). The bypass capacitors must be placed within 2.5 cm of the device pins (Figure 2 on page 4). The bypass capacitors must be placed within 2.5 cm of the device pins.

Programmer Specific Requirements

Programmer specific requirements for Silicon Sculptor I/II and FlashPro are shown below:

Silicon Sculptor I/II Specific

- Programming Clock signal—Both RCK and TCK are used
- Programming file—Both BIT and STAPL files are supported
- Silicon Sculptor I only supports the BIT file.
- Daisy Chain—Only supports chains of ProASIC or ProASIC devices. Refer to ProASIC Daisy-Chain
- Programming for similar applications
- Power Supply
  - Solution 1: 0ohm resistor link *1 and *2 should be populated if the programmer is providing the VDD and VDDP supplies. Or they can be replaced by wires on the PCB to meet easy layout and low cost requirements. Make sure the VDD and VDDP supplies from the target can handle the power supply from the programmer, otherwise use solution 2.
  - Solution 2: 0ohm resistor *1 and *2 should not be populated if the target is providing the VDD and VDDP supplies.



Notes:

1. *For FlashPro, use TCK. For Silicon Sculptor, use RCK and TCK.*
2. *This is the output of the programmer. This diagram shows the signals that the programmer will drive onto the header in programming mode.*
3. *This is the pinout of the programming header on the PCR. The signals that appear on the header must be connected to the ProASIC device.*

***Figure 2* • ProASIC ISP Board Layout and Programming Connector Top View**

FlashPro Specific

- Programming Clock signal—Only TCK is used
- Programming file—Only STAPL files are supported
- Daisy Chain–Supported. FlashPro will get the bypass devices information from the device.db file. Customer can manually edit the device.db file to add in more devices that are not in the original device list. For more details, contact Microsemi SoC Products Group Tech Support.
- Power Supply
  - Solution 1: 0 ohm resistor link *1 and *2 should be populated if the programmer is providing the VDD and VDDP supplies. Or they can be replaced by wires on the PCB to meet easy layout and low cost requirements. Make sure the VDD and VDDP supplies from the target can handle the power supply from the programmer, otherwise use solution 2.
  - Solution 2: 0 ohm resistor *1 and *2 are optional if the target is providing the VDD and VDDP supplies. Clear check boxes for the VDD and VDDP supplies from FlashPro in the software.

Signal Integrity

This section describes signal integrity in relation to ISP of Microsemi ProASIC devices and answers some common questions.

Importance of Signal Integrity

Without reasonably clean signals on the JTAG nets, reliable communication with the parts is not possible. The result of bad signal quality is programming failures with good parts, or in extreme cases, an inability to communicate with the part at all. It is even possible to cause physical damage the ProASIC device due to electrical overstress of the tunnel oxide during programming and erasing of the part.

The JTAG specification defines a state machine, the Test Access Port (TAP) controller, which controls communication over the JTAG bus. There are two TAP controllers when talking to a JTAG slave, the JTAG controller and the JTAG slave. These two controllers must dance in lock-step for communication to take place. If the slave gets out of step, communication to the slave is lost until the two controllers are synchronized again. In the case of device programming, the JTAG controller resides in the programmer and the programming software. The JTAG slave is a hardware state machine in the ProASIC device. Transitions between the different TAP states are controlled by the JTAG TMS signal, as it is clocked into the device by the JTAG clock TCK. The communication is serial, so any dropped bits result in failed state transitions.

Effect of Reflections and Crosstalk

Reflections will occur during the rise time of TCK or RCK and cause the part to see two clock edges instead of one. When this occurs during a data transfer, it corrupts the data.

Effect of Ground Bounce

Ground bounce changes the voltage on the input buffers. This changes the threshold voltage of these buffers since LVCMOS has a threshold voltage of half of the supply voltage. The ground bounce also adds a DC offset to the threshold voltage. The end result is that it raises the threshold voltage.

What Happens if TCK Gets Double-Clocked?

All of the I/O buffers in the ProASIC devices are built with the same logic macro so the JTAG signals have the same performance as the rest of the device. The APA device datasheet specifies that the device is capable of 150 MHz system performance and up to 250 MHz internal performance. The maximum clock frequency is listed as 180 MHz. A 180 MHz clock has a period of just 5.6 ns. The clock is typically high for only half of the period, or 2.8 ns. So the ProASIC inputs are capable of responding to clock pulses that are 2.8 ns wide even though the programmer is only clocking the JTAG bus at 4 MHz (FlashPro TCK rate). This means that reflections or glitches that are only 2.8 ns wide will still be seen by the device's TAP controller. If the slave controller sees a 2.8 ns clock glitch when it is not in a stable state, then the glitch will affect the programming.

The stable states for the TAP controller are: Test-Logic-Reset, Run-Test/Idle, Pause-DR, and Pause-IR. All other states of the TAP controller will have a negative side effect from a clock glitch, either the state will change or extra repeated data bits will be clocked into the part.

What Happens if RCK Gets Double-Clocked?

An occasional double clocking of RCK is not as severe as it is for TCK. Since RCK is used for timing programming pulses, an occasional double clock just shortens the programming pulse width. Since all Flash switches do not take the same amount of time to program, there is a marginal amount of overprogramming that occurs for most switches. In most cases, an infrequent double clocking of RCK will reduce the over-programming, but not cause a failure. A continuous double clocking could cut all of the programming pulses in half and this could have noticeable results. Cutting the programming pulse ramp rates can cause electrical over stress to the tunnel oxide and cause permanent damage to the device.

What is RCK and Why Is it Needed for Internal ISP?

The ProASIC device contains an internal programming controller that controls the programming of the Flash switches. Voltages used during programming are based on an internal voltage reference, but the controller needs a 1 MHz clock derived from either RCK or TCK for its time reference. The part includes an internal five bit programmable clock divider, so the external clock can be any multiple of 1 MHz, between 1 MHz and 31 MHz. The external time reference can either come from TCK or RCK. The RCK input is provided as an easy to use reference clock input. Connect an appropriate oscillator to the RCK pin and the programming controller's clock reference needs are met.

Silicon Sculptor uses the RCK input during programming because its TCK clock is under control of a program running on an internal microprocessor. Because it uses RCK, Silicon Sculptor only needs to send a TCK when it wants to communicate over the JTAG bus.

The FlashPro and FlashPro Lite programmers use TCK as the reference clock so it does not need an RCK. The tradeoff is that FlashPro or FlashPro Lite needs to have a hardware state controller that will move the ProASIC device's internal TAP controller to a stable state whenever communication with the device is not occurring. If the PC is interrupted while it is sending data to the device's Data Register, FlashPro or FlashPro Lite must control the TMS line to move the TAP controller from the Shift-DR state into the Pause-DR state. The ProASIC device can wait in the Pause-DR state until the PC resumes sending data. When the PC resumes communication, FlashPro or FlashPro Lite then needs to use the TMS line to switch the TAP controller back into the Shift-DR state.

What are the Symptoms of a Signal Integrity Problem?

A signal integrity problem can manifest itself in many ways. Because the problem shows up as extra or dropped bits during serial communication, the meaning of the communication has changed.

There is a normal variation of threshold voltage and frequency response between parts even from the same lot. Because of this, the effects of signal integrity may not always affect different devices on the same board the same way. Sometimes replacing a device appears to make signal integrity problems go away, but this is just masking the problem. Different parts on identical boards will exhibit the same problem sooner or later. As the process matures, the average speed of a device type may increase and make it more susceptible to narrow glitches. This can also uncover signal integrity problems later in the board design life cycle.

For these reasons, it is important to fix signal integrity problems early. Unless the signal integrity problems are severe enough to completely block all communication between the device and the programmer, they will show up as subtle problems. Some of the FlashPro exit codes that can cause signal integrity problems are listed below. Signal integrity problems are not the only possible cause of these errors, but this list is intended to show where problems can occur.

- Chain Integrity Test Error or Analyze Chain failure: Normally the FlashPro Analyze Chain command expects to see 0x2 on the TDO pin. If the command reports reading 0x0 or 0x3, it is seeing the TDO pin stuck at 0 or 1. The only time the TDO pin comes out of tristate is when the JTAG TAP state machine is in the Shift-IR or Shift-DR states. If noise or reflections on the TCK or TMS lines have disrupted the correct state transitions, the device’s TAP controller might not be in one of these two states when the programmer tries to read the device. In this case the output is floating when the programmer does the read and it will not match the expected. This can also be caused by a broken TDO net. Only a small amount of data is read from the device during the Analyze Chain command, so marginal problems may not always show up during this command.

- Invalid device ID (Sculptor): Silicon Sculptor has a different set of error messages when programming Microsemi flash devices with bit files. First, it tries to read the device ID code and verify that it matches what has been selected. A common place to catch signal integrity problems when using the Sculptor's ISP module is when reading the device ID.
- Exit 7: This error occurs when programming data read from the factory row of the device does not match what the STAPL file expects to see. Since signal integrity problems can disrupt communication between the programmer and the device, the data read back can be affected. This data is read before each of the STAPL file actions are executed. All ProASIC devices are programmed at the factory with a design with only input pins so that there will be no I/O conflicts when soldered to a board for ISP programming. This also verifies that the factory row data is readable before the part leaves the factory. Unless the device has been damaged during handling or assembly, if you see an EXIT 7 error the first time you try to program the part you should suspect a signal integrity problem.
- Exit 11: This error occurs during the verify stage of programming a device. After programming the design into the ProASIC device, the device is verified to ensure it is programmed correctly. The verification is done by shifting the programming data into the device. Then an internal comparison is perform within the device to verify that all switches are programmed correctly. All the switches that are not programmed (0s) are verified first, followed by the switches that are programmed (1s). Since the number of Flash switches in a ProASIC device is huge, if the board design has any signal integrity problem with writing or reading, it is very likely to show up during verify if it has not already caused a problem.
- Verify Failed (Sculptor): Sculptor can return a verify error for the same reason that the FlashPro Verify action can return an EXIT 11 error code.
- EXIT -90 programming error: There are several places in the STAPL file where testing of a status bit read from the device can result in an EXIT -90 failure. If the TAP state controller is in the wrong state, or the shift register is double clocked, the testing will not occur on the intended status bit and could result in the failure of the test. When the status bit test fails, the programmer returns an EXIT code of -90.

What do the programmer outputs look like?

Silicon Sculptor

There are two Silicon Sculptor models in use today, Silicon Sculptor and Silicon Sculptor II. Both of these require a socket module for programming. If you are doing ISP programming with a Sculptor programmer, you will be using either an SMPA-ISP-ACTEL-1, or an SMPA-ISP-ACTEL-2 socket module. Either socket module can be used with either programmer (Figure 3).

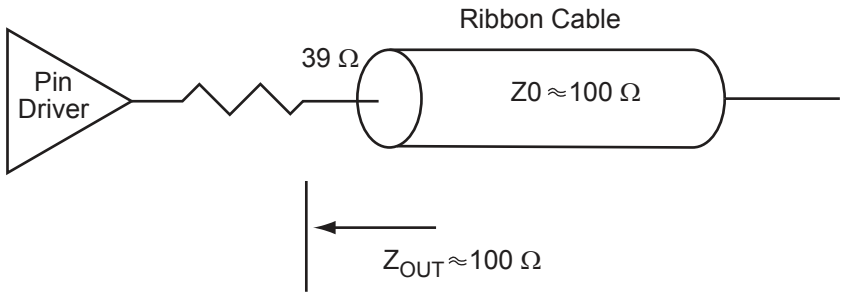


***Figure 3* • ISP-1 Socket Module**

When using the SMPA-ISP-ACTEL-1 socket module, the JTAG pins are driven directly by the programmer's pin drivers. These drivers are designed with a 39ohm resistor in series with the output to raise the driver's output impedance to close to 100ohms. The ribbon cable used with this adapter has conductors with 0.05 inch spacing. When used with the SMPA-ISP-ACTEL-1 adapter module, the characteristic impedance of this cable is approximately 100ohms as long as all of the ground pins are connected on the target board.

So the output of the pin drivers provide a series termination to the transmission line. The differences between the Sculptor and Sculptor II pin drivers involve the VOH level each is capable of driving, and indirectly the signal rise time. On a SMPA-ISP-ACTEL-1 socket module the RCK frequency is 16 MHz.

The SMPA-ISP-ACTEL-2 socket module was designed with a buffer on each of the JTAG signal lines (Figure 4).The output impedance of the buffer is approximately 33ohms, so it does not provide a good termination to the 100ohm ribbon cable. The buffer was added to improve daisy chain programming performance, but it also necessitates parallel termination of the JTAG lines to prevent reflections. The buffer has an output current limit of 20mA so it is limited to driving a 125ohm termination resistor.

To terminate the ribbon cable with a lower resistance requires using AC termination with a resistor and capacitor in series. The SMPA-ISP-ACTEL-2 socket module (Figure 4) also has a connector for the same ribbon cable used by FlashPro. The impedance of this cable is also close to 100ohms when all of the ground pins are connected at the target board. On an SMPA-ISP-ACTEL-2 socket module the RCK frequency was changed to 1 MHz. Using 1 MHz for RCK cuts down on the cross-talk between RCK and other traces.

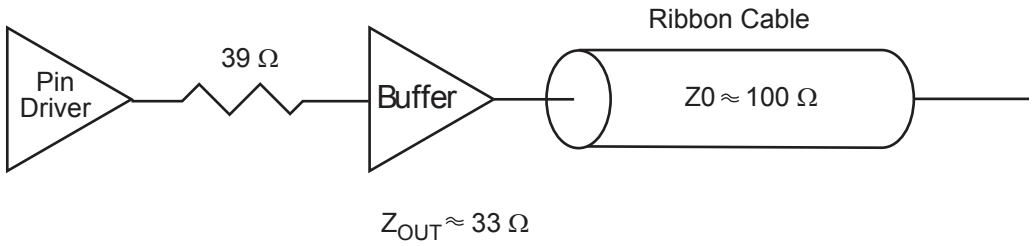


***Figure 4* • ISP-2 Socket Module**

FlashPro

The output impedance of the FlashPro programmer is similar to that of the SMPA-ISP-ACTEL-1 socket module. It is an output driver with a series termination resistor. The output impedance of the JTAG drivers is about 100ohms and approximately matches the impedance of the narrow ribbon cable used by the FlashPro. The ribbon cable used with this adapter has conductors with 0.025 inch spacing. The impedance of this cable is close to 100ohms when all of the ground pins are connected at the target board. The FlashPro cable connections are slightly different from those of Silicon Sculptor. FlashPro uses one of the ground pins, pin ten to detect that the cable is connected. This pin should still be connected to ground on the target board, but the pin is connected to a pull-up and a gate input on the FlashPro side. If the cable is not properly connected to the target board, the gate will see a logic 1 on its input instead of the 0 it expects to see. This results in an error message indicating the cable is not connected.

Header Converter

While it is not a programmer, knowing the effect of using the header converter is important in controlling signal integrity. The impedance of the header converter board is not controlled and contains stubs for each of the two unused connectors. For this reason, one of the ribbon cables used with the header converter must be as short as is physically possible to limit reflections. When using the header converter, we recommend that the wide ribbon cable connecting the socket module to the header converter be the short cable. Tools and materials for building the wide ribbon cables are readily available so this is the easier cable to build.

What Should My Board Design Look Like to Match the Programmer(s)?

To minimize reflections at the cable to board interface, the impedance of the JTAG traces must match the cable impedance. The JTAG traces should be routed with 100ohm traces. The most critical traces are the TCK signal and the RCK signal. Note that RCK is not used with FlashPro or FlashPro Lite, so terminating it is not necessary if only using these programmers.

An option if you are unable to match the cable impedance because of your board stack-up, is to buffer the JTAG signals at the programming header and terminate the buffer inputs in the cable's characteristic impedance. The output of the buffer can then drive whatever impedance trace your board stack-up dictates. This option is shown in Figure 5.

This buffer can either be on your board or it can be an adapter that s into the programming header. You may still need to terminate the buffered clock signals to match the impedance of your board traces. Treat TCK and RCK as 200 MHz clocks in your layout and you should be safe.

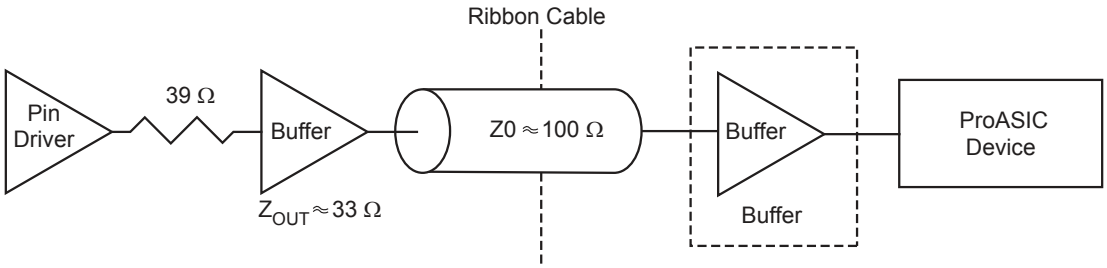


***Figure 5* • Buffering JTAG Signals**

Termination

The need to terminate the JTAG signals depend on the complexity and layout of your board. If your board design is a simple board with only one ProASIC device, the programming header is next to the part, and you are using either of the FlashPro programmers or the SMPA-ISP-ACTEL-1 socket module then you do not need additional terminators on your board for most of the time.

If your board contains multiple devices on the JTAG chain, the distance between the programming header and the ProASIC device is large, or you are using the SMPA-ISP-ACTEL-2 socket module then you should consider using some form of termination. At the very least the TCK line should be terminated. If you want to be able to use the Silicon Sculptor programmer then the RCK line will also need to be terminated. An 82 ohm resistor in series with a 220pF capacitor has given good results in our testing. The correct values for any given board will need to be determined on a case-by-case basis. Providing generic land patterns for the terminators during the board layout will give you the most flexibility when the final termination values are selected.

The type of termination to use depends on the design and layout of each individual board. Series termination at the driver works best when all device loading is at the end of the net. This occurs when only one device is connected to the clock line, or when two devices are both connected at the end of the line. With series termination, the series resistor and the trace impedance make up a voltage divider. If both the output resistance and trace impedance are matched, then the signal sent down the wire is only half the normal voltage swing. With no termination at the end of the trace, when the signal reaches the end, it is reflected back to the driver with a reflection coefficient of +1. The devices at the end of the line will see a normal signal swing and the reflection from the open ended line will be absorbed at the driver.

If there is a device attached half way down a long trace, then there is the possibility that this device will see the signal rise to the threshold voltage where it will stay until the reflection from the end of the line gets back to this device. What is considered long depends on the rise time of the signal and the input frequency response of the device.

This effect can be seen in Figure 6.

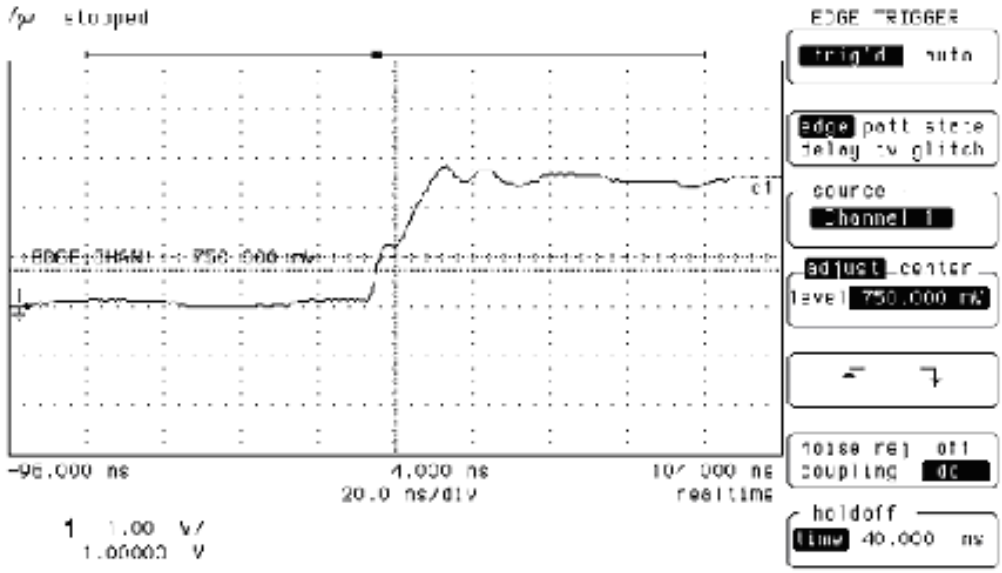


***Figure 6* • Midpoint at Point Source Terminated Net**

The cable lengths used in Figure 6 were exaggerated to show this effect. This picture used a three foot ribbon cable from a SMPA-ISP-ACTEL-1 socket module connected to a Header Converter with the normal 18 inch narrow ribbon cable to a buffer chip. The pause at threshold is clearly visible when looking at the Header Converter to simulate a device 18 inches from the end of the net.

Because of the slight impedance mismatch between the two cables and the effect of the Header Converter, the signal looks even worse at the input to the buffer (Figure 7). .

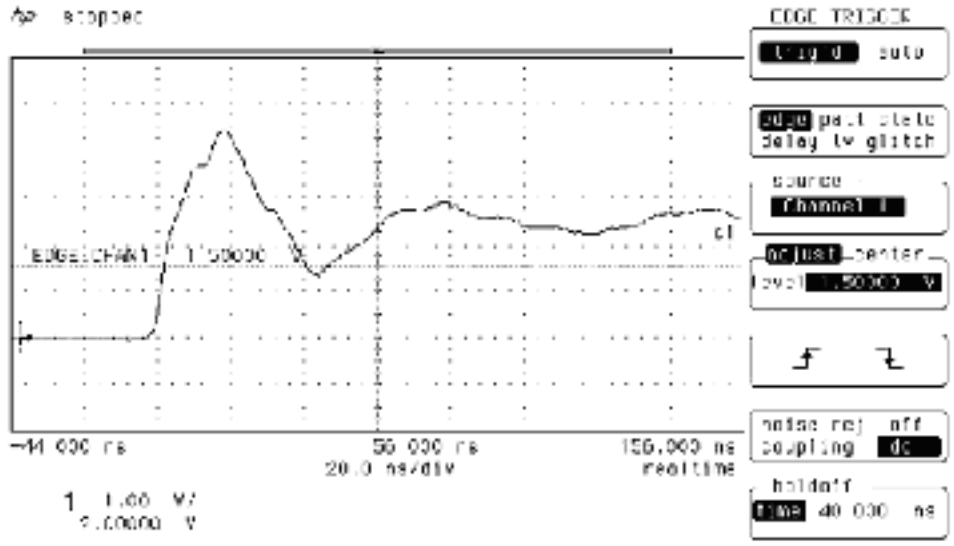


***Figure 7* • Buffer Input**

If this was the TCK input to a ProASIC device, it would cause double clocking and you would not be able to communicate with the device. The output of the buffer shows this false clock (Figure 8)..

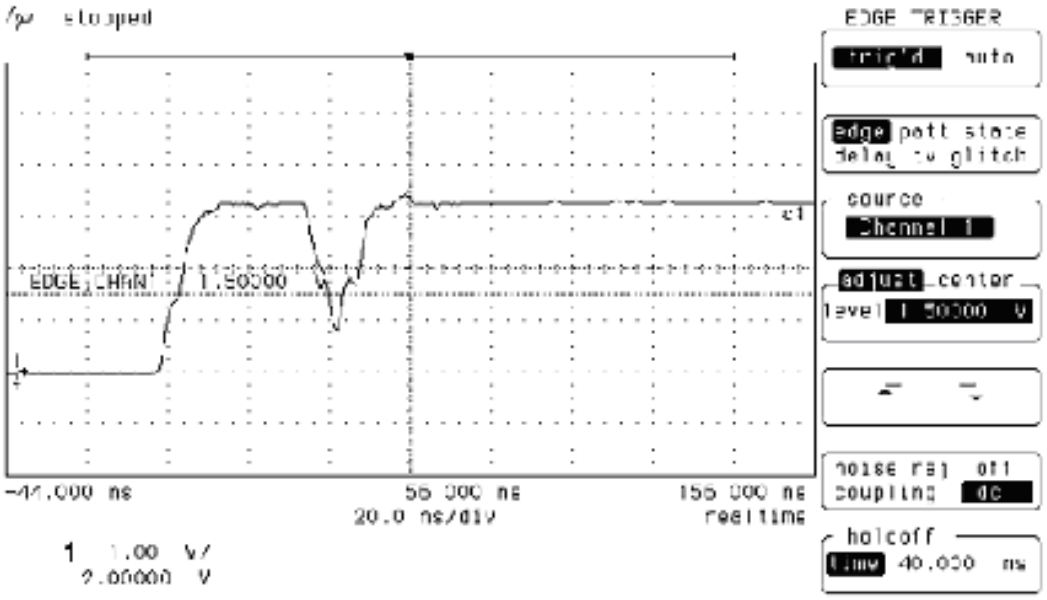


***Figure 8* • Buffer Output**

In these pictures it is easy to see the problem. Usually the problem is not so pronounced and it takes at least a 500 MHz bandwidth oscilloscope to see the evidence.

The scope trace in Figure 9 shows signs of overshoot, but unless you look closely you will miss the double clocking that it has captured. The original waveform is shown on the left side in Figure 9. On the right is a magnified image of the waveform as it crosses threshold.

The circled area shows where double clocking may be occurring.

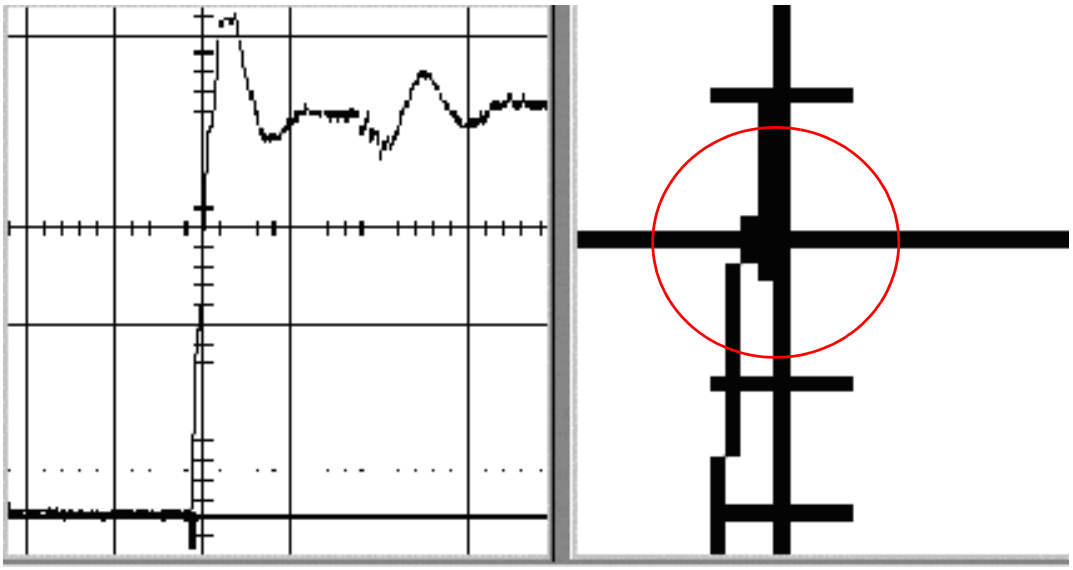


***Figure 9* • Threshold Glitch**

Whether this reflection will cause double clocking depends on the threshold voltage of this input as well as the frequency response of the input. Both of these parameters will vary from device to device, so what works with one device on a prototype board might not always work in production when variations in board impedance are also involved. Even with a single board, replacing the device may cause a working board to fail programming just because the new device has a slightly different threshold voltage. The solution is to improve the signal integrity of the nets, eliminate impedance discontinuities, and terminate the clock lines.

Another signal integrity consideration is limiting the length of parallel traces. This helps to keep crosstalk between traces to a minimum. Refer to the "References" section on page 17 for more information on crosstalk.

Programming Header

During programming, the programmer will be controlling all the power supplies (VDDL, VDDP, VPP, VPN) of the ProASIC 500K device. Note: We do not want the programmer to control the PCB board power supplies. To prevent this from happening, Microsemi recommends connecting the board power supplies to the left side of the programming header, the programmer connections to the right side of the programming header, thereby separating the power to the ProASIC device from the rest of the PCB. After successful programming, a plug-in header is put onto the programming header, allowing power from the PCB board to reach the ProASIC device (Figure 4 on page 8).

ProASIC devices also use the JTAG (IEEE Standard 1149.1 1990) pins TCK, TMS, TDI, and TDO for programming. The TRST pin, an optional JTAG pin, is not used during programming, but it must remain high during programming. This can be done from FlashPro software. For Silicon Sculptor, the RCK pin is also required during programming; it is not required for FlashPro.

Figure 10 and Figure 11 show a programming header on a PCB and how it connects to a programmer.

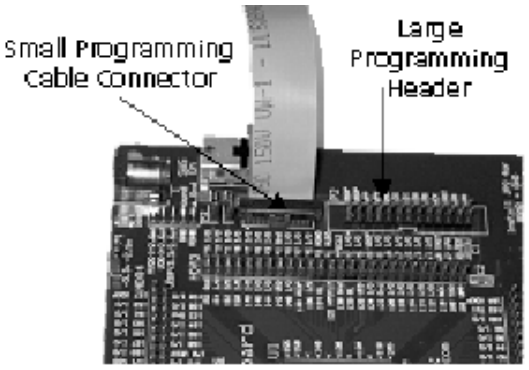


***Figure 10* • Using Small Cable Connector**

FlashPro and FlashPro Lite programmers are designed to use the small programming header. If you are using either programmer, it is recommended that you use the small programming header on your target board. If you are using the large programming header on your target board, you are required to use a header converter with your programmer (refer to Table 3 on page 15 for part numbers.)

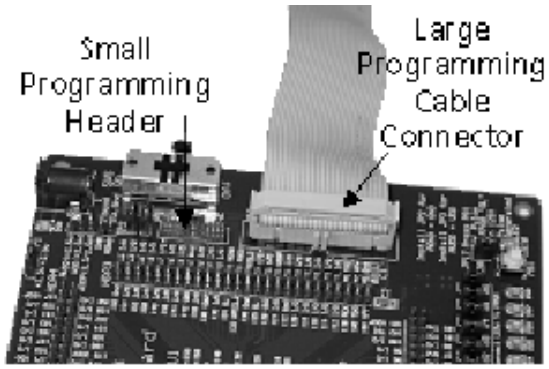


***Figure 11* • using Large Cable Connector**

ISP programming can also be done with the Silicon Sculptor I or II programmers. When using the SMPAISP-ACTEL-1 Sculptor socket module, you should use the wide 26 pin programming header on your board because it is the only connector supported by the ISP-1 socket module. When using the SMPA-ISP-ACTEL-2 or SMPA-ISP-ACTEL-3 Sculptor socket module2, you can use either the wide or the narrow 26 pin programming header on your board because both connectors are supported by the ISP-2 and ISP-3 socket modules.

General Programming Information

Microsemi recommends checking the device ID on the ISP board design before programming a device by reading the device ID from the device using Silicon Sculptor II or FlashPro. If there is a problem, the programmer will fail with a "bad IDCODE" error message. If the reason for the failure cannot be found in the connection with the circuitry or the programming voltages, it is possible that the failure was caused by noise on the TCK or RCK signals.

It is important to take all noise precautions into account for the TCK and RCK signals. Before programming a device, check the following:

- Make sure that the "1" level of all signals driving the device is within ±0.8V of VDDP
- Make sure that all ESD protection measures are taken

- Make sure only ProASIC parts are connected to the switching voltage supplies
- Make sure not to interrupt the programming

Header Converter

Microsemi also provides a header converter (Microsemi Part Number: Header-Converter) that enables the FlashPro programmer to be used with the older 100 mil spacing header. The header converter also provides an 8-pin connection from the programmer to the board, further reducing the board space required to perform ISP. This should only be used when space is critical because this could increase the chance of noise and failed programming (Table 2).If an 8-pin cable is used, a shorter cable will give better signal integrity..

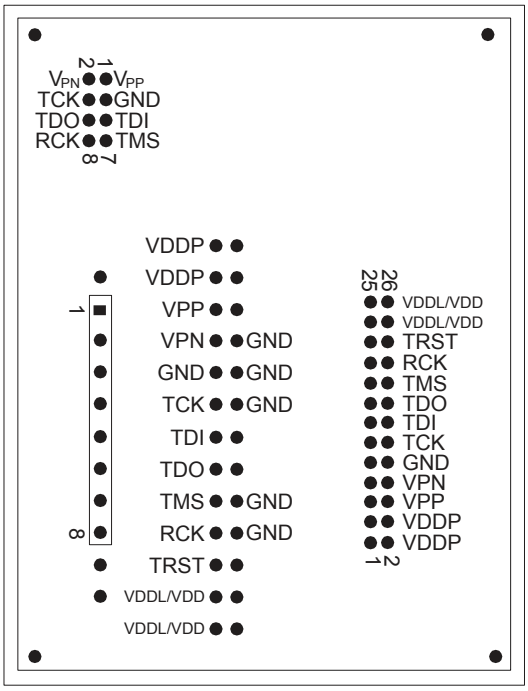


Figure 12 • **Head Converter Assembly**

Table 2 lists the pin numbers and names for Figure 12.

Table 2 • **Pin Numbers and Names**

Pin Number	Pin Name
1	VPP
2	VPN
3	GND
4	TCK
5	TDI
6	TDO
7	TMS
8	RCK

Table 3 • **Programmer Ordering Codes**

Description	Vendor	Ordering Code	Comment
FlashPro ISP Programmer	Microsemi	FlashPro	Supports Small Programming Header or Large Header through Header Converter (not included)
Silicon Sculptor II	Microsemi	SILICON-SCULPTOR II	Requires add on Adapter Modules to support devices
Silicon Sculptor ISP Module	Microsemi	SMPA-ISP-ACTEL-2-KIT	Ships with both Large and Small Header Support
Concurrent Programming Cable	Microsemi	SS-EXPANDER	Used to cascade multiple Silicon Sculptors together
Software for Silicon Sculptor	Microsemi	SCULPTOR-SOFTWARE-CD	http://www.microsemi.com/soc/custsup/updates/silisculpt/ index.html
ISP Cable for Small Header	Microsemi	ISP-CABLE-S	Supplied with ISP Module Kit
ISP Cable for Large Header	Microsemi	PA-ISP-CABLE	Supplied with ISP Module Kit
Header Converter	Microsemi	Header-Converter	Converts from Small to Large Header
Small Programming Header	Samtec	FTSH-113-01-L-D-K	Supported by FlashPro and Silicon Sculptor
Large Programming Header 0.062 Board Thickness	3M	3429-6502	Supported by Silicon Sculptor by default and FlashPro with Header Converter
Large Programming Header 0.094-0.125 Board Thickness	3M	3429-6503	Supported by Silicon Sculptor by default and FlashPro with Header Converter
Plug in Header Small	Microsemi	SMPA-ISP-HEADER-S	Required for Small Header for ProASIC only, not used for ProASIC
Plug-in Header	Microsemi	SMPA-ISP-HEADER	Required for Large Header for ProASIC only, not used for ProASIC
Vacuum Pen for PQ, TQ, VQ fewer than 208 pins	Microsemi	PENVAC	
Vacuum Pen for PQ, TQ, VQ greater/equal to 208 pins	Microsemi	PENVAC-HD	
Small Programming Header	SamTec	FTSH-113-01-L-DV-K	Surface mount header with vertical pins. This header could be used due to board thickness issues. Customer needs to consider the physical stress specs accordingly
Small Programming Header	Samtec	FTSH-113-01-L-DH-K	Surface mount header with horizontal pins. This header could be used due to board thickness issue. Customer needs to consider the physical stress specs accordingly

Related Documents

For more information about Programming with ProASIC devices, please refer to the following documents:

- IEEE 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- *Designer User's Guide*

Silicon Sculptor II

The following website provides a description of both Silicon Sculptor I and II:

http://www.microsemi.com/products/tools/silisculpt/index.html.

Silicon Sculptor User Guides

Windows User's Guide:

http://www.microsemi.com/soc/documents/SiliSculptII_WIN_UG.pdf

DOS User's Guide:

http://www.microsemi.com/soc/documents/sculptor_DOS_UG.pdf

Self-Test Procedure for the Silicon Sculptor:

http://www.microsemi.com/soc/documents/SiliSculptProgCali_UG.pdf

ProASIC Daisy-Chain Programming:

http://www.microsemi.com/soc/documents/daisy_chain_UG.pdf

Includes hardware and software setup, calibration, use instructions, and troubleshooting/error message guide.

FlashPro User’s Guides

To find detailed information about FlashPro, go to:

http://www.microsemi.com/soc/products/tools/flashpro/index.html

http://www.microsemi.com/soc/documents/flashpro_UG.pdf

Includes hardware and software setup, self-test instructions, use instructions, and a troubleshooting/error message guide.

Application Notes

Performing Internal In-System Programming Using Microsemi's ProASIC^{PLUS} Devices:

http://www.microsemi.com/soc/documents/APA_Microprocessor_AN.pdf

Contains a description of how to use an on-board processor to perform ISP.

Implementation of Security in Microsemi's ProASIC and ProASIC^{PLUS} flash-based FPGAs:

http://www.microsemi.com/soc/documents/Flash_Security_AN.pdf

Describes the different types of security available in Flash devices and how to implement the security.

References

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High-Speed Digital Design, A Handbook of Black Magic, Johnson, H.W. & M.Graham, PTR Prentice Hall, Englewood Cliffs, NJ 1993 Prentice Hall, 1993; ISBN 0-13-395724-1

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Termination Placement in PCB Design, Douglas Brooks, UltraCAD Design Inc. Available from Mentor Graphics:

http://www.mentor.com/pcb/tech_papers.cfm under heading High-Speed Design

Transmission Line Terminations, It's The End That Counts!, Douglas Brooks, UltraCAD Design Inc. Available from Mentor Graphics:

http://www.mentor.com/pcb/tech_papers.cfm under heading High- Speed Design.

List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 1 (October 2011)	Modified the "What is RCK and Why Is it Needed for Internal ISP?" section for SAR 27851.	6

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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