2Gb NAND FLASH (x16) / 1Gb LPDDR (x32)

FEATURES

- Package:
  - 152 Plastic Ball Grid Array (PBGA), 14 x 14 mm
  - 0.65 mm pitch
- Micron® NAND Flash and LPDDR components
- RoHS-compliant, “green” package
- Separate NAND Flash and LPDDR interfaces
- Space-saving multichip package/package-on-package combination
- Low-voltage operation (1.8V)
- Commercial and industrial temperature ranges
- Same footprint as Micron MT29C2G24MAKLA-XIT

NAND Flash-Specific Features

Organization

- Page size
  - x16: 1056 words (1024 + 32 words)
- Block size: 64 pages (128K + 4K bytes)

Mobile LPDDR-Specific Features

- No external voltage reference required
- No minimum clock rate requirement
- 1.8V LVCMOS-compatible inputs
- Programmable burst lengths
- Partial-array self refresh (PASR)
- Deep power-down (DPD) mode
- Status read register (SRR)
- Selectable output drive strength

* This product is under development, is not qualified or characterized and is subject to change without notice.

GENERAL DESCRIPTION

Microsemi package-on-package (PoP) MCP products combine NAND Flash and Mobile LPDRAM devices in a single MCP. These products target mobile applications with low-power, high-performance, and minimal package-footprint design requirements.

The NAND Flash and Mobile LPDRAM devices are packaged with separate interfaces (no shared address, control, data, or power balls). This bus architecture supports an optimized interface to processors with separate NAND Flash and Mobile LPDRAM buses. The NAND Flash and Mobile LPDRAM devices have separate core power connections and share a common ground (that is, V_{SS} is tied together on the two devices).

The bus architecture of this device also supports separate NAND Flash and Mobile LPDRAM functionality without concern for device interaction.

Microsemi NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#).

This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign.

A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal.

This device has an internal 4-bit ECC that can be enabled using the GET/SET features. See Internal ECC and Spare Area Mapping for ECC for more information.

The 1Gb Mobile low-power DDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 1,073,741,824. It is internally configured as a quad-bank DRAM. Each of the x32’s 268M-bit banks is organized as 8,192 rows by 1024 columns by 32 bits. In the reduced page-size (LG) option, each of the x32's 268M-bit banks is organized as 16,384 rows by 512 columns by 32 bits.

For a more detailed data sheet on operations and specifications; contact factory.

NOTES:

1. Throughout this data sheet, various figures and text refer to DQs as “DQ.” DQ should be interpreted as any and all DQ collectively, unless specifically stated otherwise. Additionally, the x16 is divided into 2 bytes: the lower byte and the upper byte. For the lower byte (DQ[7:0]), DM refers to LDM and DQS refers to LDQS. For the upper byte (DQ[15:8]), DM refers to UDM and DQS refers to UDQS. The x32 is divided into 4 bytes. For DQ[7:0], DM refers to DM0 and DQS refers to DQS0. For DQ[15:8], DM refers to DM1 and DQS refers to DQS1. For DQ[23:16], DM refers to DM2 and DQS refers to DQS2. For DQ[31:24], DM refers to DM3 and DQS refers to DQS3.
2. Complete functionality is described throughout the document; any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.
3. Any specific requirement takes precedence over a general statement.

FIGURE 1 – PIN CONFIGURATION

TOP VIEW

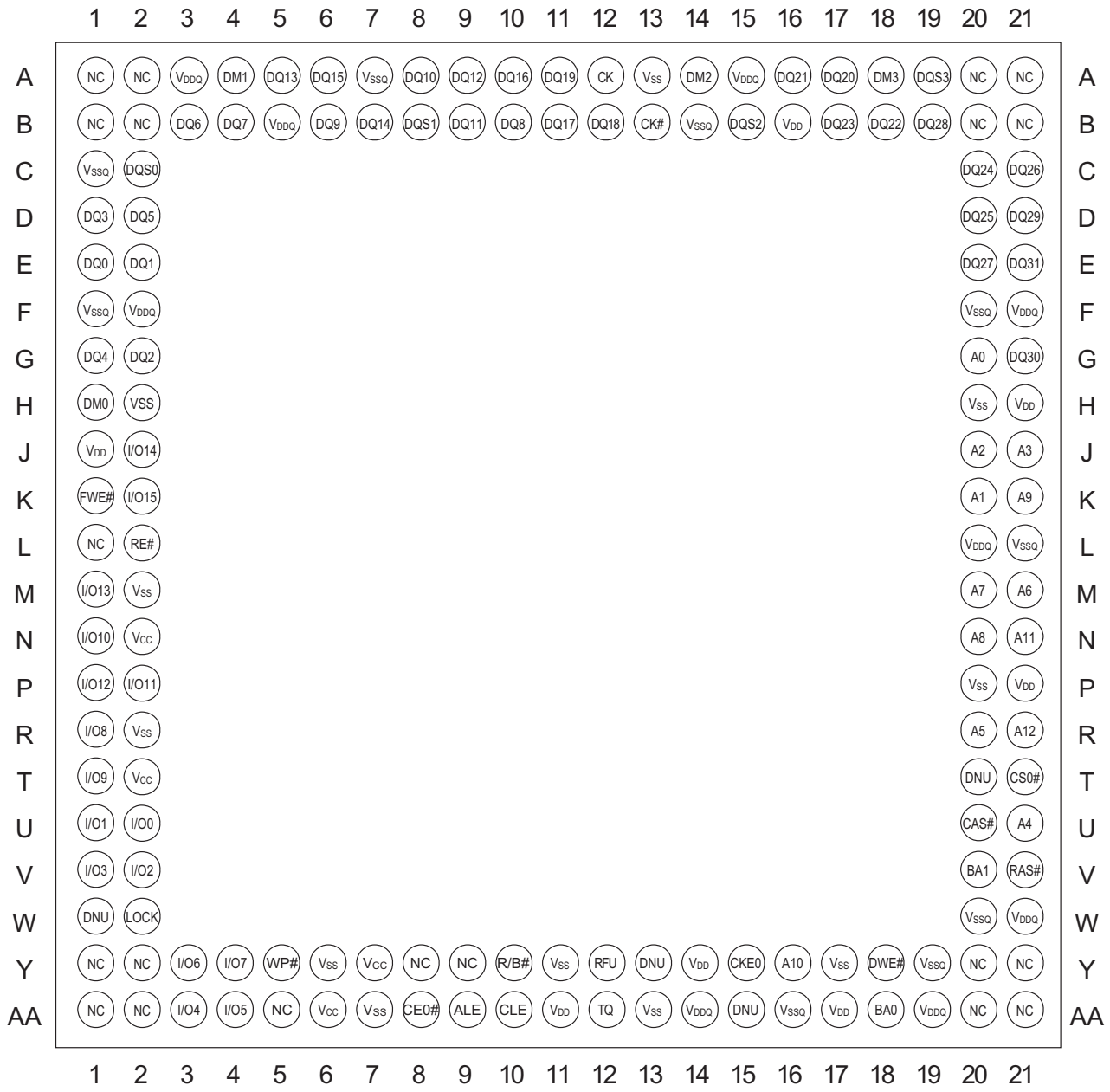
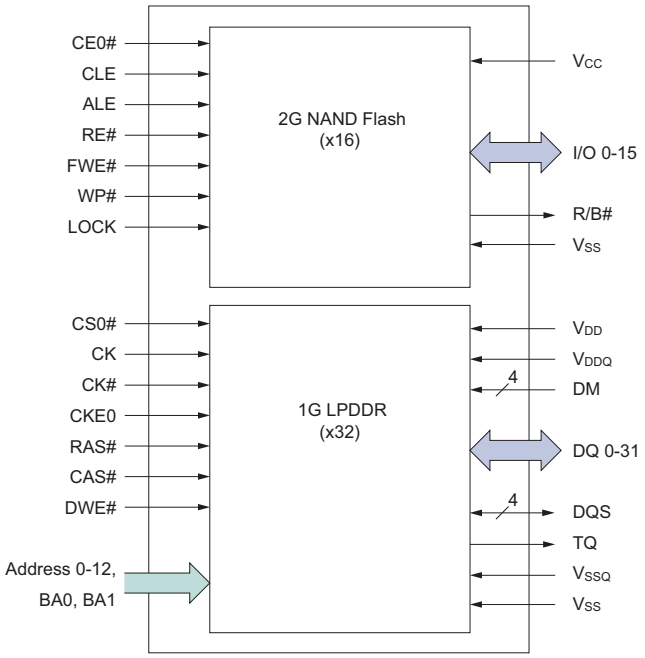


FIGURE 2 – 152-BALL (SINGLE LPDDR) FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

TABLE 1 – ABSOLUTE MAXIMUM RATINGS

Parameters/Conditions	Symbol	Min	Max	Unit
V_{CC}, V_{DD}, V_{DDQ} supply voltage relative to V_{SS}	V_{CC}, V_{DD}, V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (supply voltage[1] + 0.3V), whichever is less	V
Storage temperature range	–	–40	+125	°C

Note: 1. Supply voltage references V_{CC}, V_{DD}, or V_{DDQ}.

Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 2 – RECOMMENDED OPERATING CONDITIONS

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}, V_{DD}	1.70	1.80	1.95	V
I/O supply voltage	V_{DDQ}	1.70	1.80	1.95	V
Operating temperature range	—	–40	—	+85	°C

TABLE 3 – x16 NAND BALL DESCRIPTIONS

Symbol	Type	Description
ALE	Input	Address latch enable: When ALE is HIGH, addresses can be transferred to the on-chip address register.
CE0#	Input	Chip enable: Gates transfers between the host system and the NAND device.
CLE	Input	Command latch enable: When CLE is HIGH, commands can be transferred to the on-chip command register.
LOCK	Input	When LOCK is HIGH during power-up, the BLOCK LOCK function is enabled. To disable BLOCK LOCK, connect LOCK to V_{SS} during power-up, or leave it unconnected (internal pull-down).
RE#	Input	Read enable: Gates information from the NAND device to the host system.
FWE#	Input	Write enable: Gates information from the host system to the NAND device.
WP#	Input	Write protect: Driving WP# LOW blocks ERASE and PROGRAM operations.
I/O[15:0]	Input/output	Data inputs/outputs: The bidirectional I/Os transfer address, data, and instruction information. Data is output only during READ operations; at other times the I/Os are inputs.
R/B#	Output	Ready/busy: Open-drain, active-LOW output that indicates when an internal operation is in progress.
V_{CC}	Supply	V_{CC}: NAND power supply.

TABLE 4 – x32 LPDDR BALL DESCRIPTIONS

Symbol	Type	Description
A[12:0]	Input	Address inputs: Specifies the row or column address. Also used to load the mode registers. The maximum LPDDR address is determined by density and configuration.
BA0, BA1	Input	Bank address inputs: Specifies one of the 4 banks.
CAS#	Input	Column select: Specifies which command to execute.
CK, CK#	Input	CK is the system clock. CK and CK# are differential clock inputs. All address and control signals are sampled and referenced on the crossing of the rising edge of CK with the falling edge of CK#.
CKE0	Input	Clock enable: CKE0 is used for a single LPDDR product.
CS0#	Input	Chip select: CS0# is used for a single LPDDR product.
DM[3:0]	Input	Data mask: Determines which bytes are written during WRITE operations.
RAS#	Input	Row select: Specifies the command to execute.
DWE#	Input	Write enable: Specifies the command to execute.
DQ[31:0]	Input/output	Data bus: Data inputs/outputs.
DQS[3:0]	Input/output	Data strobe: Coordinates READ/WRITE transfers of data; one DQS per DQ byte.
TQ	Output	Temperature sensor output: TQ HIGH when LPDDR TJ exceeds 85°C.
V_{DD}	Supply	V_{DD}: LPDDR power supply.
V_{DDQ}	Supply	V_{DDQ}: LPDDR I/O power supply.
VSSQ	Supply	V_{SSQ}: LPDDR I/O ground.

TABLE 3 – NON-DEVICE-SPECIFIC DESCRIPTIONS

Symbol	Type	Description
V_{SS}	Supply	V_{SS}: Shared ground.
DNU	—	Do not use
NC	—	No connect: Not internally connected.
RFU[1]	—	Reserved for future use.

Note: 1. Balls marked RFU may or may not be connected internally. These balls should not be used. Contact factory for details.

2Gb: x16 NAND FLASH MEMORY – 1.8V

FEATURES

- Open NAND Flash Interface (ONFI) 1.0-compliant[1]
- Single-level cell (SLC) technology
- Organization
  - Page size x16: 1056 words (1024 + 32 words)
  - Block size: 64 pages (128K + 4K bytes)
  - Device size: 2Gb: 2048 blocks
- Asynchronous I/O performance
  - t_{RC}/t_{WC}: 35ns
- Array performance
  - Read page: 25µs
  - Program page: 300µs (TYP)
  - Erase block: 500µs (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
  - Program cache
  - Read cache sequential
  - Read cache random
  - One-time programmable (OTP) mode
  - Programmable drive strength
  - Interleaved die (LUN) operations
  - Read unique ID
  - Block lock
  - Internal data move
- Operation status byte provides software method for detecting
  - Operation completion
  - Pass/fail condition
  - Write-protect status
- Internal data move operations supported within the device from which data is read
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First blocks (block address 00h) is valid when shipped from factory with ECC; for minimum required ECC, see Error Management
- RESET (FFh) required as first command after power-on
- Quality and reliability
  - Data retention: 10 years
- Endurance: 100,000 program/erase cycles
- Operating voltage range
  - V_{CC}: 1.7–1.95V
- Operating temperature
  - Commercial: 0°C to +70°C
  - Industrial (IT): –40ºC to +85ºC

NOTES:
1. The ONFI 1.0 specification is available at www.onfi.org.

NAND FLASH ELECTRICAL SPECIFICATIONS

Stresses greater than those listed can cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not guaranteed. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

TABLE 6 – ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}

Parameter/Condition	Symbol	Min	Max	Unit
Voltage Input	V_{IN}	–0.6	+2.4	V
V_{CC} supply voltage	V_{CC}	–0.6	+2.4	V
Storage temperature	T_{STG}	–65	+150	°C
Short circuit output current, I/Os	–	–	5	mA

TABLE 7 – RECOMMENDED OPERATING CONDITIONS

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	+70	°C
	Industrial		–40	–	+85	°C
V_{CC} supply voltage		V_{CC}	1.65	1.8	1.95	V
Ground supply voltage		V_{SS}	0	0	0	V

TABLE 8 – VALID BLOCKS

Parameter	Symbol	Device	Min	Max	Unit	Notes
Valid block number	NVB	2G	2008	2048	blocks	1, 2

NOTES:

1. Invalid blocks are blocks that contain one or more bad bits. The device may contain bad blocks upon shipment. Additional bad blocks may develop over time; however, the total number of available blocks will not drop below NVB during the endurance life of the device. Do not erase or program blocks marked invalid by the factory.
2. Block 00h (the first block) is guaranteed to be valid with ECC when shipped from the factory.

TABLE 9 – CAPACITANCE

Description	Symbol	Max	Unit	Notes
Input capacitance	C_{IN}	10	pF	1, 2
Input/output capacitance (I/O)	C_{IO}	10	pF	1, 2

NOTES:

1. These parameters are verified in device characterization and are not tested.
2. Test conditions: TC = 25°C; f = 1 MHz; Vin = 0V.

TABLE 10 – TEST CONDITIONS

Parameter	Device	Value	Notes
Input pulse levels	2G	0.0V to V_{CC}	
Input rise and fall times		5ns	
Input and output timing levels		$V_{CC/2}$	
Output load		1 TTL GATE and CL = 30pF	1

NOTE:

1. Verified in device characterization, not tested.

NAND FLASH ELECTRICAL SPECIFICATIONS – AC CHARACTERISTICS AND OPERATING CONDITIONS

TABLE 11 – AC CHARACTERISTICS: COMMAND, DATA, AND ADDRESS INPUT

Parameter	Symbol	Min	Max	Unit	Notes
ALE to data start	t_{ADL}	100	–	ns	1
ALE hold time	t_{ALH}	4	–	ns	
ALE setup time	t_{ALS}	15	–	ns	
CE# hold time	t_{CH}	4	–	ns	
CLE hold time	t_{CLH}	5	–	ns	
CLE setup time	t_{CLS}	15	–	ns	
CE# setup time	t_{CS}	24	–	ns	
Data hold time	t_{DH}	4	–	ns	
Data setup time	t_{DS}	15	–	ns	
WRITE cycle time	t_{WC}	35	–	ns	
WE# pulse width HIGH	t_{WH}	15	–	ns	
WE# pulse width	t_{WP}	17	–	ns	
WP# setup time	t_{WW}	100	–	ns	

NOTE:
1. Timing for tADL begins in the address cycle on the final rising edge of WE# and ends with the first rising edge of WE# for data input.

TABLE 12 – AC CHARACTERISTICS: NORMAL OPERATION

Note 1 applies to all

Parameter	Symbol	Min	Max	Unit	Notes
ALE to RE# delay	t_{AR}	10	–	ns	
CE# access time	t_{CEA}	–	30	ns	
CE# HIGH to output High-Z	t_{CHZ}	–	45	ns	2
CLE to RE# delay	t_{CLR}	10	–	ns	
CE# HIGH to output hold	t_{COH}	15	–	ns	
Output High-Z to RE# LOW	t_{IR}	0	–	ns	
READ cycle time	t_{RC}	35	–	ns	
RE# access time	t_{REA}	–	24	ns	
RE# HIGH hold time	t_{REH}	15	–	ns	
RE# HIGH to output hold	t_{RHOH}	15	–	ns	
RE# HIGH to WE# LOW	t_{RHW}	100	–	ns	
RE# HIGH to output High-Z	t_{RHZ}	–	100	ns	2
RE# LOW to output hold	t_{RLOH}	0	–	ns	
RE# pulse width	t_{RP}	17	–	ns	
Ready to RE# LOW	t_{RR}	20	–	ns	
Reset time (READ/PROGRAM/ERASE)	t_{RST}	–	5/10/500	µs	3
WE# HIGH to busy	t_{WB}	–	100	ns	4
WE# HIGH to RE# LOW	t_{WHR}	80	–	ns	

NOTES:
1. AC characteristics may need to be relaxed if I/O drive strength is not set to full.
2. Transition is measured ±200mV from steady-state voltage with load. This parameter is not tested.
3. The first time the RESET (FFh) command is issued while the device is idle, the device will be busy for a maximum of 1ms. Thereafter, the device will be busy for maximum 5µs.
4. Do not issue a new command during t_{WB}, even if R/B# is ready.

NAND FLASH ELECTRICAL SPECIFICATIONS – DC CHARACTERISTICS AND OPERATING CONDITIONS (cont'd)

TABLE 12 – DC CHARACTERISTICS AND OPERATING CONDITIONS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	Notes
Sequential READ current	$t_{RC} = t_{RC\ (MIN)}$; CE# = V_{IL}; I_{OUT} = 0mA	I_{CC1}	–	10	20	mA	
PROGRAM current	–	I_{CC2}	–	10	20	mA	
ERASE current	–	I_{CC3}	–	10	20	mA	
Standby current (TTL)	CE# = V_{IH}; LOCK = WP# = 0V/V_{CC}	I_{SB1}	–	–	1	mA	
Standby current (CMOS)	CE# = V_{CC} - 0.2V; LOCK = WP# = 0V/V_{CC}	I_{SB2}	–	10	50	µA	
Staggered power-up current	Rise time = 1ms Line capacitance = 0.1µF	I_{ST}	–	–	10 per die	mA	1
Input leakage current	V_{IN} = 0V to V_{CC}	I_{LI}	–	–	±10	µA	
Output leakage current	V_{OUT} = 0V to V_{CC}	I_{LO}	–	–	±10	µA	
Input high voltage	I/O[15:0], CE#, CLE, ALE, WE#, RE#,WP#, R/B#	V_{IH}	0.8 x V_{CC}	–	V_{CC} + 0.3	V	
Input low voltage, all inputs	–	V_{IL}	–0.3	–	0.2 x V_{CC}	V	
Output high voltage	I_{OH} = –100µA	V_{OH}	V_{CC} – 0.1	–	–	V	2
Output low voltage	I_{OL} = –100µA	V_{OL}	–	–	0.1	V	2
Output low current	V_{OL} = 0.4V	$I_{OL\ (R/B\#)}$	3	4	–	mA	3

NOTES:
1. Measurement is taken with 1ms averaging intervals and begins after V_{CC} reaches $V_{CC\ (MIN)}$.
2. V_{OH} and V_{OL} may need to be relaxed if I/O drive strength is not set to full.
3. I_{OL} (RB#) may need to be relaxed if R/B pull-down strength is not set to full.

TABLE 13 – PROGRAM/ERASE CHARACTERISTICS

Parameter	Symbol	Typ	Max	Unit	Notes
Number of partial page programs	NOP	–	4	Cycles	1
BLOCK ERASE operation time	t_{BERS}	0.5	3	ms	
Busy time for PROGRAM CACHE operation (1.8V)	t_{CBSY}	3	600	µs	2
Busy time for SET FEATURES and GET FEATURES operations (1.8V)	t_{FEAT}	–	3	µs	
Busy time for PROGRAM/ERASE on locked block	t_{LBSY}	–	3	µs	
LAST PAGE PROGRAM operation time	t_{LPROG}	–	–	–	3
Busy time for OTP DATA PROGRAM operation if OTP is protected	t_{OBSY}	–	30	µs	
PAGE PROGRAM operation time (1.8V)	t_{PROG}	300	600	µs	
Data transfer from Flash array to data register	t_R	–	25	µs	
Busy time for READ CACHE operation	t_{RCBSY}	3	25	µs	

NOTES:
1. Four total partial-page programs to the same page.
2. t_{CBSY} MAX time depends on timing between internal program completion and data-in.
3. t_{LPROG} = t_{PROG} (last page) + t_{PROG} (last - 1 page) - command load time (last page) - address load time (last page) - data load time (last page).

FIGURE 3 – ARRAY ORGANIZATION

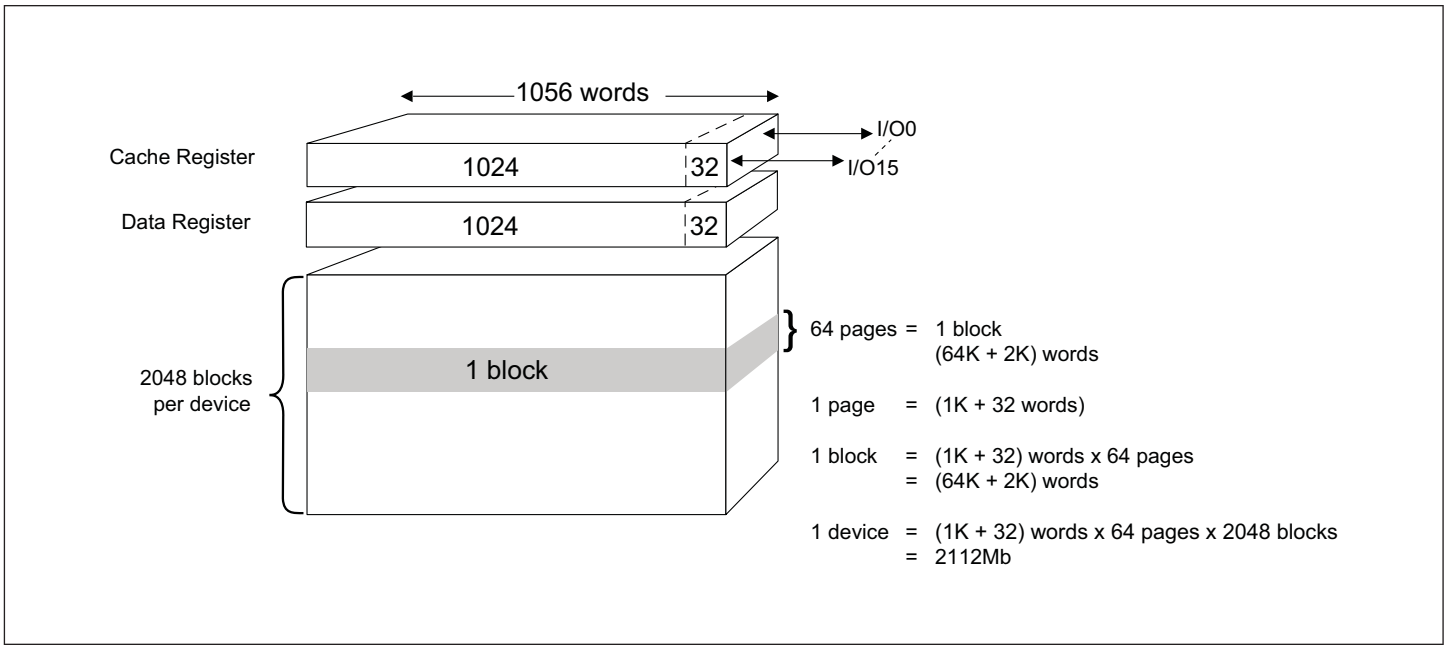


TABLE 14 – ARRAY ADDRESSING

Cycle	I/O[15:8]	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
First	LOW	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
Second	LOW	LOW	LOW	LOW	LOW	LOW	CA10[1]	CA9	CA8
Third	LOW	BA7	BA6	PA5	PA4	PA3	PA2	PA1	PA0
Fourth	LOW	BA15	BA14	BA13	BA12	BA11	BA10	BA9	BA8
Fifth	LOW	LOW	LOW	LOW	LOW	LOW	LOW	LOW	BA16

NOTES:
1. If CA10 is 1, then CA[9:5] must be 0.
2. Block address concatenated with page address = actual page address. CAx = column address; PAx = page address; BAx = block address.
3. I/O[15:8] are not used during the addressing sequence and should be driven LOW.

1Gb: x32 MOBILE LPDDR SDRAM

Features

- V_{DD}/V_{DDQ} = 1.8V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- 4 internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh and self refresh modes
- 1.8V LVCMOS-compatible inputs
- Partial-array self refresh (PASR)
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability
- 64ms refresh

TABLE 15 – CONFIGURATION ADDRESING – 1Gb

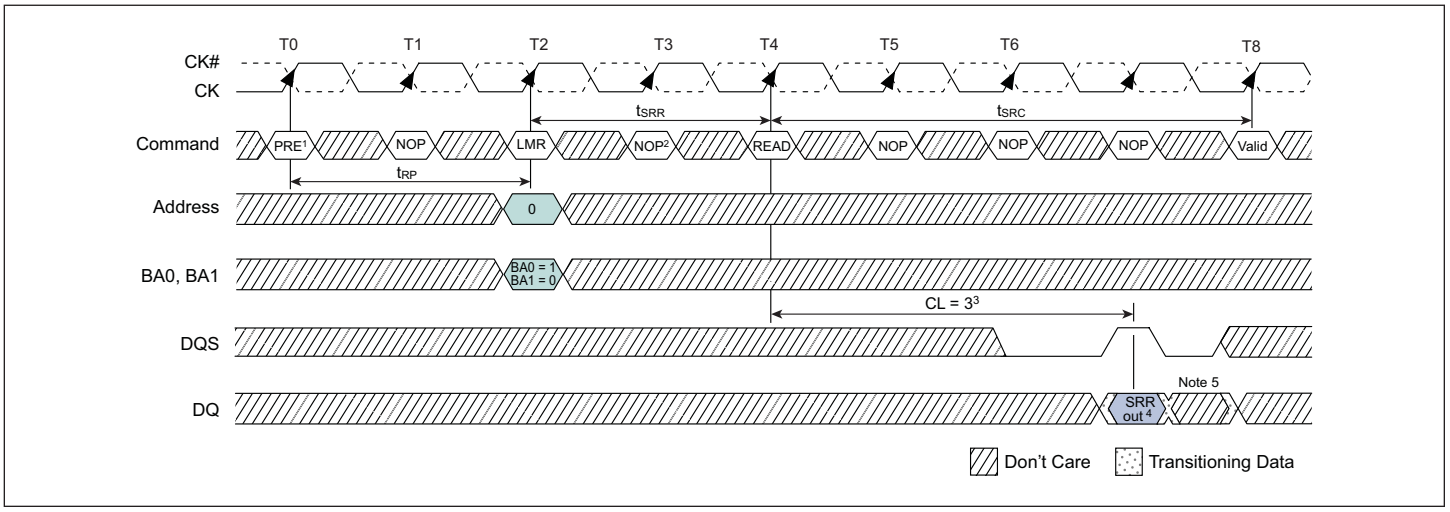
Architecture	32 Meg x 32
Configuration	8 Meg x 32 x 4 banks
Refresh count	8K
Row addressing	8K A[13:0]
Column addressing	1K A[9:0]

Status Read Register

The status read register (SRR) is used to read the manufacturer ID, revision ID, refresh multiplier, width type, and density of the device, as shown in Figure 4. The SRR is read via the LOAD MODE REGISTER command with BA0 = 1 and BA1 = 0. The sequence to perform an SRR command is as follows:

1. The device must be properly initialized and in the idle or all banks precharged state.
2. Issue a LOAD MODE REGISTER command with BA[1:0] = 01 and all address pins set to 0.
3. Wait t_{SRR}; only NOP or DESELECT commands are supported during the t_{SRR} time.
4. Issue a READ command.
5. Subsequent commands to the device must be issued t_{SRC} after the SRR READ command is issued; only NOP or DESELECT commands are supported during t_{SRC}. SRR output is read with a burst length of 2. SRR data is driven to the outputs on the first bit of the burst, with the output being “Don’t Care” on the second bit of the burst.

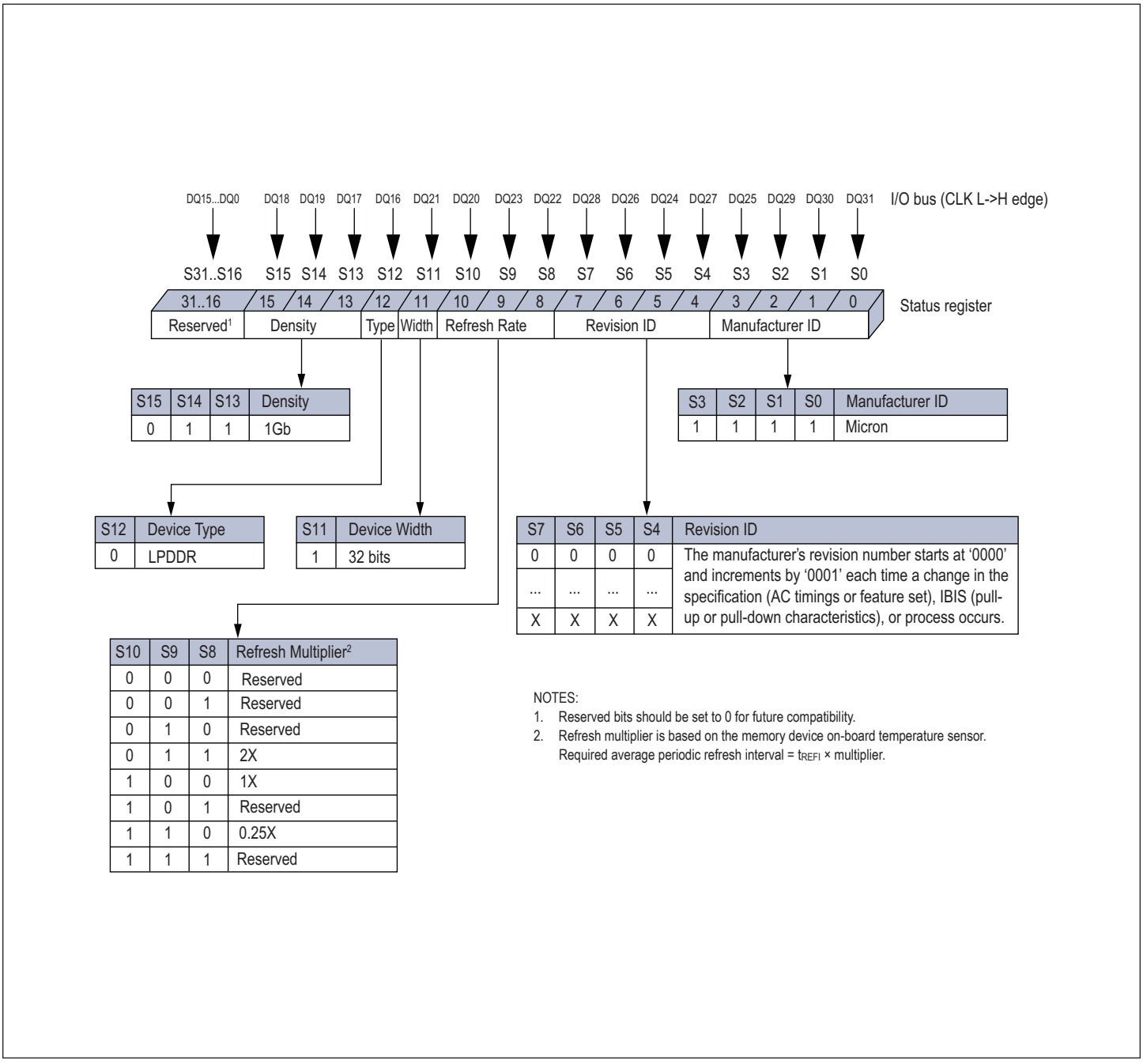
FIGURE 4 – STATUS READ REGISTER TIMING



Notes on next page.

NOTES for figure 4:
1. All banks must be idle prior to status register read.
2. NOP or DESELECT commands are required between the LMR and READ commands (t_{SRR}), and between the READ and the next VALID command (t_{SRC}).
3. CAS latency is predetermined by the programming of the mode register. CL = 3 is shown as an example only.
4. Burst length is fixed to 2 for SRR regardless of the value programmed by the mode register.
5. The second bit of the data-out burst is a "Don't Care."

Figure 5 – Status Register Definition



NOTES:
1. Reserved bits should be set to 0 for future compatibility.
2. Refresh multiplier is based on the memory device on-board temperature sensor. Required average periodic refresh interval = t_{REFI} × multiplier.

LPDDR ELECTRICAL SPECIFICATIONS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TABLE 16 – ABSOLUTE MAXIMUM RATINGS

Note 1 applies to all parameters in this table

Parameter	Symbol	Min	Max	Unit
V_{DD}/V_{DDQ} supply voltage relative to V_{SS}	V_{DD}/V_{DDQ}	–1.0	2.4	V
Voltage on any pin relative to V_{SS}	V_{IN}	–0.5	2.4 or (V_{DDQ} + 0.3V), whichever is less	V
Storage temperature (plastic)	T_{STG}	–55	150	˚C

NOTE: 1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

TABLE 17 – AC/DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Notes 1–5 apply to all parameters/conditions in this table; V_{CC}/V_{CCQ} = 1.70–1.95V

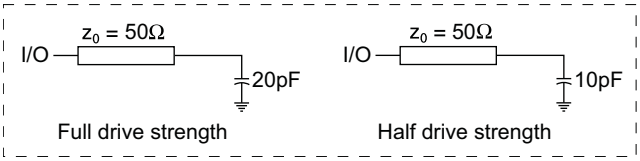
Parameter/Condition	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{DD}	1.70	1.95	V	6, 7
I/O supply voltage	V_{DDQ}	1.70	1.95	V	6, 7
Address and command inputs					
Input voltage high	V_{IH}	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9
Input voltage low	V_{IL}	–0.3	0.2 × V_{DDQ}	V	8, 9
Clock inputs (CK, CK#)					
DC input voltage	V_{IN}	–0.3	V_{DDQ} + 0.3	V	10
DC input differential voltage	$V_{ID(DC)}$	0.4 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC input differential voltage	$V_{ID(AC)}$	0.6 × V_{DDQ}	V_{DDQ} + 0.6	V	10, 11
AC differential crossing voltage	V_{IX}	0.4 × V_{DDQ}	0.6 × V_{DDQ}	V	10, 12
Data inputs					
DC input high voltage	$V_{IH(DC)}$	0.7 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
DC input low voltage	$V_{IL(DC)}$	–0.3	0.3 × V_{DDQ}	V	8, 9, 13
AC input high voltage	$V_{IH(AC)}$	0.8 × V_{DDQ}	V_{DDQ} + 0.3	V	8, 9, 13
AC input low voltage	$V_{IL(AC)}$	–0.3	0.2 × V_{DDQ}	V	8, 9, 13
Data outputs					
DC output high voltage: Logic 1 (I_{OH} = –0.1mA)	V_{OH}	0.9 × V_{DDQ}	–	V	
DC output low voltage: Logic 0 (I_{OL} = 0.1mA)	V_{OL}	–	0.1 × V_{DDQ}	V	
Leakage current					
Input leakage current Any input 0V ≤ V_{IN} ≤ V_{DD} (All other pins not under test = 0V)	I_I	–1	1	µA	
Output leakage current (DQ are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	–5	5	µA	
Operating temperature					
Commercial	TA	0	70	˚C	
Industrial	TA	–40	85	˚C	

Notes on next page

LPDDR ELECTRICAL SPECIFICATIONS (cont'd)

NOTES:

1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing, I_{CC}, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. Outputs measured with equivalent load; transmission line delay is assumed to be very small:



5. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
6. Any positive glitch must be less than one-third of the clock cycle and not more than +200mV or 2.0V, whichever is less. Any negative glitch must be less than one-third of the clock cycle and not exceed either –150mV or +1.6V, whichever is more positive.
7. V_{DD} and V_{DDQ} must track each other and V_{DDQ} must be less than or equal to V_{DD}.
8. To maintain a valid level, the transitioning edge of the input must:
   8a. Sustain a constant slew rate from the current AC level through to the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.
   8b. Reach at least the target AC level.
   8c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.
9. V_{IH} overshoot: $V_{IHmax} = V_{DDQ} + 1.0V$ for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate. V_{IL} undershoot: $V_{ILmin} = –1.0V$ for a pulse width ≤3ns and the pulse width cannot be greater than one-third of the cycle rate.
10. CK and CK# input slew rate must be ≥1 V/ns (2 V/ns if measured differentially).
11. V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
12. The value of V_{IX} is expected to equal $V_{DDQ/2}$ of the transmitting device and must track variations in the DC level of the same.
13. DQ and DM input slew rates must not deviate from DQS by more than 10%. 50ps must be added to t_{DS} and t_{DH} for each 100 mV/ns reduction in slew rate. If slew rate exceeds 4 V/ns, functionality is uncertain.

TABLE 18 – CAPACITANCE (X32)

Note 1 applies to all the parameters in this table

Parameter	Symbol	Min	Max	Unit	Notes
Input capacitance: CK, CK#	C_{CK}	1.5	3.0	pF	
Delta input capacitance: CK, CK#	C_{DCK}	–	0.25	pF	2
Input capacitance: command and address	C_I	1.5	3.0	pF	
Delta input capacitance: command and address	C_{DI}	–	0.5	pF	2
Input/output capacitance: DQ, DQS, DM	C_{IO}	1.5	4.5	pF	
Delta input/output capacitance: DQ, DQS, DM	C_{DIO}	–	0.5	pF	3

NOTES:

1. This parameter is guaranteed by design, not tested.
2. The input capacitance per pin group will not differ by more than this maximum amount for any given device.
3. The I/O capacitance per DQS and DQ byte/group will not differ by more than this maximum amount for any given device.

LPDDR ELECTRICAL SPECIFICATIONS – I_{DD} PARAMETERS

TABLE 19 – I_{DD} SPECIFICATIONS AND CONDITIONS

Notes 1–5 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Max				Unit	Notes
			-5	-54	-6	-75		
Operating 1 bank active precharge current: $t_{RC} = t_{RC\ (MIN)}$; $t_{CK} = t_{CK\ (MIN)}$; CKE is HIGH; CS is HIGH between valid commands; Address inputs are switching every 2 clock cycles; Data bus inputs are stable		I_{DD0}	110	105	100	70	mA	6
Precharge power-down standby current: All banks idle; CKE is LOW; CS is HIGH; $t_{CK} = t_{CK\ (MIN)}$; Address and control inputs are switching; Data bus inputs are stable		I_{DD2P}	600	600	600	600	µA	7, 8
Precharge power-down standby current: Clock stopped; All banks idle; CKE is LOW; CS is HIGH, CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2PS}	600	600	600	600	µA	7
Precharge nonpower-down standby current: All banks idle; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK\ (MIN)}$; Address and control inputs are switching; Data bus inputs are stable		I_{DD2N}	18	17	15	12	mA	9
Precharge nonpower-down standby current: Clock stopped; All banks idle; CKE = HIGH; CS = HIGH; CK = LOW, CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD2NS}	14	13	8	8	mA	9
Active power-down standby current: 1 bank active; CKE = LOW; CS = HIGH; $t_{CK} = t_{CK\ (MIN)}$; Address and control inputs are switching; Data bus inputs are stable		I_{DD3P}	3.6	3.6	3.6	3.6	mA	8
Active power-down standby current: Clock stopped; 1 bank active; CKE = LOW; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3PS}	3.6	3.6	3.6	3.6	mA	
Active nonpower-down standby: 1 bank active; CKE = HIGH; CS = HIGH; $t_{CK} = t_{CK\ (MIN)}$; Address and control inputs are switching; Data bus inputs are stable		I_{DD3N}	20	19	18	16	mA	6
Active nonpower-down standby: Clock stopped; 1 bank active; CKE = HIGH; CS = HIGH; CK = LOW; CK# = HIGH; Address and control inputs are switching; Data bus inputs are stable		I_{DD3NS}	16	15	14	12	mA	6
Operating burst read: 1 bank active; BL = 4; CL = 3; $t_{CK} = t_{CK\ (MIN)}$; Continuous READ bursts; Iout = 0mA; Address inputs are switching every 2 clock cycles; 50% data changing each burst		I_{DD4R}	150	145	140	120	mA	6
Operating burst write: One bank active; BL = 4; $t_{CK} = t_{CK\ (MIN)}$; Continuous WRITE bursts; Address inputs are switching; 50% data changing each burst		I_{DD4W}	150	145	140	120	mA	6
Auto refresh: Burst refresh; CKE = HIGH; Address and control inputs are switching; Data bus inputs are stable	t_{RFC} = 138ns	I_{DD5}	140	140	140	140	mA	10
	$t_{RFC} = t_{REFI}$	I_{DD5A}	15	15	15	14	mA	10, 11
Typical deep power-down current at 25°C: Address and control pins are stable; Data bus inputs are stable		I_{DD8}	10	10	10	10	µA	7, 13

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LPDDR ELECTRICAL SPECIFICATIONS – I_{DD} PARAMETERS (cont'd)

TABLE 20 – I_{DD6} SPECIFICATIONS AND CONDITIONS

Notes 1–5, 7, and 12 apply to all the parameters/conditions in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter/Condition		Symbol	Low Power	Standard	Units
Self refresh: CKE = LOW; t_{CK} = $t_{CK\ (MIN)}$; Address and control inputs are stable; Data bus inputs are stable	Full array, 85˚C	I_{DD6}	1000	1200	µA
	Full array, 45˚C		500	750	µA
	1/2 array, 85˚C		750	900	µA
	1/2 array, 45˚C		440	730	µA
	1/4 array, 85˚C		600	750	µA
	1/4 array, 45˚C		380	680	µA
	1/8 array, 85˚C		550	750	µA
	1/8 array, 45˚C		350	620	µA
	1/16 array, 85˚C		500	700	µA
	1/16 array, 45˚C		330	540	µA

NOTES:

1. All voltages referenced to V_{SS}.
2. Tests for I_{DD} characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
3. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ (or to the crossing point for CK/CK#). The output timing reference voltage level is $V_{DDQ/2}$.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
5. I_{DD} specifications are tested after the device is properly initialized and values are averaged at the defined cycle rate.
6. MIN (t_{RC} or t_{RFC}) for I_{DD} measurements is the smallest multiple of t_{CK} that meets the minimum absolute value for the respective parameter. t_{RASmax} for I_{DD} measurements is the largest multiple of t_{CK} that meets the maximum absolute value for t_{RAS}.
7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
8. V_{DD} must not vary more than 4% if CKE is not active while any bank is active.
9. I_{DD2N} specifies DQ, DQS, and DM to be driven to a valid high or low logic level.
10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until t_{RFC} later.
11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (t_{RFC} (MIN)) else CKE is LOW (for example, during standby).
12. Values for I_{DD6} 85˚C are guaranteed for the entire temperature range. All other I_{DD6} values are estimated.
13. Typical values at 25˚C, not a maximum value.

LPDDR ELECTRICAL SPECIFICATIONS – AC OPERATING CONDITIONS

TABLE 21 – ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Notes 1–9 apply to all the parameters in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter		Symbol	-5		-54		-6		-75		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Access window of DQ from CK/CK#	CL = 3	t_{AC}	2.0	5.0	2.0	5.0	2.0	5.5	2.0	6.0	ns	
	CL = 2		2.0	6.5	2.0	6.5	2.0	6.5	2.0	6.5		
Clock cycle time	CL = 3	t_{CK}	5.0	–	5.4	–	6	–	7.5	–	ns	10
	CL = 2		12	–	12	–	12	–	12	–		
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	t_{CK}	
CKE minimum pulse width (high and low)		t_{CKE}	1	–	1	–	1	–	1	–	t_{CK}	11
Auto precharge write recovery + precharge time		t_{DAL}	–	–	–	–	–	–	–	–	–	12
DQ and DM input hold time relative to DQS (fast slew rate)		t_{DHf}	0.6	–	0.6	–	0.6	–	0.8	–	ns	13, 14, 15
DQ and DM input hold time relative to DQS (slow slew rate)		t_{DHs}	0.7	–	0.7	–	0.7	–	0.9	–	ns	
DQ and DM input setup time relative to DQS (fast slew rate)		t_{DSf}	0.6	–	0.6	–	0.6	–	0.8	–	ns	13, 14, 15
DQ and DM input setup time relative to DQS (slow slew rate)		t_{DSs}	0.7	–	0.7	–	0.7	–	0.9	–	ns	
DQ and DM input pulse width (for each input)		t_{DIPW}	1.8	–	1.9	–	2.1	–	1.8	–	ns	16
Access window of DQS from CK/CK#	CL = 3	t_{DQSCK}	2.0	5.0	2.0	5.0	2.0	5.5	2.0	6.0	ns	
	CL = 2		2.0	6.5	2.0	6.5	2.0	6.5	2.0	6.5	ns	
DQS input high pulse width		t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS input low pulse width		t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
DQS–DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	–	0.4	–	0.45	–	0.45	–	0.6	ns	13, 17
WRITE command to first DQS latching transition		t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	
DQS falling edge from CK rising – hold time		t_{DSH}	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
DQS falling edge to CK rising – setup time		t_{DSS}	0.2	–	0.2	–	0.2	–	0.2	–	t_{CK}	
Data valid output window (DVW)		n/a	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns	17
Half-clock period		t_{HP}	t_{CH}, t_{CL}	–	t_{CH}, t_{CL}	–	t_{CH}, t_{CL}	–	t_{CH}, t_{CL}	–	ns	18
Data-out High-Z window from CK/ CK#	CL = 3	t_{HZ}	–	5.0	–	5.0	–	5.5	–	6.0	ns	19, 20
	CL = 2		–	6.5	–	6.5	–	6.5	–	6.5	ns	
Data-out Low-Z window from CK/CK#		t_{LZ}	1.0	–	1.0	–	1.0	–	1.0	–	ns	19
Address and control input hold time (fast slew rate)		t_{IHf}	0.9	–	1.0	–	1.1	–	1.3	–	ns	15, 21
Address and control input hold time (slow slew rate)		t_{IHs}	1.1	–	1.2	–	1.2	–	1.5	–	ns	
Address and control input setup time (fast slew rate)		t_{ISf}	0.9	–	1.0	–	1.1	–	1.3	–	ns	15, 21
Address and control input setup time (slow slew rate)		t_{ISs}	1.1	–	1.2	–	1.2	–	1.5	–	ns	
Address and control input pulse width		t_{IPW}	2.3	–	2.5	–	2.6	–	t_{IS} + t_{IH}	–	ns	16
LOAD MODE REGISTER command cycle time		t_{MRD}	2	–	2	–	2	–	2	–	t_{CK}	
DQ–DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}	t_{HP} - t_{QHS}	–	t_{HP} - t_{QHS}	–	t_{HP} - t_{QHS}	–	t_{HP} - t_{QHS}	–	ns	13, 17
Data hold skew factor		t_{QHS}	–	0.5	–	0.5	–	0.65	–	0.75	ns	
ACTIVE-to-PRECHARGE command		t_{RAS}	40	70,000	42	70,000	42	70,000	45	70,000	ns	22
ACTIVE to ACTIVE/ACTIVE to AUTO REFRESH command period		t_{RC}	55	–	58.2	–	60	–	67.5	–	ns	
Active to read or write delay		t_{RCD}	15	–	16.2	–	18	–	22.5	–	ns	
Refresh period		t_{REF}	–	64	–	64	–	64	–	64	ms	28

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LPDDR ELECTRICAL SPECIFICATIONS – AC OPERATING CONDITIONS (cont'd)

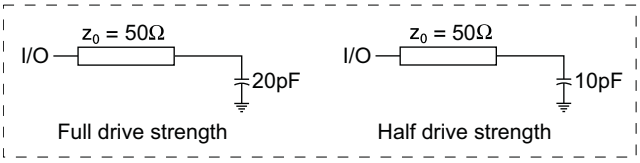
TABLE 22 – ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (cont'd)

Notes 1–9 apply to all the parameters in this table; V_{DD}/V_{DDQ} = 1.70–1.95V

Parameter		Symbol	-5		-54		-6		-75		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Average periodic refresh interval		t_{REFI}	–	7.8	–	7.8	–	7.8	–	7.8	µs	23
AUTO REFRESH command period		t_{RFC}	110	–	110	–	110	–	110	–	ns	
PRECHARGE command period		t_{RP}	15	–	16.2	–	18	–	22.5	–	ns	
DQS read preamble	CL = 3	t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}	
	CL = 2	t_{RPRE}	0.5	1.1	0.5	1.1	0.5	1.1	0.5	1.1	t_{CK}	
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	
Active bank a to active bank b command		t_{RRD}	10	–	10.8	–	12	–	15	–	ns	
Read of SRR to next valid command		t_{SRC}	CL + 1	–	CL + 1	–	CL + 1	–	CL + 1	–	t_{CK}	
SRR to read		t_{SRR}	2	–	2	–	2	–	2	–	t_{CK}	
DQS write preamble		t_{WPRE}	0.25	–	0.25	–	0.25	–	0.25	–	t_{CK}	
DQS write preamble setup time		t_{WPRES}	0	–	0	–	0	–	0	–	ns	24, 25
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	26
Write recovery time		t_{WR}	15	–	15	–	15	–	15	–	ns	27
Internal WRITE-to-READ command delay		t_{WTR}	2	–	2	–	1	–	1	–	t_{CK}	
Exit power-down mode to first valid command		t_{XP}	2	–	2	–	1	–	1	–	t_{CK}	
Exit self refresh to first valid command		t_{XSR}	112.5	–	112.5	–	112.5	–	112.5	–	ns	28

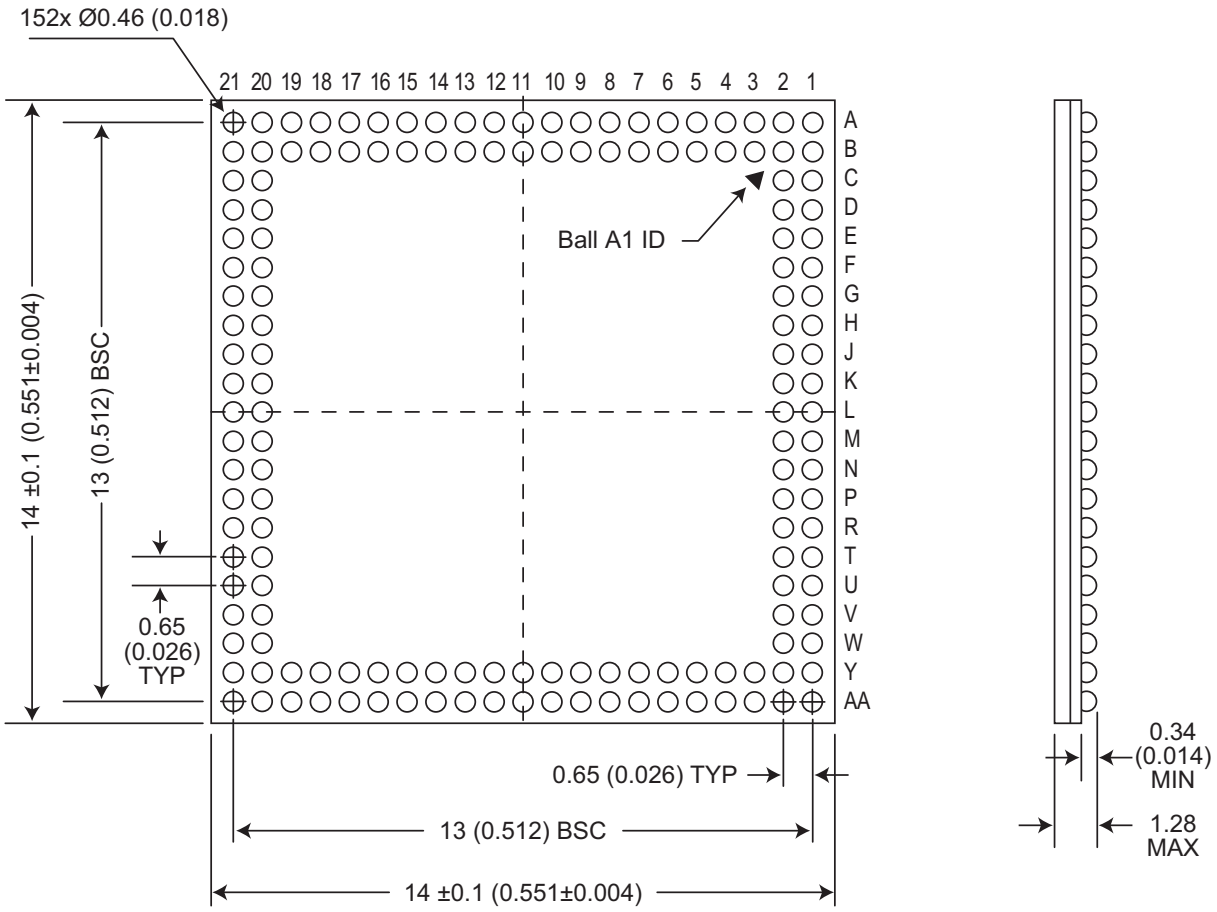
NOTES:

1. All voltages referenced to V_{SS}.
2. All parameters assume proper device initialization.
3. Tests for AC timing and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage ranges specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Specifications are correlated to production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half-strength driver with a nominal 10pF load, parameters t_{AC} and t_{QH} are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design/characterization. Use of I_{BIS} or other simulation tools for system design validation is suggested.



5. The CK/CK# input reference voltage level (for timing referenced to CK/CK#) is the point at which CK and CK# cross; the input reference voltage level for signals other than CK/ CK# is $V_{DDQ/2}$.
6. A CK and CK# input slew rate ≥1 V/ns (2 V/ns if measured differentially) is assumed for all parameters.
7. All AC timings assume an input slew rate of 1 V/ns.
8. CAS latency definition: with CL = 2, the first data element is valid at (t_{CK} + t_{AC}) after the clock at which the READ command was registered; for CL = 3, the first data element is valid at (2 × t_{CK} + t_{AC}) after the first clock at which the READ command was registered.
9. Timing tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ/2}$ or to the crossing point for CK/CK#. The output timing reference voltage level is $V_{DDQ/2}$.
10. Clock frequency change is only permitted during clock stop, power-down, or self refresh mode.
11. In cases where the device is in self refresh mode for t_{CKE}, t_{CKE} starts at the rising edge of the clock and ends when CKE transitions HIGH.
12. t_{DAL} = (t_{WR}/t_{CK}) + (t_{RP}/t_{CK}): for each term, if not already an integer, round up to the next highest integer.
13. Referenced to each output group: For x32, DQS0 with DQ[7:0]; DQS1 with DQ[15:8]; DQS2 with DQ[23:16]; and DQS3 with DQ[31:24].
14. DQ and DM input slew rates must not deviate from DQS by more than 10%. If the DQ/DM/ DQS slew rate is less than 1.0 V/ns, timing must be derated: 50ps must be added to t_{DS} and t_{DH} for each 100 mV/ns reduction in slew rate. If the slew rate exceeds 4 V/ns, functionality is uncertain.
15. The transition time for input signals (CAS#, CKE, CS#, DM, DQ, DQS, RAS#, WE#, and addresses) are measured between $V_{IL(DC)}$ to $V_{IH(AC)}$ for rising input signals and $V_{IH(DC)}$ to $V_{IL(AC)}$ for falling input signals.
16. These parameters guarantee device timing but are not tested on each device.
17. The valid data window is derived by achieving other specifications: t_{HP} ($t_{CK/2}$), t_{DQSQ}, and t_{QH} (t_{HP} - t_{QHS}). The data valid window derates directly proportional with the clock duty cycle and a practical data valid window can be derived. The clock is provided a maximum duty cycle variation of 45/55. Functionality is uncertain when operating beyond a 45/55 ratio.
18. $t_{HP\ (MIN)}$ is the lesser of $t_{CL\ (MIN)}$ and $t_{CH\ (MIN)}$ actually applied to the device CK and CK# inputs, collectively.
19. t_{HZ} and t_{LZ} transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (t_{HZ}) or begins driving (t_{LZ}).
20. $t_{HZ\ (MAX)}$ will prevail over $t_{DQSCK\ (MAX)}$ + $t_{RPST\ (MAX)}$ condition.
21. Fast command/address input slew rate ≥1 V/ns. Slow command/address input slew rate ≥0.5 V/ns. If the slew rate is less than 0.5 V/ns, timing must be derated: t_{IS} has an additional 50ps per each 100 mV/ns reduction in slew rate from the 0.5 V/ns. t_{IH} has 0ps added, therefore, it remains constant. If the slew rate exceeds 4.5 V/ns, functionality is uncertain.
22. READs and WRITEs with auto precharge must not be issued until $t_{RAS\ (MIN)}$ can be satisfied prior to the internal PRECHARGE command being issued.
23. The refresh period equals 64ms. This equates to an average refresh rate of 7.8125µs
24. This is not a device limit. The device will operate with a negative value, but system performance could be degraded due to bus turnaround.
25. It is recommended that DQS be valid (HIGH or LOW) on or before the WRITE command. The case shown (DQS going from High-Z to logic low) applies when no WRITEs were previously in progress on the bus. If a previous WRITE was in progress, DQS could be HIGH during this time, depending on t_{DQSS}.
26. The maximum limit for this parameter is not a device limit. The device will operate with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
27. At least 1 clock cycle is required during t_{WR} time when in auto precharge mode.
28. Clock must be toggled a minimum of two times during the t_{XSR} period.

FIGURE 6 – 152-BALL BGA PACKAGE



NOTE: (1) Dimension applies to solder ball post reflow on Ø0.35 ball pad.

All linear dimensions are millimeters and parenthetically in inches

ORDERING INFORMATION

MS 29C 2G 24M A K L A 1 - X X

MICROSEMI CORPORATION
MS

PRODUCT FAMILY
29C-2Gb/1Gb

NAND FLASH DENSITY
2G = 2Gb NAND FLASH

LPDRAM DENSITY
24M = 1G LPDDR

OPERATING VOLTAGE RANGE
A = 1.8V

NAND FLASH CONFIGURATION
K = x16

LPDRAM CONFIGURATION
L = x32

CHIP COUNT
A = 2; 1 NAND FLASH / 1 LPDDR SDRAM

PACKAGE CODES
1 = 152 Ball BGA

LPDRAM ACCESS TIME
X = CLOCK CYCLE TIME

Speed Grade	Clock Rate	CAS Latency
-5	200 MHz	CL3
-54	185 MHz	CL3
-6	166 MHz	CL3
-75	133 MHz	CL3

OPERATING TEMPERATURE
I = INDUSTRIAL TEMPERATURE (-40°C to +85°C)
C = COMMERCIAL TEMPERATURE (0°C to +70°C)

Document Title

2GB NAND / 1GB LPDDR

Revision History

Rev #	History	Release Date	Status
Rev 0	Changes (Pg. 1-19) 0.1 Create new data sheet	April 2011	Advanced
Rev 1	Changes (Pg. 2-4) 1.1 Figure 1 – pin AA15 from A13 to DNU 1.2 Figure 2 – changed Address 0-14 to 0-12 1.3 Table 4 – changed A[14:0] to A[12:0]	July 2011	Advanced
Rev 2	Changes (Pg. 1) 2.1 Change status to Preliminary and add bullet to Features section "Same footprint as Micron MT29C2G24MAKLA-XIT"	October 2011	Preliminary
Rev 3	Changes (Pg. 1, 3, 13, 14) 3.1 Add status read register (SRR) 3.2 Change storage temperature to -40°C to 125°C 3.3 Change data sheet status to final	September 2012	Final