



a  **MICROCHIP** company

Total Ionizing Dose Test Report

No. 22T-RT4G150-LG1657- K7KAR

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO ₂)
2. Power Supply Current	Passed 125 krad(SiO ₂)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO ₂)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO ₂)
5. Propagation Delay	Passed 125 krad(SiO ₂) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO ₂)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at <http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports>

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K7KAR
Quantity Tested	6
Serial Number (Dose)	07573 (125 krad), 07585 (125 krad), 07596 (125 krad), 07617 (125 krad), 07622 (125 krad), 07640 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

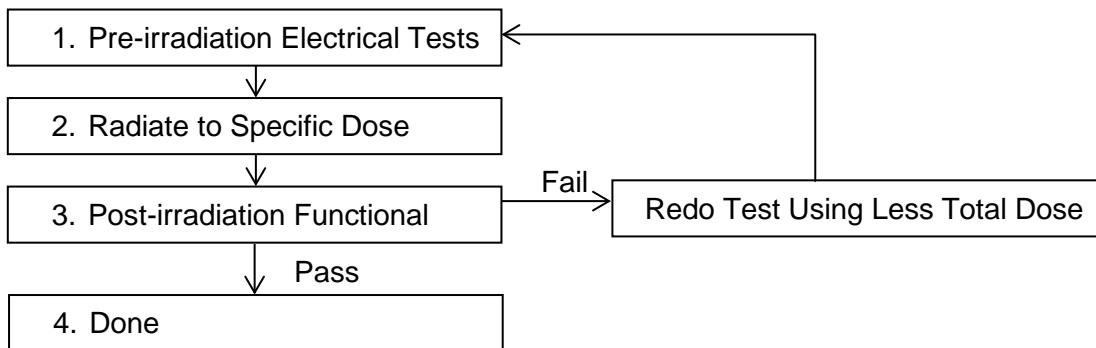


Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07573	125 krad	0.3897	0.4059	4.16
07585	125 krad	0.3995	0.4157	4.06
07596	125 krad	0.4225	0.4413	4.45
07617	125 krad	0.3965	0.4027	1.56
07622	125 krad	0.3762	0.3932	4.52
07640	125 krad	0.3713	0.3829	3.12

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07573	125 krad	0.0098	0.0121	23.47
07585	125 krad	0.0094	0.0116	23.40
07596	125 krad	0.0128	0.0120	-6.25
07617	125 krad	0.0093	0.0111	19.35
07622	125 krad	0.0110	0.0132	20.00
07640	125 krad	0.0100	0.0121	21.00

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07573	125 krad	0.0343	0.0372	8.45
07585	125 krad	0.0337	0.0365	8.31
07596	125 krad	0.0338	0.0373	10.36
07617	125 krad	0.0337	0.0363	7.72
07622	125 krad	0.0343	0.0372	8.45
07640	125 krad	0.0345	0.0373	8.12

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
07573	125 krad	0.0153	0.0153	0.00
07585	125 krad	0.0152	0.0153	0.66
07596	125 krad	0.0152	0.0161	5.92
07617	125 krad	0.0151	0.0153	1.32
07622	125 krad	0.0152	0.0160	5.26
07640	125 krad	0.0154	0.0158	2.60

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

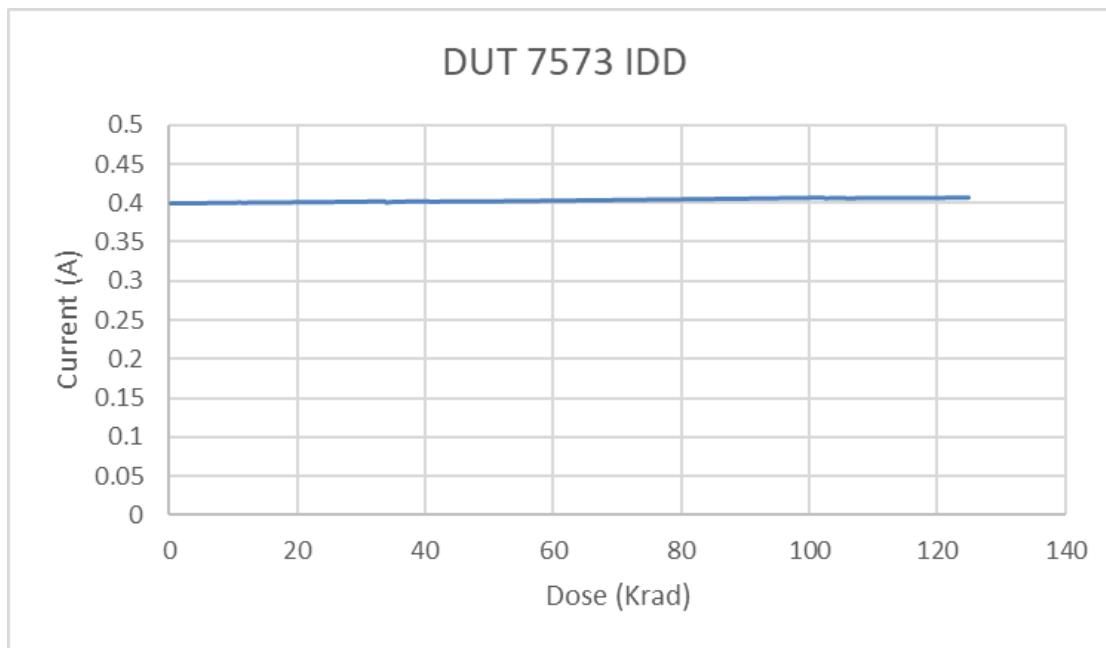


Fig. 2. DUT 07573 core power supply current (I_{DD}) versus TID

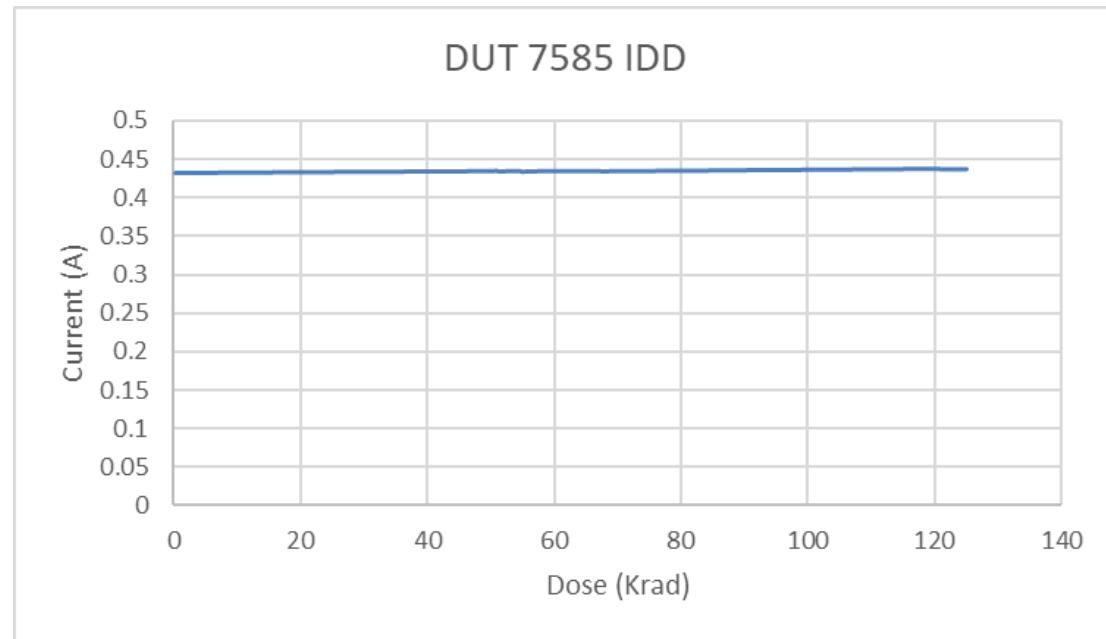


Fig. 3. DUT 07585 core power supply current (I_{DD}) versus TID

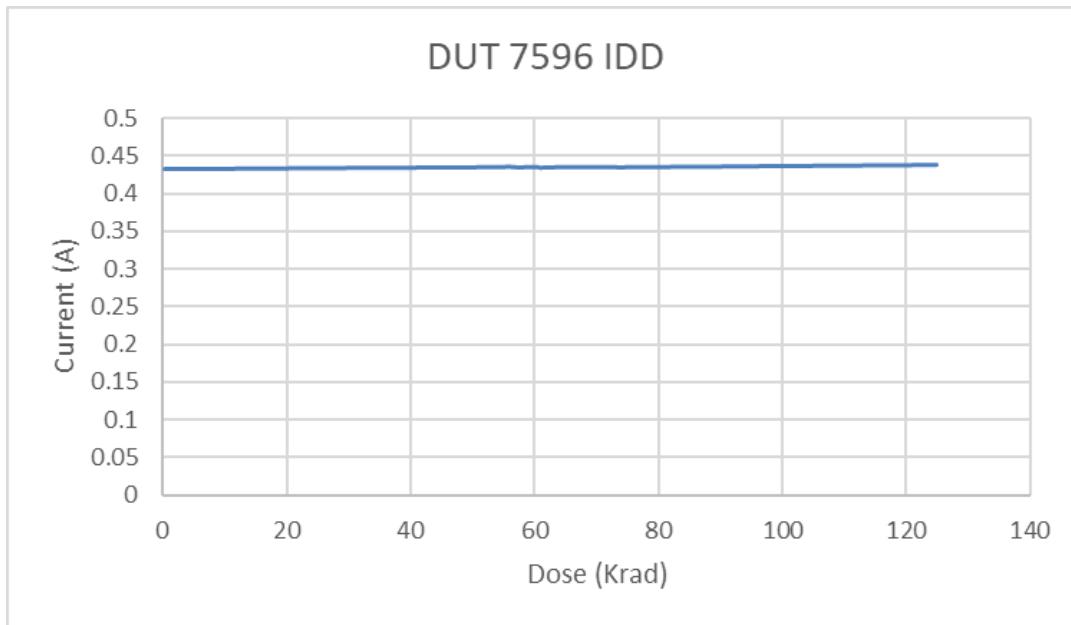


Fig. 4. DUT 07596 core power supply current (I_{DD}) versus TID

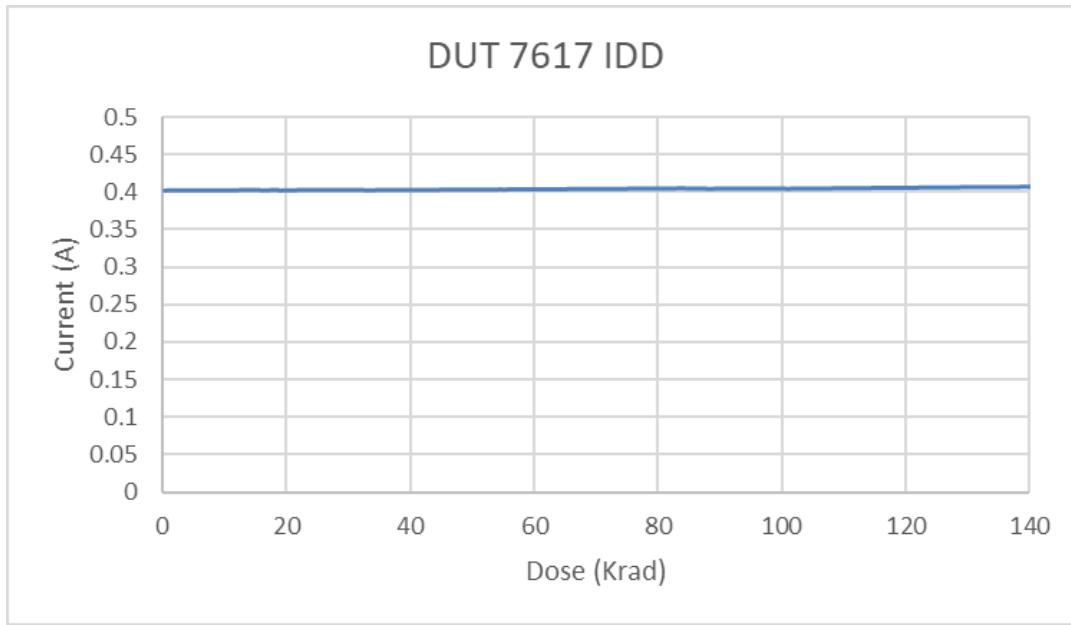


Fig. 5. DUT 07617 core power supply current (I_{DD}) versus TID

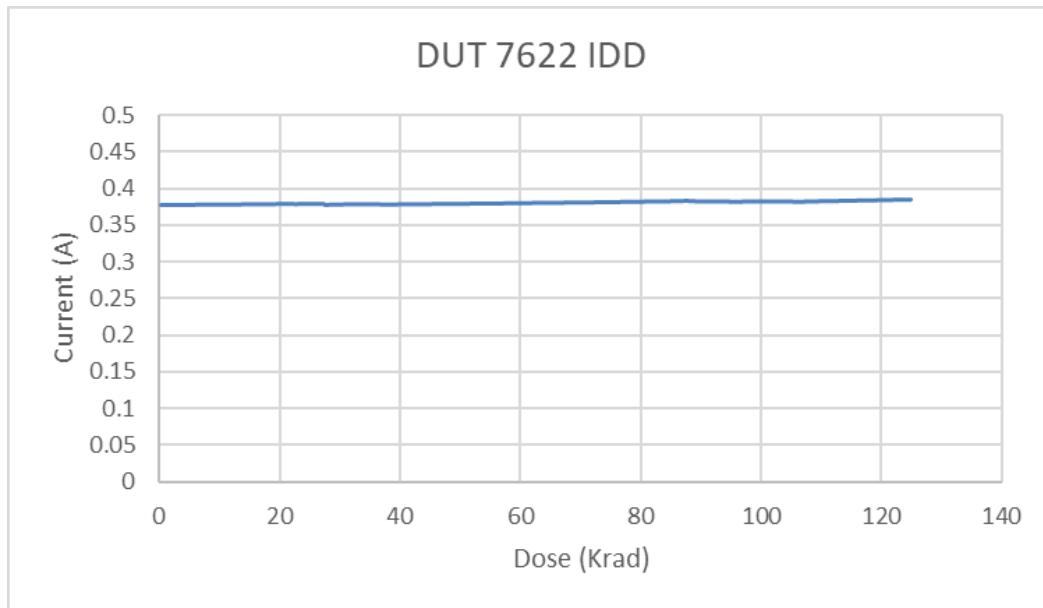


Fig. 6. DUT 07622 core power supply current (I_{DD}) versus TID

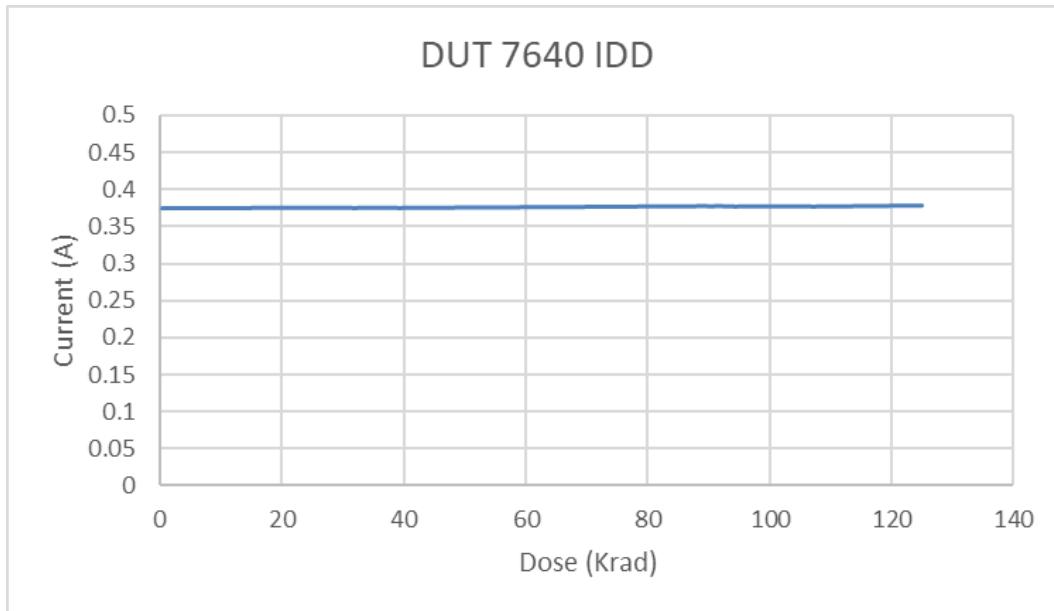


Fig. 7. DUT 07640 core power supply current (I_{DD}) versus TID

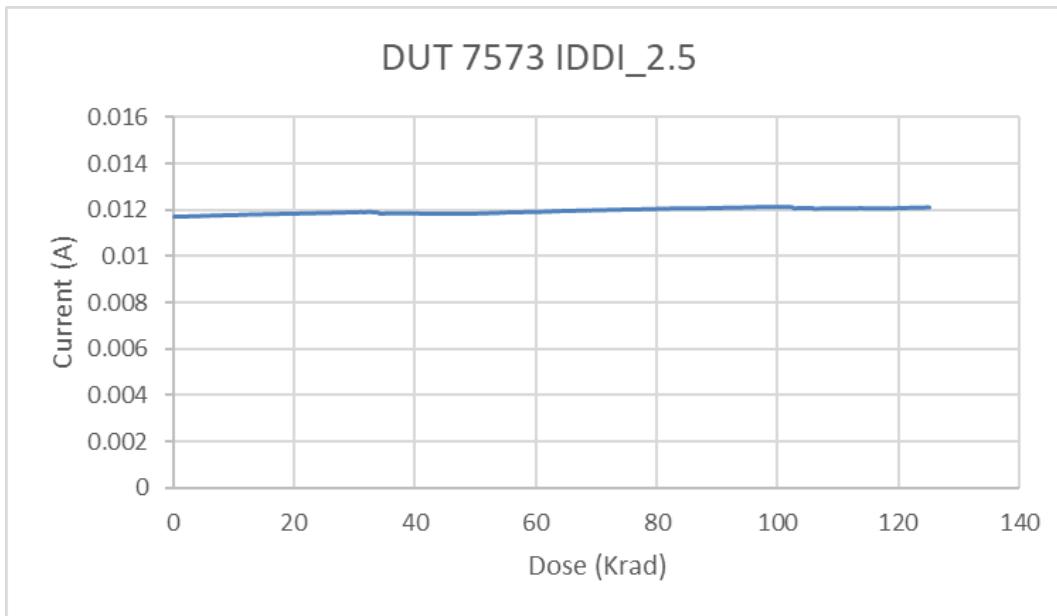


Fig. 8. DUT 07573 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

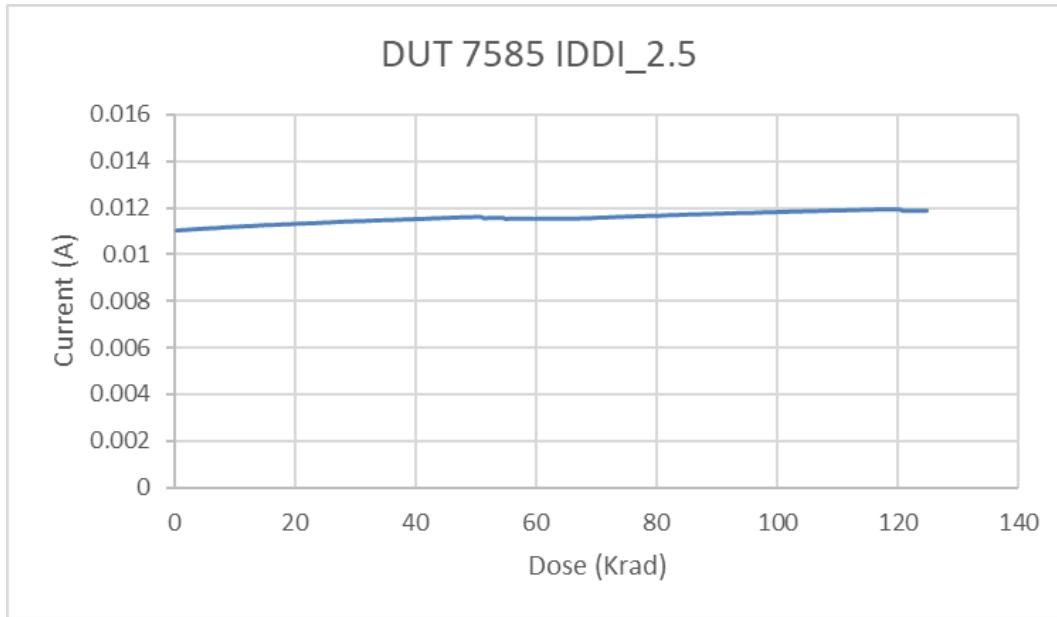


Fig. 9. DUT 07585 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

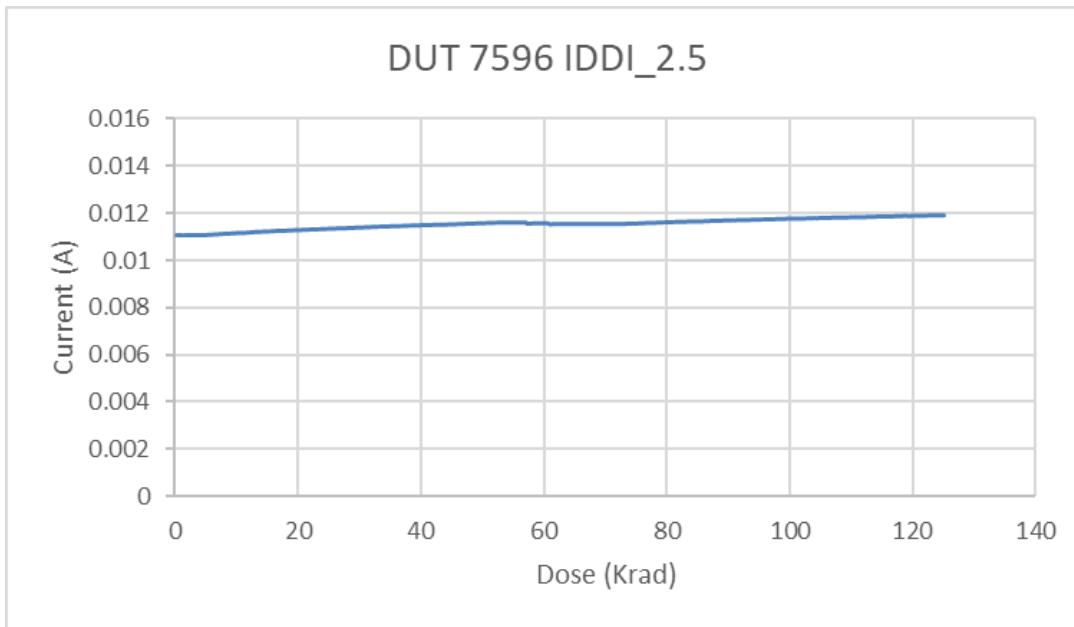


Fig. 10. DUT 07596 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

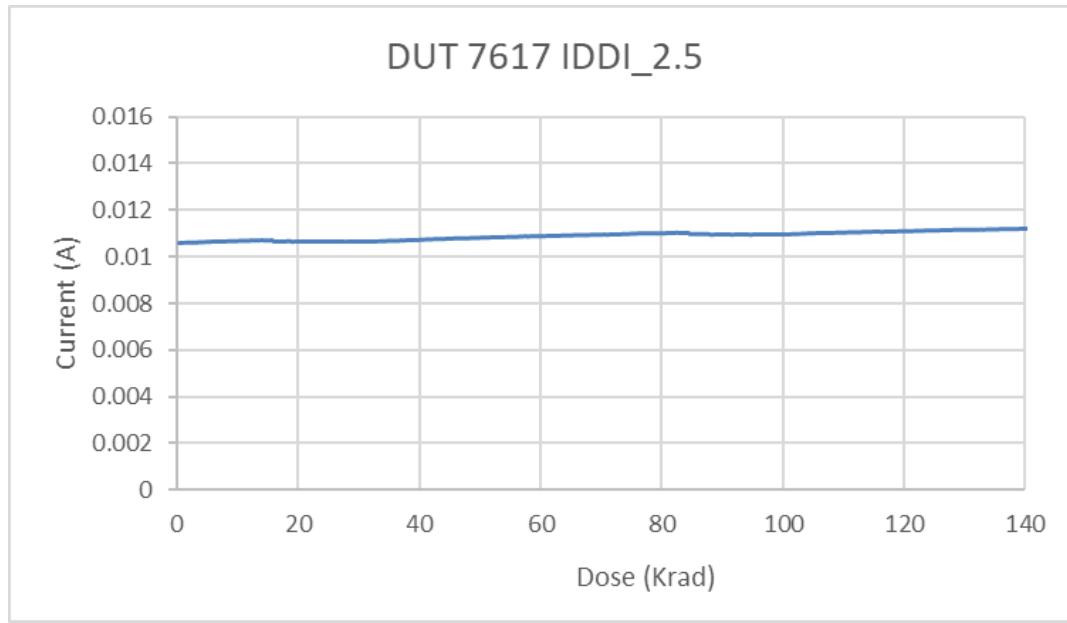


Fig. 11. DUT 07617 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

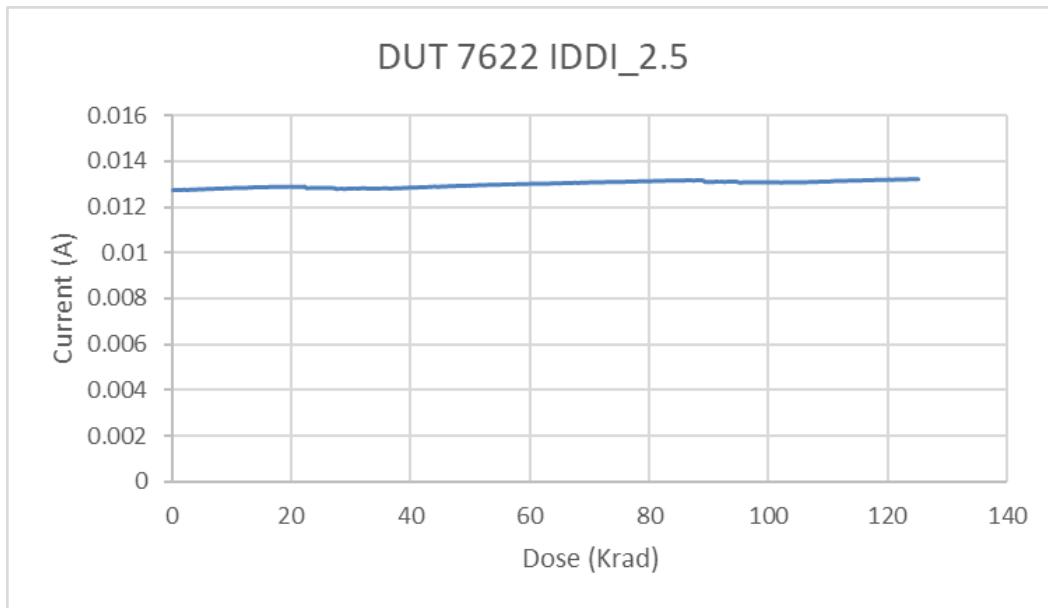


Fig. 12. DUT 07622 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

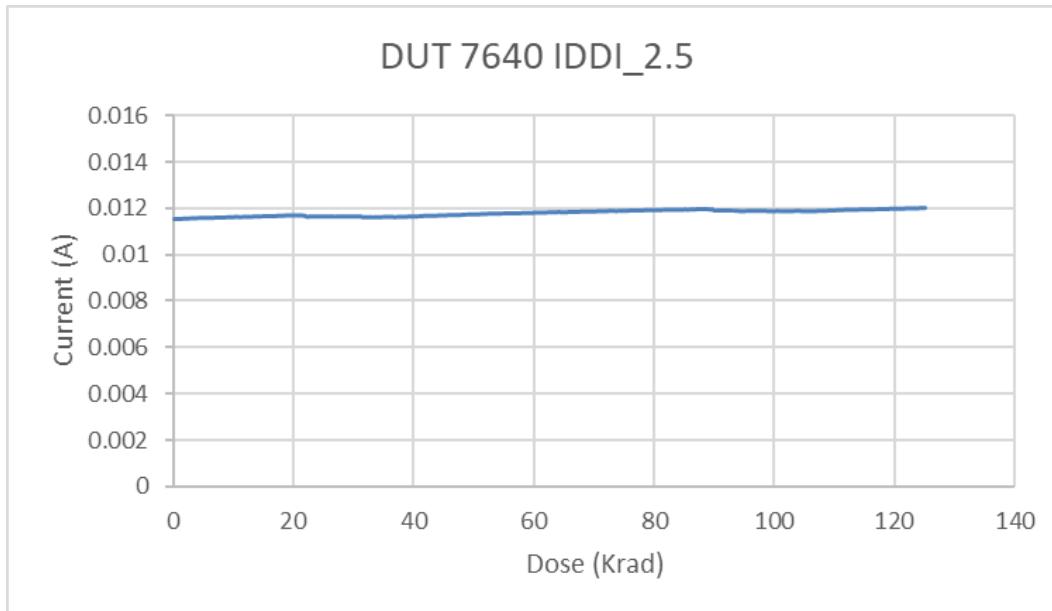


Fig. 13. DUT 07640 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

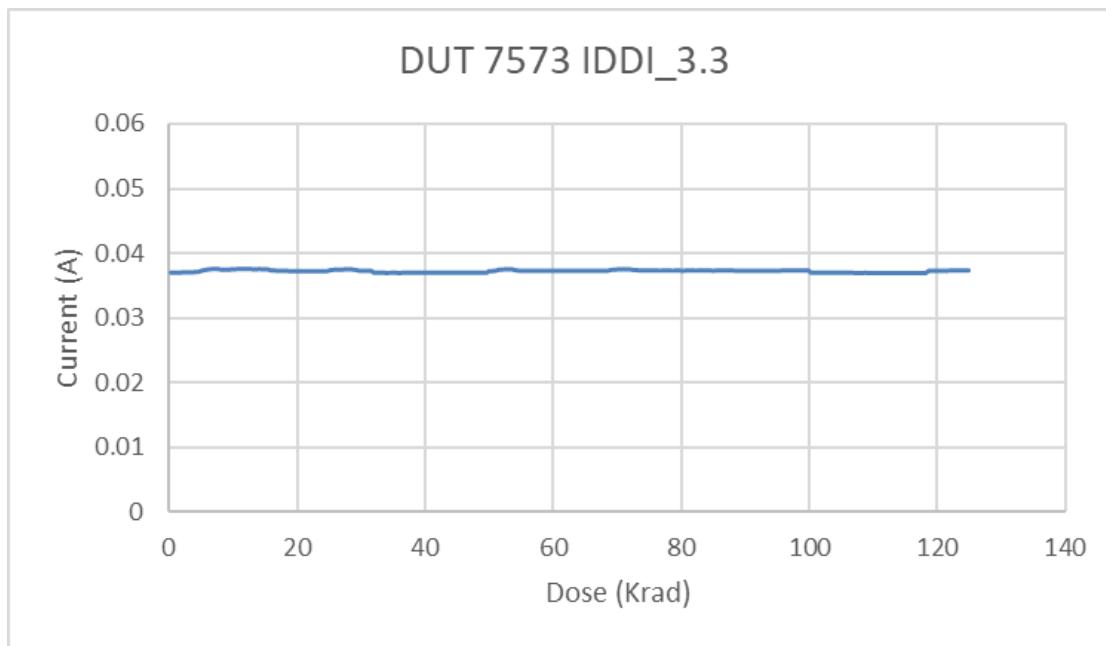


Fig. 14. DUT 07573 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

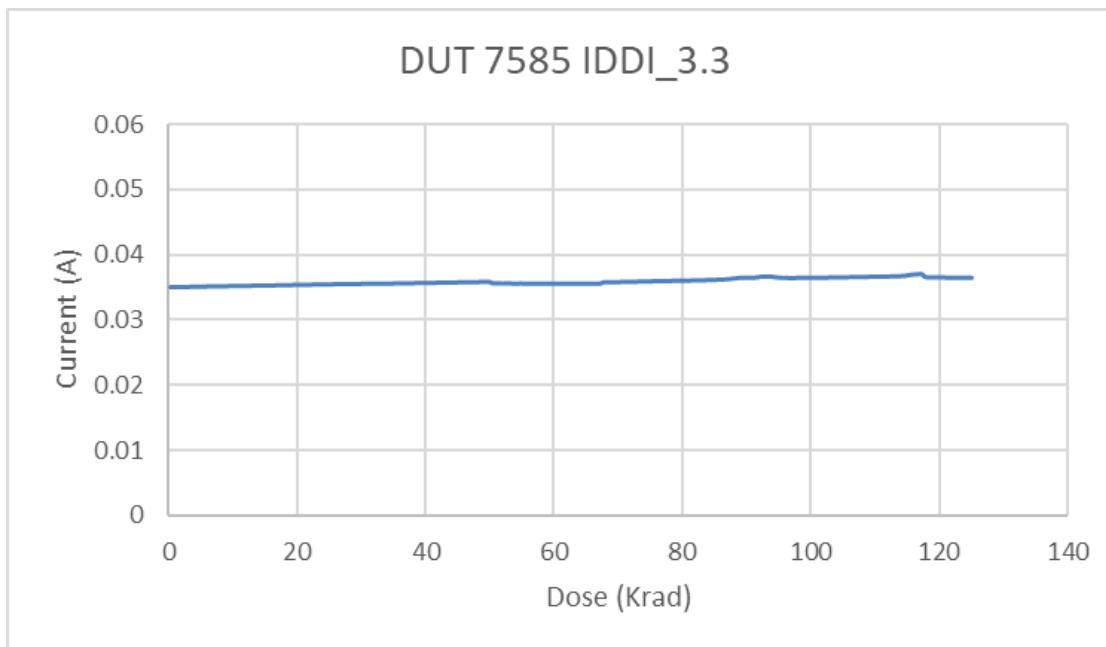


Fig. 15. DUT 07585 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

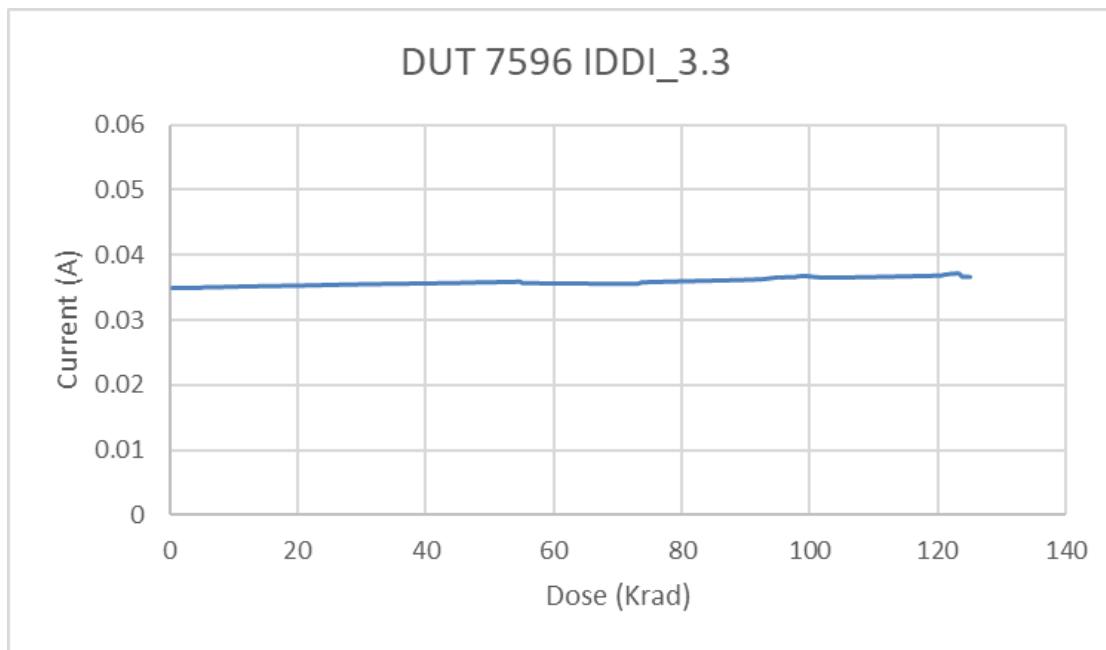


Fig. 16. DUT 07596 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

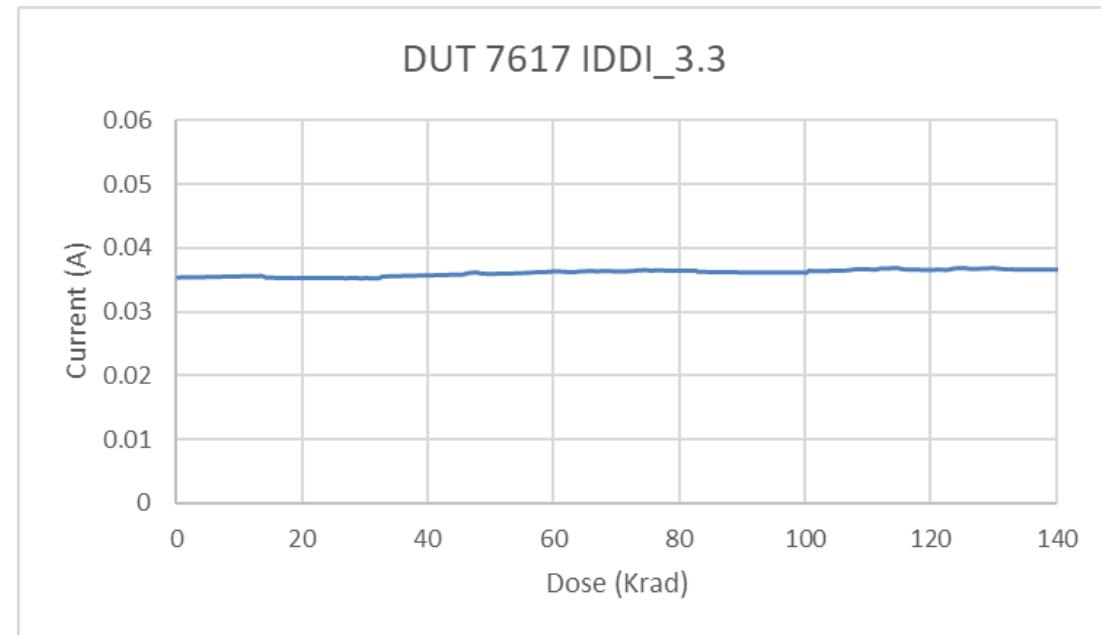


Fig. 17. DUT 07617 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

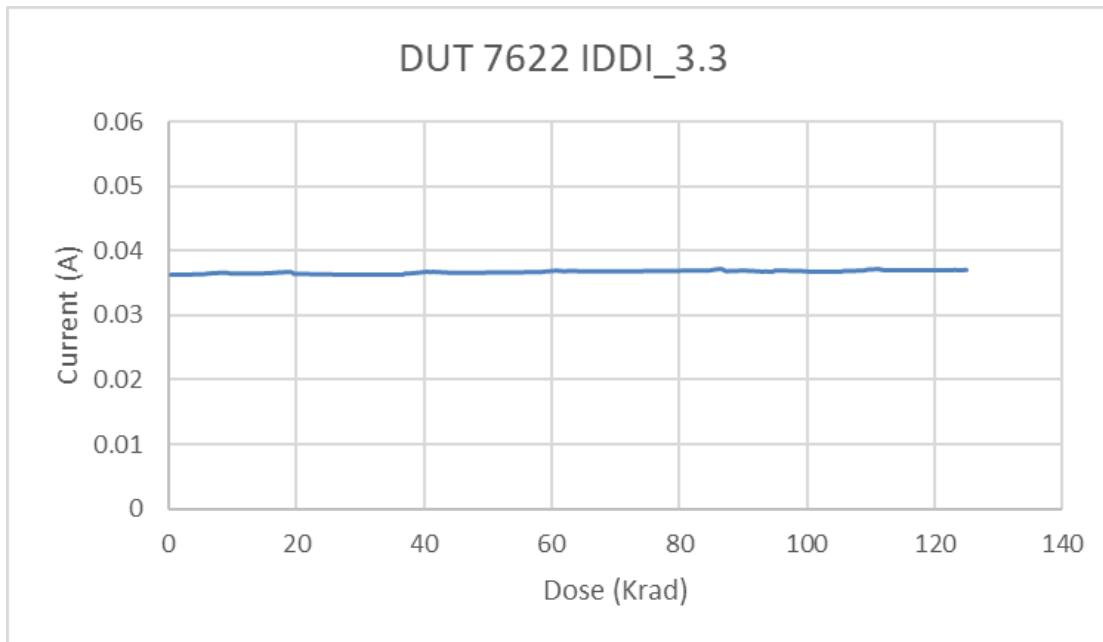


Fig. 18. DUT 07622 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

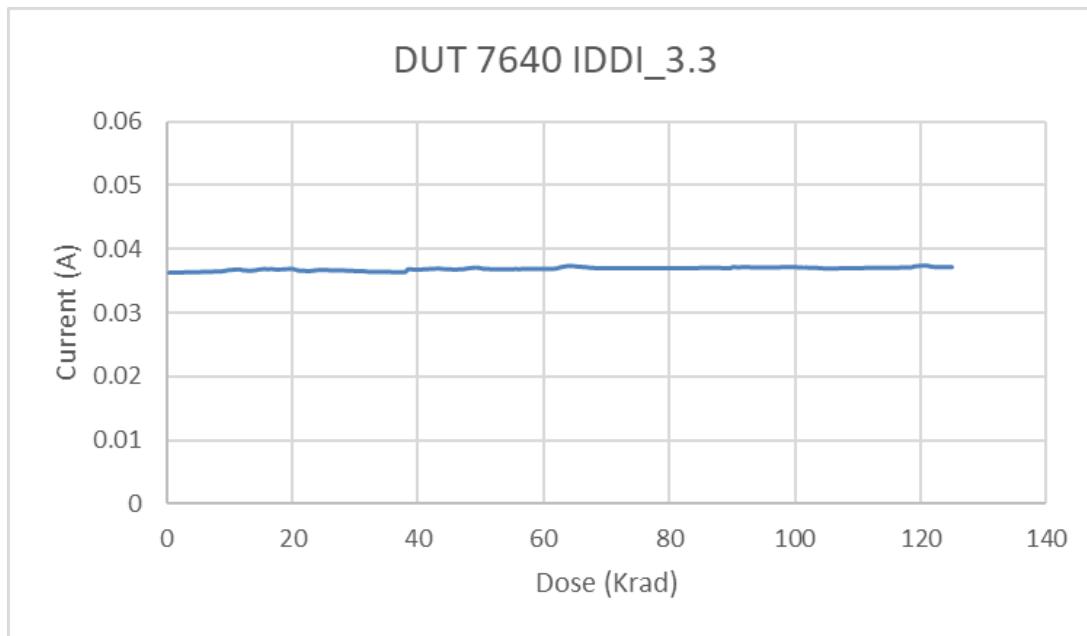


Fig. 19. DUT 07640 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

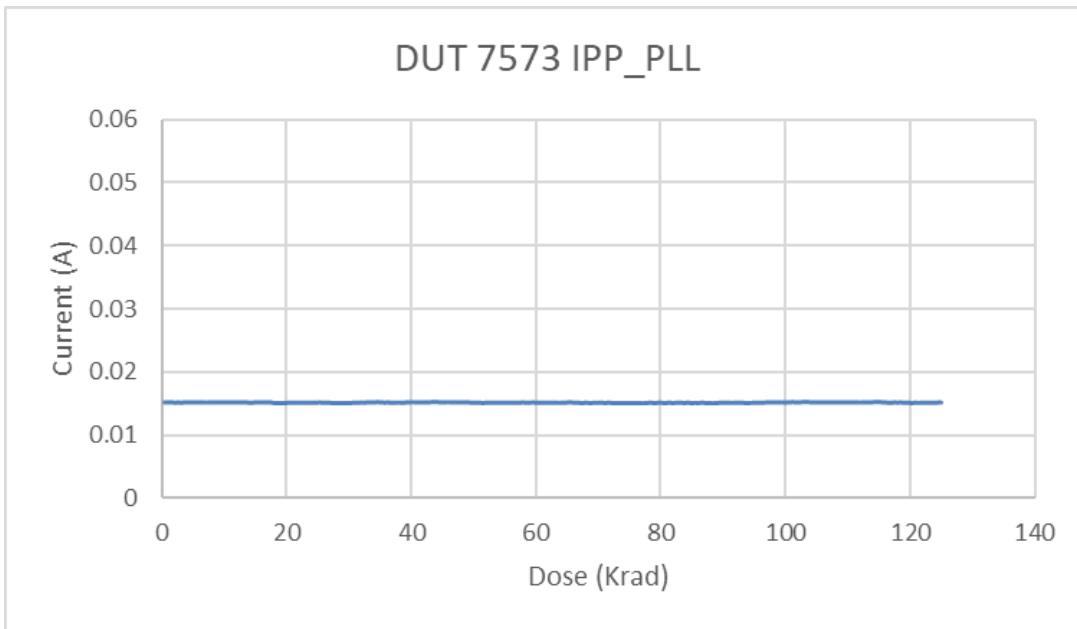


Fig. 20. DUT 07573 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

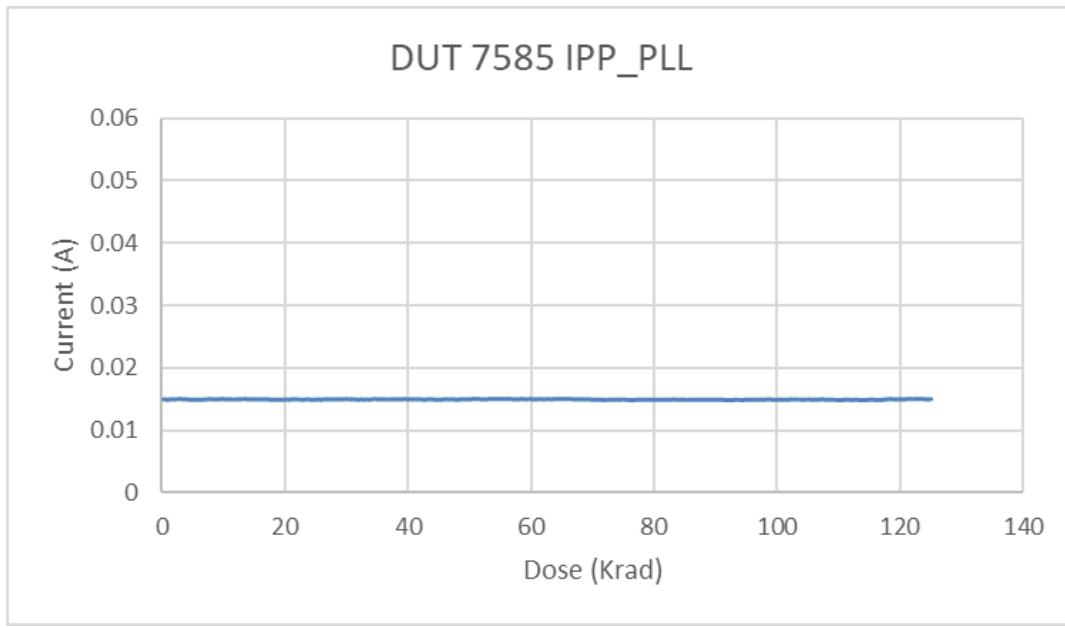


Fig. 21. DUT 07585 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

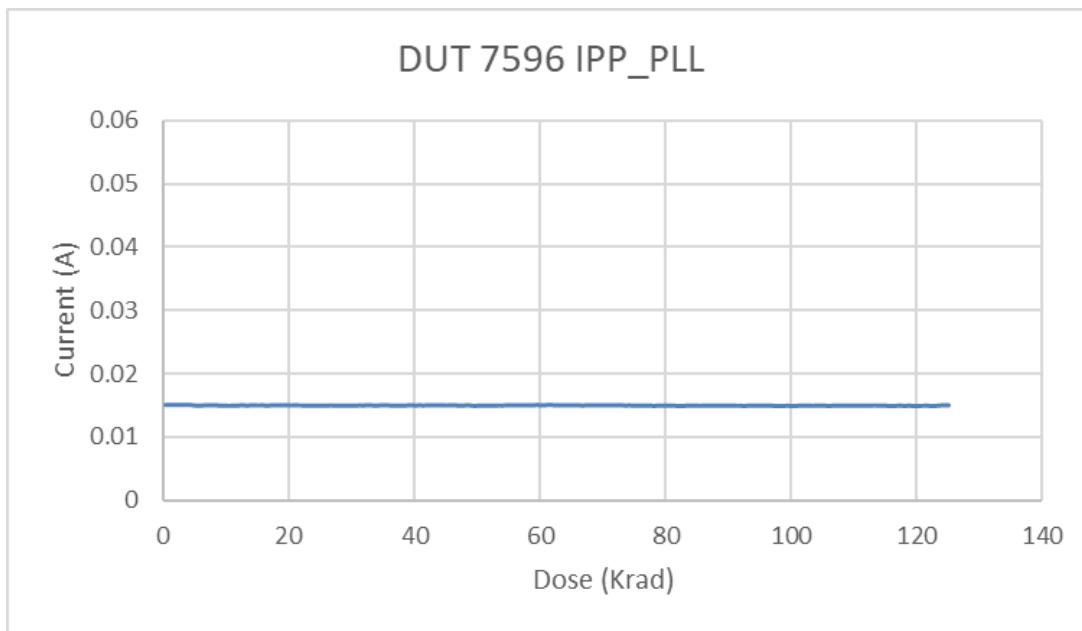


Fig. 22. DUT 07596 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

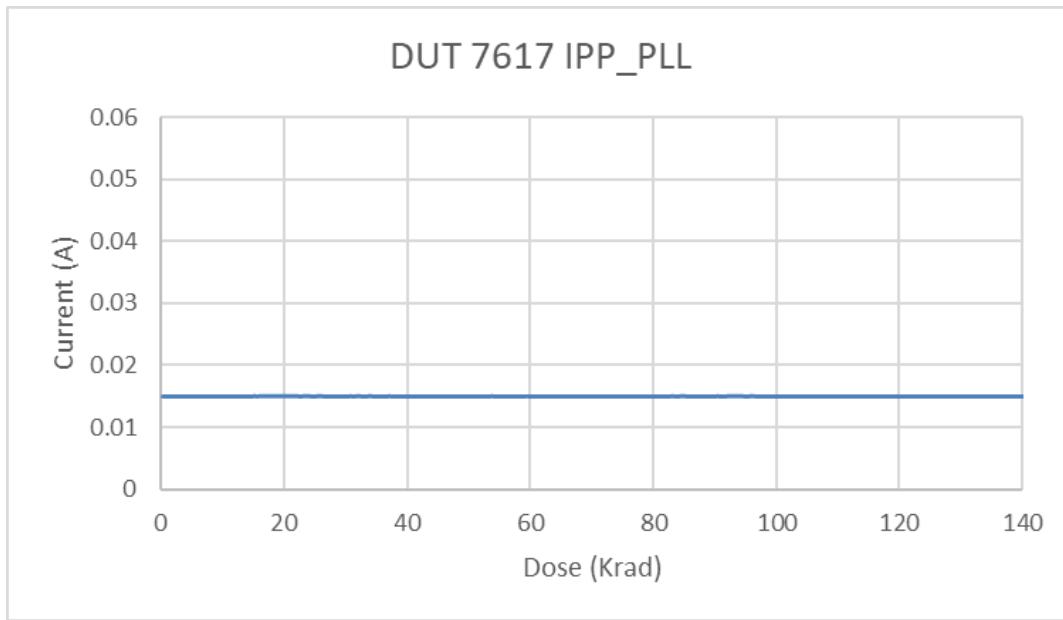


Fig. 23. DUT 07617 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

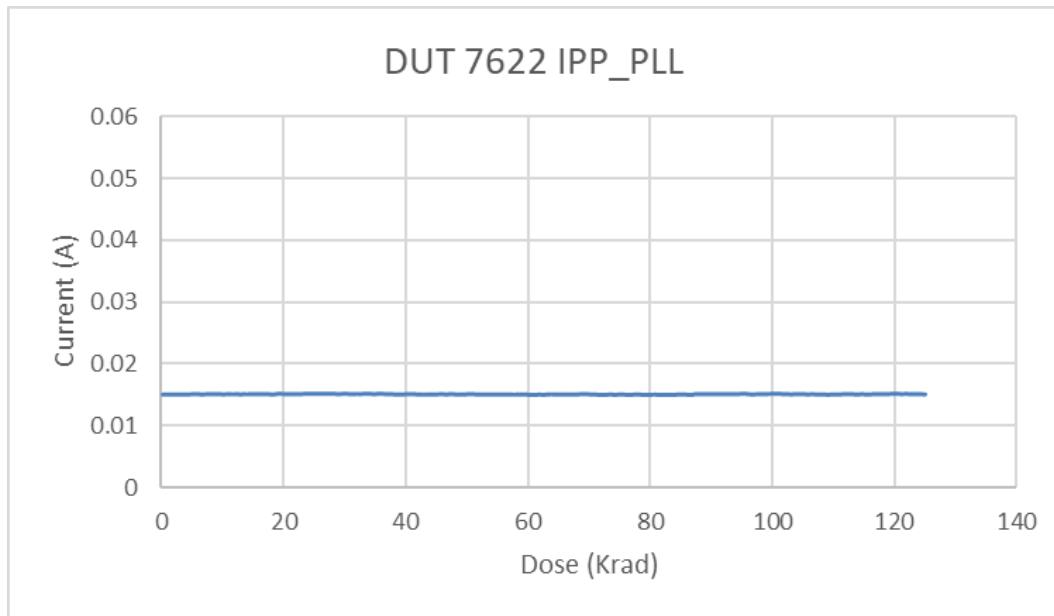


Fig. 24. DUT 07622 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

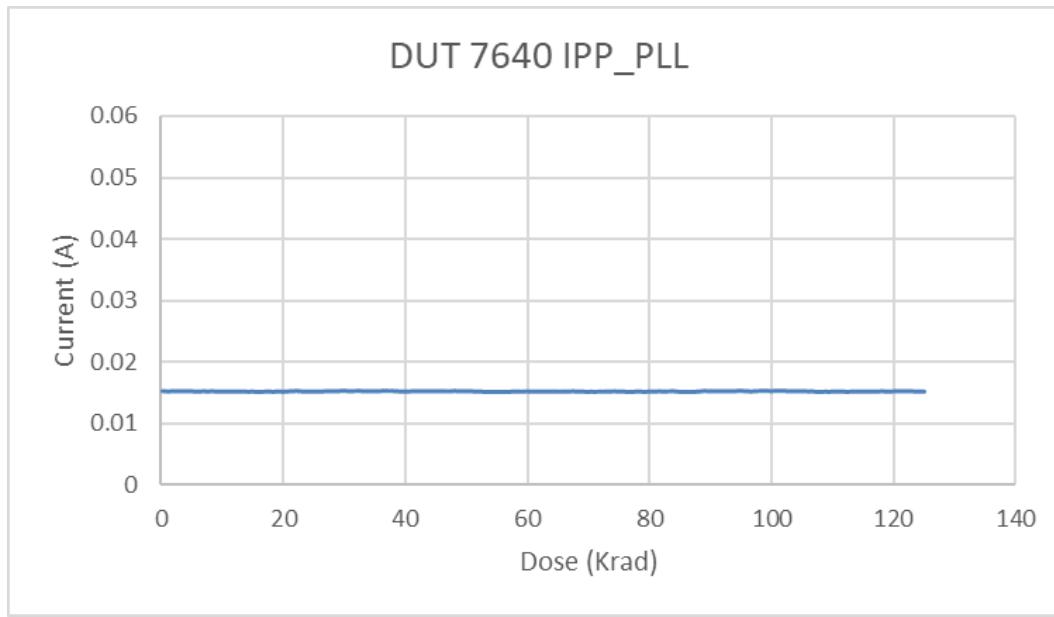


Fig. 25. DUT 07640 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
07573	Passed	Passed
07585	Passed	Passed
07596	Passed	Passed
07617	Passed	Passed
07622	Passed	Passed
07640	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
07573	Passed	Passed
07585	Passed	Passed
07596	Passed	Passed
07617	Passed	Passed
07622	Passed	Passed
07640	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 07573

Pin Name	Pin#	2mA	4mA	6mA	8mA	12mA	14mA
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.134	2.131	2.204	2.200	2.176	2.171
EPCSRST_N_0	B31	2.134	2.132	2.203	2.202	2.174	2.173
EPCSRST_N_1	B32	2.135	2.133	2.204	2.203	2.175	2.174
EPCSRST_N_2	B34	2.134	2.132	2.202	2.201	2.173	2.172
EPCSRST_N_3	B35	2.134	2.133	2.204	2.203	2.175	2.174
EPCSRST_N_4	B36	2.133	2.131	2.201	2.200	2.172	2.171
EPCSRST_N_5	B37	2.133	2.132	2.203	2.202	2.174	2.173
MONITOR	K23	2.132	2.131	2.203	2.202	2.175	2.174
PLL_MON	L20	2.135	2.133	2.207	2.204	2.180	2.178
TOGGLE_MON	L22	2.132	2.132	2.203	2.202	2.175	2.175

Table. 11. LVCMOS 25 VOH – DUT 07585

Pin Name	Pin#	2mA	4mA	6mA	8mA	12mA	14mA
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.134	2.131	2.204	2.200	2.176	2.171
EPCSRST_N_0	B31	2.135	2.133	2.203	2.202	2.174	2.173
EPCSRST_N_1	B32	2.136	2.133	2.204	2.203	2.176	2.174
EPCSRST_N_2	B34	2.134	2.132	2.203	2.201	2.174	2.172
EPCSRST_N_3	B35	2.135	2.133	2.204	2.203	2.176	2.175
EPCSRST_N_4	B36	2.134	2.132	2.202	2.201	2.173	2.171
EPCSRST_N_5	B37	2.135	2.132	2.203	2.202	2.175	2.173
MONITOR	K23	2.133	2.131	2.203	2.202	2.175	2.174
PLL_MON	L20	2.136	2.133	2.207	2.204	2.181	2.178
TOGGLE_MON	L22	2.134	2.132	2.204	2.203	2.176	2.175

Table. 12. LVCMOS 25 VOH – DUT 07596

Pin Name	Pin#	2mA	4mA	6mA	8mA	12mA	14mA
		Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.135	2.133	2.205	2.201	2.177	2.172
EPCSRST_N_0	B31	2.135	2.134	2.203	2.203	2.175	2.174
EPCSRST_N_1	B32	2.136	2.135	2.205	2.204	2.176	2.176
EPCSRST_N_2	B34	2.134	2.132	2.203	2.202	2.174	2.173
EPCSRST_N_3	B35	2.135	2.134	2.204	2.203	2.176	2.175
EPCSRST_N_4	B36	2.133	2.132	2.202	2.201	2.173	2.171
EPCSRST_N_5	B37	2.135	2.133	2.203	2.203	2.175	2.174
MONITOR	K23	2.134	2.133	2.204	2.203	2.176	2.176
PLL_MON	L20	2.137	2.135	2.208	2.205	2.182	2.179
TOGGLE_MON	L22	2.134	2.133	2.204	2.204	2.176	2.176

Table. 13. LVC MOS 25 VOH – DUT 07617

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.134	2.131	2.204	2.200	2.176	2.171	2.157	2.150	2.126	2.116	2.113	2.102
EPCSRST_N_0	B31	2.134	2.133	2.203	2.202	2.175	2.173	2.154	2.153	2.122	2.120	2.108	2.107
EPCSRST_N_1	B32	2.135	2.134	2.204	2.203	2.176	2.175	2.156	2.154	2.124	2.123	2.111	2.110
EPCSRST_N_2	B34	2.134	2.132	2.203	2.202	2.174	2.173	2.153	2.151	2.121	2.119	2.107	2.105
EPCSRST_N_3	B35	2.135	2.133	2.204	2.203	2.176	2.175	2.156	2.154	2.125	2.123	2.112	2.110
EPCSRST_N_4	B36	2.133	2.132	2.202	2.201	2.172	2.171	2.151	2.150	2.118	2.116	2.104	2.102
EPCSRST_N_5	B37	2.134	2.133	2.203	2.202	2.174	2.174	2.154	2.152	2.123	2.120	2.109	2.107
MONITOR	K23	2.133	2.132	2.203	2.203	2.176	2.175	2.156	2.155	2.126	2.125	2.113	2.113
PLL_MON	L20	2.135	2.134	2.206	2.205	2.179	2.178	2.162	2.159	2.134	2.131	2.122	2.120
TOGGLE_MON	L22	2.133	2.133	2.204	2.204	2.176	2.176	2.156	2.156	2.126	2.127	2.114	2.114

Table. 14. LVC MOS 25 VOH – DUT 07622

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.133	2.131	2.204	2.200	2.176	2.171	2.156	2.151	2.126	2.117	2.113	2.103
EPCSRST_N_0	B31	2.134	2.132	2.203	2.202	2.174	2.173	2.154	2.152	2.121	2.120	2.108	2.106
EPCSRST_N_1	B32	2.135	2.133	2.204	2.203	2.176	2.175	2.155	2.154	2.124	2.123	2.111	2.109
EPCSRST_N_2	B34	2.133	2.132	2.202	2.201	2.173	2.172	2.153	2.151	2.120	2.119	2.107	2.105
EPCSRST_N_3	B35	2.134	2.133	2.204	2.203	2.176	2.175	2.155	2.154	2.125	2.123	2.112	2.110
EPCSRST_N_4	B36	2.133	2.132	2.201	2.201	2.172	2.171	2.151	2.149	2.118	2.116	2.103	2.101
EPCSRST_N_5	B37	2.134	2.133	2.203	2.202	2.174	2.173	2.154	2.153	2.122	2.120	2.108	2.107
MONITOR	K23	2.132	2.131	2.203	2.202	2.175	2.174	2.155	2.155	2.125	2.125	2.113	2.112
PLL_MON	L20	2.135	2.133	2.206	2.204	2.180	2.177	2.163	2.159	2.136	2.131	2.125	2.119
TOGGLE_MON	L22	2.132	2.131	2.203	2.202	2.175	2.175	2.156	2.156	2.126	2.126	2.113	2.114

Table. 15. LVC MOS 25 VOH – DUT 07640

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.135	2.132	2.204	2.201	2.176	2.172	2.157	2.151	2.127	2.118	2.113	2.104
EPCSRST_N_0	B31	2.135	2.134	2.204	2.203	2.175	2.174	2.155	2.153	2.122	2.121	2.109	2.107
EPCSRST_N_1	B32	2.135	2.134	2.204	2.204	2.176	2.175	2.156	2.154	2.125	2.123	2.112	2.110
EPCSRST_N_2	B34	2.135	2.133	2.203	2.202	2.174	2.173	2.154	2.152	2.121	2.119	2.108	2.106
EPCSRST_N_3	B35	2.135	2.134	2.204	2.204	2.176	2.175	2.157	2.155	2.126	2.124	2.113	2.111
EPCSRST_N_4	B36	2.134	2.133	2.202	2.201	2.173	2.172	2.152	2.150	2.119	2.117	2.105	2.103
EPCSRST_N_5	B37	2.135	2.133	2.204	2.203	2.175	2.174	2.155	2.153	2.123	2.121	2.110	2.108
MONITOR	K23	2.133	2.132	2.203	2.203	2.176	2.175	2.156	2.155	2.126	2.126	2.114	2.113
PLL_MON	L20	2.135	2.133	2.207	2.205	2.181	2.178	2.163	2.160	2.136	2.131	2.126	2.120
TOGGLE_MON	L22	2.134	2.133	2.203	2.203	2.176	2.176	2.157	2.156	2.126	2.127	2.114	2.114

Table. 16. LVC MOS 25 VOL – DUT 07573

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	235.4	236.8	166.6	169.3	194.0	197.9	214.7	219.6	244.5	252.1	257.2	266.2
EPCSRST_N_0	B31	235.0	235.6	167.8	168.3	195.9	196.5	217.5	218.1	248.9	249.8	262.5	263.6
EPCSRST_N_1	B32	234.5	234.9	166.5	167.0	194.1	194.8	214.9	215.0	245.4	246.2	258.6	259.2
EPCSRST_N_2	B34	235.7	236.3	168.3	169.0	196.6	197.4	217.8	218.2	249.1	249.9	262.6	263.5
EPCSRST_N_3	B35	235.4	235.8	167.0	167.5	194.5	195.2	215.1	215.4	245.4	246.1	258.2	258.9
EPCSRST_N_4	B36	237.1	237.6	169.5	169.9	198.1	198.8	219.6	219.9	251.9	252.6	265.8	266.9
EPCSRST_N_5	B37	236.1	236.5	167.7	168.2	195.5	196.2	216.6	216.6	247.5	248.2	260.7	261.5
MONITOR	K23	234.8	235.4	166.2	166.5	193.2	193.5	212.8	213.5	242.1	242.9	254.8	255.3
PLL_MON	L20	233.4	234.2	163.0	164.5	188.7	190.7	207.1	209.5	233.2	237.0	244.1	248.5
TOGGLE_MON	L22	234.5	234.8	166.2	166.1	193.2	192.9	213.1	212.4	242.7	241.7	255.1	254.1

Table. 17. LVC MOS 25 VOL – DUT 07585

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	234.3	236.3	166.0	168.8	193.1	197.2	213.9	219.1	243.4	251.1	256.1	265.0
EPCSRST_N_0	B31	233.4	234.4	166.6	167.6	194.6	195.7	216.1	217.3	247.3	248.7	260.8	262.5
EPCSRST_N_1	B32	232.9	233.9	165.6	166.5	193.0	194.1	213.6	214.2	243.7	245.0	256.8	258.2
EPCSRST_N_2	B34	234.8	235.7	167.3	168.3	195.3	196.5	216.3	217.0	247.3	248.6	260.6	262.2
EPCSRST_N_3	B35	234.0	234.9	166.1	166.9	193.3	194.3	213.8	214.4	243.7	244.9	256.5	257.8
EPCSRST_N_4	B36	235.2	236.2	168.4	169.2	196.6	197.8	218.2	218.8	250.0	251.4	263.8	265.2
EPCSRST_N_5	B37	234.4	235.3	166.9	167.7	194.3	195.5	215.2	215.8	245.8	246.9	259.0	260.4
MONITOR	K23	233.8	234.5	165.8	165.8	193.1	192.9	212.9	212.8	242.5	241.9	255.1	254.2
PLL_MON	L20	232.0	233.2	162.2	163.9	187.7	190.1	206.1	208.8	232.0	236.2	242.6	247.6
TOGGLE_MON	L22	233.5	234.1	165.1	165.2	191.9	192.1	211.8	211.4	240.9	240.5	253.1	252.5

Table. 18. LVC MOS 25 VOL – DUT 07596

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	234.3	235.7	165.7	168.2	192.8	196.5	213.4	218.3	242.8	250.2	255.4	264.2
EPCSRST_N_0	B31	234.2	234.3	166.9	167.3	194.9	195.4	216.4	216.9	247.5	248.3	261.0	262.0
EPCSRST_N_1	B32	233.2	233.4	165.6	166.1	193.0	193.4	213.8	213.7	244.0	244.4	257.0	257.5
EPCSRST_N_2	B34	235.2	235.6	167.5	168.0	195.5	196.2	216.4	216.7	247.6	248.3	261.0	261.8
EPCSRST_N_3	B35	234.8	235.0	166.4	166.7	193.6	194.2	214.2	214.1	244.1	244.5	256.9	257.3
EPCSRST_N_4	B36	235.8	236.1	168.7	169.1	197.1	197.6	218.6	218.7	250.5	251.2	264.5	265.3
EPCSRST_N_5	B37	234.6	234.9	167.0	167.4	194.7	195.2	215.6	215.5	246.3	246.5	259.2	259.8
MONITOR	K23	233.0	233.4	164.9	165.2	191.8	192.1	211.4	211.9	240.7	241.2	253.1	253.7
PLL_MON	L20	232.0	232.5	162.1	163.4	187.3	189.3	205.7	208.2	231.7	235.6	242.4	247.0
TOGGLE_MON	L22	233.1	232.9	165.1	164.9	192.1	191.6	211.9	211.1	241.1	240.1	253.5	252.2

Table. 19. LVC MOS 25 VOL – DUT 07617

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	234.7	236.0	166.0	168.9	193.2	197.6	214.0	219.6	243.6	252.1	256.4	266.3
EPCSRST_N_0	B31	234.0	234.5	167.0	167.4	195.0	195.5	216.4	216.9	247.7	248.3	261.3	262.0
EPCSRST_N_1	B32	233.4	233.6	165.8	166.4	193.4	193.9	214.0	214.0	244.4	244.8	257.3	257.9
EPCSRST_N_2	B34	234.6	234.9	167.4	167.9	195.6	196.1	216.7	216.8	248.0	248.7	261.5	262.2
EPCSRST_N_3	B35	234.3	234.4	166.3	166.6	193.8	194.2	214.4	214.3	244.3	244.6	257.1	257.6
EPCSRST_N_4	B36	235.7	236.1	168.7	169.2	197.2	197.8	219.0	218.9	251.1	251.6	265.0	265.6
EPCSRST_N_5	B37	235.1	235.4	167.2	167.5	195.0	195.6	215.9	216.0	246.8	247.2	259.9	260.6
MONITOR	K23	233.2	233.6	165.1	165.5	192.2	192.4	211.8	212.2	241.1	241.5	253.6	253.9
PLL_MON	L20	232.9	232.8	163.4	163.7	189.1	189.6	208.0	208.3	234.8	235.6	246.1	247.0
TOGGLE_MON	L22	233.6	233.3	165.2	165.0	192.1	191.7	211.9	211.0	241.4	240.1	253.8	252.3

Table. 20. LVC MOS 25 VOL – DUT 07622

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	236.0	237.2	166.9	169.5	194.1	197.8	214.7	219.7	244.3	251.7	256.9	265.7
EPCSRST_N_0	B31	235.2	235.4	167.7	168.2	195.8	196.4	217.5	218.0	248.5	249.4	262.2	263.2
EPCSRST_N_1	B32	234.1	234.5	166.3	166.7	193.8	194.3	214.6	214.9	244.9	245.6	258.0	258.7
EPCSRST_N_2	B34	236.1	236.6	168.2	168.8	196.3	197.1	217.5	218.0	248.8	249.6	262.2	263.3
EPCSRST_N_3	B35	235.5	235.9	166.9	167.3	194.3	194.8	215.0	215.3	244.8	245.4	257.8	258.4
EPCSRST_N_4	B36	236.7	237.2	169.5	169.9	198.1	198.7	219.9	220.2	252.3	253.0	266.2	267.1
EPCSRST_N_5	B37	235.5	235.9	167.9	168.3	195.7	196.3	216.8	217.2	247.9	248.4	260.9	261.7
MONITOR	K23	234.8	235.1	166.2	166.4	193.4	193.5	213.1	213.2	242.3	242.7	254.9	255.3
PLL_MON	L20	233.9	234.5	163.4	164.7	188.8	190.9	207.5	210.1	233.5	237.4	244.3	248.8
TOGGLE_MON	L22	235.6	235.4	166.4	166.3	193.5	193.0	213.3	212.6	242.7	241.7	254.8	253.8

Table. 21. LVC MOS 25 VOL – DUT 07640

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	235.1	236.1	166.4	168.7	193.6	197.1	214.3	218.9	243.9	251.0	256.6	265.1
EPCSRST_N_0	B31	234.2	234.5	167.2	167.6	195.3	195.7	216.8	217.4	248.1	248.8	261.7	262.4
EPCSRST_N_1	B32	234.1	234.4	166.1	166.5	193.7	194.2	214.2	214.4	244.7	245.2	257.8	258.4
EPCSRST_N_2	B34	235.7	236.0	167.9	168.4	195.9	196.5	217.2	217.3	248.3	249.1	261.8	262.6
EPCSRST_N_3	B35	235.0	235.3	166.6	167.0	194.2	194.6	214.6	214.6	244.5	245.0	257.3	257.9
EPCSRST_N_4	B36	236.4	236.6	169.0	169.4	197.5	198.1	219.0	219.2	251.1	251.8	265.0	266.0
EPCSRST_N_5	B37	235.0	235.3	167.5	167.7	195.3	195.8	216.2	216.2	247.0	247.3	260.1	260.6
MONITOR	K23	234.5	234.6	165.9	166.1	192.8	193.1	212.5	213.0	241.7	242.2	254.1	254.8
PLL_MON	L20	233.4	234.0	162.9	164.2	188.3	190.2	206.9	209.0	232.8	236.5	243.5	247.9
TOGGLE_MON	L22	234.3	234.0	165.7	165.6	192.7	192.4	212.6	211.8	242.0	241.0	254.4	253.1

Table. 22. LVTTL VOH – DUT 07573

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.918	2.915	2.909	2.906	2.892	2.886	2.875	2.866	2.858	2.847
EPCSRST_N_0	B31	2.917	2.916	2.908	2.907	2.889	2.888	2.870	2.869	2.852	2.850
EPCSRST_N_1	B32	2.918	2.917	2.909	2.908	2.891	2.890	2.873	2.872	2.856	2.854
EPCSRST_N_2	B34	2.917	2.916	2.908	2.906	2.888	2.887	2.870	2.868	2.851	2.849
EPCSRST_N_3	B35	2.918	2.917	2.909	2.908	2.891	2.890	2.874	2.872	2.857	2.855
EPCSRST_N_4	B36	2.916	2.915	2.906	2.905	2.887	2.885	2.867	2.866	2.848	2.845
EPCSRST_N_5	B37	2.917	2.916	2.908	2.907	2.890	2.889	2.872	2.870	2.853	2.852
MONITOR	K23	2.919	2.918	2.911	2.910	2.894	2.894	2.878	2.877	2.861	2.861
PLL_MON	L20	2.922	2.920	2.915	2.913	2.901	2.898	2.888	2.883	2.875	2.869
TOGGLE_MON	L22	2.920	2.919	2.911	2.911	2.895	2.895	2.878	2.879	2.862	2.862

Table. 23. LVTTL VOH – DUT 07585

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.918	2.915	2.909	2.906	2.893	2.886	2.876	2.867	2.859	2.848
EPCSRST_N_0	B31	2.918	2.917	2.909	2.907	2.890	2.889	2.872	2.869	2.853	2.851
EPCSRST_N_1	B32	2.919	2.917	2.910	2.908	2.892	2.890	2.875	2.873	2.857	2.854
EPCSRST_N_2	B34	2.917	2.916	2.908	2.906	2.890	2.888	2.871	2.869	2.853	2.850
EPCSRST_N_3	B35	2.919	2.917	2.910	2.908	2.892	2.891	2.875	2.873	2.858	2.856
EPCSRST_N_4	B36	2.917	2.916	2.908	2.906	2.888	2.886	2.869	2.867	2.850	2.847
EPCSRST_N_5	B37	2.918	2.917	2.909	2.907	2.891	2.889	2.873	2.871	2.855	2.852
MONITOR	K23	2.920	2.919	2.911	2.910	2.894	2.894	2.877	2.878	2.861	2.861
PLL_MON	L20	2.922	2.920	2.916	2.913	2.902	2.898	2.889	2.884	2.876	2.869
TOGGLE_MON	L22	2.920	2.919	2.912	2.911	2.896	2.895	2.880	2.879	2.863	2.863

Table. 24. LVTTL VOH – DUT 07596

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.919	2.917	2.911	2.907	2.894	2.888	2.877	2.868	2.860	2.849
EPCSRST_N_0	B31	2.918	2.917	2.909	2.908	2.890	2.889	2.872	2.871	2.854	2.852
EPCSRST_N_1	B32	2.920	2.918	2.910	2.909	2.893	2.891	2.875	2.874	2.857	2.856
EPCSRST_N_2	B34	2.917	2.916	2.909	2.907	2.890	2.888	2.871	2.870	2.853	2.851
EPCSRST_N_3	B35	2.918	2.917	2.910	2.909	2.892	2.891	2.875	2.874	2.858	2.856
EPCSRST_N_4	B36	2.917	2.916	2.907	2.906	2.888	2.886	2.869	2.867	2.849	2.847
EPCSRST_N_5	B37	2.918	2.917	2.909	2.908	2.891	2.890	2.873	2.871	2.855	2.853
MONITOR	K23	2.921	2.920	2.913	2.912	2.896	2.895	2.880	2.879	2.863	2.863
PLL_MON	L20	2.923	2.922	2.916	2.914	2.903	2.900	2.890	2.885	2.877	2.870
TOGGLE_MON	L22	2.921	2.921	2.913	2.912	2.896	2.896	2.880	2.880	2.864	2.864

Table. 25. LVTTL VOH – DUT 07617

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.918	2.916	2.910	2.906	2.893	2.886	2.876	2.866	2.859	2.846
EPCSRST_N_0	B31	2.918	2.917	2.909	2.908	2.890	2.889	2.871	2.870	2.853	2.852
EPCSRST_N_1	B32	2.919	2.918	2.910	2.909	2.892	2.891	2.874	2.873	2.857	2.855
EPCSRST_N_2	B34	2.918	2.916	2.908	2.907	2.889	2.888	2.870	2.869	2.852	2.850
EPCSRST_N_3	B35	2.918	2.917	2.909	2.908	2.892	2.891	2.875	2.873	2.857	2.856
EPCSRST_N_4	B36	2.917	2.916	2.907	2.906	2.887	2.886	2.868	2.866	2.848	2.846
EPCSRST_N_5	B37	2.917	2.916	2.908	2.907	2.890	2.889	2.872	2.871	2.854	2.852
MONITOR	K23	2.920	2.919	2.912	2.911	2.895	2.895	2.879	2.878	2.862	2.862
PLL_MON	L20	2.922	2.921	2.914	2.913	2.900	2.899	2.886	2.884	2.872	2.870
TOGGLE_MON	L22	2.920	2.920	2.912	2.912	2.895	2.896	2.879	2.880	2.863	2.864

Table. 26. LVTTL VOH – DUT 07622

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.917	2.915	2.909	2.905	2.892	2.886	2.875	2.867	2.858	2.848
EPCSRST_N_0	B31	2.917	2.916	2.908	2.907	2.889	2.888	2.870	2.869	2.852	2.850
EPCSRST_N_1	B32	2.918	2.917	2.909	2.908	2.892	2.890	2.874	2.872	2.856	2.855
EPCSRST_N_2	B34	2.917	2.916	2.907	2.906	2.889	2.887	2.870	2.869	2.852	2.850
EPCSRST_N_3	B35	2.917	2.917	2.909	2.908	2.892	2.891	2.874	2.873	2.857	2.856
EPCSRST_N_4	B36	2.917	2.916	2.906	2.905	2.886	2.885	2.867	2.866	2.847	2.846
EPCSRST_N_5	B37	2.918	2.917	2.908	2.907	2.890	2.889	2.871	2.870	2.853	2.852
MONITOR	K23	2.919	2.918	2.910	2.910	2.894	2.893	2.878	2.877	2.861	2.861
PLL_MON	L20	2.921	2.920	2.914	2.912	2.901	2.898	2.888	2.883	2.875	2.869
TOGGLE_MON	L22	2.919	2.918	2.911	2.910	2.895	2.894	2.878	2.878	2.862	2.862

Table. 27. LVTTL VOH – DUT 07640

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.918	2.916	2.910	2.906	2.893	2.887	2.876	2.868	2.859	2.849
EPCSRST_N_0	B31	2.918	2.917	2.909	2.908	2.890	2.889	2.872	2.870	2.853	2.852
EPCSRST_N_1	B32	2.918	2.917	2.910	2.909	2.892	2.891	2.875	2.873	2.857	2.855
EPCSRST_N_2	B34	2.917	2.917	2.908	2.907	2.889	2.888	2.871	2.869	2.853	2.850
EPCSRST_N_3	B35	2.919	2.917	2.910	2.909	2.893	2.891	2.875	2.874	2.858	2.856
EPCSRST_N_4	B36	2.917	2.916	2.907	2.906	2.888	2.886	2.868	2.867	2.849	2.847
EPCSRST_N_5	B37	2.918	2.917	2.909	2.908	2.890	2.889	2.873	2.871	2.855	2.853
MONITOR	K23	2.920	2.919	2.912	2.911	2.895	2.894	2.879	2.878	2.863	2.862
PLL_MON	L20	2.922	2.920	2.916	2.913	2.902	2.898	2.889	2.884	2.876	2.870
TOGGLE_MON	L22	2.920	2.920	2.912	2.912	2.895	2.896	2.879	2.880	2.863	2.863

Table. 28. LVTTL VOL – DUT 07573

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	215.3	216.6	225.6	228.0	240.1	245.2	257.0	264.7	275.3	285.2
EPCSRST_N_0	B31	215.4	215.8	226.9	226.7	242.9	243.7	261.3	262.6	281.4	282.5
EPCSRST_N_1	B32	215.0	215.2	224.7	224.1	240.8	241.8	258.5	259.4	277.0	277.8
EPCSRST_N_2	B34	216.0	216.2	226.3	225.6	244.0	244.7	262.3	263.3	281.7	282.6
EPCSRST_N_3	B35	215.6	216.0	225.1	224.4	241.1	241.7	258.2	259.4	276.4	277.2
EPCSRST_N_4	B36	217.3	217.5	227.7	227.0	245.7	246.6	264.9	266.2	285.4	286.2
EPCSRST_N_5	B37	216.5	216.8	225.8	225.0	242.5	243.2	260.5	261.4	279.4	280.2
MONITOR	K23	214.6	215.1	223.6	223.9	238.8	239.3	255.0	255.5	272.3	272.8
PLL_MON	L20	213.4	214.2	221.2	221.8	232.7	235.5	246.3	250.0	260.1	265.1
TOGGLE_MON	L22	214.6	214.8	223.9	222.9	238.9	238.3	255.3	254.5	272.8	271.5

Table. 29. LVTTL VOL – DUT 07585

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	214.6	216.1	224.9	227.3	239.1	244.4	256.1	263.8	274.0	283.9
EPCSRST_N_0	B31	214.0	214.8	225.2	225.7	241.2	242.7	259.7	261.2	279.5	281.2
EPCSRST_N_1	B32	213.6	214.4	223.2	222.4	239.1	240.5	256.7	258.3	275.0	276.4
EPCSRST_N_2	B34	215.3	216.0	225.1	224.7	242.1	243.5	260.3	262.0	279.3	280.9
EPCSRST_N_3	B35	214.6	215.1	223.8	223.0	239.5	240.8	256.8	258.3	274.6	276.0
EPCSRST_N_4	B36	215.5	216.3	226.2	225.5	243.8	245.3	263.1	264.5	282.9	284.5
EPCSRST_N_5	B37	214.9	215.5	224.9	224.3	241.1	242.4	258.8	260.5	277.3	278.8
MONITOR	K23	213.8	214.0	222.7	223.3	238.5	238.3	255.4	254.5	272.8	271.6
PLL_MON	L20	212.3	213.0	220.2	220.9	231.8	234.7	244.7	249.2	258.6	264.0
TOGGLE_MON	L22	213.7	214.0	222.5	222.2	237.3	237.3	253.3	253.2	270.7	269.9

Table. 30. LVTTL VOL – DUT 07596

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	214.6	215.8	224.4	226.4	238.3	243.6	255.4	262.8	273.0	283.0
EPCSRST_N_0	B31	214.3	214.7	225.5	225.4	241.6	242.1	259.9	260.8	279.7	280.6
EPCSRST_N_1	B32	213.6	213.8	223.2	222.2	239.0	239.6	256.8	257.6	275.0	275.7
EPCSRST_N_2	B34	215.3	215.8	225.3	224.6	242.3	243.2	260.6	261.8	279.7	280.7
EPCSRST_N_3	B35	215.1	215.2	224.5	223.4	240.0	240.5	257.1	257.8	274.9	275.4
EPCSRST_N_4	B36	216.1	216.4	226.7	225.7	244.4	245.1	263.6	264.6	283.7	284.5
EPCSRST_N_5	B37	214.9	215.2	225.0	223.9	241.5	242.0	259.2	259.9	277.7	278.4
MONITOR	K23	213.1	213.4	221.5	222.2	237.1	237.4	253.4	253.7	270.3	270.9
PLL_MON	L20	212.0	212.7	220.1	220.2	231.1	233.9	244.2	248.4	258.1	263.4
TOGGLE_MON	L22	213.3	213.0	222.3	221.2	237.4	237.0	253.6	252.8	270.8	269.4

Table. 31. LVTTL VOL – DUT 07617

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	214.8	216.1	224.7	227.0	239.1	244.8	256.0	264.6	274.1	285.4
EPCSRST_N_0	B31	214.4	214.6	225.5	225.3	241.7	242.3	259.9	260.6	279.7	280.5
EPCSRST_N_1	B32	214.0	214.0	223.5	222.6	239.7	240.2	257.1	257.8	275.4	276.0
EPCSRST_N_2	B34	215.0	215.2	225.2	224.3	242.4	243.2	261.0	262.1	280.2	281.1
EPCSRST_N_3	B35	214.7	214.9	224.3	223.3	240.0	240.7	257.2	258.1	275.3	275.8
EPCSRST_N_4	B36	216.3	216.3	226.6	225.7	244.5	245.6	264.2	264.9	284.3	285.0
EPCSRST_N_5	B37	215.4	215.9	225.1	224.3	241.6	242.2	259.6	260.4	278.4	278.9
MONITOR	K23	213.3	213.3	222.2	222.7	237.3	237.9	253.7	254.0	270.9	271.1
PLL_MON	L20	212.9	212.8	221.1	220.4	233.6	234.2	247.7	248.6	262.5	263.4
TOGGLE_MON	L22	213.3	213.3	222.5	221.3	237.5	236.6	253.9	252.8	271.1	269.6

Table. 32. LVTTL VOL – DUT 07622

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	216.2	217.4	226.6	228.9	240.4	245.3	257.0	264.5	275.0	284.8
EPCSRST_N_0	B31	215.8	216.0	226.9	227.1	243.1	243.6	261.3	262.3	281.1	282.1
EPCSRST_N_1	B32	214.9	215.1	224.5	224.2	240.3	241.1	258.3	258.9	276.4	277.1
EPCSRST_N_2	B34	216.5	216.8	226.6	226.6	243.7	244.4	261.9	262.9	281.1	282.1
EPCSRST_N_3	B35	216.1	216.2	225.3	224.8	241.1	241.4	258.4	258.9	276.0	276.6
EPCSRST_N_4	B36	217.2	217.4	228.0	227.7	246.1	246.7	265.4	266.4	285.8	286.8
EPCSRST_N_5	B37	216.0	216.3	226.2	225.7	242.8	243.6	261.1	261.9	279.9	280.5
MONITOR	K23	215.0	214.9	223.9	224.1	239.0	239.4	255.2	255.6	272.6	272.8
PLL_MON	L20	214.1	214.7	222.1	223.0	233.4	236.1	246.3	250.6	260.4	265.6
TOGGLE_MON	L22	215.5	215.4	224.3	224.0	239.1	238.8	255.5	254.5	272.7	271.4

Table. 33. LVTTL VOL – DUT 07640

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	215.4	216.5	226.1	227.9	239.9	245.0	256.8	263.9	274.7	284.2
EPCSRST_N_0	B31	214.9	215.2	226.3	226.3	242.1	242.9	260.8	261.6	280.6	281.6
EPCSRST_N_1	B32	215.0	215.2	224.4	223.5	240.5	241.0	257.8	258.7	276.3	276.9
EPCSRST_N_2	B34	216.4	216.6	226.7	225.6	243.2	244.2	261.6	262.6	280.7	281.7
EPCSRST_N_3	B35	215.6	215.7	225.0	224.2	240.7	241.4	257.8	258.8	275.5	276.3
EPCSRST_N_4	B36	217.1	217.3	227.4	226.7	245.4	246.2	264.4	265.5	284.6	285.6
EPCSRST_N_5	B37	216.0	215.8	225.6	224.6	242.3	243.0	260.3	261.2	278.9	279.5
MONITOR	K23	214.6	214.8	223.5	223.8	238.6	239.1	254.9	255.3	271.8	272.6
PLL_MON	L20	214.0	214.4	221.2	221.5	232.7	235.3	245.7	249.7	259.9	264.9
TOGGLE_MON	L22	214.6	214.5	223.6	222.7	238.5	238.0	254.9	254.1	272.2	270.8

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (μs)	Post-irradiation (μs)	Change Degradation (%)
07573	125 krad	0.461	0.465	0.87
07585	125 krad	0.465	0.468	0.65
07596	125 krad	0.468	0.471	0.64
07617	125 krad	0.467	0.469	0.43
07622	125 krad	0.469	0.472	0.64
07640	125 krad	0.466	0.468	0.43

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

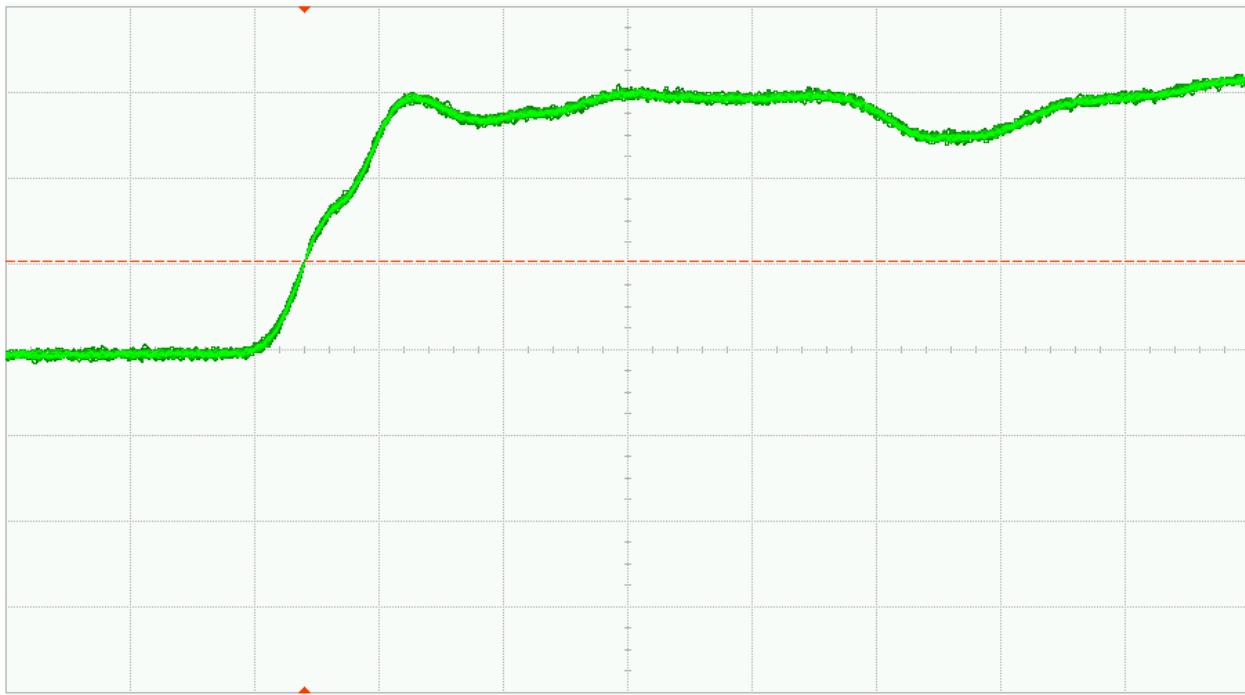


Fig. 26 (a). DUT 07573 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

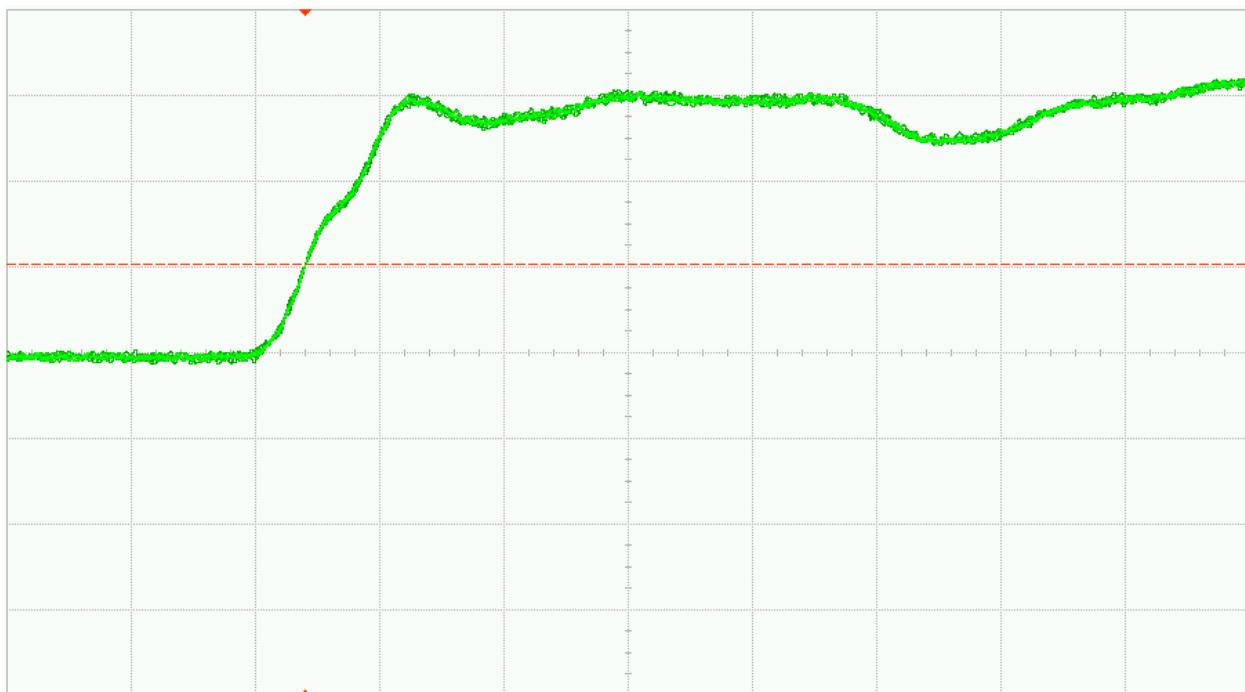


Fig. 26 (b). DUT 07573 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

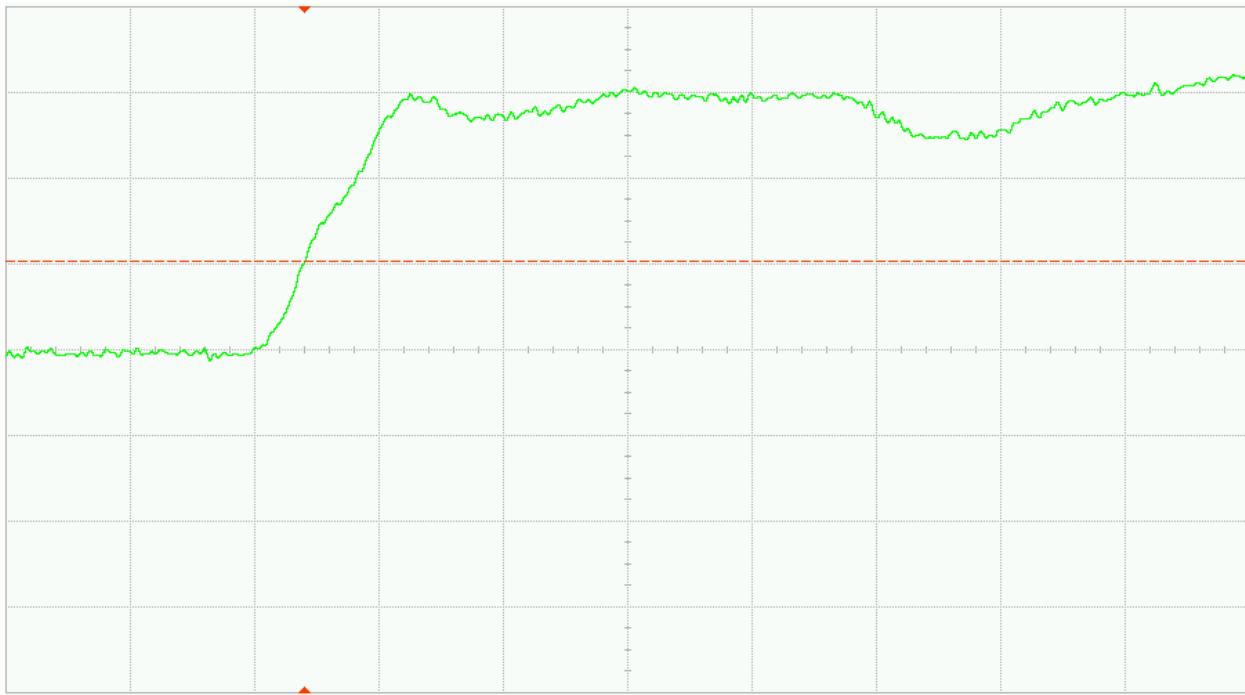


Fig. 27 (a). DUT 07585 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

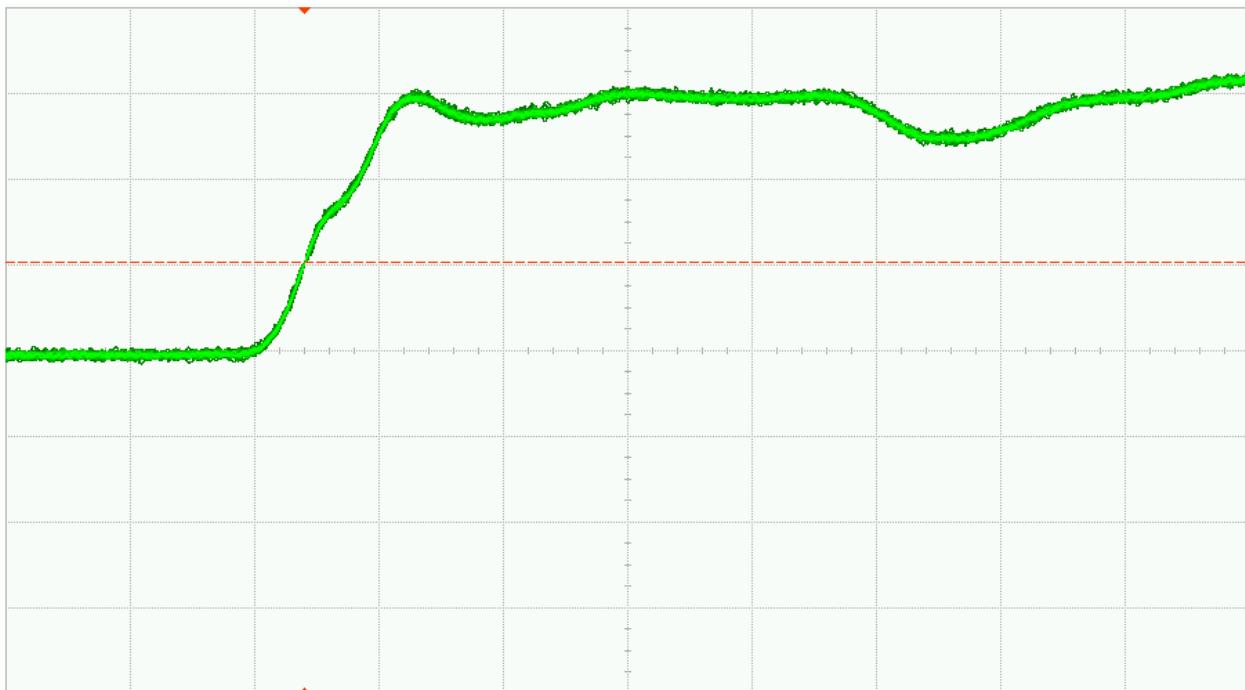


Fig. 27 (b). DUT 07585 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

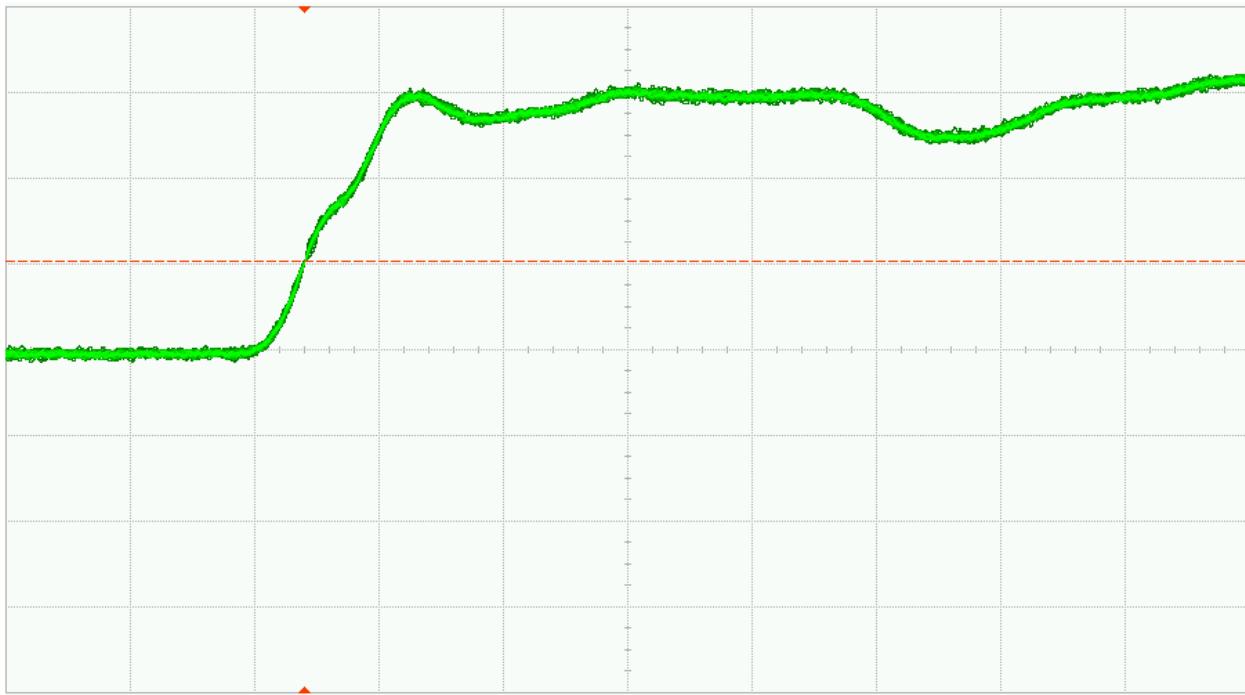


Fig. 28 (a). DUT 07596 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

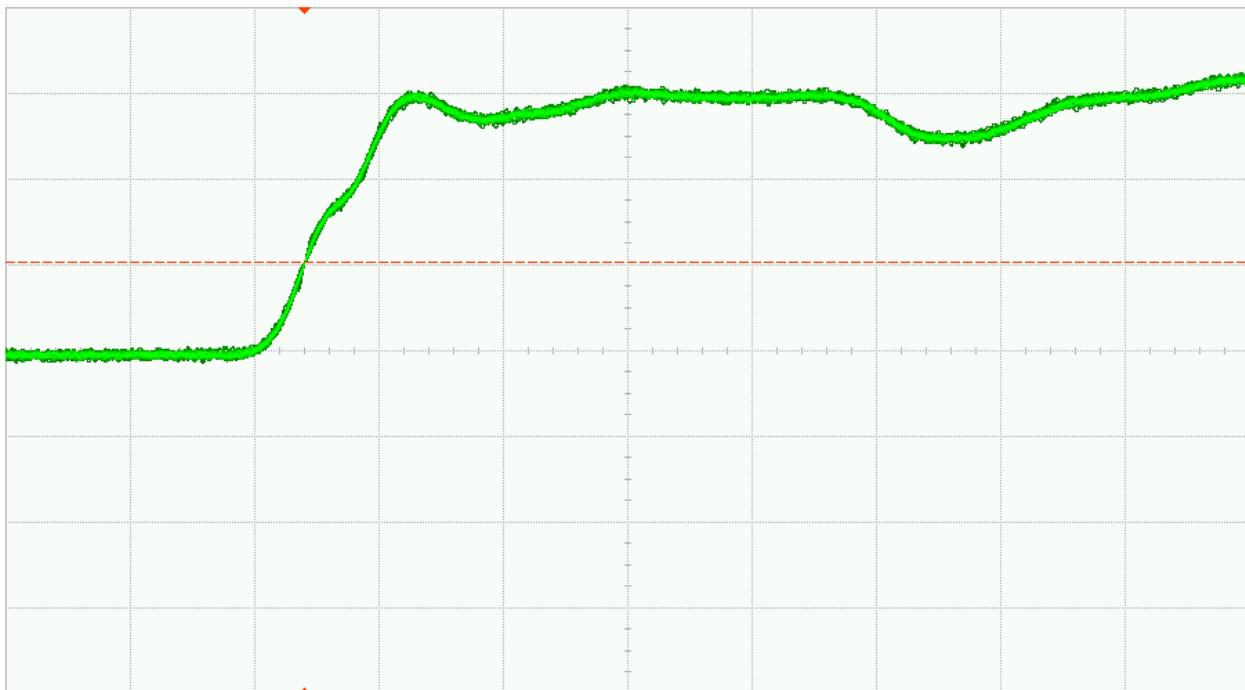


Fig. 28 (b). DUT 07596 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

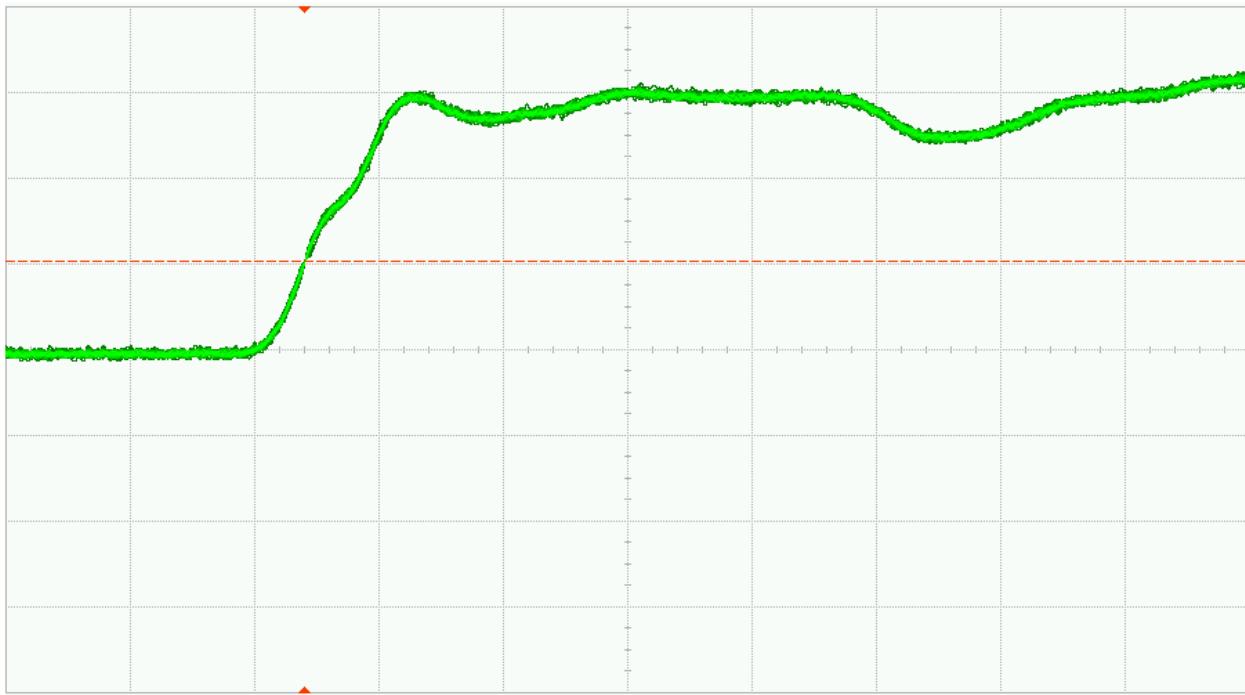


Fig. 29 (a). DUT 07617 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

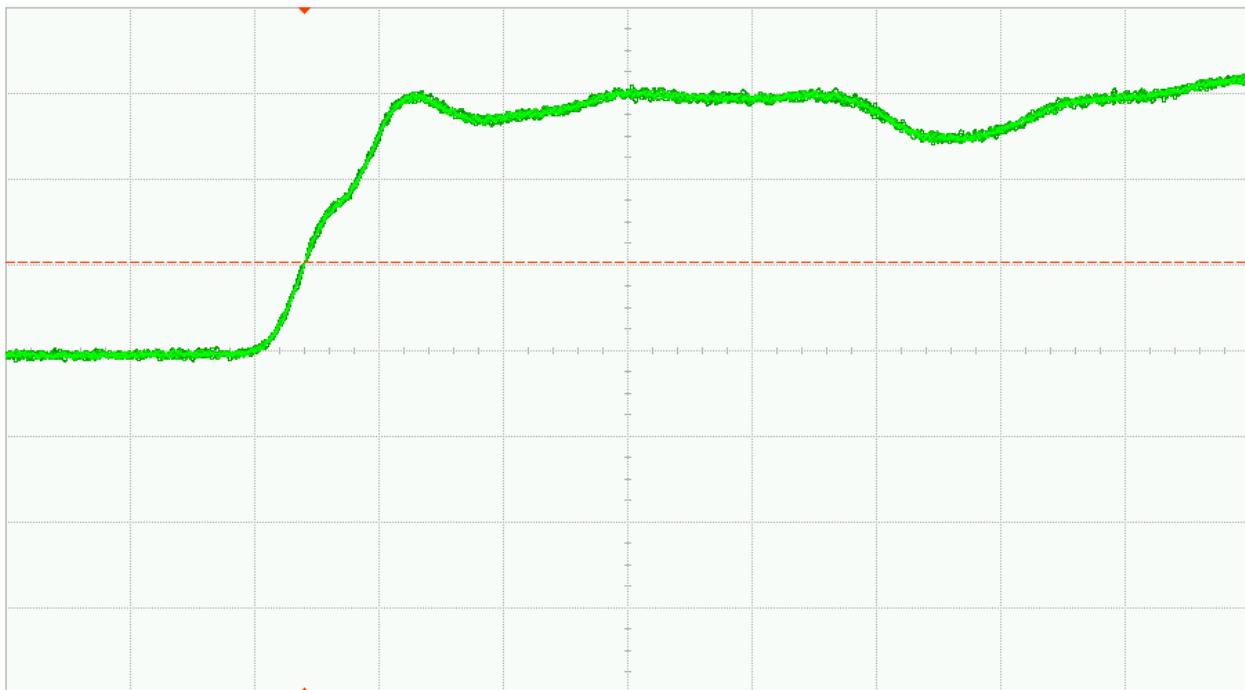


Fig. 29 (b). DUT 07617 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

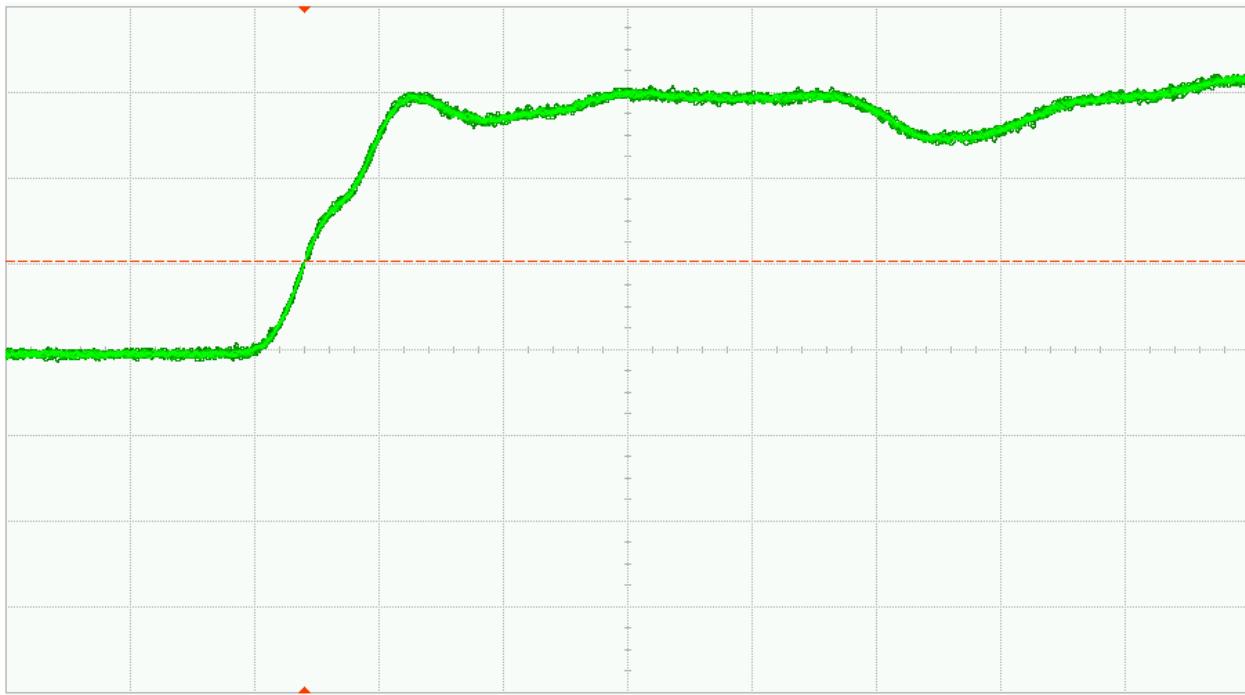


Fig. 30 (a). DUT 07622 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

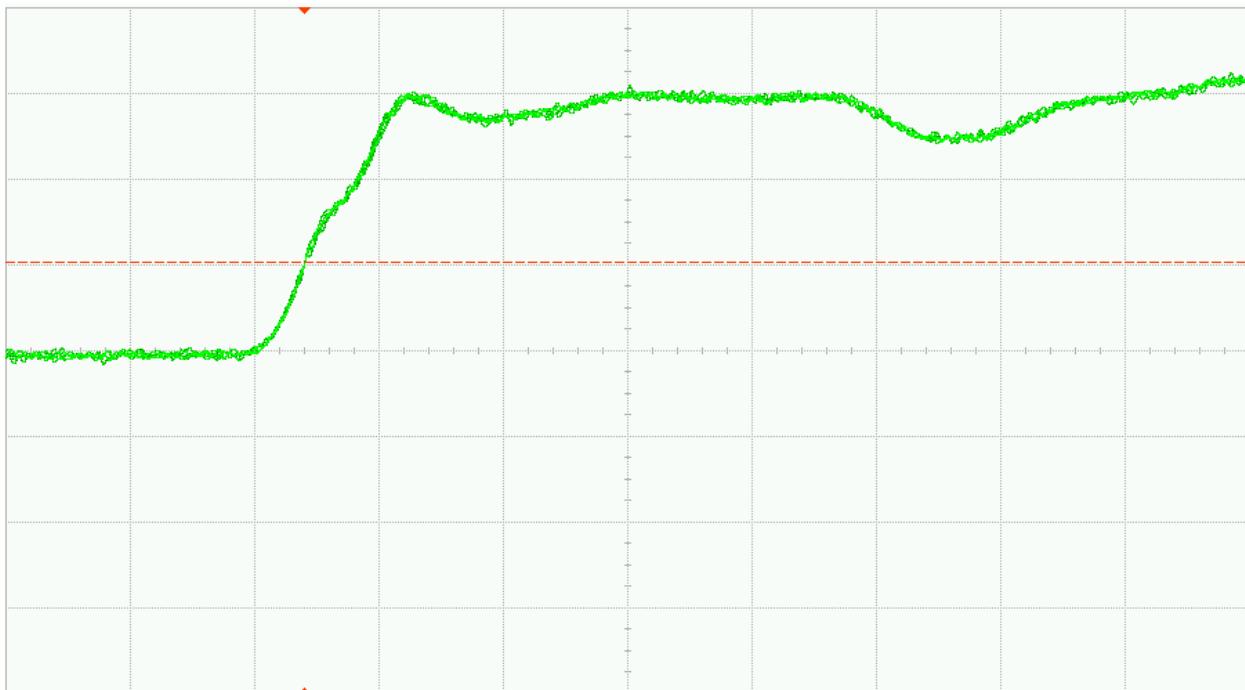


Fig. 30 (b). DUT 07622 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

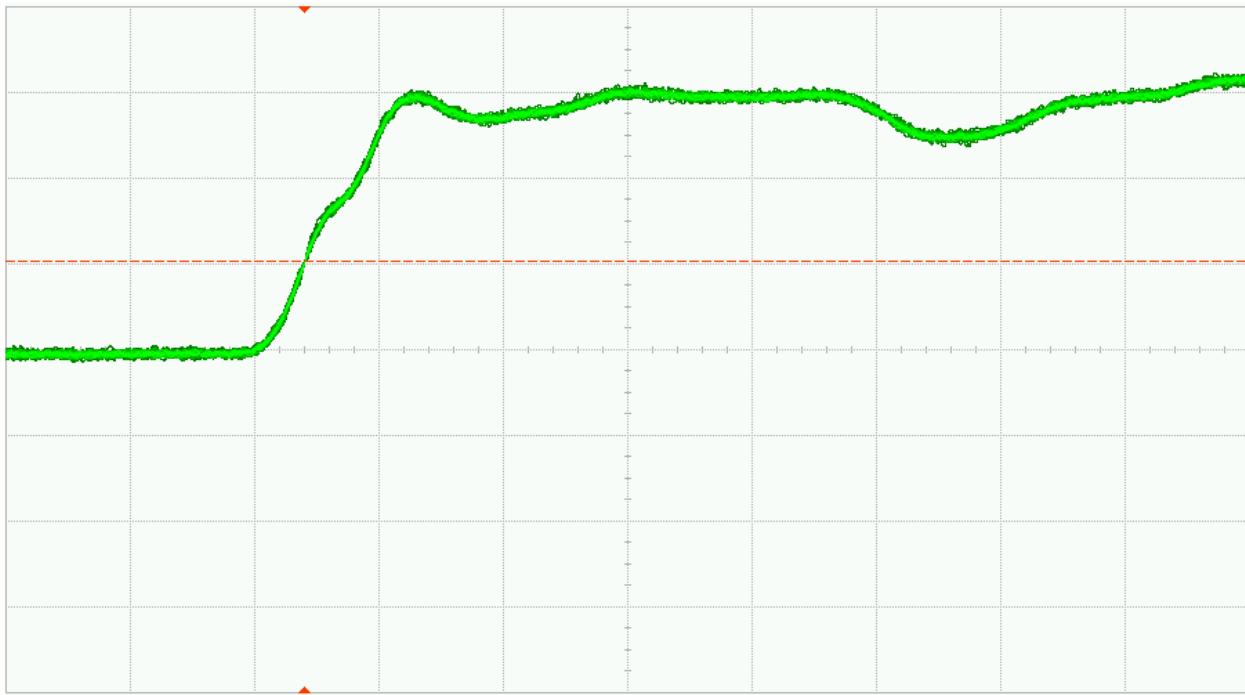


Fig. 31 (a). DUT 07640 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

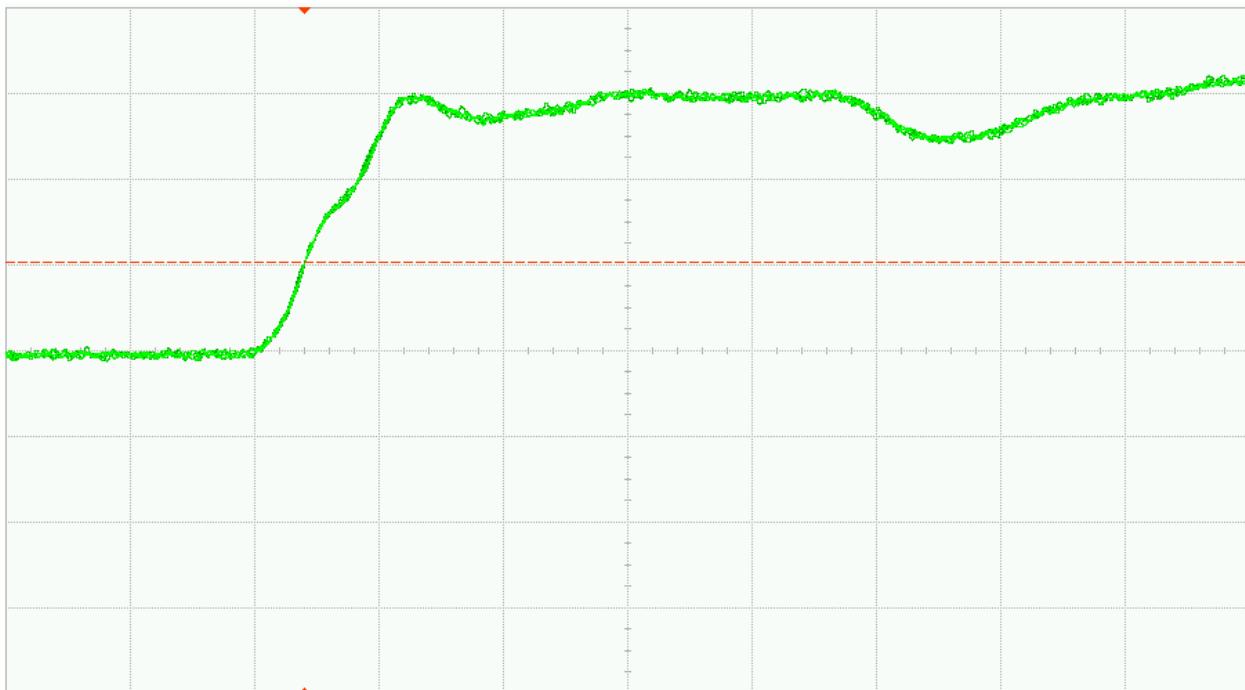


Fig. 31 (b). DUT 07640 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 32 (a). DUT 07573 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 32 (b). DUT 07573 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 33 (a). DUT 07585 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 33 (b). DUT 07585 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 34 (a). DUT 07596 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 34 (b). DUT 07596 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

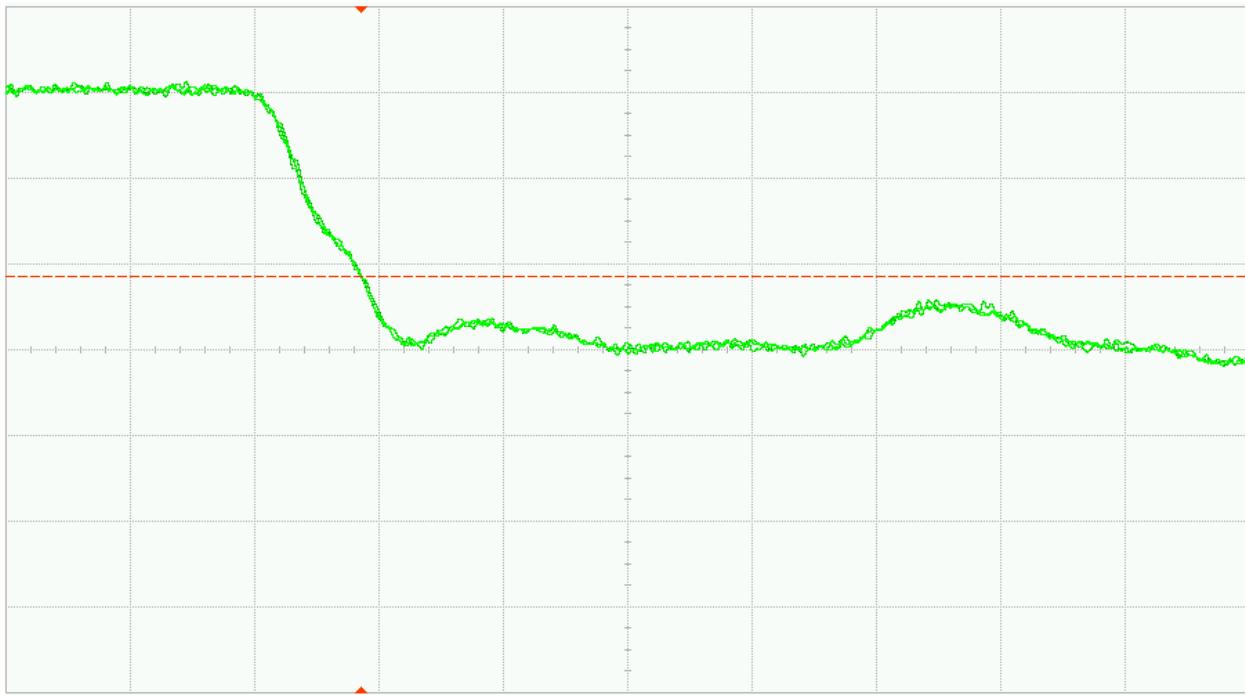


Fig. 35 (a). DUT 07617 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 35 (b). DUT 07617 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 36 (a). DUT 07622 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

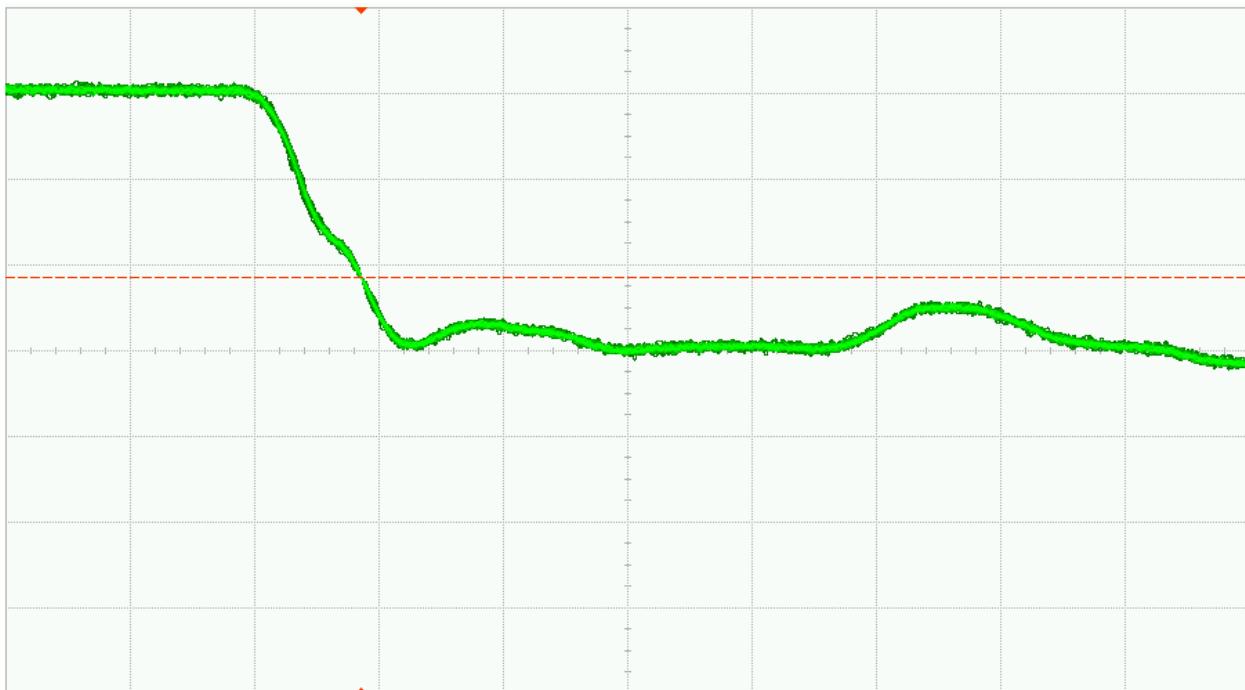


Fig. 36 (b). DUT 07622 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 37 (a). DUT 07640 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

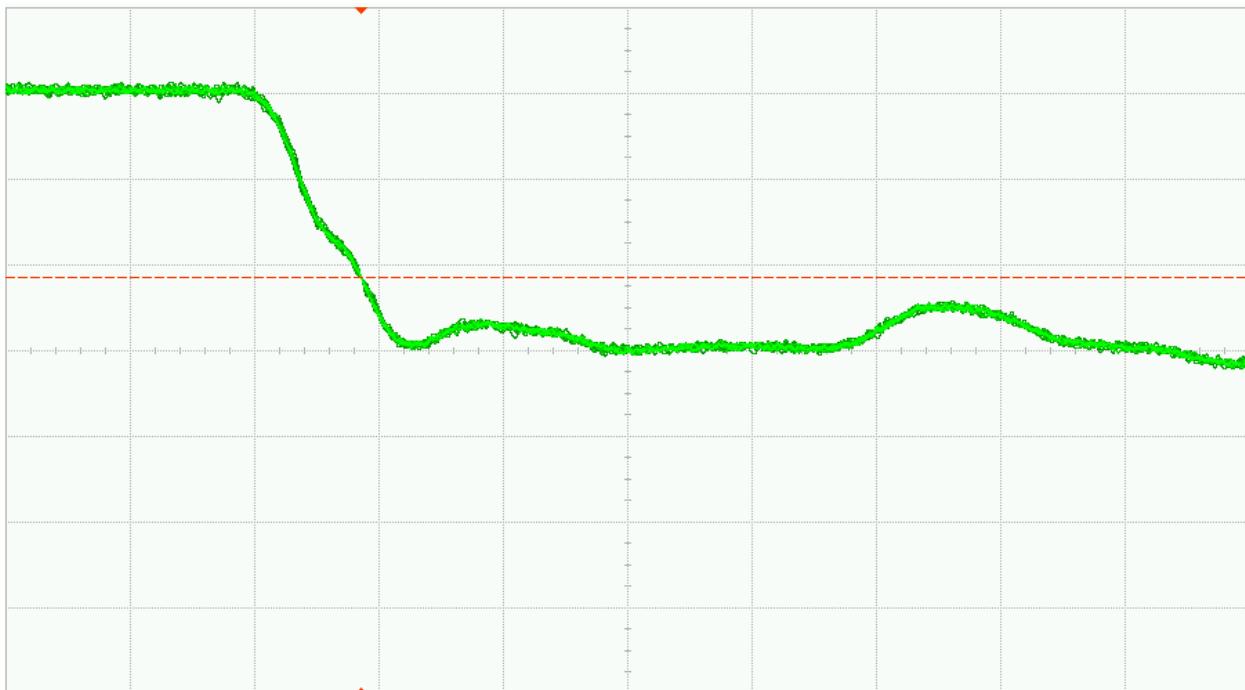


Fig. 37 (b). DUT 07640 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 μ RAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

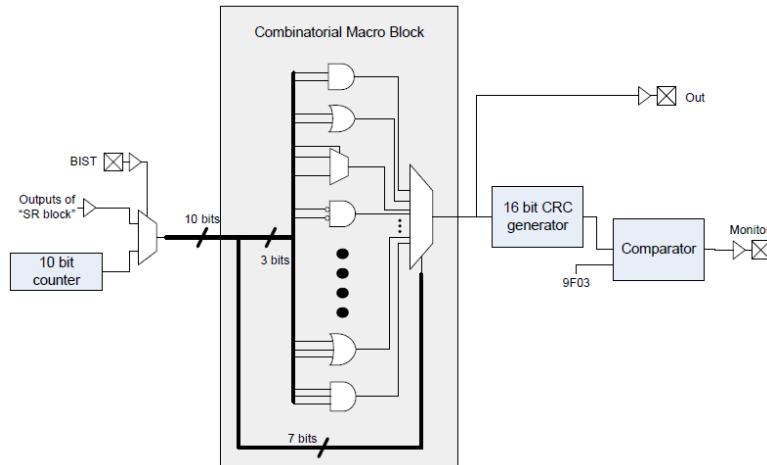


Fig. 38. Combo Block

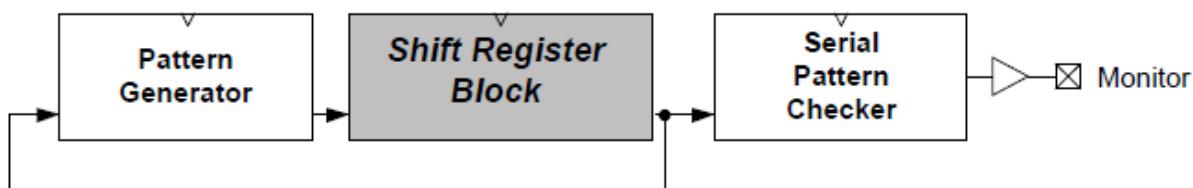


Fig. 39. Shift Register Block

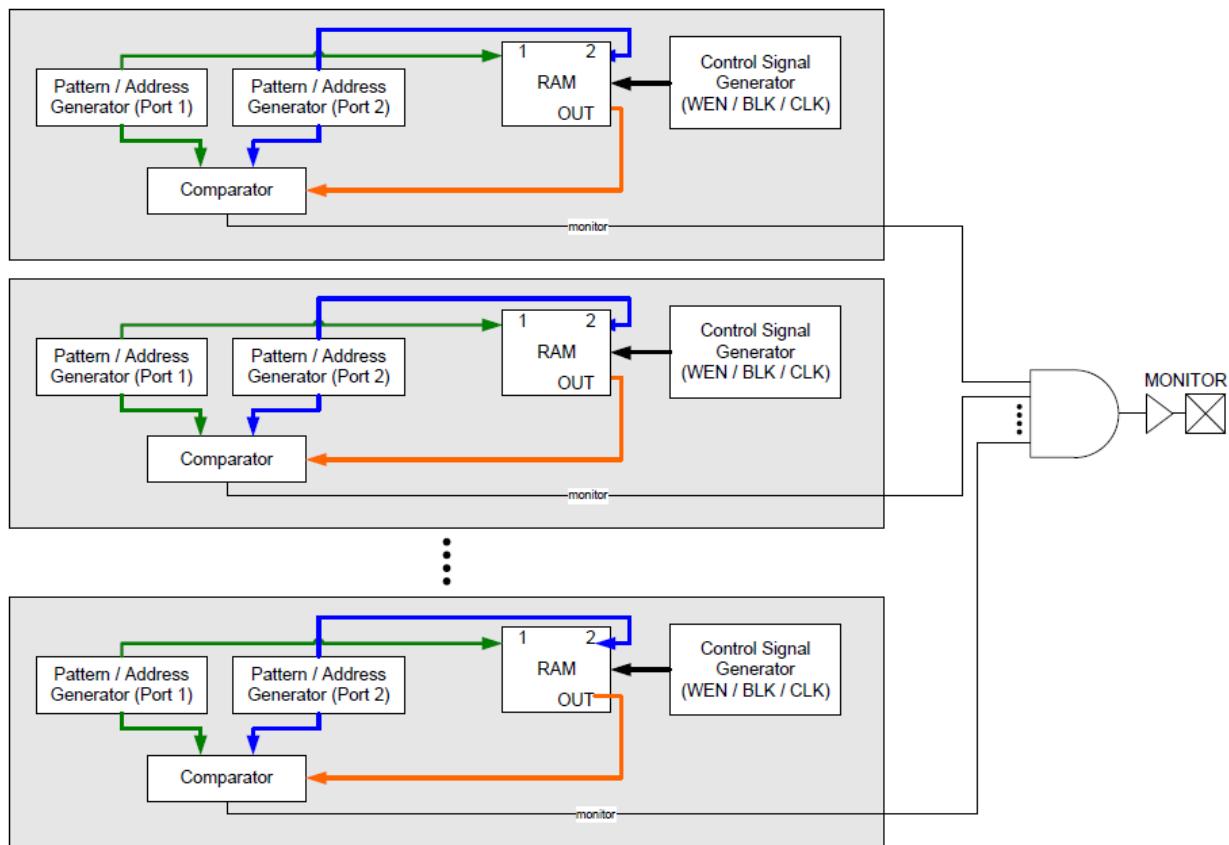


Fig. 40. Embedded Ram Blocks

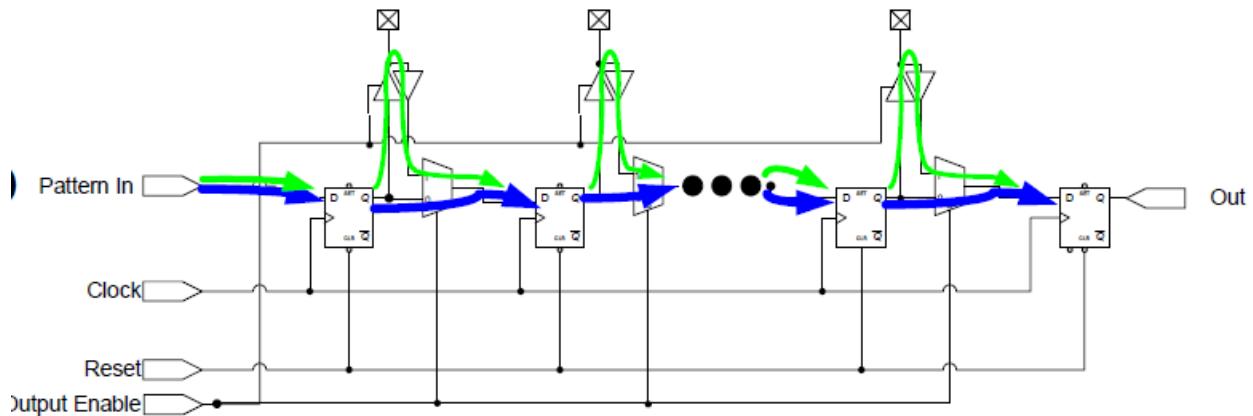


Fig. 41. IO Block

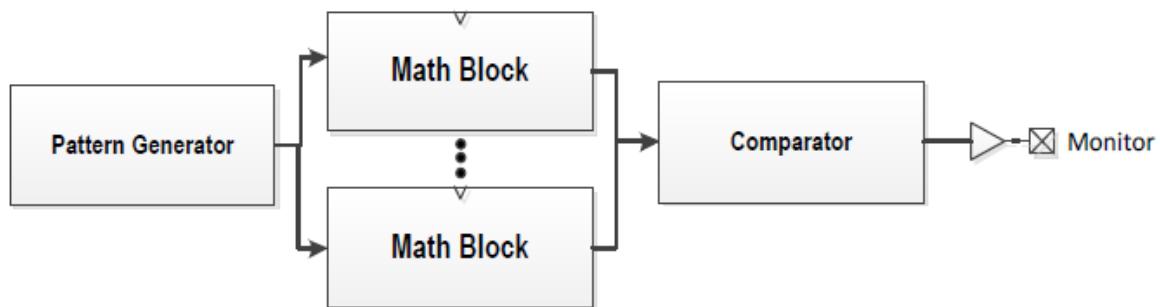


Fig. 42. Math Block



**Total Ionizing Dose Test Report
No. 22T-RT4G150-LG1657- K7KAR**

Rev. 0



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