PolarFire® FPGA H.264 Encoder IP User Guide

Introduction

H.264 is a popular video compression standard for compression of digital video. It is also known as MPEG-4 Part10 or Advanced Video Coding (MPEG-4 AVC). H.264 uses block wise approach for compressing the video where the block size is defined as 16x16 and such block is called a macro block. The compression standard supports various profiles that define the compression ratio and complexity of implementation. The video frames to be compressed are treated as *I* frame, *P* frame and *B* frame. An *I* frame is an intra-coded frame where compression is done by using the information contained within the frame. No other frames are required to decode an *I* frame. A *P* frame is compressed by using the changes with respect to an earlier frame that can be an *I* frame or a *P* frame. The compression of *B* frame is done by using the motion changes with respect to both an earlier frame and an upcoming frame.

The *I* frame compression process has four stages—Intra prediction, Integer transformation, Quantization and Entropy encoding. H.264 supports two types of encoding—Context Adaptive Variable Length Coding (CAVLC) and Context Adaptive Binary Arithmetic Coding (CABAC). The current version of the IP implements Baseline profile and uses CAVLC for entropy encoding. Also, the IP supports encoding of only *I* frames.

Key Features

- Implements compression on YCbCr 420 video format
- Expects the input in YCbCr 422 video format
- Supports 8-bit for each component (Y, Cb, and Cr)
- ITU-T H.264 Annex B compliant NAL byte stream output
- Standalone operation, CPU, or processor assistance not required
- User configurable quality factor QP during run time
- Computation at the rate of 1 pixel per clock
- Supports compression up to resolution of 1080p 60 fps

Supported Families

- PolarFire® SoC FPGA
- PolarFire® FPGA

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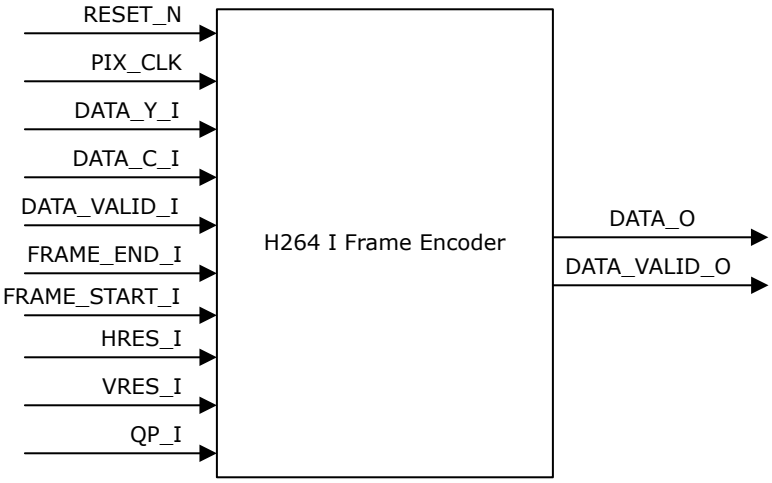
1. Hardware Implementation

The following figure shows the H.264 *I* frame Encoder IP block diagram.

Figure 1-1. H.264 I Frame Encoder IP Block Diagram



1.1 Inputs and Outputs

The following table lists the input and output ports of H.264 Frame Encoder IP.

Table 1-1. Input and Output Ports of H.264 I Frame Encoder IP

Signal Name	Direction	Width	Port Valid Under	Description
RESET_N	Input	1	—	Active-low Asynchronous reset signal to the design.
SYS_CLK	Input	1	—	Input clock with which incoming pixels are sampled.
DATA_Y_I	Input	8	—	8-bit Luma pixel input in 422 format.
DATA_C_I	Input	8	—	8-bit Chroma pixel input in 422 format.
DATA_VALID_I	Input	1	—	Input Pixel data valid signal.
FRAME_END_I	Input	1	—	End of Frame indication.
FRAME_START_I	Input	1	—	Start of Frame indication. The rising edge of this signal is considered as frame start.
HRES_I	Input	16	—	Horizontal resolution of input image. It must be multiple of 16.
VRES_I	Input	16	—	Vertical resolution of input image. It must be multiple of 16.
QP_I	Input	6	—	Quality factor for H.264 quantization. The value ranges from 0 to 51 where 0 represents highest quality and lowest compression and 51 represents highest compression.
DATA_O	Output	8	—	H.264 encoded data output that contains NAL unit, slice header, SPS, PPS, and the encoded data of macro blocks.
DATA_VALID_O	Output	1	—	Signal denoting encoded data is valid.

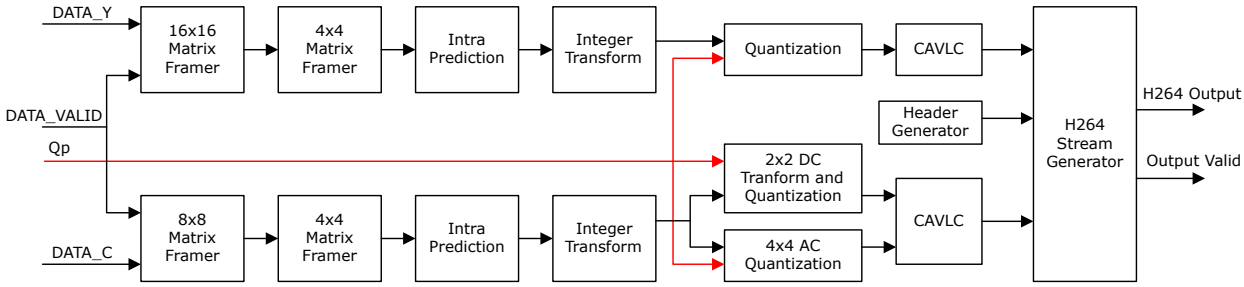
1.2 Configuration Parameters

The H.264 / Frame Encoder IP does not use configuration parameters.

1.3 Hardware Implementation of H.264 I Frame Encoder IP

The following figure shows the H.264 / Frame Encoder IP block diagram.

Figure 1-2. H.264 I Frame Encoder IP Block Diagram



1.3.1 Design Description for H.264 I Frame Encoder IP

This section describes the different internal modules of the H.264 / frame generator IP. Data input to the IP must be in the form of a raster scan image in YCbCr 422 format. The IP uses 422 format as input and implements compression in 420 format.

1.3.1.1 16x16 Matrix Framer

This module frames the 16x16 macro blocks for Y component as per H.264 specification. Line buffers are used to store 16 horizontal lines of input image and a 16x16 matrix is framed using shift registers.

1.3.1.2 8x8 Matrix Framer

This module frames the 8x8 macro blocks for C component as per H.264 specification for 420 format. Line buffers are used to store 8 horizontal lines of input image and an 8x16 matrix is framed using shift registers. From the 8x16 matrix, the Cb and Cr components are separated to frame each 8x8 matrix.

1.3.1.3 4x4 Matrix Framer

The integer transform, quantization, and CAVLC encoding operate on a 4x4 sub-block within a macro block. The 4x4 matrix framer generates a 4x4 sub-block from 16x16 or 8x8 macro block. This matrix generator spans through all the sub-blocks of a macro block before going to the next macro block.

1.3.1.4 Intra Prediction

H.264 uses various intra-prediction modes to reduce the information in a 4x4 block. The intra-prediction block in the IP uses only DC prediction on 4x4 matrix size. The DC component is computed from the adjacent top and left 4x4 blocks.

1.3.1.5 Integer Transform

H.264 uses integer discrete cosine transform where the coefficients are distributed across the integer transform matrix and the quantization matrix such that there are no multiplications or divisions in the integer transform. The integer transform stage implements the transformation using shift and add operations.

1.3.1.6 Quantization

The quantization multiplies each output of integer transform with a predetermined quantization value defined by the QP user input value. The range of QP value is from 0 to 51. Any value more than 51 is clamped to 51. A lower QP value denotes lower compression and higher quality and vice versa.

1.3.1.7 CAVLC

H.264 uses two types of entropy encoding—Context Adaptive Variable Length Coding (CAVLC) and Context Adaptive Binary Arithmetic Coding (CABAC). The IP uses CAVLC for encoding the quantized output.

1.3.1.8 Header Generator

The header generator block generates the block headers, slice headers, Sequence Parameter Set (SPS), Picture Parameter Set (PPS), and Network Abstraction Layer (NAL) unit depending on the instance of the video frame.

1.3.1.9 H.264 Stream Generator

The H.264 stream generator block combines the CAVLC output along with the headers to create the encoded output as per the H.264 standard format.

2. Testbench

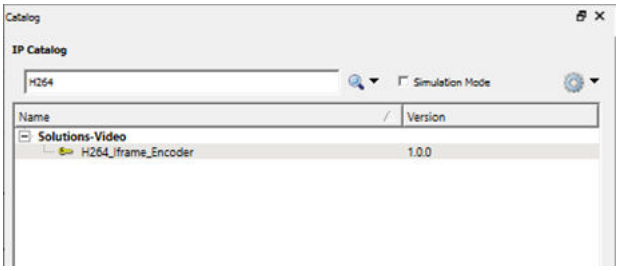
Testbench is provided to check the functionality of H.264 *I* frame Encoder IP.

2.1 Simulation

The simulation uses a 224x224 image in YCbCr422 format represented by two files, each for Y and C as input and generates a H.264 file format that contains two frames. The following steps describe how to simulate the core using the testbench.

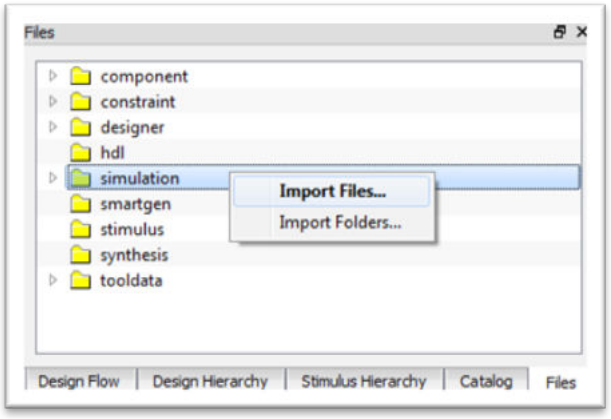
1. Go to Libero SoC **Catalog** > **View** > **Windows** > **Catalog**, and then expand **Solutions-Video**. Double-click **H264_Iframe_Encoder**, and then click **OK**.

   Figure 2-1. H.264 I Frame Encoder IP Core in Libero SoC Catalog



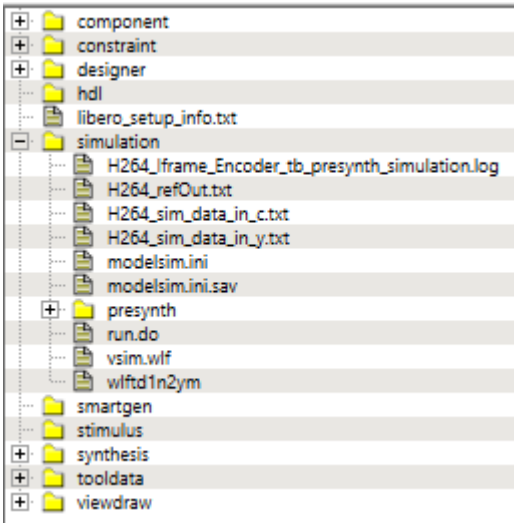
2. Go to the **Files** tab and select **simulation** > **Import Files**.

   Figure 2-2. Import Files



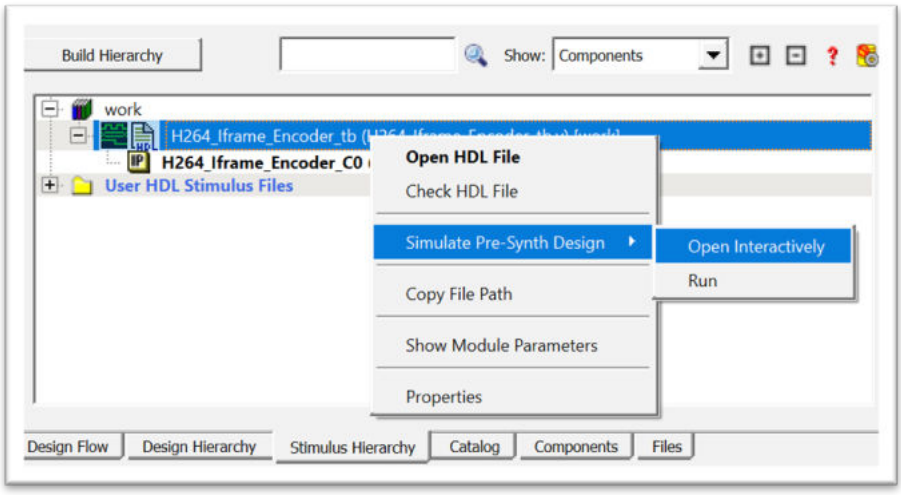
3. Import the `H264_sim_data_in_y.txt`, `H264_sim_data_in_c.txt`, and `H264_refOut.txt` files from the following path: `..\<Project_name>\component\Microsemi\SolutionCore\H264_Iframe_Encoder\ 1.0.0\Stimulus`.
4. To import a different file, browse the folder that contains the required file, and click **Open**. The imported file is listed under simulation, see the following figure.

Figure 2-3. Imported Files



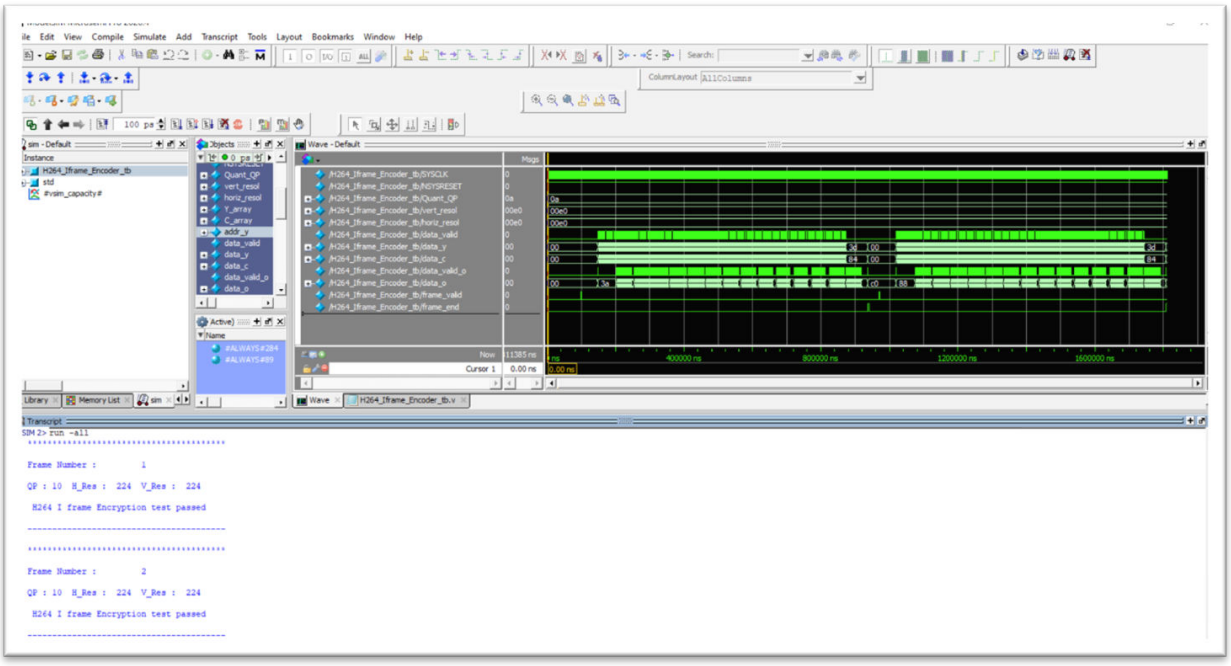
5. Go to the **Stimulus Hierarchy** tab and select **H264_frame_Encoder_tb (H264_frame_Encoder_tb. v)** > **Simulate Pre-Synth Design** > **Open Interactively**. The IP is simulated for two frames.

Figure 2-4. Simulating Pre-Synthesis Design



ModelSim opens with the testbench file as shown in the following figure.

Figure 2-5. ModelSim Simulation Window



Note: If the simulation is interrupted due to the runtime limit specified in the DO file, use the `run -all` command to complete the simulation.

3. License

H.264 / frame Encoder IP is provided in encrypted form only under license.

4. Installation Instructions

The core must be installed into Libero SoC software. It is done automatically through the Catalog update function in Libero SoC software, or the CPZ file can be manually added using the **Add Core** catalog feature. When the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

For more instructions on core installation, licensing, and general use, see Libero SoC Online Help.

5. Resource Utilization

The following table lists the resource utilization of a sample H.264 / frame Encoder IP design made for PolarFire FPGA (MPF300TS-1FCG1152I package) and generates compressed data by using 4:2:2 sampling of input data.

Table 5-1. Resource Utilization of the H.264 / Frame Encoder IP

Element	Usage
4LUTs	15160
DFFs	15757
LSRAM	67
µSRAM	23
Math Blocks	18
Interface 4-input LUTs	3336
Interface DFFs	3336

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	01/2022	The first publication of the document.

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