



a  **MICROCHIP** company

Total Ionizing Dose Test Report

No. 20T-RT4G150-LG1657- K7A9F

September 13, 2021

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I. SUMMARY TABLE

Table. 1. Summary

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO ₂)
2. Power Supply Current	Passed 125 krad(SiO ₂)
3. Input Threshold (VIL/VIH)	Passed 125 krad(SiO ₂)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO ₂)
5. Propagation Delay	Passed 125 krad(SiO ₂) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO ₂)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at <http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports>

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the Automatic Test Equipment (ATE) program. The report summarizes sample pins.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	K7A9F
Quantity Tested	6
Serial Number (Dose)	01020 (125 krad), 01027 (125 krad), 01033 (125 krad), 01042 (125 krad), 01153 (125 krad), 01167 (125 krad)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO ₂)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

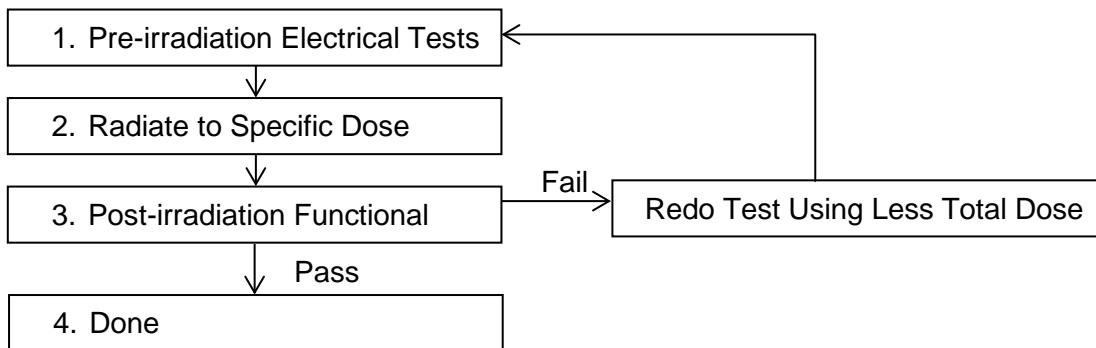


Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 3. Fabric Functional Coverage

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 µRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump and PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design. LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents are reported.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-25 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL.

Table. 4. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
01020	125 krad	0.3164	0.3375	6.67
01027	125 krad	0.3083	0.3277	6.29
01033	125 krad	0.2928	0.3114	6.35
01042	125 krad	0.3410	0.3589	5.25
01153	125 krad	0.3030	0.3230	6.60
01167	125 krad	0.3383	0.3578	5.76

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
01020	125 krad	0.0091	0.0116	27.47
01027	125 krad	0.0090	0.0114	26.67
01033	125 krad	0.0087	0.0112	28.74
01042	125 krad	0.0099	0.0123	24.24
01153	125 krad	0.0093	0.0116	24.73
01167	125 krad	0.0087	0.0112	28.74

Table. 6. Pre-irradiation and Post-irradiation $I_{DDI_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
01020	125 krad	0.0341	0.0368	7.92
01027	125 krad	0.0340	0.0369	8.53
01033	125 krad	0.0339	0.0370	9.14
01042	125 krad	0.0346	0.0375	8.38
01153	125 krad	0.0346	0.0373	7.80
01167	125 krad	0.0335	0.0365	8.96

Table. 7. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
01020	125 krad	0.0153	0.0152	-0.65
01027	125 krad	0.0154	0.0154	0.00
01033	125 krad	0.0154	0.0154	0.00
01042	125 krad	0.0152	0.0154	1.32
01153	125 krad	0.0154	0.0156	1.30
01167	125 krad	0.0153	0.0155	1.31

The following figures (2-25) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

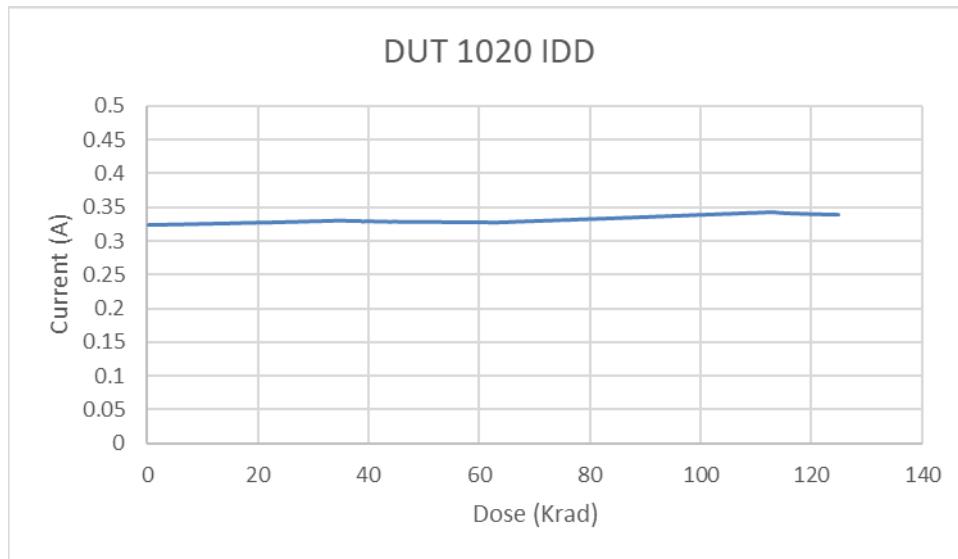


Fig. 2. DUT 01020 core power supply current (I_{DD}) versus TID

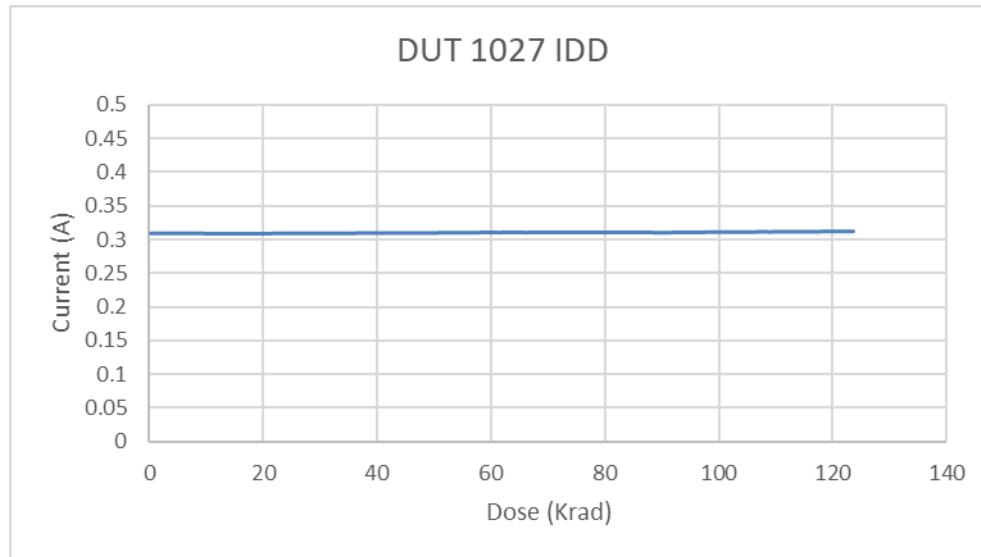


Fig. 3. DUT 01027 core power supply current (I_{DD}) versus TID

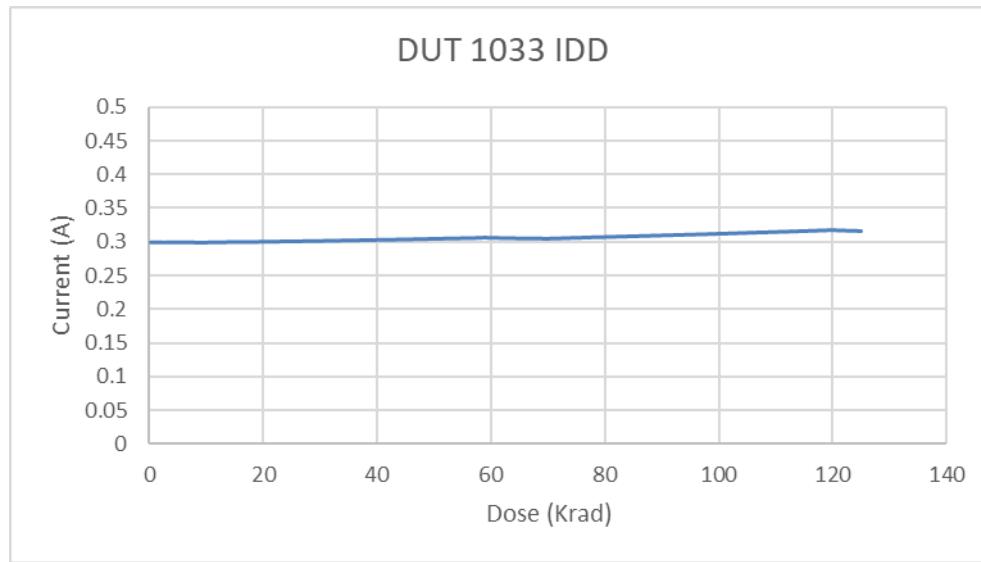


Fig. 4. DUT 01033 core power supply current (I_{DD}) versus TID

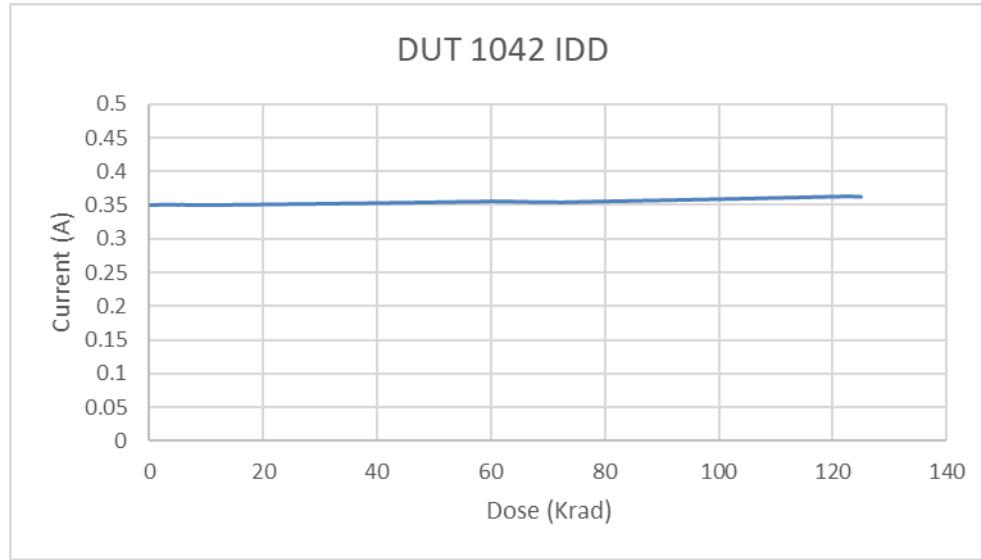


Fig. 5. DUT 01042 core power supply current (I_{DD}) versus TID

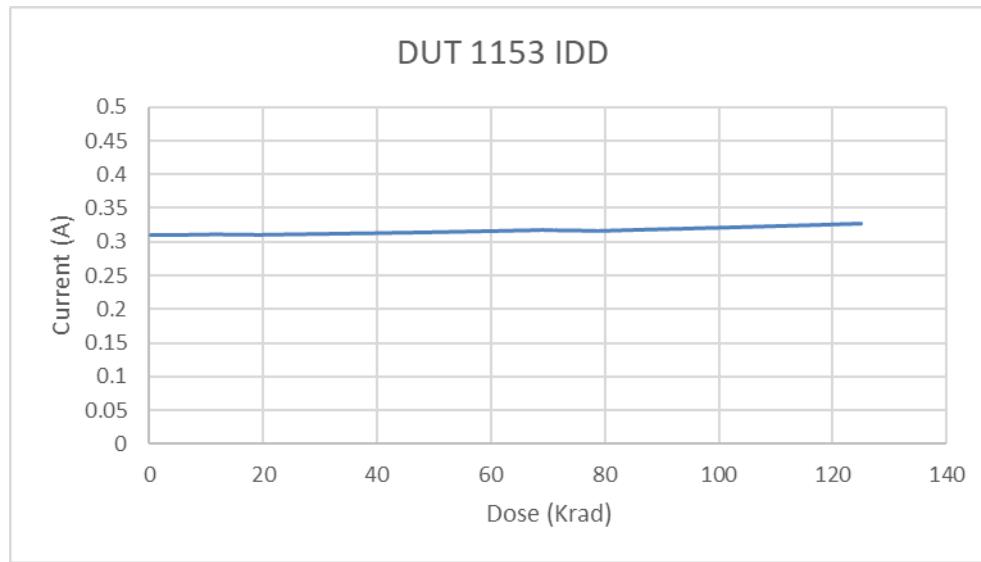


Fig. 6. DUT 01153 core power supply current (I_{DD}) versus TID

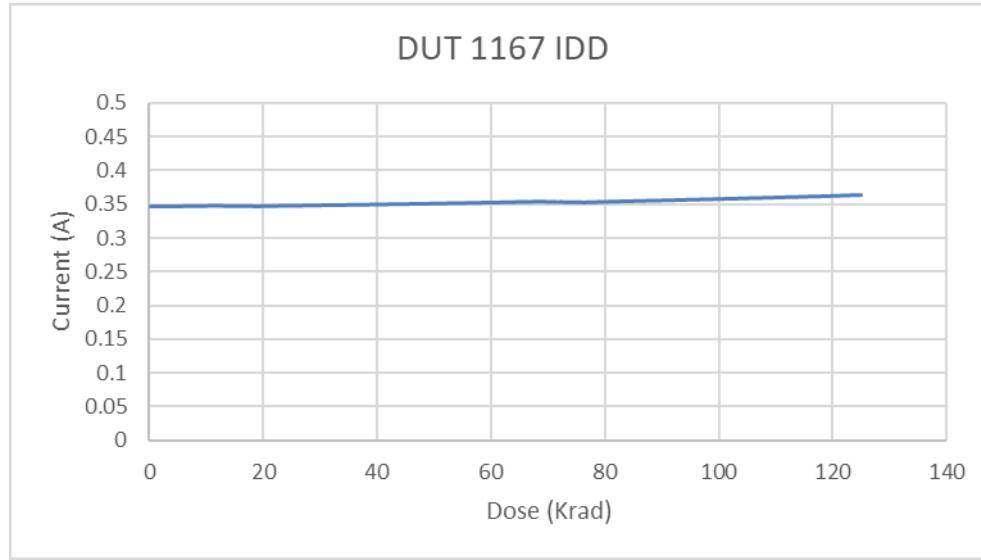


Fig. 7. DUT 01167 core power supply current (I_{DD}) versus TID

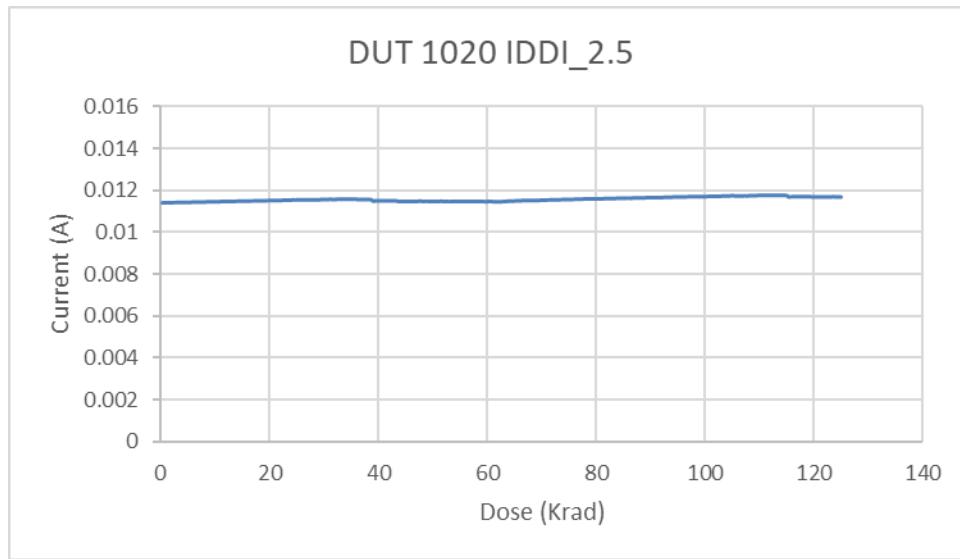


Fig. 8. DUT 01020 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

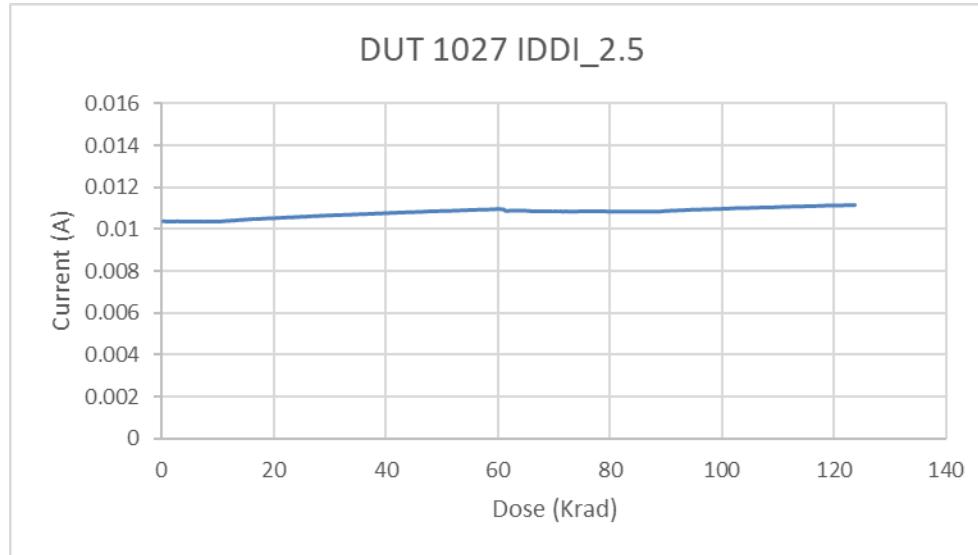


Fig. 9. DUT 01027 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

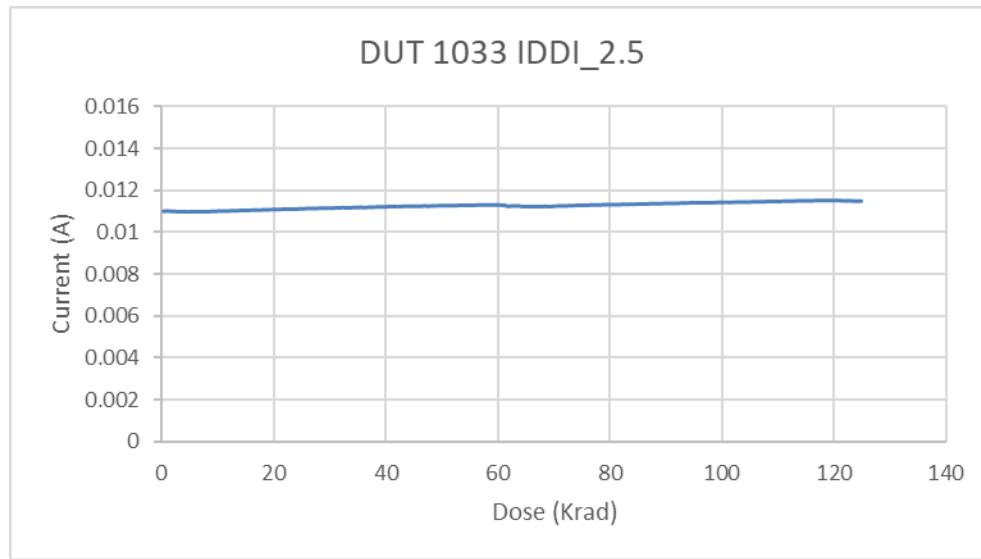


Fig. 10. DUT 01033 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

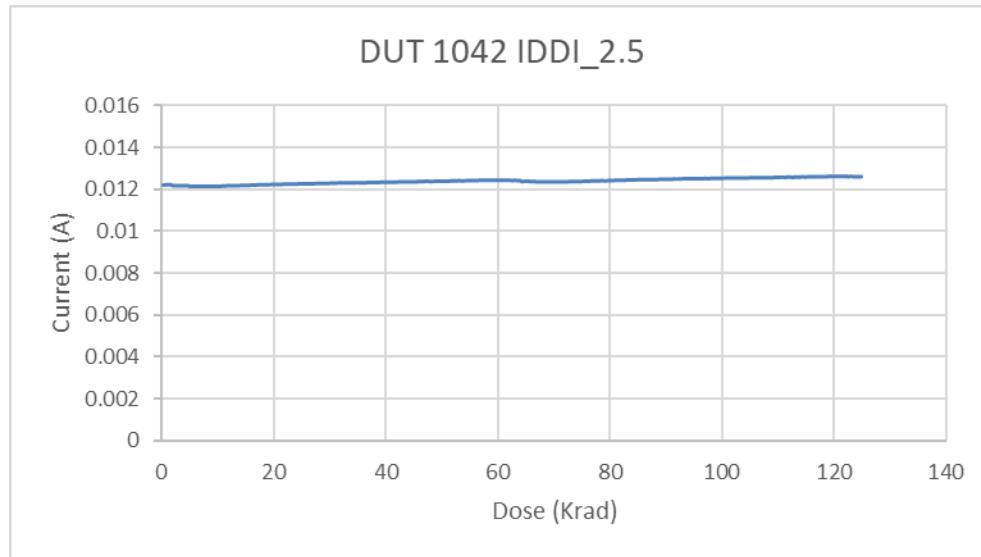


Fig. 11. DUT 01042 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

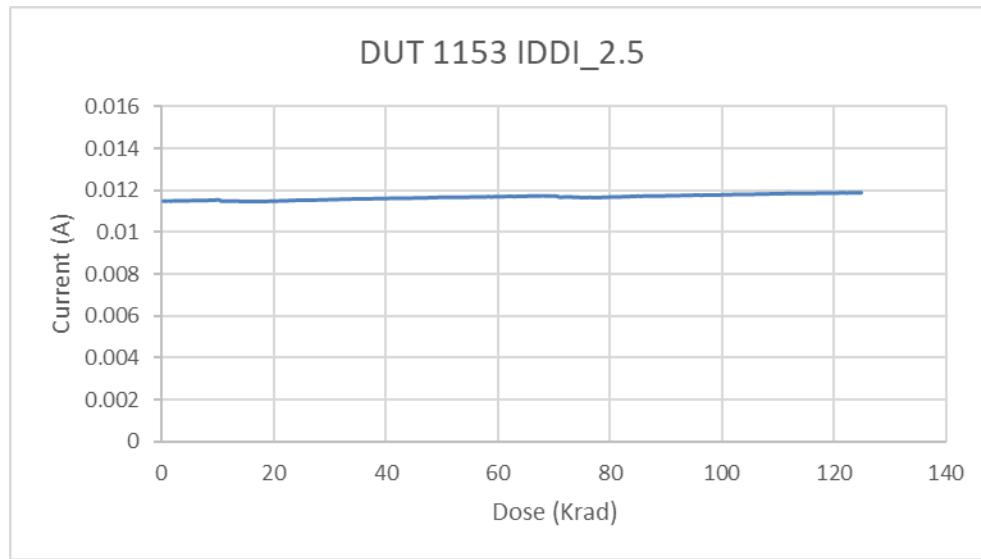


Fig. 12. DUT 01153 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

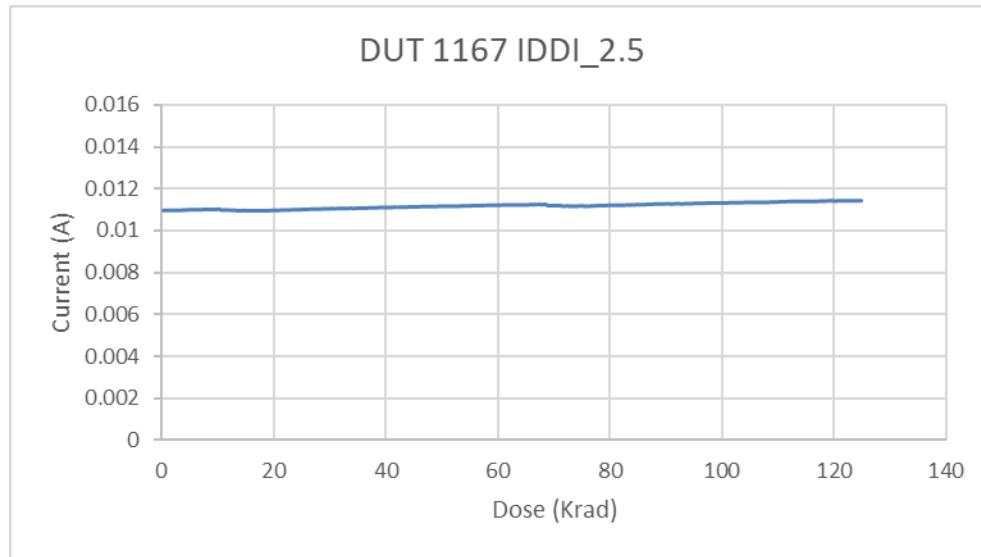


Fig. 13. DUT 01167 I/O bank 2.5V power supply current ($I_{DDI_2.5}$) versus TID

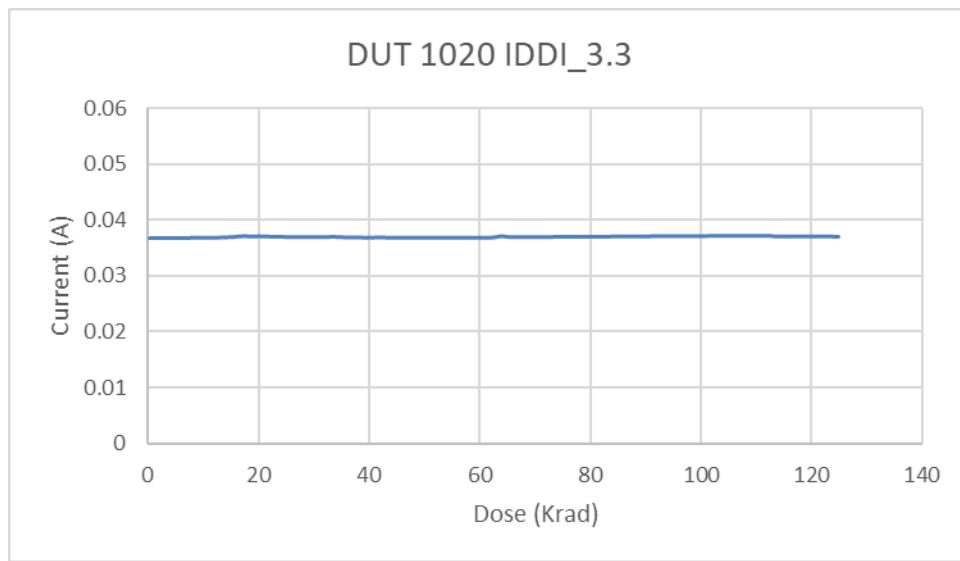


Fig. 14. DUT 01020 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

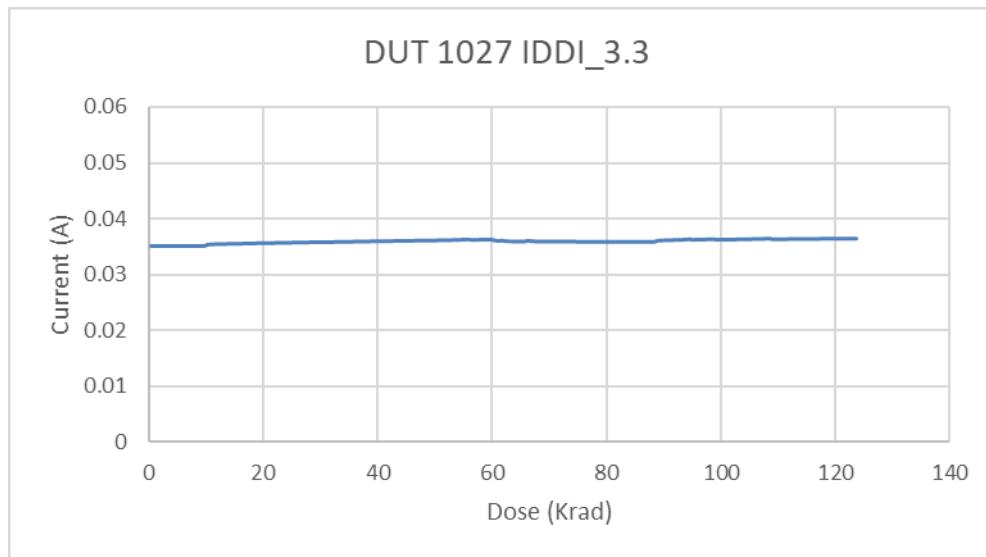


Fig. 15. DUT 01027 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

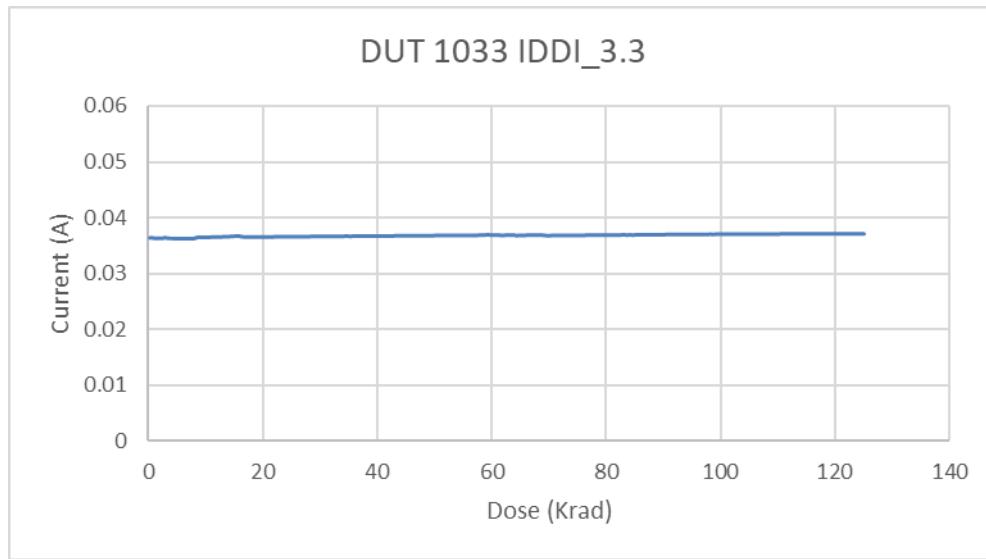


Fig. 16. DUT 01033 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

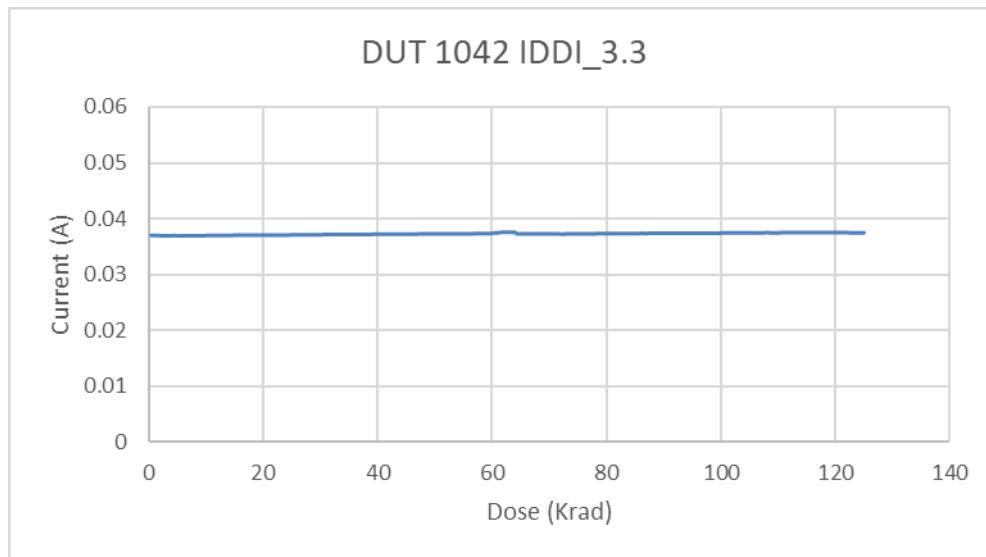


Fig. 17. DUT 01042 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

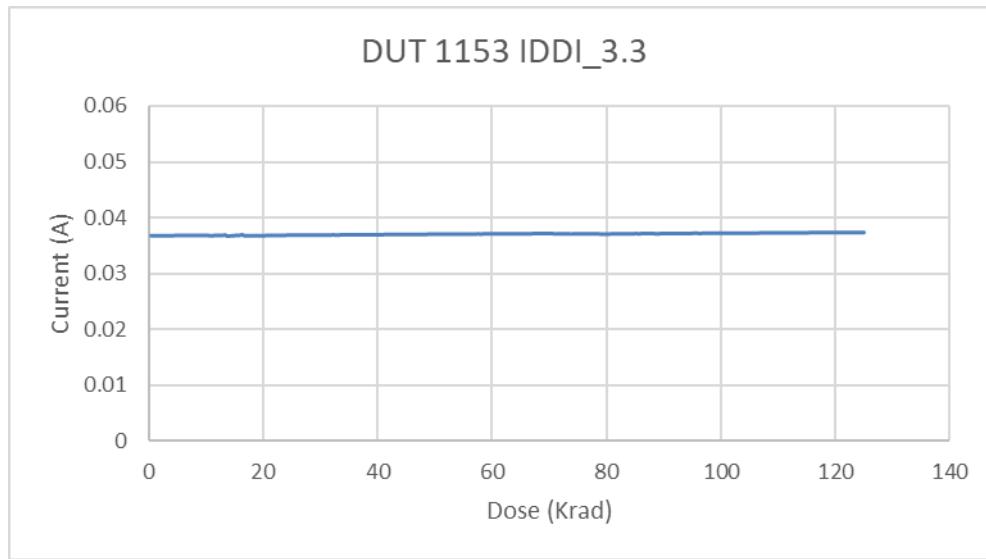


Fig. 18. DUT 01153 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

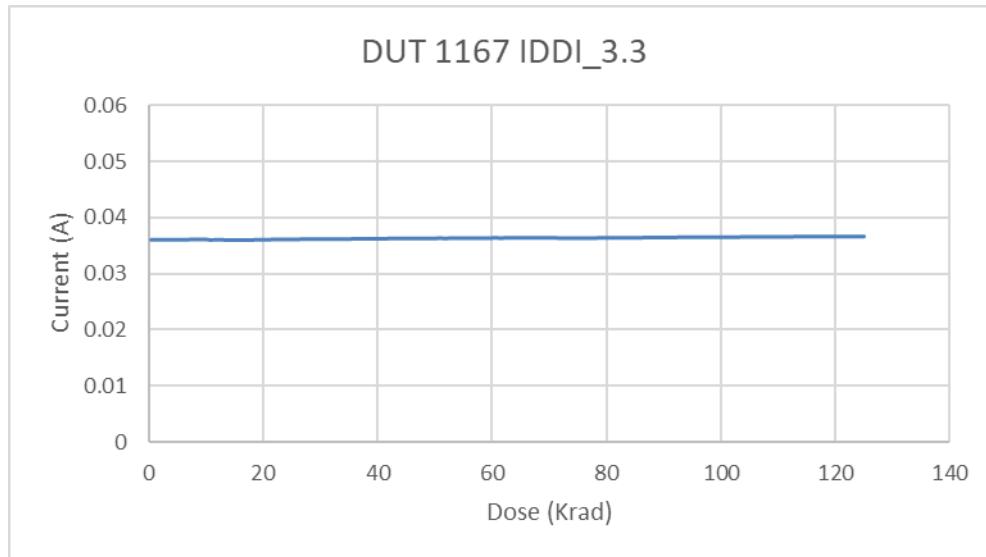


Fig. 19. DUT 01167 I/O bank 3.3V power supply current ($I_{DDI_3.3}$) versus TID

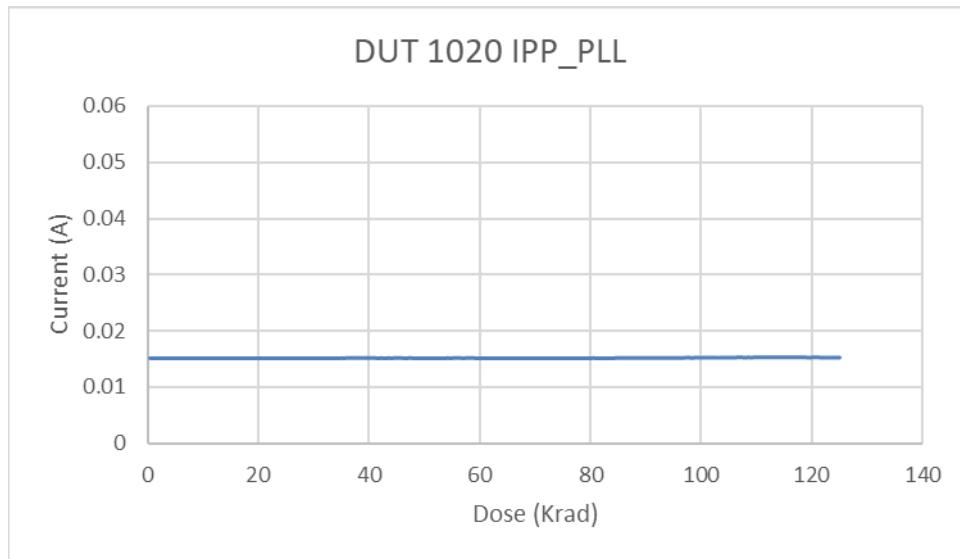


Fig. 20. DUT 01020 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

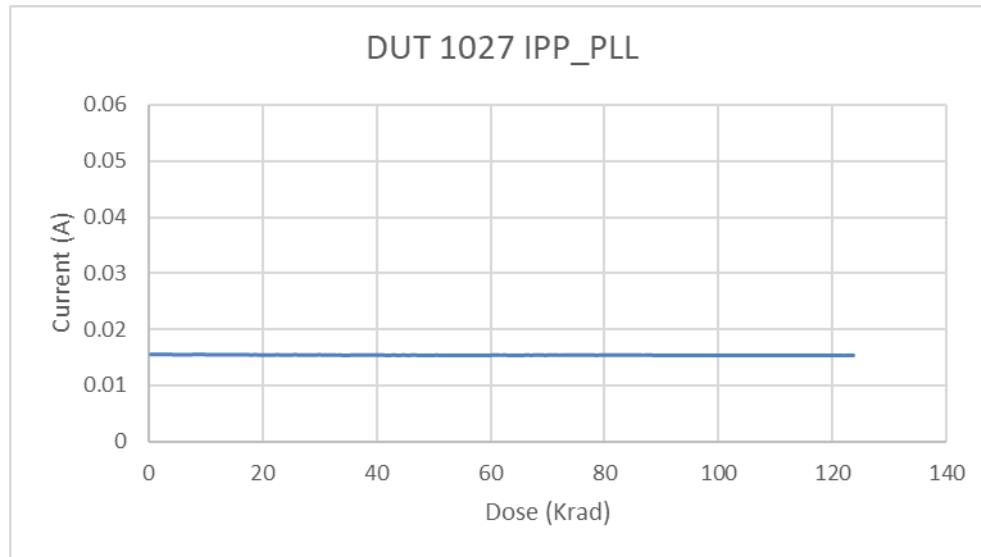


Fig. 21. DUT 01027 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

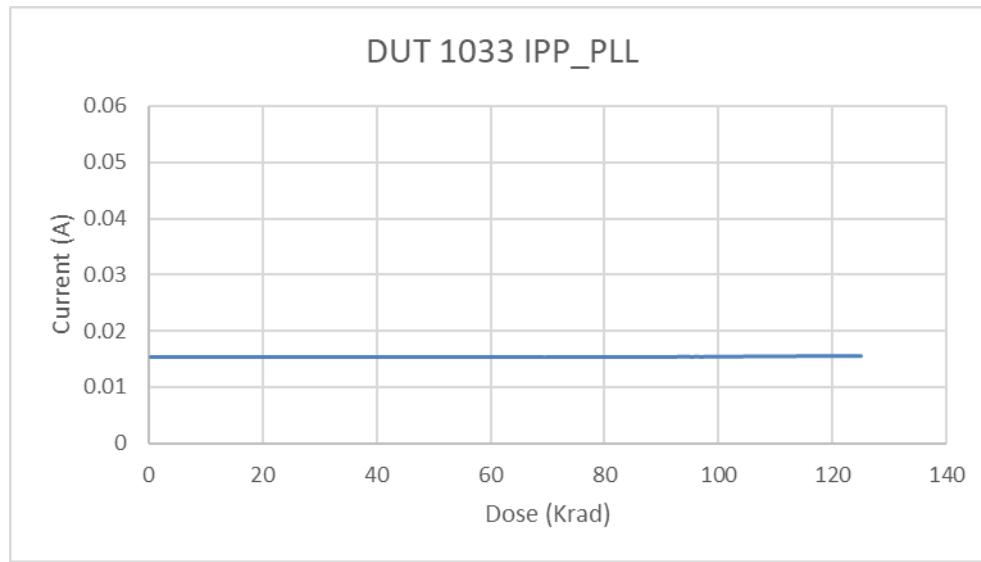


Fig. 22. DUT 01033 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

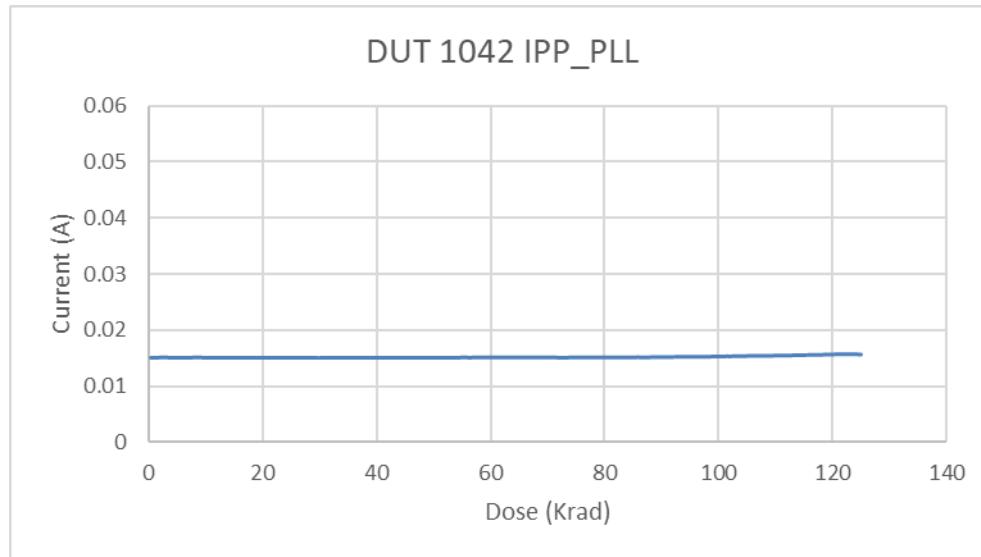


Fig. 23. DUT 01042 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

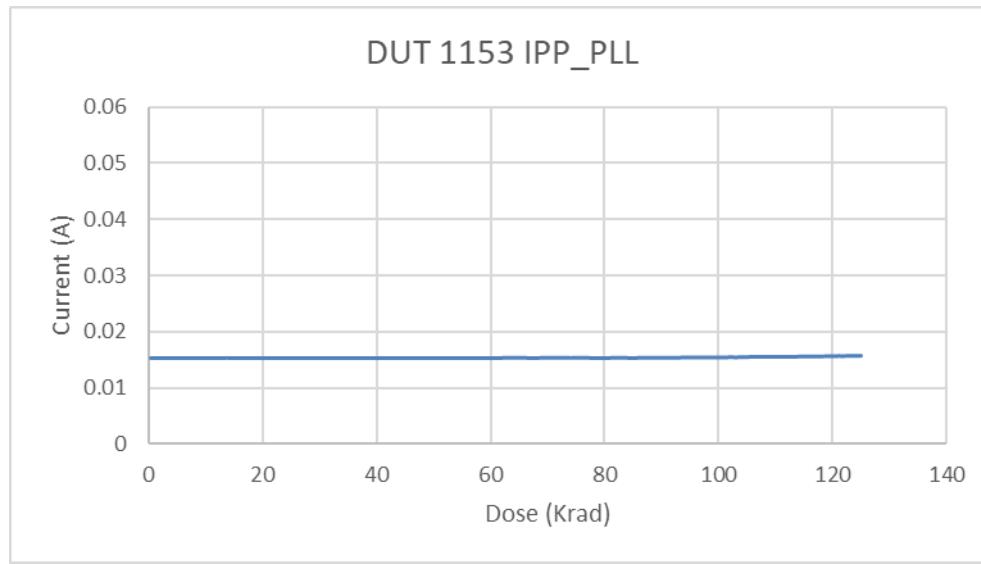


Fig. 24. DUT 01153 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

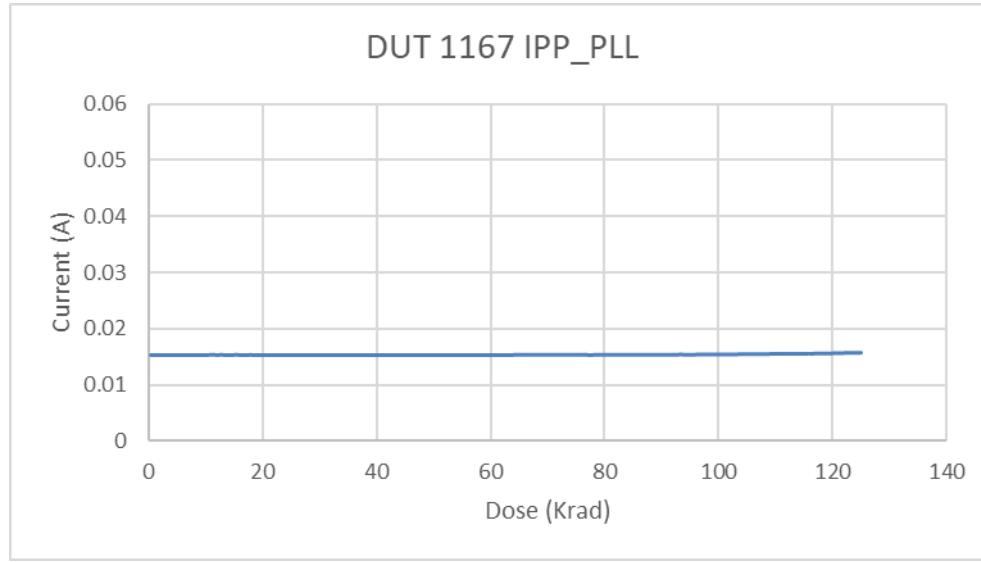


Fig. 25. DUT 01167 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and

recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 8. VIH Summary

DUT	Pre-irradiation	Post-irradiation
01020	Passed	Passed
01027	Passed	Passed
01033	Passed	Passed
01042	Passed	Passed
01153	Passed	Passed
01167	Passed	Passed

Table. 9. VIL Summary

DUT	Pre-irradiation	Post-irradiation
01020	Passed	Passed
01027	Passed	Passed
01033	Passed	Passed
01042	Passed	Passed
01153	Passed	Passed
01167	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 10 through 33 are sampled on several pins used in the burn in design.

Table. 10. LVCMOS 25 VOH – DUT 01020

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
TID_BUF_OUT	A33	2.128	2.127	2.196	2.196	2.164	2.165	2.141	2.143	2.103	2.107	2.087	2.092
EPCSRST_N_0	B31	2.131	2.128	2.199	2.196	2.170	2.165	2.149	2.143	2.115	2.106	2.100	2.091
EPCSRST_N_1	B32	2.132	2.127	2.201	2.193	2.173	2.160	2.151	2.135	2.119	2.096	2.106	2.079
EPCSRST_N_2	B34	2.131	2.128	2.200	2.197	2.171	2.168	2.149	2.146	2.116	2.111	2.102	2.097

EPCSRST_N_3	B35	2.131	2.129	2.202	2.199	2.173	2.169	2.152	2.148	2.121	2.115	2.107	2.101
EPCSRST_N_4	B36	2.130	2.128	2.199	2.196	2.169	2.166	2.146	2.143	2.112	2.107	2.098	2.092
EPCSRST_N_5	B37	2.131	2.128	2.200	2.197	2.171	2.167	2.149	2.145	2.117	2.110	2.103	2.095
MONITOR	K23	2.130	2.128	2.201	2.199	2.173	2.170	2.153	2.149	2.123	2.118	2.110	2.104
PLL_MON	L20	2.132	2.130	2.204	2.202	2.177	2.175	2.157	2.156	2.129	2.127	2.118	2.115
TOGGLE_MON	L22	2.131	2.129	2.202	2.201	2.175	2.172	2.155	2.152	2.125	2.122	2.113	2.109

Table. 11. LVCMOS 25 VOH – DUT 01027

Pin Name	Pin#	2mA	4mA	6mA	8mA	12mA	14mA
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.128	2.127	2.195	2.196	2.163	2.165
EPCSRST_N_0	B31	2.130	2.128	2.200	2.196	2.169	2.165
EPCSRST_N_1	B32	2.131	2.126	2.201	2.192	2.172	2.160
EPCSRST_N_2	B34	2.130	2.127	2.199	2.195	2.170	2.164
EPCSRST_N_3	B35	2.131	2.129	2.201	2.199	2.172	2.169
EPCSRST_N_4	B36	2.129	2.127	2.199	2.196	2.168	2.166
EPCSRST_N_5	B37	2.130	2.128	2.200	2.197	2.171	2.168
MONITOR	K23	2.130	2.128	2.201	2.200	2.174	2.170
PLL_MON	L20	2.131	2.130	2.204	2.202	2.177	2.175
TOGGLE_MON	L22	2.131	2.130	2.202	2.200	2.175	2.172

Table. 12. LVCMOS 25 VOH – DUT 01033

Pin Name	Pin#	2mA	4mA	6mA	8mA	12mA	14mA
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.127	2.126	2.195	2.195	2.163	2.165
EPCSRST_N_0	B31	2.130	2.127	2.199	2.196	2.169	2.165
EPCSRST_N_1	B32	2.131	2.126	2.201	2.192	2.172	2.159
EPCSRST_N_2	B34	2.129	2.127	2.199	2.197	2.170	2.167
EPCSRST_N_3	B35	2.130	2.127	2.200	2.198	2.172	2.168
EPCSRST_N_4	B36	2.129	2.127	2.198	2.196	2.168	2.165
EPCSRST_N_5	B37	2.130	2.128	2.200	2.197	2.170	2.167
MONITOR	K23	2.129	2.127	2.200	2.198	2.172	2.170
PLL_MON	L20	2.130	2.129	2.203	2.201	2.176	2.174
TOGGLE_MON	L22	2.130	2.129	2.201	2.200	2.174	2.171

Table. 13. LVC MOS 25 VOH – DUT 01042

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.127	2.127	2.195	2.196	2.163	2.165	2.140	2.142	2.102	2.106	2.086	2.091
EPCSRST_N_0	B31	2.130	2.127	2.199	2.196	2.169	2.165	2.148	2.142	2.114	2.106	2.099	2.091
EPCSRST_N_1	B32	2.131	2.126	2.201	2.192	2.172	2.159	2.151	2.135	2.118	2.095	2.105	2.077
EPCSRST_N_2	B34	2.129	2.127	2.199	2.197	2.170	2.167	2.148	2.145	2.115	2.110	2.101	2.096
EPCSRST_N_3	B35	2.130	2.128	2.201	2.198	2.172	2.168	2.151	2.147	2.119	2.114	2.105	2.099
EPCSRST_N_4	B36	2.129	2.127	2.198	2.196	2.168	2.165	2.146	2.143	2.112	2.107	2.097	2.092
EPCSRST_N_5	B37	2.130	2.128	2.200	2.197	2.170	2.167	2.149	2.145	2.116	2.111	2.102	2.096
MONITOR	K23	2.130	2.128	2.201	2.199	2.173	2.170	2.153	2.149	2.123	2.117	2.110	2.104
PLL_MON	L20	2.131	2.130	2.204	2.202	2.176	2.174	2.157	2.156	2.129	2.126	2.118	2.114
TOGGLE_MON	L22	2.130	2.129	2.202	2.200	2.174	2.171	2.154	2.150	2.125	2.120	2.113	2.107

Table. 14. LVC MOS 25 VOH – DUT 01153

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.126	2.126	2.195	2.195	2.163	2.165	2.140	2.142	2.102	2.106	2.086	2.091
EPCSRST_N_0	B31	2.129	2.127	2.199	2.196	2.169	2.165	2.147	2.142	2.113	2.106	2.099	2.091
EPCSRST_N_1	B32	2.131	2.125	2.201	2.191	2.172	2.158	2.151	2.133	2.119	2.093	2.105	2.075
EPCSRST_N_2	B34	2.129	2.127	2.199	2.197	2.170	2.167	2.148	2.145	2.115	2.110	2.101	2.096
EPCSRST_N_3	B35	2.130	2.128	2.200	2.198	2.171	2.168	2.150	2.147	2.119	2.114	2.105	2.099
EPCSRST_N_4	B36	2.128	2.127	2.198	2.196	2.168	2.165	2.146	2.143	2.112	2.107	2.097	2.092
EPCSRST_N_5	B37	2.130	2.128	2.200	2.197	2.170	2.167	2.148	2.146	2.116	2.111	2.102	2.097
MONITOR	K23	2.128	2.127	2.200	2.199	2.172	2.170	2.152	2.148	2.121	2.117	2.108	2.103
PLL_MON	L20	2.130	2.129	2.203	2.201	2.176	2.173	2.157	2.155	2.128	2.126	2.117	2.114
TOGGLE_MON	L22	2.128	2.128	2.201	2.199	2.173	2.171	2.153	2.151	2.124	2.120	2.112	2.108

Table. 15. LVC MOS 25 VOH – DUT 01167

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	2.127	2.127	2.195	2.196	2.164	2.166	2.140	2.143	2.103	2.107	2.087	2.092
EPCSRST_N_0	B31	2.130	2.128	2.199	2.196	2.170	2.166	2.148	2.143	2.114	2.107	2.100	2.092
EPCSRST_N_1	B32	2.130	2.125	2.201	2.191	2.172	2.158	2.151	2.133	2.119	2.093	2.106	2.075
EPCSRST_N_2	B34	2.129	2.128	2.200	2.197	2.170	2.167	2.148	2.145	2.115	2.111	2.101	2.096
EPCSRST_N_3	B35	2.130	2.128	2.201	2.198	2.172	2.169	2.151	2.147	2.120	2.114	2.106	2.100
EPCSRST_N_4	B36	2.129	2.127	2.198	2.196	2.168	2.166	2.146	2.143	2.112	2.107	2.097	2.092
EPCSRST_N_5	B37	2.130	2.128	2.200	2.198	2.171	2.168	2.149	2.146	2.116	2.112	2.103	2.097
MONITOR	K23	2.129	2.128	2.201	2.199	2.173	2.170	2.153	2.150	2.123	2.118	2.110	2.105
PLL_MON	L20	2.132	2.130	2.204	2.202	2.177	2.175	2.158	2.156	2.129	2.127	2.118	2.115
TOGGLE_MON	L22	2.131	2.130	2.202	2.200	2.174	2.172	2.154	2.152	2.125	2.122	2.113	2.109

Table. 16. LVC MOS 25 VOL – DUT 01020

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	238.5	237.2	173.3	171.5	204.1	201.4	227.5	224.3	264.2	259.0	280.4	274.1
EPCSRST_N_0	B31	236.0	237.0	169.2	171.7	198.1	201.7	219.7	224.8	252.7	260.1	267.1	275.5
EPCSRST_N_1	B32	234.9	238.7	167.4	175.1	195.4	206.6	215.9	231.0	247.2	269.7	260.6	286.8
EPCSRST_N_2	B34	236.3	237.1	169.0	170.5	197.5	199.6	218.4	221.4	250.5	254.5	264.4	268.8
EPCSRST_N_3	B35	236.1	237.0	167.8	169.5	195.5	198.0	215.9	219.3	246.8	251.7	260.0	265.4
EPCSRST_N_4	B36	237.4	238.1	170.4	171.9	199.6	201.7	221.1	224.0	254.5	258.5	268.9	273.5
EPCSRST_N_5	B37	236.4	237.3	169.0	170.9	197.4	200.2	218.3	222.1	250.4	255.8	264.1	270.3
MONITOR	K23	235.1	235.8	166.2	167.9	193.5	195.9	212.9	215.9	242.6	247.0	255.1	259.9
PLL_MON	L20	233.7	233.9	164.3	165.0	190.6	191.5	208.8	211.6	236.6	239.8	248.0	251.6
TOGGLE_MON	L22	234.2	234.9	165.4	166.6	192.1	193.8	210.7	213.7	239.9	243.5	252.0	256.0

Table. 17. LVC MOS 25 VOL – DUT 01027

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	239.8	238.3	174.0	172.0	204.8	202.0	228.4	225.0	265.1	259.9	281.3	275.0
EPCSRST_N_0	B31	237.0	237.7	169.9	171.8	198.8	201.9	220.5	224.8	253.7	260.0	268.1	275.3
EPCSRST_N_1	B32	235.8	239.5	168.0	175.6	195.9	207.4	216.3	231.8	247.5	270.7	261.0	287.9
EPCSRST_N_2	B34	237.6	238.9	169.7	172.7	198.4	202.6	219.3	225.1	251.6	260.0	265.4	275.1
EPCSRST_N_3	B35	236.8	237.4	168.4	169.9	196.4	198.5	216.8	219.9	248.0	252.5	261.5	266.4
EPCSRST_N_4	B36	237.9	238.5	170.9	172.2	200.2	201.9	221.7	224.2	255.2	258.9	269.8	273.9
EPCSRST_N_5	B37	237.3	237.8	169.4	170.6	198.0	199.7	218.8	221.5	251.0	255.0	264.7	269.1
MONITOR	K23	235.5	236.6	166.4	168.1	193.5	196.0	213.0	216.3	242.6	247.2	255.2	259.9
PLL_MON	L20	234.5	234.6	164.4	165.1	190.7	191.8	208.6	211.9	236.3	240.1	247.8	251.8
TOGGLE_MON	L22	234.3	235.0	165.6	166.8	192.4	194.1	211.1	214.1	240.5	244.1	252.7	256.7

Table. 18. LVC MOS 25 VOL – DUT 01033

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	240.5	239.1	174.4	172.4	205.1	202.3	228.7	225.2	265.4	260.0	281.5	275.1
EPCSRST_N_0	B31	237.8	238.5	170.3	172.2	199.3	202.3	221.0	225.3	254.1	260.4	268.6	275.7
EPCSRST_N_1	B32	236.7	240.5	168.2	176.1	196.3	207.7	216.8	232.3	248.0	271.3	261.6	288.5
EPCSRST_N_2	B34	238.0	238.5	170.2	171.6	198.8	200.6	219.7	222.4	252.0	255.8	265.9	270.2
EPCSRST_N_3	B35	237.9	238.6	168.9	170.6	197.0	199.3	217.5	220.7	248.5	253.4	261.7	267.1
EPCSRST_N_4	B36	238.6	239.0	171.3	172.5	200.4	202.2	222.0	224.5	255.4	259.2	270.0	274.1
EPCSRST_N_5	B37	237.9	238.4	170.0	171.2	198.5	200.3	219.3	222.2	251.5	255.3	265.2	269.7
MONITOR	K23	236.6	237.4	167.2	168.7	194.5	196.8	213.9	217.1	243.7	247.3	256.1	260.2
PLL_MON	L20	236.0	236.1	165.3	165.9	191.5	192.4	209.5	212.6	237.3	240.8	248.7	252.4
TOGGLE_MON	L22	235.8	236.2	166.3	167.5	193.2	194.8	212.1	214.8	241.1	244.8	253.4	257.3

Table. 19. LVCMOS 25 VOL – DUT 01042

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	240.3	238.9	174.4	172.6	205.2	202.5	229.0	225.5	265.8	260.4	282.1	275.6
EPCSRST_N_0	B31	238.0	238.5	170.4	172.4	199.2	202.4	221.2	225.5	254.3	260.6	268.6	276.0
EPCSRST_N_1	B32	236.8	240.5	168.5	176.2	196.6	207.9	217.1	232.6	248.7	271.7	262.2	288.7
EPCSRST_N_2	B34	238.8	239.4	170.4	171.8	199.1	201.0	220.1	222.9	252.4	256.2	266.4	270.6
EPCSRST_N_3	B35	238.0	238.7	169.2	170.6	197.5	199.5	218.0	220.7	249.1	253.4	262.6	267.4
EPCSRST_N_4	B36	238.9	239.4	171.4	172.8	200.7	202.5	222.3	225.0	255.7	259.7	270.2	274.7
EPCSRST_N_5	B37	238.3	238.9	170.0	171.5	198.7	200.7	219.5	222.7	251.7	256.2	265.6	270.5
MONITOR	K23	236.0	236.7	167.1	169.0	194.2	196.9	213.7	216.8	243.3	248.1	255.7	260.3
PLL_MON	L20	235.1	235.4	165.1	165.8	191.4	192.4	209.5	212.6	237.1	240.9	248.6	252.5
TOGGLE_MON	L22	235.4	236.2	166.4	168.0	193.1	195.6	212.0	215.7	241.0	246.2	253.1	258.9

Table. 20. LVCMOS 25 VOL – DUT 01153

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	240.8	239.4	174.3	172.5	205.1	202.3	228.6	225.1	265.2	259.8	281.3	275.0
EPCSRST_N_0	B31	238.1	238.4	170.4	172.3	199.4	202.2	221.1	225.2	254.1	260.3	268.6	275.6
EPCSRST_N_1	B32	236.5	240.5	168.4	176.6	196.4	208.7	217.0	233.7	248.2	273.2	261.6	290.7
EPCSRST_N_2	B34	237.9	238.4	170.2	171.3	198.7	200.2	219.7	222.3	251.9	255.5	265.8	269.9
EPCSRST_N_3	B35	237.6	238.0	168.9	170.4	197.1	199.1	217.4	220.6	248.6	253.0	261.9	266.8
EPCSRST_N_4	B36	239.1	239.6	171.3	172.6	200.6	202.3	222.1	224.8	255.6	259.3	270.0	274.1
EPCSRST_N_5	B37	237.8	238.4	169.7	170.8	198.4	199.8	219.2	221.7	251.4	255.0	265.1	269.1
MONITOR	K23	236.8	237.3	167.4	168.8	194.8	197.0	214.5	217.5	244.2	248.3	256.9	261.3
PLL_MON	L20	236.0	235.9	165.3	166.0	191.5	192.7	209.7	212.9	237.1	241.1	248.7	252.8
TOGGLE_MON	L22	237.0	237.5	166.8	168.0	193.5	195.3	212.3	215.3	241.5	245.1	253.6	257.7

Table. 21. LVCMOS 25 VOL – DUT 01167

Pin Name	Pin#	2mA		4mA		6mA		8mA		12mA		14mA	
		Pre-rad	Post-rad										
TID_BUF_OUT	A33	240.0	238.3	173.7	171.7	204.5	201.5	228.0	224.4	264.4	258.9	280.4	273.9
EPCSRST_N_0	B31	236.8	237.3	169.6	171.5	198.5	201.3	220.2	224.4	253.2	259.5	267.4	274.7
EPCSRST_N_1	B32	236.5	240.4	168.1	176.6	196.2	208.7	216.5	233.8	247.8	273.5	261.1	290.9
EPCSRST_N_2	B34	237.9	238.4	169.9	171.2	198.5	200.2	219.4	222.1	251.4	255.4	265.2	269.7
EPCSRST_N_3	B35	237.8	238.2	168.7	170.2	196.6	198.9	216.9	220.6	247.8	252.7	260.9	266.6
EPCSRST_N_4	B36	238.6	239.0	171.2	172.4	200.4	202.2	221.8	224.7	255.3	259.3	269.8	274.2
EPCSRST_N_5	B37	237.9	238.2	169.6	170.8	198.2	199.8	219.0	221.5	250.8	254.7	264.6	268.7
MONITOR	K23	235.5	236.2	166.6	168.2	193.8	195.9	213.3	216.5	242.8	247.0	255.2	259.9
PLL_MON	L20	234.5	234.2	164.7	165.0	190.8	191.7	209.1	211.9	236.5	240.0	248.1	251.7
TOGGLE_MON	L22	234.7	235.1	165.8	166.8	192.6	194.2	211.3	214.2	240.5	244.0	252.6	256.4

Table. 22. LVTTL VOH – DUT 01020

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.916	2.916	2.904	2.905	2.880	2.883	2.856	2.861	2.832	2.839
EPCSRST_N_0	B31	2.918	2.916	2.908	2.905	2.887	2.882	2.867	2.860	2.847	2.837
EPCSRST_N_1	B32	2.919	2.914	2.909	2.901	2.891	2.875	2.873	2.849	2.854	2.824
EPCSRST_N_2	B34	2.918	2.917	2.908	2.906	2.889	2.885	2.869	2.865	2.850	2.845
EPCSRST_N_3	B35	2.918	2.917	2.909	2.908	2.892	2.888	2.873	2.869	2.856	2.849
EPCSRST_N_4	B36	2.917	2.916	2.907	2.905	2.886	2.883	2.866	2.861	2.845	2.839
EPCSRST_N_5	B37	2.918	2.917	2.908	2.906	2.889	2.885	2.870	2.864	2.850	2.843
MONITOR	K23	2.917	2.916	2.909	2.907	2.893	2.889	2.876	2.871	2.859	2.853
PLL_MON	L20	2.920	2.918	2.912	2.910	2.897	2.895	2.883	2.879	2.868	2.864
TOGGLE_MON	L22	2.919	2.917	2.911	2.909	2.895	2.892	2.879	2.875	2.863	2.858

Table. 23. LVTTL VOH – DUT 01027

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.915	2.915	2.903	2.904	2.879	2.882	2.855	2.860	2.832	2.838
EPCSRST_N_0	B31	2.917	2.916	2.907	2.905	2.887	2.882	2.867	2.860	2.847	2.838
EPCSRST_N_1	B32	2.918	2.914	2.909	2.901	2.891	2.875	2.873	2.849	2.854	2.823
EPCSRST_N_2	B34	2.917	2.915	2.907	2.904	2.888	2.881	2.868	2.859	2.849	2.837
EPCSRST_N_3	B35	2.918	2.917	2.909	2.907	2.891	2.887	2.873	2.868	2.854	2.848
EPCSRST_N_4	B36	2.916	2.916	2.906	2.904	2.885	2.883	2.865	2.861	2.844	2.839
EPCSRST_N_5	B37	2.918	2.917	2.908	2.906	2.889	2.885	2.869	2.865	2.850	2.845
MONITOR	K23	2.917	2.916	2.909	2.907	2.893	2.889	2.877	2.871	2.860	2.853
PLL_MON	L20	2.919	2.918	2.912	2.910	2.898	2.895	2.883	2.879	2.869	2.865
TOGGLE_MON	L22	2.919	2.917	2.910	2.909	2.895	2.892	2.879	2.875	2.863	2.858

Table. 24. LVTTL VOH – DUT 01033

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.914	2.915	2.902	2.904	2.878	2.882	2.855	2.860	2.831	2.838
EPCSRST_N_0	B31	2.917	2.915	2.906	2.904	2.886	2.882	2.866	2.860	2.846	2.838
EPCSRST_N_1	B32	2.918	2.913	2.909	2.900	2.890	2.874	2.872	2.848	2.853	2.821
EPCSRST_N_2	B34	2.916	2.915	2.907	2.905	2.887	2.884	2.868	2.864	2.848	2.843
EPCSRST_N_3	B35	2.917	2.916	2.908	2.906	2.890	2.886	2.872	2.867	2.854	2.847
EPCSRST_N_4	B36	2.916	2.915	2.906	2.904	2.885	2.882	2.865	2.861	2.844	2.839
EPCSRST_N_5	B37	2.917	2.916	2.907	2.905	2.888	2.885	2.869	2.865	2.849	2.844
MONITOR	K23	2.917	2.915	2.908	2.906	2.892	2.889	2.875	2.870	2.859	2.853
PLL_MON	L20	2.918	2.917	2.911	2.909	2.897	2.894	2.882	2.878	2.868	2.864
TOGGLE_MON	L22	2.917	2.917	2.910	2.908	2.894	2.891	2.878	2.874	2.862	2.857

Table. 25. LVTTL VOH – DUT 01042

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.915	2.915	2.903	2.904	2.879	2.882	2.855	2.860	2.831	2.838
EPCSRST_N_0	B31	2.917	2.915	2.907	2.904	2.886	2.882	2.866	2.860	2.847	2.838
EPCSRST_N_1	B32	2.918	2.914	2.908	2.900	2.890	2.874	2.872	2.848	2.853	2.822
EPCSRST_N_2	B34	2.916	2.915	2.907	2.905	2.887	2.884	2.868	2.864	2.848	2.843
EPCSRST_N_3	B35	2.917	2.916	2.908	2.906	2.890	2.887	2.872	2.867	2.853	2.847
EPCSRST_N_4	B36	2.916	2.915	2.906	2.904	2.886	2.882	2.865	2.861	2.844	2.839
EPCSRST_N_5	B37	2.917	2.916	2.908	2.906	2.888	2.885	2.869	2.864	2.850	2.844
MONITOR	K23	2.917	2.916	2.909	2.907	2.893	2.889	2.876	2.871	2.860	2.853
PLL_MON	L20	2.919	2.917	2.911	2.909	2.897	2.894	2.883	2.879	2.868	2.864
TOGGLE_MON	L22	2.918	2.916	2.910	2.908	2.894	2.890	2.878	2.873	2.862	2.856

Table. 26. LVTTL VOH – DUT 01153

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.914	2.914	2.902	2.904	2.878	2.882	2.855	2.860	2.832	2.838
EPCSRST_N_0	B31	2.917	2.915	2.906	2.904	2.886	2.882	2.866	2.860	2.846	2.838
EPCSRST_N_1	B32	2.918	2.913	2.909	2.899	2.890	2.872	2.872	2.845	2.853	2.818
EPCSRST_N_2	B34	2.916	2.915	2.907	2.905	2.887	2.885	2.868	2.864	2.848	2.844
EPCSRST_N_3	B35	2.917	2.916	2.908	2.906	2.890	2.886	2.872	2.867	2.853	2.848
EPCSRST_N_4	B36	2.916	2.915	2.905	2.904	2.885	2.882	2.864	2.860	2.844	2.839
EPCSRST_N_5	B37	2.917	2.916	2.907	2.905	2.888	2.885	2.869	2.865	2.849	2.845
MONITOR	K23	2.916	2.915	2.908	2.906	2.892	2.888	2.874	2.870	2.858	2.852
PLL_MON	L20	2.918	2.917	2.911	2.909	2.897	2.894	2.882	2.878	2.868	2.864
TOGGLE_MON	L22	2.916	2.915	2.909	2.907	2.893	2.890	2.878	2.873	2.862	2.857

Table. 27. LVTTL VOH – DUT 01167

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	2.915	2.915	2.903	2.905	2.879	2.883	2.856	2.861	2.832	2.839
EPCSRST_N_0	B31	2.917	2.916	2.907	2.905	2.887	2.883	2.867	2.861	2.847	2.839
EPCSRST_N_1	B32	2.918	2.912	2.908	2.898	2.890	2.870	2.872	2.842	2.854	2.814
EPCSRST_N_2	B34	2.917	2.916	2.907	2.905	2.888	2.885	2.869	2.864	2.849	2.844
EPCSRST_N_3	B35	2.917	2.916	2.909	2.906	2.890	2.887	2.873	2.867	2.855	2.848
EPCSRST_N_4	B36	2.916	2.915	2.906	2.905	2.886	2.883	2.865	2.861	2.844	2.839
EPCSRST_N_5	B37	2.917	2.916	2.907	2.906	2.888	2.885	2.869	2.865	2.850	2.845
MONITOR	K23	2.917	2.916	2.909	2.907	2.893	2.889	2.876	2.871	2.860	2.853
PLL_MON	L20	2.920	2.918	2.912	2.910	2.897	2.895	2.883	2.879	2.869	2.865
TOGGLE_MON	L22	2.918	2.917	2.910	2.909	2.894	2.892	2.879	2.875	2.863	2.858

Table. 28. LVTTL VOL – DUT 01020

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	218.6	217.5	230.9	229.5	253.5	250.0	277.1	271.8	301.3	294.4
EPCSRST_N_0	B31	216.2	217.3	226.7	229.7	245.7	250.6	265.7	272.9	286.4	296.2
EPCSRST_N_1	B32	215.4	218.9	224.0	231.7	242.2	257.2	260.8	283.1	279.2	309.4
EPCSRST_N_2	B34	216.4	216.9	225.7	227.3	244.9	247.0	264.1	267.8	283.3	288.6
EPCSRST_N_3	B35	216.5	216.9	224.2	225.8	242.4	245.2	260.3	264.7	278.2	284.6
EPCSRST_N_4	B36	217.7	218.0	227.1	228.4	247.9	249.9	268.0	271.6	288.6	293.9
EPCSRST_N_5	B37	216.7	217.3	225.4	227.5	244.9	248.0	264.1	268.8	283.1	290.1
MONITOR	K23	215.1	215.8	222.7	224.4	239.5	242.4	255.8	260.2	272.7	278.4
PLL_MON	L20	213.8	213.9	220.3	224.0	235.5	236.9	250.2	252.1	264.6	268.6
TOGGLE_MON	L22	214.2	214.8	221.5	223.3	237.5	239.6	253.4	256.4	269.1	273.8

Table. 29. LVTTL VOL – DUT 01027

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	219.3	218.1	231.6	230.0	254.3	250.5	277.7	272.3	302.2	295.1
EPCSRST_N_0	B31	216.9	217.7	227.6	230.1	246.3	250.6	266.4	272.7	287.3	295.8
EPCSRST_N_1	B32	215.9	219.3	224.2	232.3	242.6	257.8	261.0	283.8	279.5	310.7
EPCSRST_N_2	B34	217.6	218.6	226.3	229.4	245.9	251.1	264.8	273.1	284.4	295.8
EPCSRST_N_3	B35	216.7	217.1	225.0	226.5	243.4	245.6	261.3	265.1	279.7	285.4
EPCSRST_N_4	B36	218.1	218.3	227.7	229.0	248.1	250.1	268.5	271.8	289.2	293.9
EPCSRST_N_5	B37	217.0	217.3	226.0	227.5	245.1	247.1	264.3	267.8	283.5	288.5
MONITOR	K23	215.2	214.1	222.6	225.4	239.3	241.4	255.7	260.0	272.4	278.6
PLL_MON	L20	214.4	214.3	219.9	224.1	235.4	237.0	249.9	252.4	264.1	268.6
TOGGLE_MON	L22	214.2	214.7	221.5	223.7	237.7	239.7	253.8	256.6	269.7	274.1

Table. 30. LVTTL VOL – DUT 01033

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	220.3	219.1	232.4	230.8	254.7	250.9	278.1	272.7	302.4	295.3
EPCSRST_N_0	B31	217.6	218.4	228.1	230.5	247.1	251.0	267.2	273.1	287.8	296.0
EPCSRST_N_1	B32	216.8	220.2	225.0	233.1	243.2	258.8	261.8	285.1	280.1	312.0
EPCSRST_N_2	B34	217.9	218.4	227.1	228.4	246.4	248.4	265.5	268.9	285.1	289.9
EPCSRST_N_3	B35	217.8	218.3	226.1	227.7	244.1	246.9	261.9	266.4	280.2	286.4
EPCSRST_N_4	B36	218.6	218.8	228.1	229.5	248.8	250.4	269.0	272.1	289.6	294.3
EPCSRST_N_5	B37	218.0	218.3	226.7	228.1	246.0	248.0	265.0	268.1	284.2	289.2
MONITOR	K23	216.5	216.7	223.9	225.4	240.5	243.2	256.7	260.8	273.4	279.0
PLL_MON	L20	215.8	215.6	221.4	225.3	236.4	237.9	250.9	252.9	265.1	269.3
TOGGLE_MON	L22	215.5	215.8	222.3	224.4	239.0	240.6	254.6	257.4	270.5	274.8

Table. 31. LVTTL VOL – DUT 01042

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	219.8	218.7	232.2	230.6	254.9	251.2	278.8	273.1	303.1	295.6
EPCSRST_N_0	B31	217.8	218.6	227.9	230.5	246.9	251.2	266.9	273.2	287.7	296.2
EPCSRST_N_1	B32	217.0	220.3	225.4	233.1	243.5	258.4	262.1	284.6	280.7	311.3
EPCSRST_N_2	B34	218.7	218.7	227.3	228.9	246.8	248.8	265.8	269.0	285.4	290.2
EPCSRST_N_3	B35	217.9	218.2	226.0	227.5	244.5	246.6	262.7	266.3	280.9	286.5
EPCSRST_N_4	B36	218.8	218.9	228.0	229.3	248.8	251.0	269.3	272.8	289.7	294.8
EPCSRST_N_5	B37	218.2	218.2	226.5	228.5	246.1	248.4	265.1	268.9	284.4	290.0
MONITOR	K23	215.6	216.4	223.8	225.5	240.2	243.3	256.4	261.2	273.2	279.5
PLL_MON	L20	215.2	215.4	221.0	225.1	236.4	238.0	250.7	253.0	264.9	269.4
TOGGLE_MON	L22	215.3	215.9	222.3	224.9	239.1	241.7	254.4	258.9	270.2	276.7

Table. 32. LVTTL VOL – DUT 01153

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	220.5	219.2	232.6	231.0	254.6	250.7	277.9	272.7	302.0	295.0
EPCSRST_N_0	B31	218.0	218.5	228.5	230.6	247.1	251.1	267.3	272.8	287.9	295.9
EPCSRST_N_1	B32	216.7	220.6	224.9	234.0	243.5	260.7	261.8	287.9	280.0	315.7
EPCSRST_N_2	B34	218.2	218.0	226.9	228.5	246.2	248.1	265.4	268.5	284.8	289.6
EPCSRST_N_3	B35	217.5	217.8	225.8	227.5	244.3	246.5	262.4	265.8	280.4	286.0
EPCSRST_N_4	B36	219.3	219.1	228.3	230.0	248.9	251.0	269.1	272.3	289.7	294.3
EPCSRST_N_5	B37	217.9	218.0	226.7	228.0	245.9	247.5	264.9	268.0	284.2	288.7
MONITOR	K23	216.6	217.1	224.2	225.9	241.0	243.3	257.4	261.1	274.3	279.7
PLL_MON	L20	215.6	215.8	221.7	225.6	236.5	238.0	250.7	253.4	265.1	269.5
TOGGLE_MON	L22	216.7	217.1	223.4	225.5	239.5	241.3	255.0	257.8	270.8	275.3

Table. 33. LVTTL VOL – DUT 01167

Pin Name	Pin#	2mA		4mA		8mA		12mA		16mA	
		Pre-rad	Post-rad								
TID_BUF_OUT	A33	219.6	218.2	231.9	230.1	253.9	250.0	277.2	271.6	301.2	293.9
EPCSRST_N_0	B31	216.7	217.4	227.3	229.9	245.9	250.0	266.3	272.0	286.5	294.8
EPCSRST_N_1	B32	216.7	221.1	224.9	235.0	243.0	262.2	261.1	290.0	279.5	318.9
EPCSRST_N_2	B34	217.9	218.0	226.7	228.4	245.7	247.9	264.9	268.1	284.3	289.3
EPCSRST_N_3	B35	217.5	217.9	225.5	227.4	243.7	246.2	261.2	265.7	279.2	285.9
EPCSRST_N_4	B36	218.7	218.7	228.0	229.3	248.6	250.5	268.7	272.2	289.1	294.5
EPCSRST_N_5	B37	218.1	217.9	226.5	228.0	245.6	247.2	264.4	267.3	283.3	288.2
MONITOR	K23	215.7	216.0	223.1	224.8	239.6	242.2	256.0	259.9	272.5	278.2
PLL_MON	L20	214.3	214.3	220.7	224.1	235.6	236.9	250.0	252.1	264.3	268.5
TOGGLE_MON	L22	214.5	214.9	221.8	223.9	238.2	239.8	253.8	256.5	269.4	274.0

E. Propagation Delay

Table 34 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 34. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (μs)	Post-irradiation (μs)	Change Degradation (%)
01020	125 krad	0.462	0.467	1.08
01027	125 krad	0.471	0.476	1.06
01033	125 krad	0.48	0.483	0.63
01042	125 krad	0.466	0.469	0.64
01153	125 krad	0.48	0.483	0.63
01167	125 krad	0.462	0.465	0.65

F. Transition Time

The figures below show the pre-irradiation and post-irradiation transitions edges. In each case the radiation induced transition degradation is not observable.

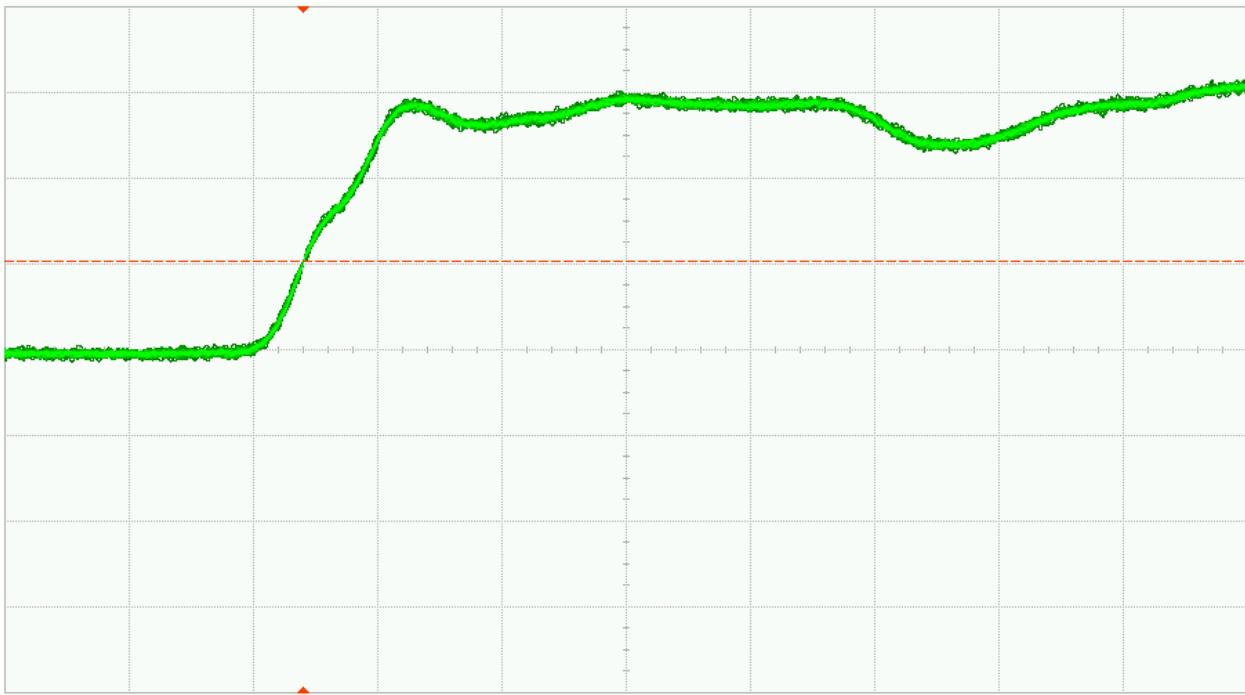


Fig. 26 (a). DUT 01020 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

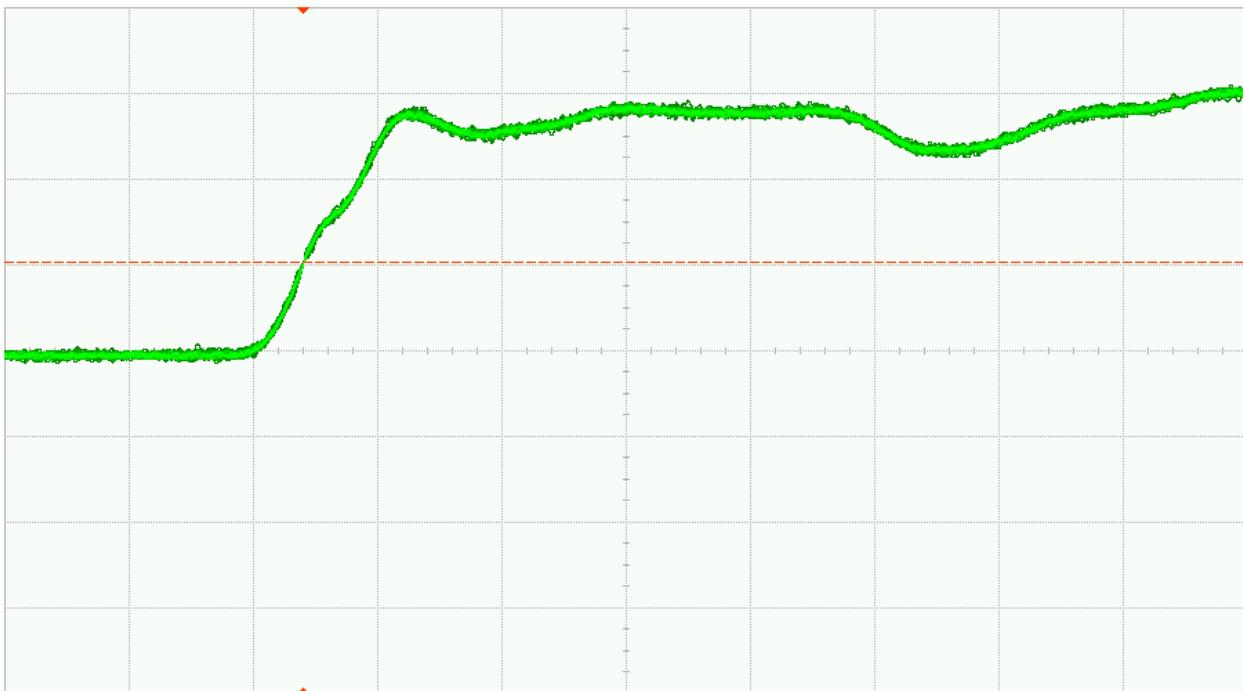


Fig. 26 (b). DUT 01020 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

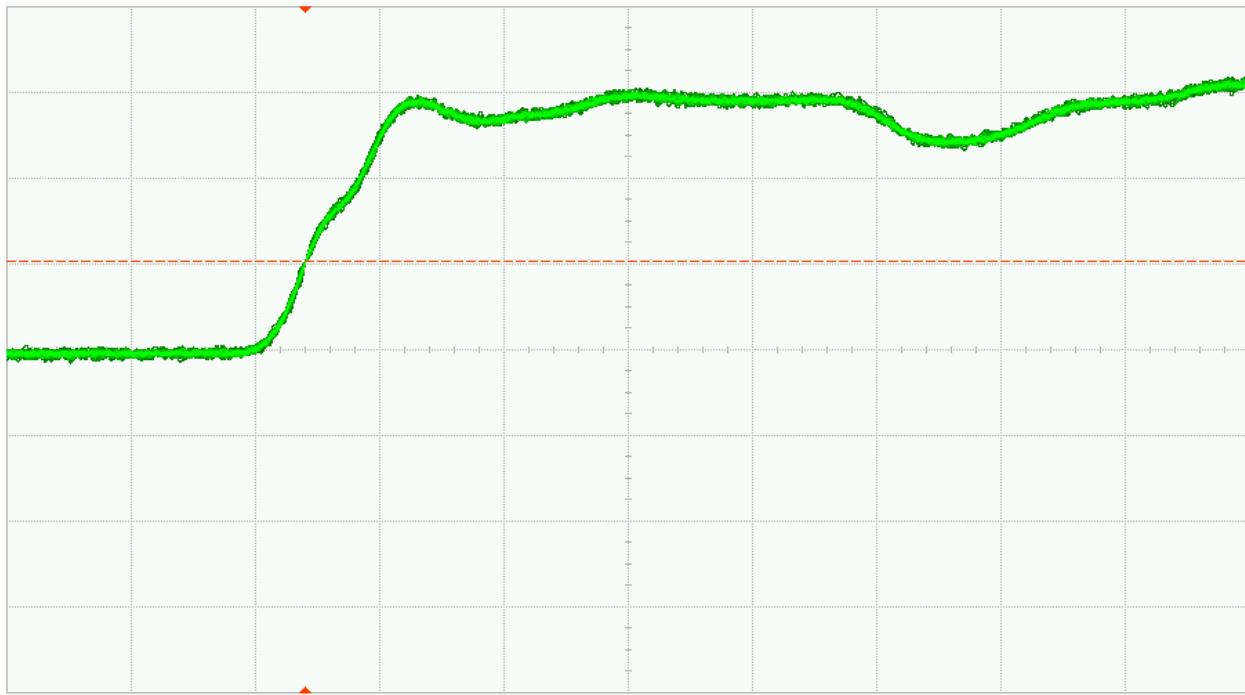


Fig. 27 (a). DUT 01027 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

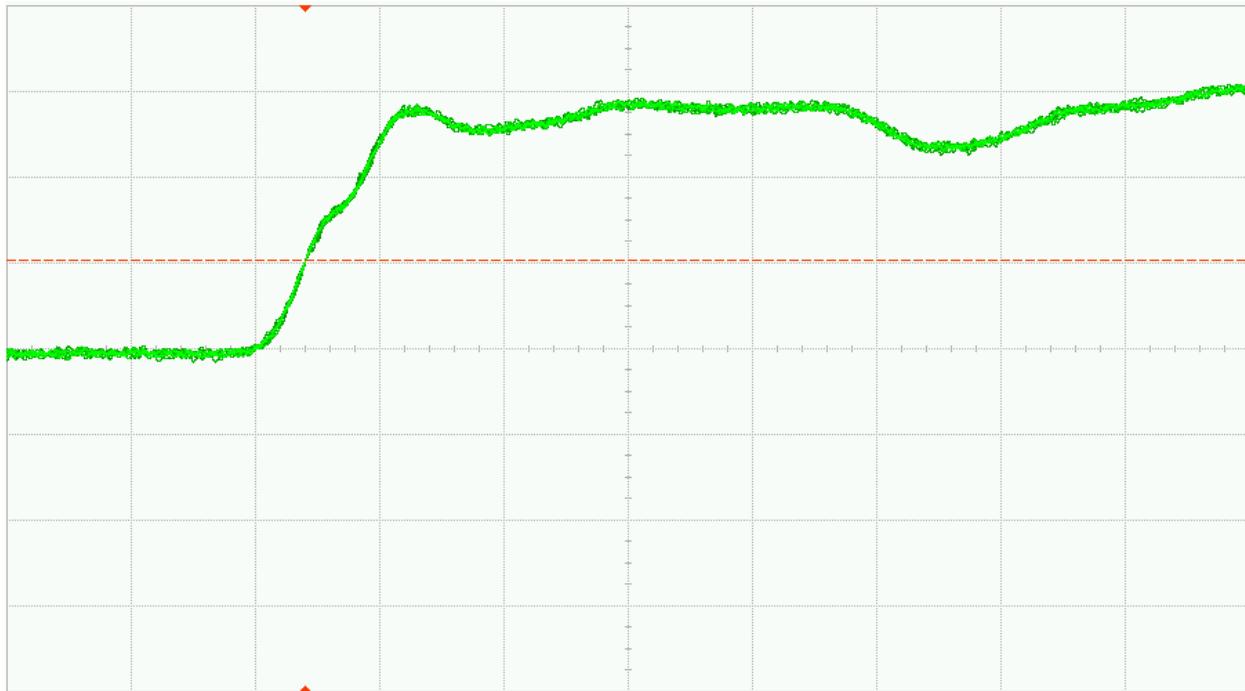


Fig. 27 (b). DUT 01027 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 28 (a). DUT 01033 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

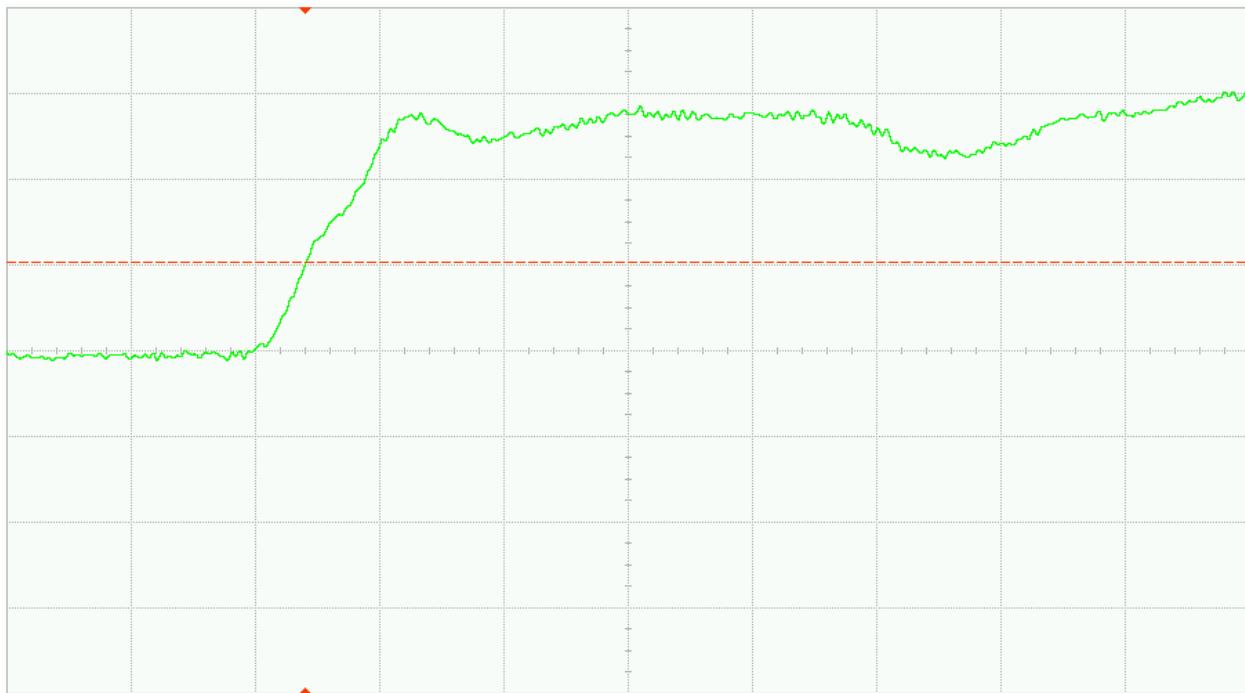


Fig. 28 (b). DUT 01033 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

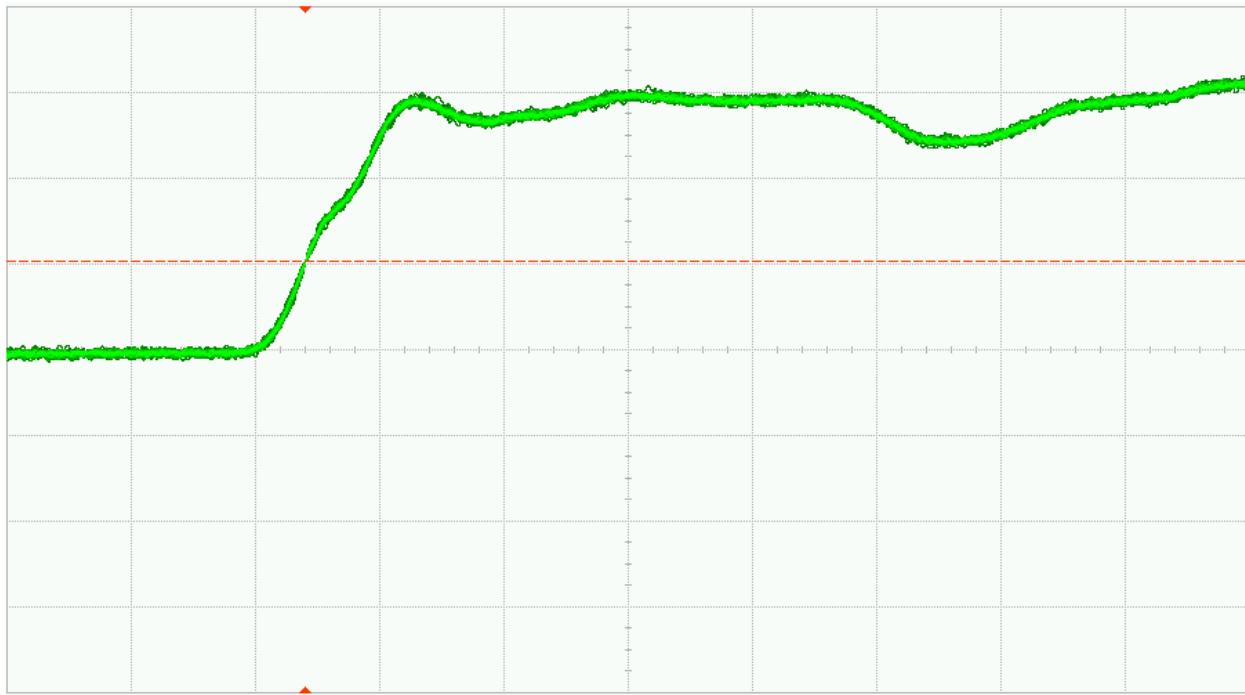


Fig. 29 (a). DUT 01042 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

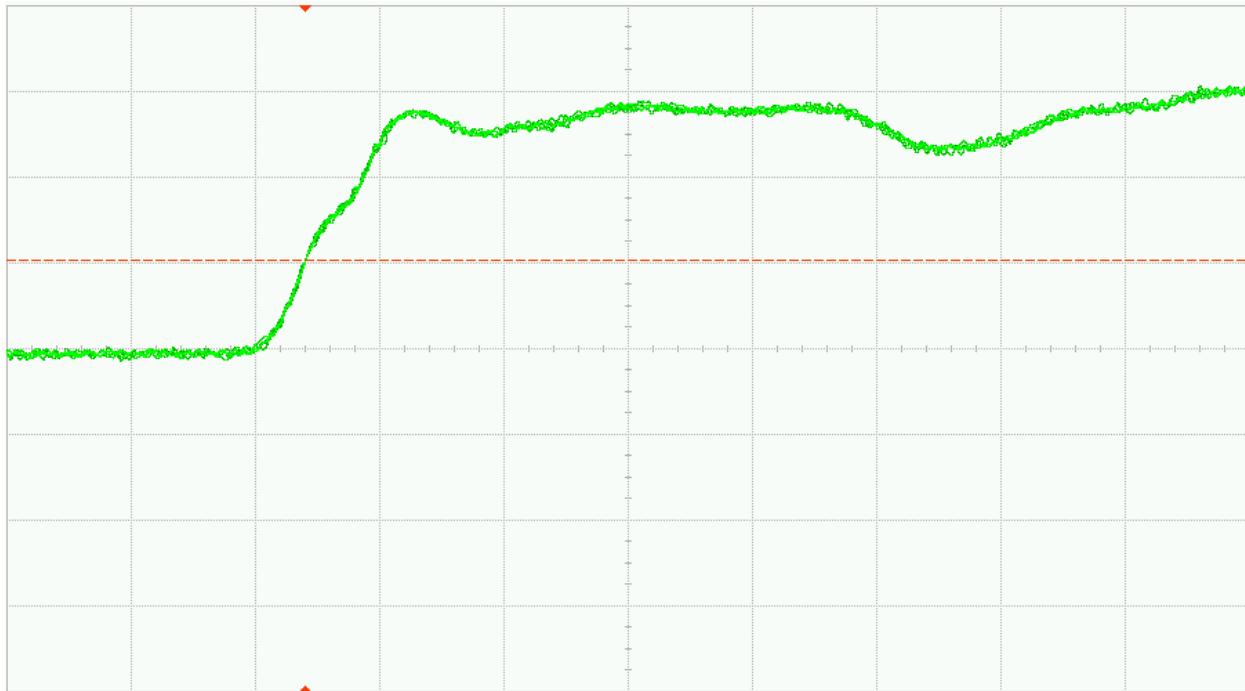


Fig. 29 (b). DUT 01042 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

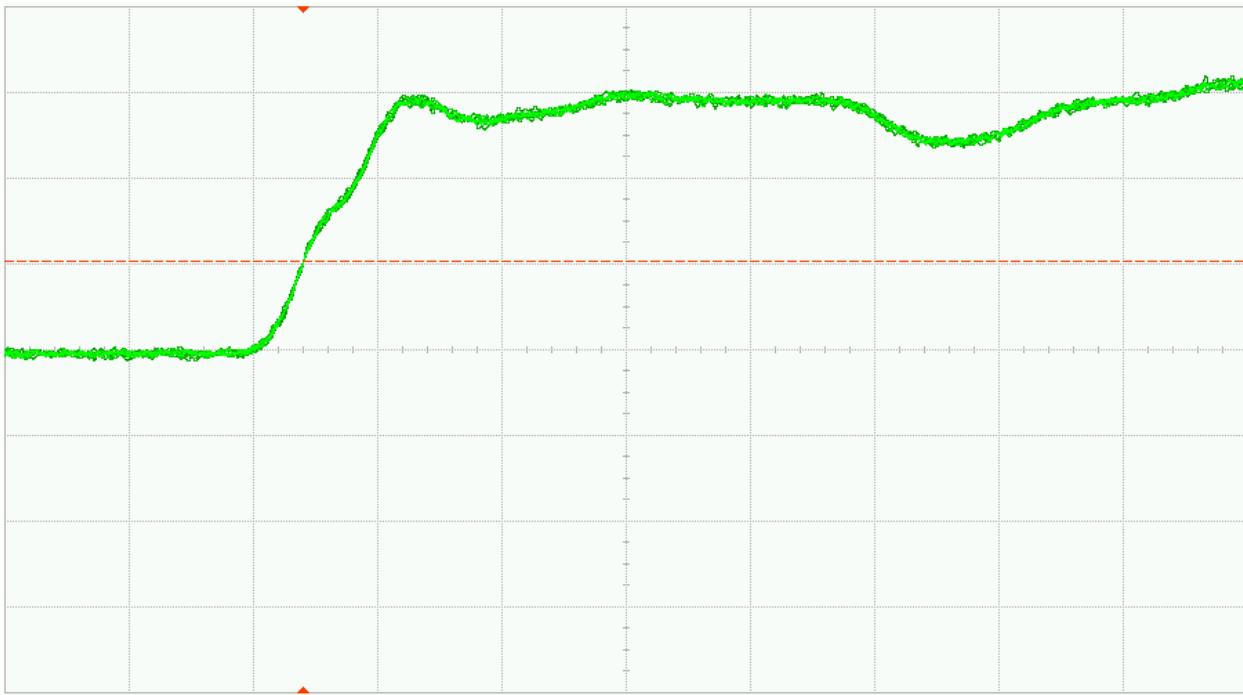


Fig. 30 (a). DUT 01153 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 30 (b). DUT 01153 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

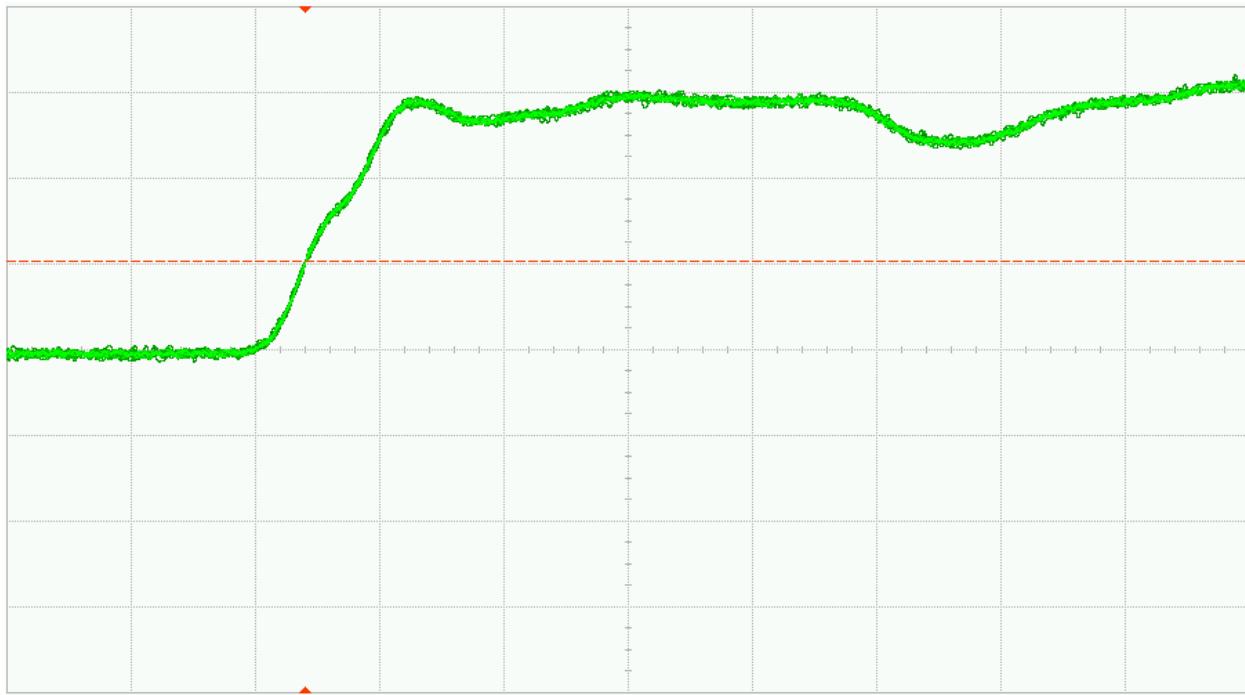


Fig. 31 (a). DUT 01167 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 31 (b). DUT 01167 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

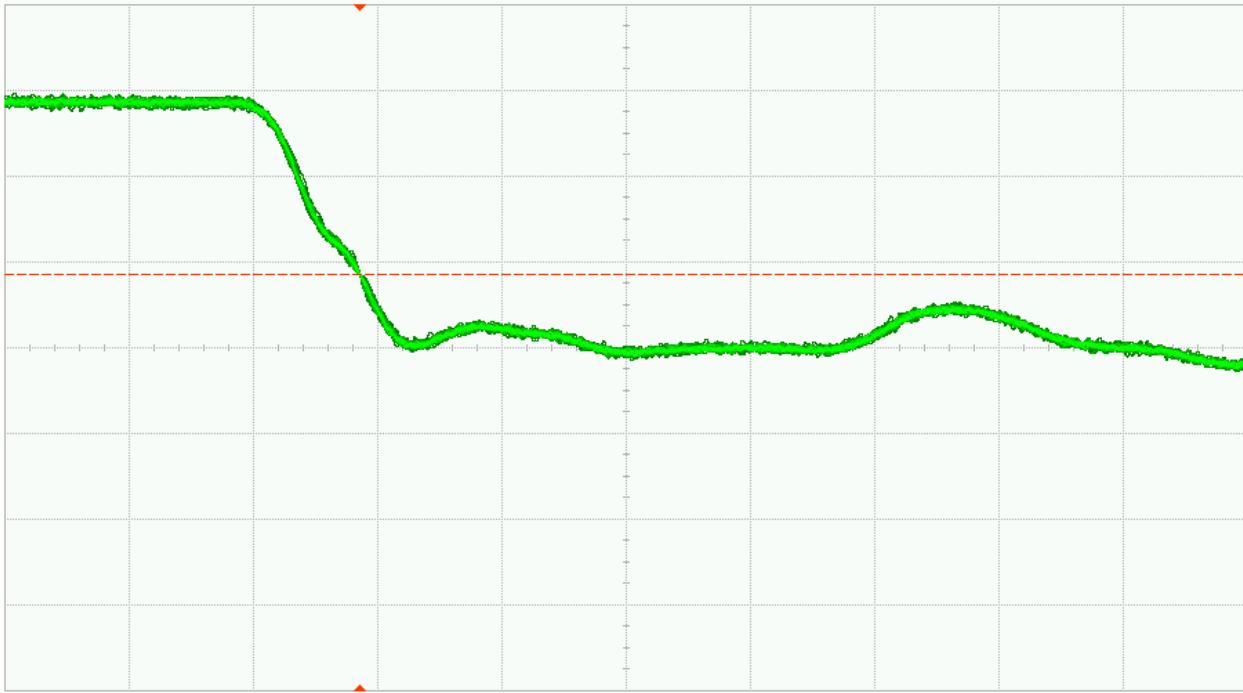


Fig. 32 (a). DUT 01020 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 32 (b). DUT 01020 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 33 (a). DUT 01027 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 33 (b). DUT 01027 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

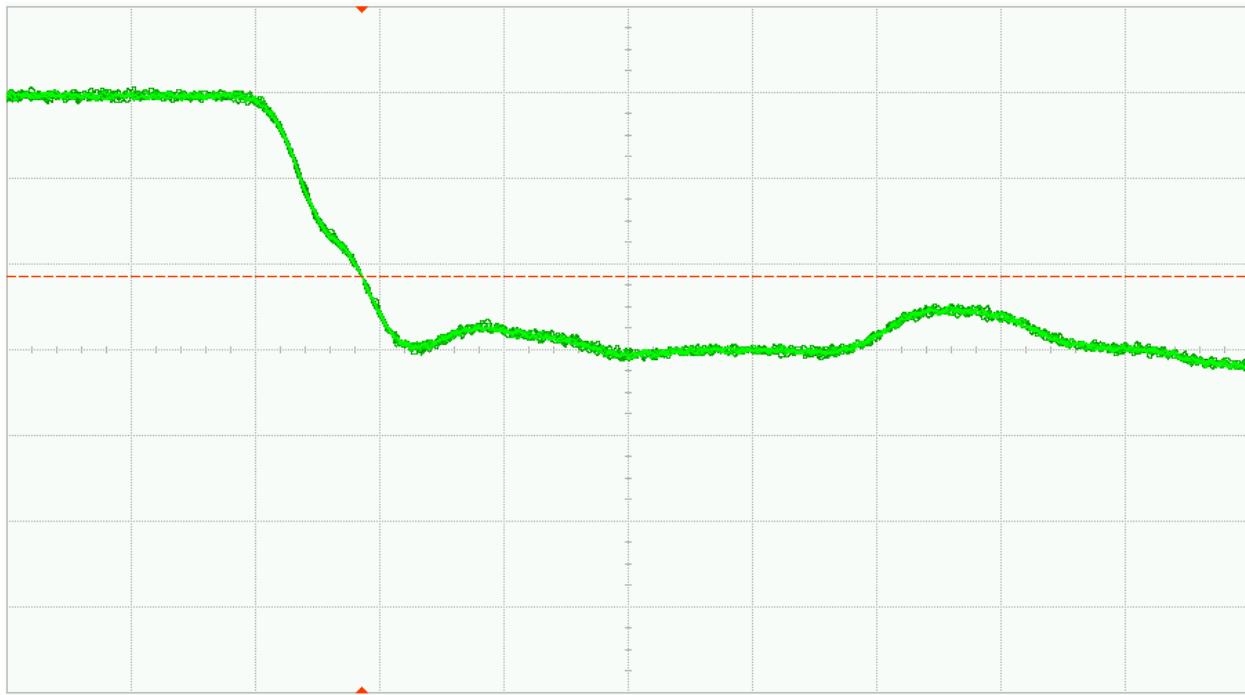


Fig. 34 (a). DUT 01033 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 34 (b). DUT 01033 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 35 (a). DUT 01042 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

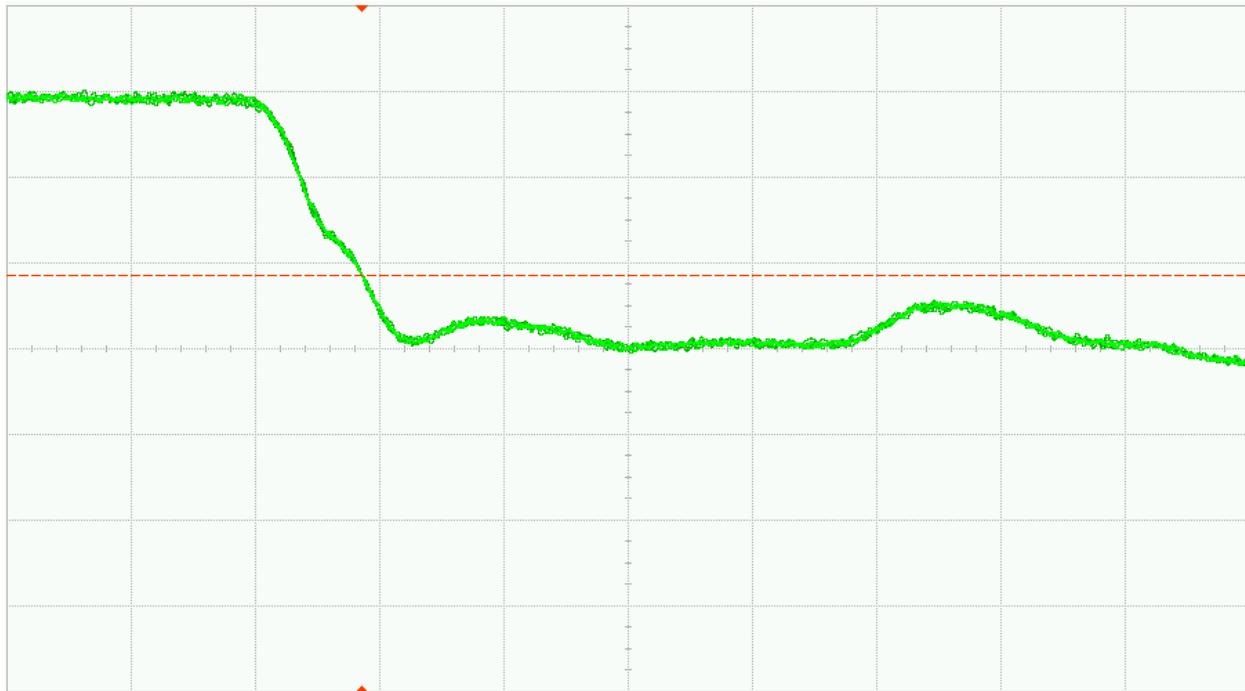


Fig. 35 (b). DUT 01042 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 36 (a). DUT 01153 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 36 (b). DUT 01153 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 37 (a). DUT 01167 pre-irradiation falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div



Fig. 37 (b). DUT 01167 post-annealing falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 35. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	Coverage
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 μ RAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

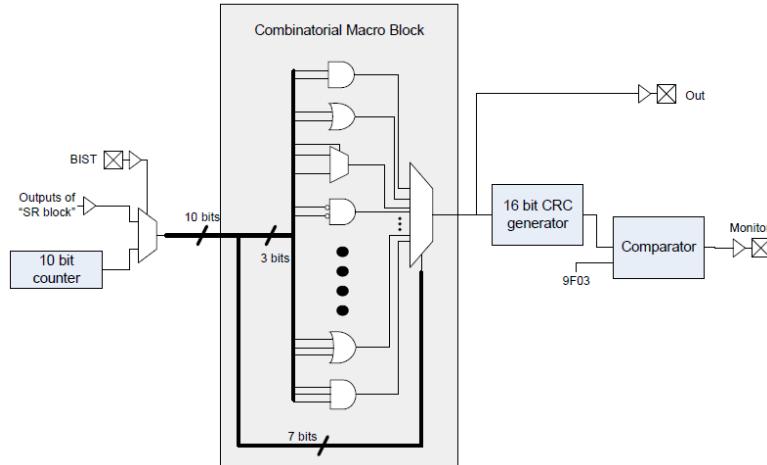


Fig. 38. Combo Block

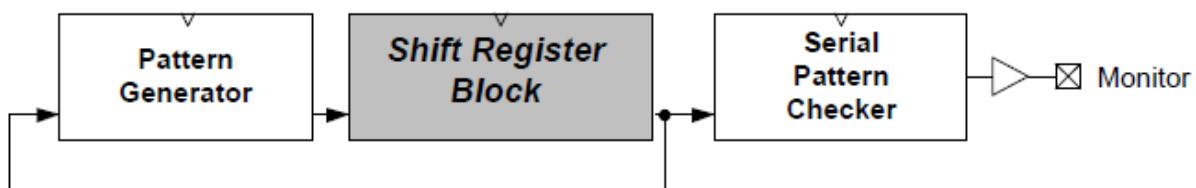


Fig. 39. Shift Register Block

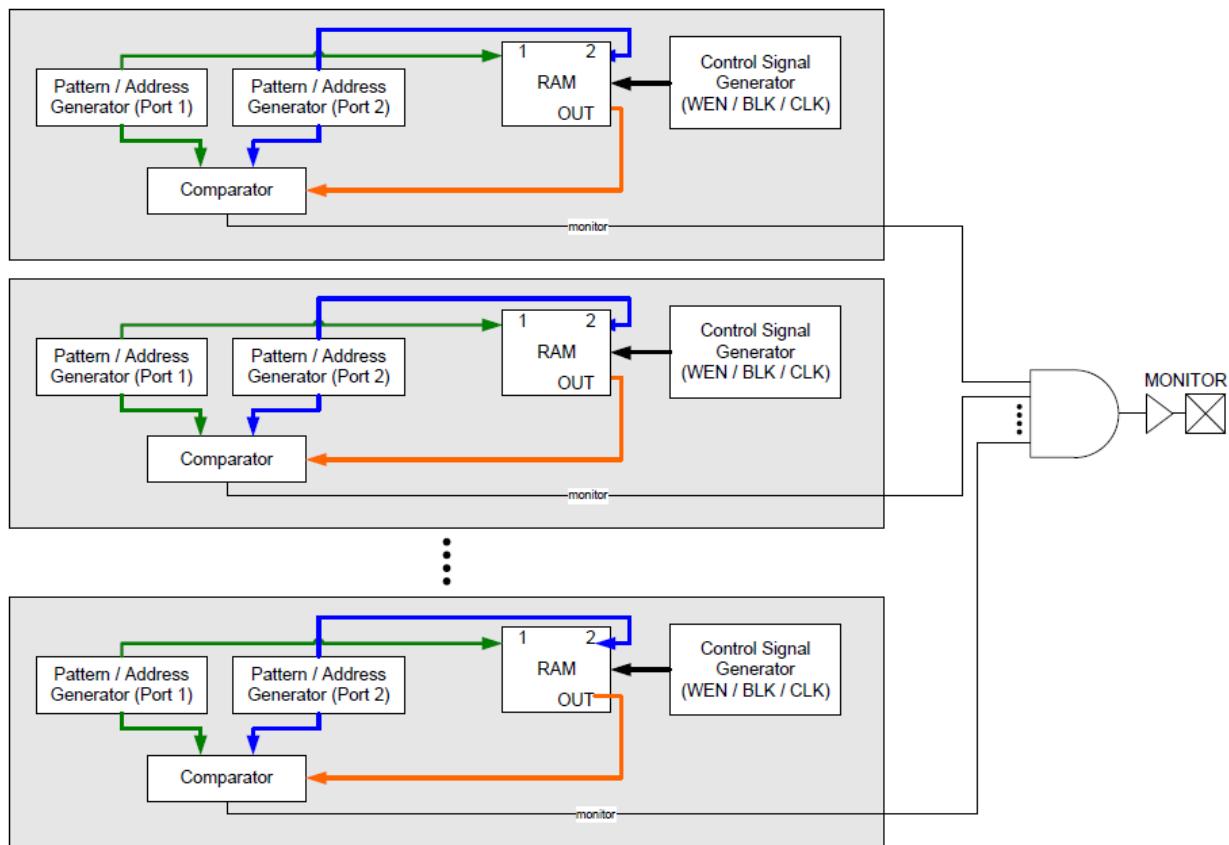


Fig. 40. Embedded Ram Blocks

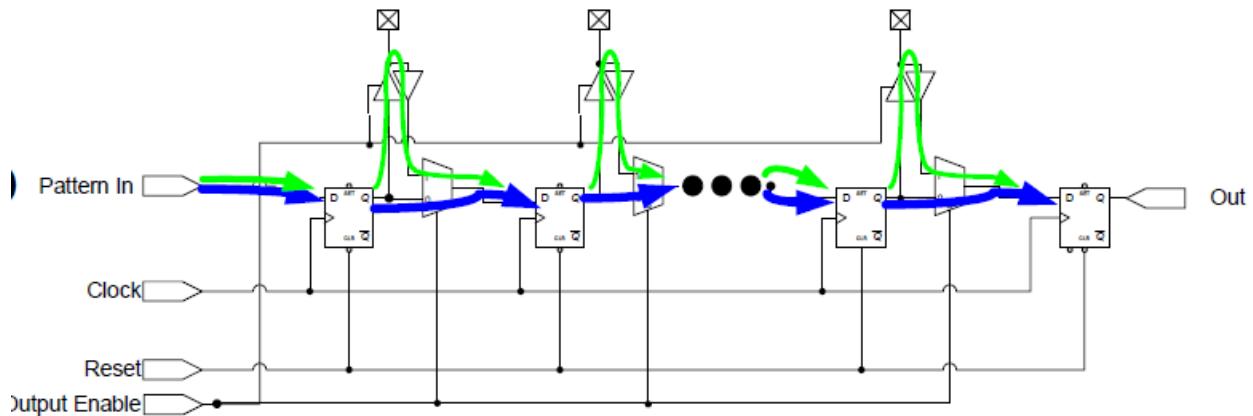


Fig. 41. IO Block

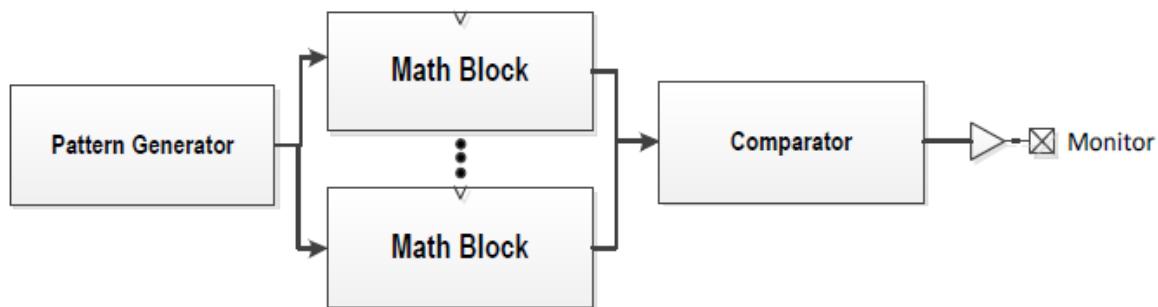


Fig. 42. Math Block



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