RT PolarFire® FPGA Board Design User Guide

Introduction

Good board design practices are required to achieve expected performance from both PCBs and RT PolarFire® devices. High-quality and reliable results depend on minimizing noise levels, preserving signal integrity, meeting impedance and power requirements, and using appropriate transceiver protocols. These guidelines must be treated as a supplement to the standard board-level design practices.

This document is intended for readers who are familiar with the RT PolarFire device, experienced in digital board design, and know about the electrical characteristics of systems. It discusses power supplies, high-speed interfaces, various control interfaces, and the associated peripheral components of RT PolarFire FPGAs.

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1. Designing the Board

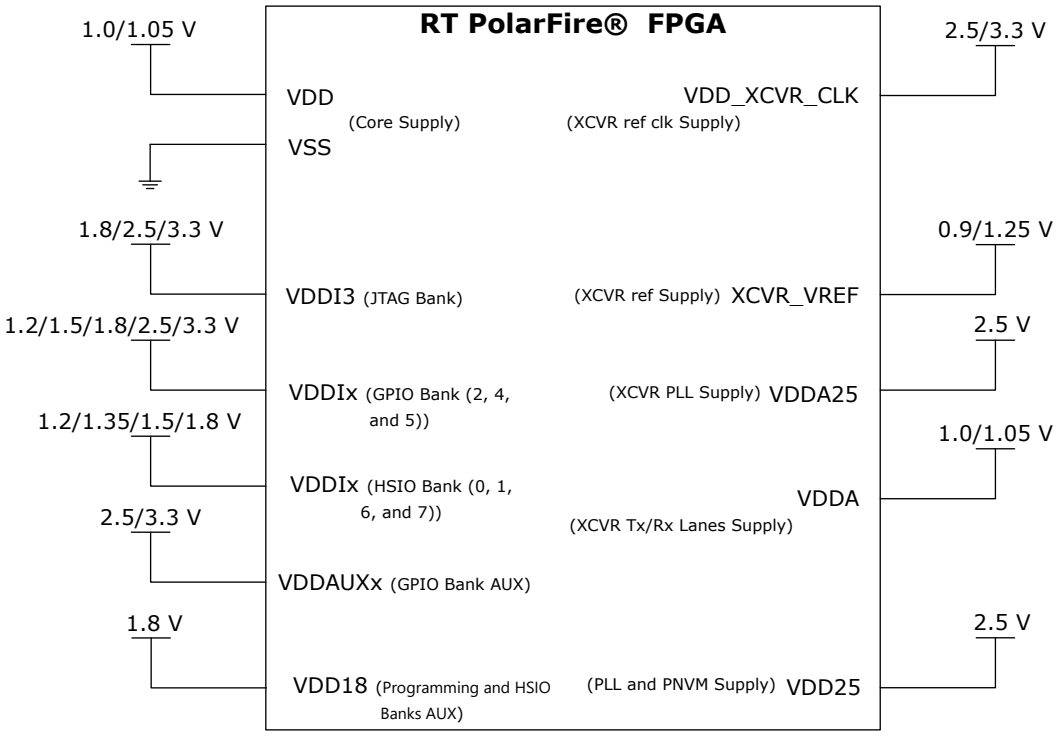
RT PolarFire FPGAs are flash-based FPGAs that support various high-speed memory interfaces such as DDR3/DDR4, lowest power 10 Gbps transceiver (XCVR), built-in low-power dual PCIe Gen2, and fabric I/O such as high-speed I/O (HSIO) and general-purpose I/O (GPIO).

Subsequent sections discuss the following:

1.1 Power Supplies

The following illustration shows the typical power supply requirements for RT PolarFire devices, and the recommended connections of power rails when every part of the device is used in a system. For information on decoupling capacitors associated with individual power supplies, see 1.1.1. RT PolarFire Decoupling Capacitors.

Figure 1-1. Power Supplies



For the device to operate successfully, power supplies must be free from unregulated spikes and the associated grounds must be free from noise. All overshoots and undershoots must be within the absolute maximum ratings provided in the RT PolarFire FPGA Datasheet.

The following table lists the various power supplies required for RT PolarFire FPGAs.

Table 1-1. Supply Pins

Name	Description
XCVR_VREF	Voltage reference for transceivers
VDD_XCVR_CLK	Power to input buffers for the transceiver reference clock
VDDA25	Power to the transceiver PLL
VDDA	Power to the transceiver TX and RX lanes
VSS	Core digital ground
VDD	Device core digital supply
VDDI3 (JTAG Bank)	Power to JTAG bank pins
VDDIx (GPIO Banks)	Power to GPIO bank pins
VDDIx (HSIO Banks)	Power to HSIO bank pins
VDD25	Power to corner PLLs and PNVM
VDD18	Power to programming and HSIO auxiliary supply
VDDAUXx	Power to GPIO auxiliary supply

(1) VDDA—This supply can be powered to 1.0V or 1.05V. For more information, see tables 4-2 in RT PolarFire FPGA Datasheet. This is a quiet supply for the device. One method would be to use a Linear regulator to ensure the supply is quiet.
(2) VDD —This supply can be powered to 1.0V or 1.05V. For more information, see tables 4-2 in RT PolarFire FPGA Datasheet.

VREFx—is the reference voltage for DDR3 and DDR4 signals. VREF voltages can be generated internally and externally.

- Internal VREF - not subjected to PCB and package inductance and capacitance loss. These changes provide the highest performance and can be programmed as required by DDR controller.
- External VREF—is fixed and cannot be programed as required. The PCB and package inductance and capacitance impact the VREF performance.

If VDDI and VDDAUX need to be configured to the same voltage (2.5V or 3.3V), ensure both VDDI and VDDAUX are supplied from the same regulator. Do not use different regulators to source these rails. This prevents any voltage variations between VDDI and VDDAUX. In this case, the board must not supply the VDDI and VDDAUX from individual voltage supplies.

When a GPIO bank requires the VDDI to be less than 2.5V (1.2V, 1.5V, or 1.8V), the VDDAUX for that bank must be tied to 2.5V supply irrespective of the VDDI supply. The VDDI requires a separate supply for the specific I/O type (1.5V or 1.8V).

Note: The on-chip power-on reset circuitry requires the VDD, VDD18, and VDD25 supplies to ramp monotonically from 0V to the minimum recommended operating voltage.

Note: You must initiate the I/O calibration only when both the VDDA and XCVR_VREF supplies are up.

For a detailed pin description, see UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide.

1.1.1 RT PolarFire Decoupling Capacitors

The following table lists the requirement of all decoupling capacitors for the RTPF500-CG1509 device.

Table 1-2. Power-Supply Decoupling Capacitors[1]—RTPF500T - CG1509 (1 mm)

Pin Name	Ceramic								Tantalum
	47 nF	4.7 nF	10 nF	0.1 µF	1 µF	1 nF	10 µF	47 µF	330 µF
VDD	4	—	10	6	—	—	—	2	3
VDD18	—	—	—	2	—	—	—	3	—
VDD25	—	2	2	1	—	—	—	1	—
VDDA	—	2	2	2	—	2	—	2	—
VDDA25	—	—	1	1	—	2	—	2	—
VDDI3	—	—	—	2	—	—	1	—	—
VDDAUXx[2]	—	—	2	1	—	—	—	1	—
GPIO Bank[3]	—	—	—	—	—	2	—	1	—
HSIO Bank[4]	—	1	1	—	—	1	—	1	—
VDD_XCVR_CLK	—	—	—	2	—	—	1	—	—
XCVR_VREF	—	—	—	1	—	—	—	—	—

(1) The guidelines are provided on how to effectively decouple only the FPGA device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the FPGA. Also, follow the recommended operational conditions as per RT PolarFire FPGA Datasheet.
(2) Required Decoupling Capacitor for each VDDAUXx.

(3) Required Decoupling Capacitor for each GPIO bank.

(4) Required Decoupling Capacitor for each HSIO bank.

The following table lists the requirement of all decoupling capacitors for the RTPF500-LG1509 (1 mm) device.

Table 1-3. Power-Supply Decoupling Capacitors[1]—RTPF500T - LG1509 (1 mm)

Pin Name	Ceramic								Tantalum
	47 nF	4.7 nF	10 nF	0.1 µF	1 µF	1 nF	10 µF	47 µF	330 µF
VDD	4	—	10	6	—	—	—	2	3
VDD18	—	—	—	2	—	—	—	3	—
VDD25	—	2	2	1	—	—	—	1	—
VDDA	—	2	2	2	—	2	—	2	—
VDDA25	—	—	1	1	—	2	—	2	—
VDDI3	—	—	—	2	—	—	1	—	—
VDDAUXx[2]	—	—	2	1	—	—	—	1	—
GPIO Bank[3]	—	—	—	—	—	2	—	1	—
HSIO Bank[4]	—	1	1	—	—	1	—	1	—
VDD_XCVR_CLK	—	—	—	2	—	—	1	—	—
XCVR_VREF	—	—	—	1	—	—	—	—	—

(1) The guidelines are provided on how to effectively decouple only the FPGA device. If the power source is placed on a different PCB or delivered through interconnects (flex cables or connectors), ensure an effective power delivery to the FPGA. Also, follow the recommended operational conditions as per RT PolarFire FPGA Datasheet.
(2) Required Decoupling Capacitor for each VDDAUXx.

(3) Required Decoupling Capacitor for each GPIO bank.

(4) Required Decoupling Capacitor for each HSIO bank.

Decoupling capacitors other than those listed in the preceding tables can be used if the physical sizes of capacitors meet or exceed the performance of the network given in this example. Substitution requires analyzing the resulting power distribution system's impedance versus frequency to ensure that no resonant impedance spikes the result. See Figure 1-1 for power supply design.

For more information about the internal package capacitance for power supplies associated with RT PolarFire packages, see Table 6 of UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide.

The following table lists the required decoupling capacitors for RT PolarFire packages.

Table 1-4. Recommended Decoupling Capacitors For RT PolarFire Devices

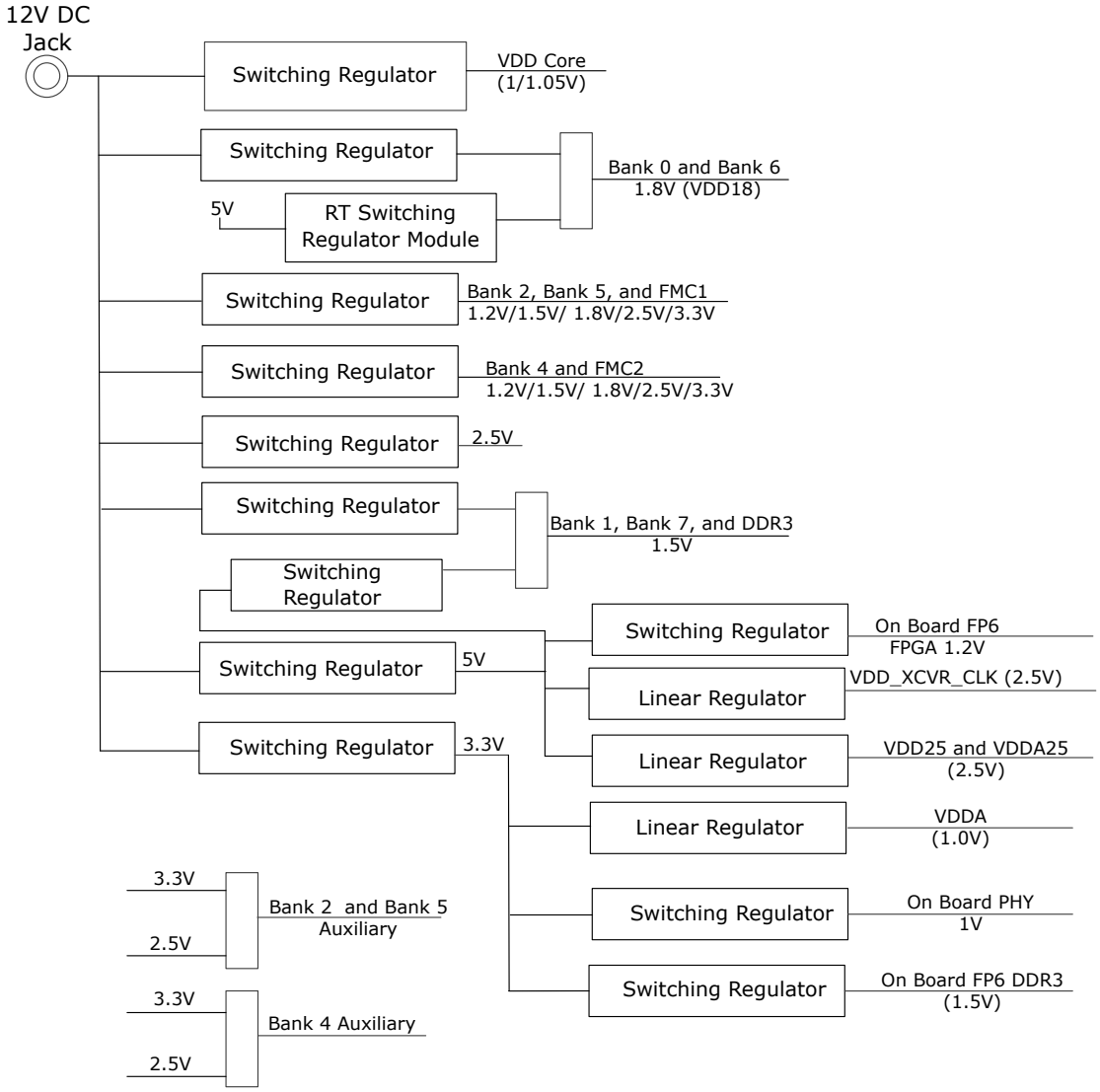
De-Cap Value	Package Size	Part Number	Manufacturer
330 µF	7343	T495D337M006ATE070	KEMET
47 µF	1206	GRM31CR61A476KE15	Murata
0.1 µF	0402	GRM155R71C104KA88	Murata
47 nF	0402	GRM155R11C473KA01	Murata
10 nF	0402	GRM15XR11C103KA86	Murata
4.7 nF	0402	GRM155R11H472KA01	Murata
1 nF	0402	GRM15XR71H102KA86	Murata
10 µF	0805	GRM21BR71A106KE51	Murata

Note: You must use equivalent hi-reliability decoupling capacitor parts. For more information about Packaging Decoupling Capacitors, see UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide.

1.1.2 Power-Supply Topology

RT PolarFire FPGAs require multiple power supplies. The following figure shows a power supply topology example for generating the required power supplies from a single 12 V source. This example is based on the RT PolarFire Evaluation Kit with RTPF500 device with DDR3 and DDR4 interfaces.

Figure 1-2. Example Power-Supply Topology



The following table lists the suggested Microchip power regulators for RT PolarFire FPGA voltage rails.

Table 1-5. Power Regulators

Voltage Rail	Part Number	Description	Current
5V	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
3.3V	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDD18, Bank 0, and Bank 6 (1.8V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
	MHP50601A	Radiation Hardness Assurance 3 – 7 Vin, 6 A, Synchronous Hybrid Point-of-Load DC-DC Converter	6A
2.5V	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A

.....continued

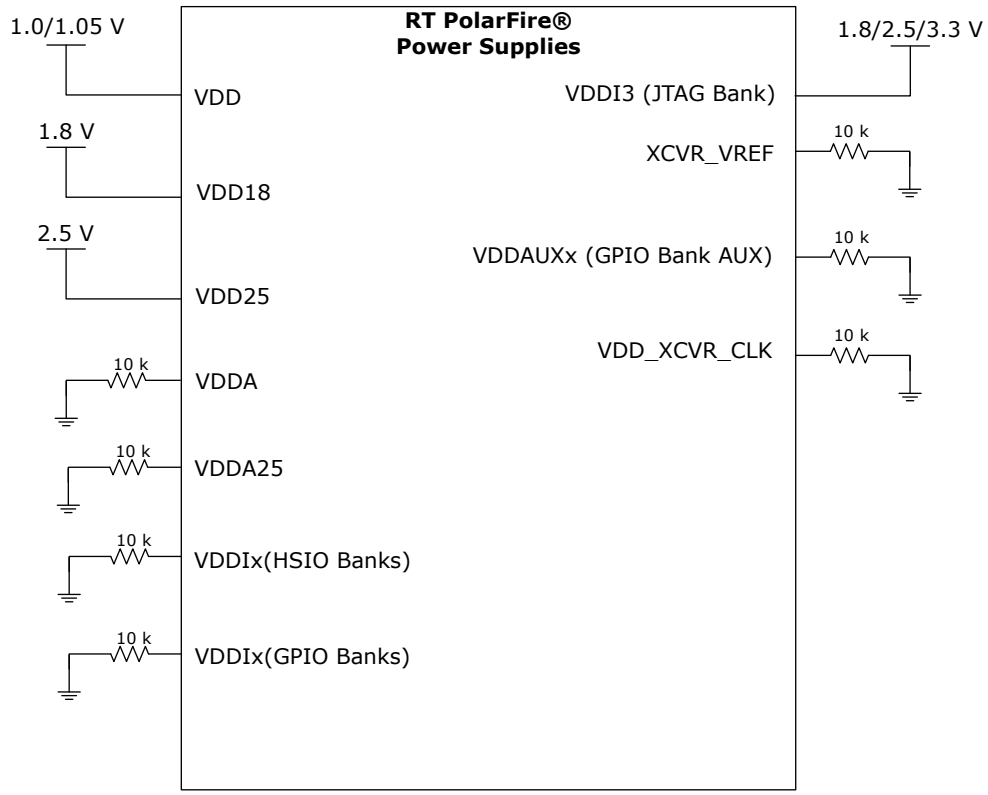
Voltage Rail	Part Number	Description	Current
VDD (1.0/1.05V)	TPS544B25RVFT	IC REG BUCK ADJ 20A 40LQFN	20A
Bank 1 and Bank 7 (1.2/1.5V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
	MHP8565ASC	Radiation Hardened Current-mode, 3A, 560 kHz Switching Freq-Max, Hybrid	3A
VDDI2_5 (1.2/1.5/1.8/2.5/3.3V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDDI4, VADJ_FMC2 (1.2/1.5/1.8/2.5/3.3V)	MIC26950YJL-TR	IC REG BUCK ADJUSTABLE 12A 28MLF	12A
VDDA (1/1.05V)	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD25, VDDDA25 (2.5V)	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD_XCVR_CLK (2.5V)	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
1P2V_FP6 (1.2V)	MIC22705YML-TR	IC REG BUCK ADJUSTABLE 7A 24MLF	7A
1P5V_DDR3 (1.5V)	MIC23303YML-T5	IC REG BUCK ADJUSTABLE 3A 12DFN	3A
1P0V_PHY_VSC8541 (1.0V)	MIC23303YML-T5	IC REG BUCK ADJUSTABLE 3A 12DFN	3A
VTT and VREF - DDR3 DIMM B17	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3A
VTT and VREF - FP6 DDR3	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3A

Note: You must use equivalent hi-reliability parts.

1.1.3 Unused Power Supply

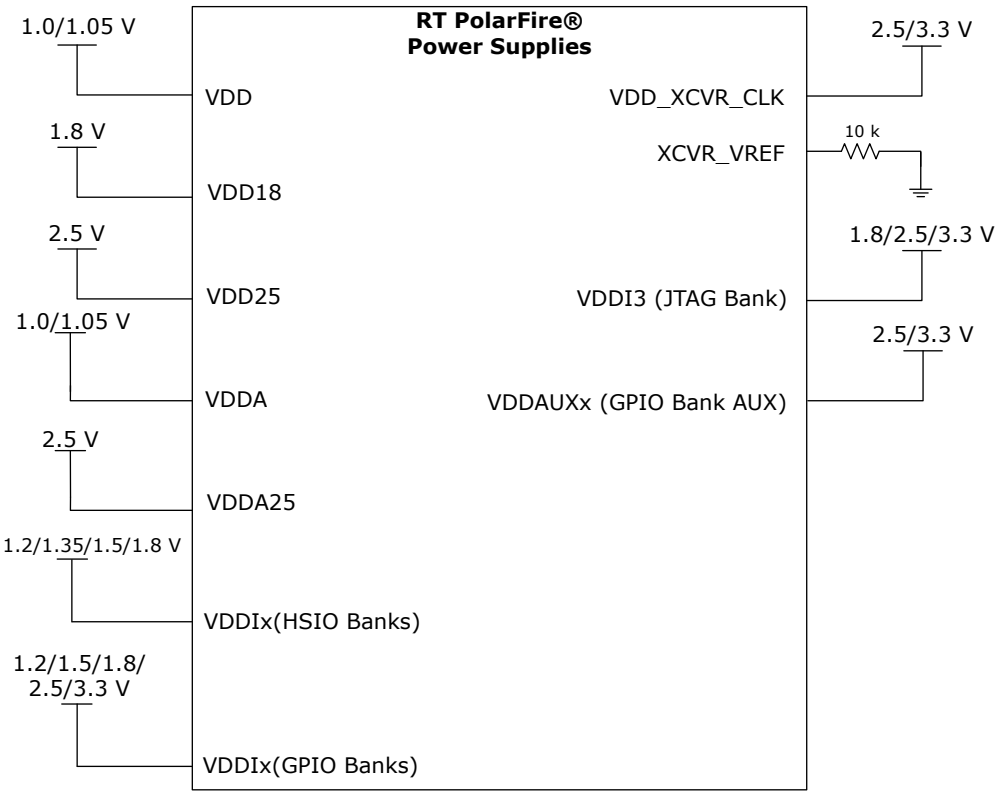
The following figure shows how power supplies may be configured when not in use and also to reduce leakage and power for the system.

Figure 1-3. Option 1 for Unused Connections



The following figure also shows the power configuration of unused supplies. This option can be used when there is an intent to power-up the various supplies at a later time in the system and the I/Os are not being used.

Figure 1-4. Option 2 for Unused Connections



Note: To simplify the board-level routing, multiple 10 kΩ resistors can be used as required. Or the power supplies can also be grouped into a single 10 kΩ resistor and tied-off to VSS.

1.1.4 Pin Assignment Tables

The Packaging Pin Assignment Table (PPAT) is available on the RT PolarFire documentation web page (https://www.microsemi.com/product-directory/rad-tolerant-fpgas/5559-rt-polarfire-fpgas#documents). PPAT contains information about the recommended DDR pin-outs, PCI EXPRESS capability for XCVR-0, DDR Lane information for IO CDR, generic IOD interface pin placement, and unused condition for package pins.

1.2 I/O Glitch

A glitch may occur during power-up or power-down for GPIO/HSIO outputs in RT PolarFire devices. Glitch can occur before or after the device reaches a functional state. These glitches are not observed on LVDS outputs or Transceiver I/Os. No reliability issues are caused by either of the glitch types. There are three types of glitch that can occur.

- Parasitic glitches may occur for GPIOs or HSIOs before the device reaches functional state with a maximum glitch of 1V with a 0.4 ms width. This type of glitch can typically be ignored. It is recommended to use a 100K pull-down resistor on critical signals[1] of the GPIO or HSIO pins if this type of glitch cannot be ignored. No glitches are observed once mitigation recommendations are placed. This may occur for both erased/blank and programmed units.
- Another type of glitch may occur on GPIOs and HSIOs during power-on sequencing or boot-up. This is due to a weak pull-up resistor being enabled by default on an input, output or bidirectional I/O. To mitigate this glitch, use the Libero SoC I/O Editor or PDC constraint to program a weak pull-down on the output buffer on the specified I/O. This may occur for both erased/blank and programmed units.

[1] Critical outputs such as reset or clock of the HSIO or GPIOs going into another device.

- The last type of glitch may occur after the device reaches functional state and may occur for both erased/blank and programmed units. This type of glitch is related to the power-up and power-down sequence of VDDI and VDDAUX supplies. This occurs only on GPIOs where the VDDI is 1.5V or 1.8V only with a maximum glitch of 1V with a 0.8 ms width during power-up and a maximum glitch of 1.8V with a 1 ms width during power down. For HSIOs where the VDDI is 1.5V or 1.8V only a maximum glitch of 600 mV and 1.5 ms width may occur at Power-Up and a maximum glitch of 220 mV and 200 µs width may occur at Power-Down.

To mitigate the post functional state glitch, follow the recommendations in the following tables.

Table 1-6. Power Sequencing[1]

Use Cases for GPIO		Power-up Sequencing Requirement for Mitigating Glitches[2]	Power-down Sequencing Requirements for Mitigating Glitches[2]
VDDI	VDDAUX		
1.2V	2.5V	No Glitch occurs	No Glitch occurs
1.5V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
1.8V	2.5V	Power up VDDAUX before VDDI of that bank	Power down VDDI before VDDAUX of that bank
2.5V	2.5V	Power VDDAUX and VDDI from the same Regulator	No Glitch occurs
3.3V	3.3V	Power VDDAUX and VDDI from the same Regulator	No Glitch occurs

(1) No glitches are observed once mitigation recommendations are placed.
(2) This power sequence does not mitigate any parasitic glitches. As mentioned above, add a 100K pull down resistors to critical signals of GPIO or HSIO pins for mitigation of parasitic glitches.

Table 1-7. Power Sequencing[1]

Use Cases for HSIO		Power-up Sequencing Requirement for Mitigating Glitches[2]	Power-down Sequencing Requirements for Mitigating Glitches[2]
VDDI	VDD18		
1.2V	1.8V	No Glitch occurs	No Glitch occurs
1.5V	1.8V	Power up VDD18 before VDDI of that bank	Power down VDDI before VDD18, VDD, VDD25 of that bank
1.8V	1.8V	Power up VDD18 before VDDI of that bank	Power down VDDI before VDD18, VDD, VDD25 of that bank

(1) No glitches are observed once mitigation recommendations are placed.
(2) This power sequence does not mitigate any parasitic glitches. As mentioned above, add a 100K pull down resistors to critical signals of GPIO or HSIO pins for mitigation of parasitic glitches.

1.3 User I/O

RT PolarFire FPGAs have two types of I/O buffers: HSIO and GPIO. HSIO buffers are optimized for single-ended buffers with supplies from 1.2V to 1.8V. GPIO buffers support single-ended and true differential interfaces with supplies from 1.2V to 3.3V.

Note: When the HSIO bank is configured as an LVDS receiver, the concerned I/Os must be connected externally by a 100Ω resistor.

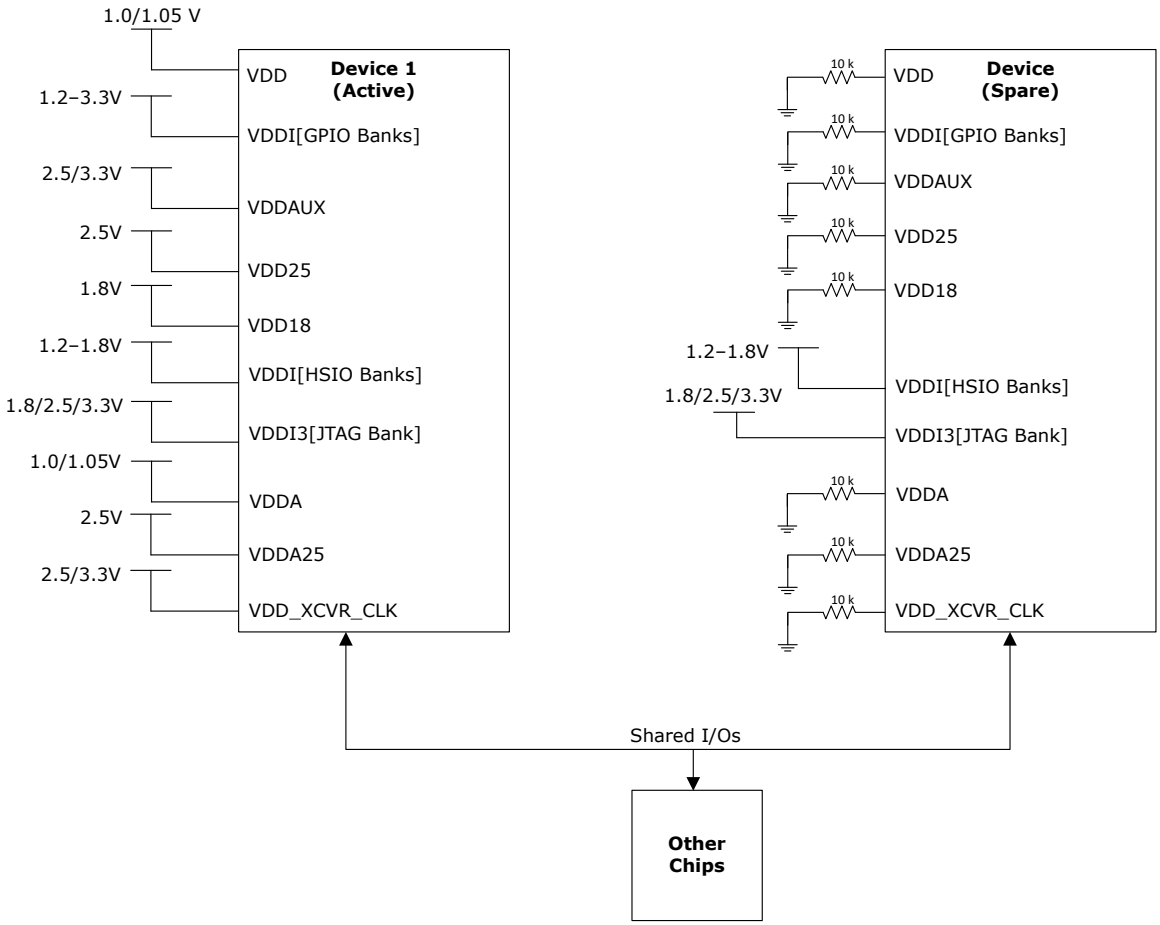
For more information about key features of I/O buffers and supported standards, see UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide UG0931: RT PolarFire FPGA User I/O User Guide. and UG0931: RT PolarFire FPGA User I/O User Guide.

1.3.1 Cold Sparing

RT PolarFire devices support cold sparing for GPIO and HSIO. Cold sparing is implemented by connecting the devices as shown in the following figure. The system board has two RT PolarFire devices in parallel and the devices share I/O. The spare device has its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes. As a result, low power and a protected state for the spare device is established. The spare device can be changed to active device by powering-up all the supplies. The active device can be changed to spare device by powering down all the supplies except HSIO VDDI banks.

A typical cold sparing application integrates two parallel devices with shared I/O connections, as shown in the following figure.

Figure 1-5. Cold Sparing



Note: Transceiver pins do not support the cold sparing feature.

1.3.2 Hot Socketing (GPIO Only)

Hot socketing (also known as hot swapping or hot plug-in) prevents damage to the RT PolarFire FPGA if, at any time, voltage is detected at I/O while the device is powered off. It also helps prevent disruptions that may occur in the rest of the system if the I/O of a device are connected without a valid power supply.

Only GPIOs support hot socketing. In hot socketing, GPIOs are in high-impedance (hi-Z) state.

The GPIO maintains the following high-impedance state until the power supplies are at a valid state.

- VDDAUx is greater than or equal to 1.6V.
- VDDIx is greater than or equal to 0.8V.
- VDD and VDD25 are both high and the RT PolarFire FPGA controller has asserted the global I/O ring signal (IO_EN).

Note: TMS, TDI, TRSTB, DEVRST_N and FF_EXIT_N do not support hot socketing.

1.3.2.1 Over-Voltage Tolerance for GPIO

If GPIO is configured with the following settings, GPIO supports over-voltage tolerance, ensuring that the I/O signal at the pad is at a higher potential than the VDDIx power supply.

Table 1-8. Over-Voltage Tolerance

Standard	OE	Clamp Diode	VREF (Input)	Weak Pull-Up/ Pull-Down	Termination	Hot-plug
PCI	x	ON	ON	ON	ON	Disabled
GPIO	1	ON	ON	ON	ON	Disabled
	0	OFF	OFF	OFF	OFF	Enabled

For recommended operating conditions about over-voltage tolerance, see RT PolarFire FPGA Datasheet.

1.4 Clocks

RT PolarFire devices offer two on-chip RC oscillators (one 2 MHz and one 160 MHz) to generate free-running clocks. The clocks do not have any I/O pads and do not require external components to operate.

The following table lists the number of RC oscillators available in RT PolarFire devices.

Table 1-9. RC Oscillator Count

Resource	Supported Range (MHz)	RTPF500
On-chip oscillator	2	1
	160	1

You must understand the regional clock implications when targeting designs that might be migrated to different device sizes. You must also go through the pin planning before finalizing it on the board while targeting a die. For more information about clocking in RT PolarFire devices, see PolarFire and PolarFire SoC FPGA Clocking Resources User Guide.

For information about the preferred clock inputs connectivity to PLLs, DLLs, and global clock network, see the Packaging Pin Assignment Table (PPAT) on the RT PolarFire documentation web page.

1.5 Reset

For designing a robust system, you can use the dedicated DEVRST_N pin or a general purpose reset signal using any GPIO/HSIO as a global system level reset.

For the following cases, you can use the DEVRST_N pin as a warm reset for the device:

- A user design modifies auto-initialized fabric RAMs or PCIe configuration during operation.
- A user design, which includes PCIe, transceivers or user crypto.

For all other use cases, it is recommended to use a general purpose reset signal using any GPIO/HSIO IO because they take much shorter time for design to come out of reset.

If the dedicated DEVRST_N is not used for warm resets, the DEVRST_N pin must be configured using one of the following methods:

- Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted till the system/clocks are stable and the chip is properly powered up.
- Connect DEVRST_N to VDDI3 through a 1 kΩ resistor per pin without sharing with any other pins.
  - In this case, ensure that all clocks are stable going to the device before the user design is released from power-on reset. The details of the minimum time taken for the fabric design to be activated after power-on is specified in the RT PolarFire Datasheet (Power-Up To Functional section).

1.6 DDR

RT PolarFire devices support DDR3, DDR3L, LPDDR3, and DDR4. For more information about the DDR support in RT PolarFire devices, see RT PolarFire FPGA Datasheet.

The reliability of the DDR interface depends on the quality of the layout. For detailed information on board layout and routing, see RT PolarFire FPGA DDR Memory Controller User Guide (to be published).

1.7 Device Programming

The RT PolarFire device can be programmed using one of two dedicated interfaces: JTAG or SPI. These two interfaces support the following programming modes:

- JTAG programming
- SPI master mode programming
- SPI slave mode programming

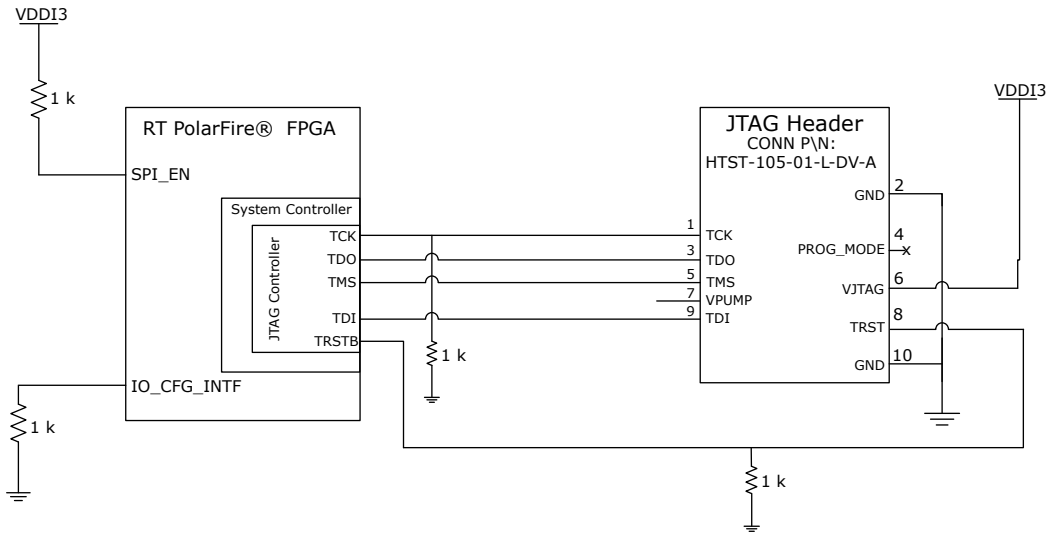
The RT PolarFire FPGA supports programming modes through the internal system controller using SPI master mode, or an external master using JTAG or SPI interfaces. For detailed information on hardware connections for each programming mode, see RT PolarFire FPGA Programming User Guide (to be published).

1.7.1 JTAG Programming

The JTAG interface is used for device programming and testing, or for debugging firmware. When the device reset (DEVRST_N) is asserted, JTAG I/Os are not accessible. JTAG I/Os are powered by Bank 3 VDDI.

The following illustration shows the board-level connectivity for JTAG programming mode in RT PolarFire devices.

Figure 1-6. JTAG Programming



The following table lists the JTAG pin names and descriptions.

Table 1-10. JTAG Pins

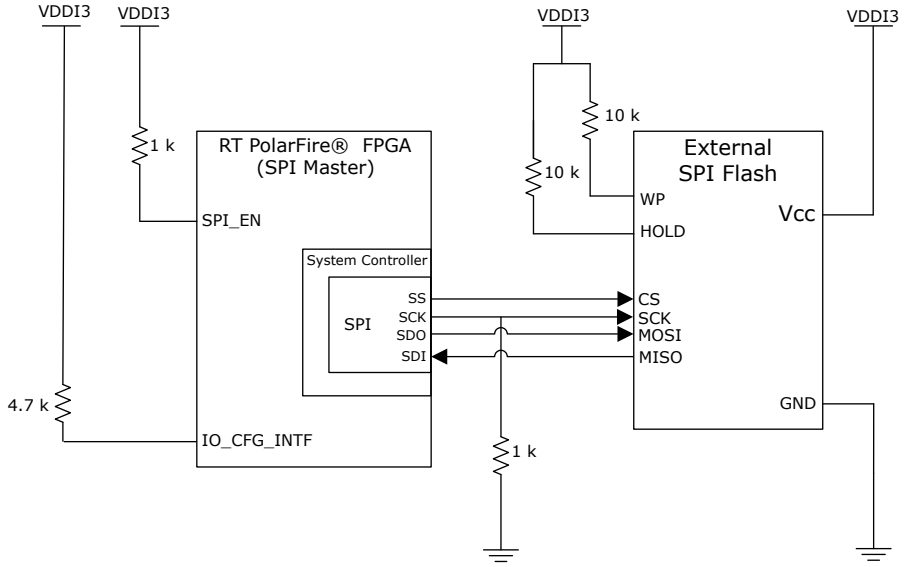
Pin Names	Direction	Unused Condition	Description
TMS	Input	DNC	JTAG test mode select.
TRSTB	Input	Must be connected to VDDI3 through a 1 kΩ resistor	JTAG test reset. Must be held low during device operation.
TDI	Input	DNC	JTAG test data in.
TCK	Input	Must be connected to VSS through a 10 kΩ resistor	JTAG test clock.
TDO	Output	DNC	JTAG test data out.

1.7.2 SPI Master Mode Programming

The embedded system controller contains a dedicated SPI block for programming, which can operate in master or slave mode. In master mode, the RT PolarFire device interfaces are used to download programming data through the external SPI flash. In slave mode, the SPI block communicates with a remote device that initiates download of programming data to the device.

The following illustration shows the board-level connectivity for SPI master mode programming in RT PolarFire devices.

Figure 1-7. SPI Master Mode Programming



The following table lists the SPI master mode programming pins.

Table 1-11. SPI Master Mode Programming Pins

SPI Pin Name	Direction	Unused Condition	Description
SCK	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI clock.
SS	Bidirectional	Connect to VSS through a 10 kΩ resistor	SPI slave select.[1]

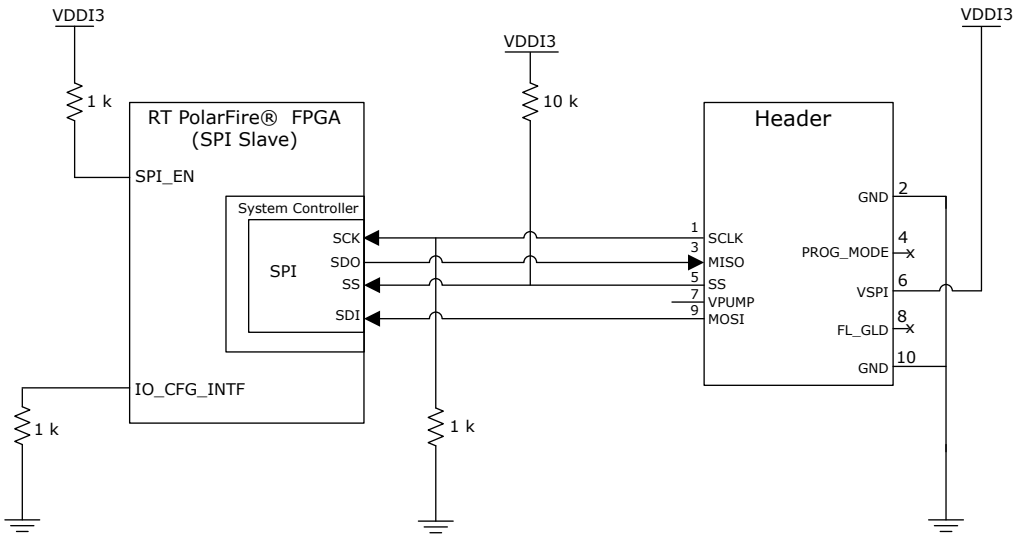
.....continued			
SPI Pin Name	**Direction**	**Unused Condition**	**Description**
SDI	Input	Connect to VDDI3 through a 10 kΩ resistor	SDI input.[1]
SDO	Output	DNC	SDO output.[1]
SPI_EN	Input	Connect to VSS through a 10 kΩ resistor	SPI enable. 0: SPI output tri-stated 1: Enabled Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Connect to VSS through a 10 kΩ resistor	SPI I/O configuration. 0: SPI slave interface 1: SPI master interface Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI is a master or slave.

(1) The SCK, SS, SDI, and SDO pins are shared between the system controller and the FPGA fabric. When the system controller's SPI is enabled and configured as a master, the system controller hands over the control of the SPI to the fabric (after device power-up).

1.7.3 SPI Slave Mode Programming

The following illustration shows the board-level connectivity for SPI slave mode programming in RT PolarFire devices.

Figure 1-8. SPI Slave Mode Programming



1.7.4 Special Pins

For information about special pins, see Table 14 of UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide.

1.8 Transceiver

The following table lists the transceiver features supported in RT PolarFire devices, and transceiver blocks are located on the east corner of the device. RT PolarFire devices support PCIe interface only on Transceiver quad 0.

For more information about implementing PCIe interfaces, see PolarFire and PolarFire SoC FPGA PCI Express User Guide. For more information about implementing other transceiver based interfaces and power supplies, see UG0936: RT PolarFire FPGA Transceiver User Guide.

The following table lists the number of transceivers supported in various RT PolarFire devices.

Table 1-12. Transceiver Support in RT PolarFire Devices

Device	Transceiver Lane	Tx PLL	Reference Clock I/O
RTPF500	24	15	30

For more information about supported I/O standards, see UG0931: RT PolarFire FPGA User I/O User Guide.

1.8.1 Reference Clock

A transceiver reference clock is delivered to each transmit PLL for transmit functions and to each receiver lane for receive clock data recovery (CDR).

1.8.1.1 Transceiver Reference Clock Requirements

The following are requirements for the transceiver reference clock:

- When differential clock input is provided to the reference clock:
  - ODT must be enabled for transceiver reference clock pins.
  - Must be within the range of 20 MHz to 400 MHz.
- Must be within the tolerance range of I/O standards. The reference input buffer is provided and is expected to support these input standards directly without external components on the board. The reference I/O standards such as LVCMOS25, SSTL18, LVDS25, and HCSL25 are supported. For more information, see UG0936: RT PolarFire FPGA Transceiver User Guide.

See the PCI Express Base specification Rev 2.1 for detailed PHY specifications. Also, see the PCIe Add-in Card Electro-Mechanical (CEM) specifications.

1.9 AC and DC Coupling

Each transmit channel of a PCIe lane must be AC-coupled to allow link detection. Capacitors used for AC coupling must be external to the device and large enough to avoid excessive low-frequency drops when the data signal contains a long string of consecutive identical bits. For non-PCIe applications, Microchip recommends that an RT PolarFire device receives inputs that are AC-coupled to prevent common-mode mismatches between devices. Suitable values (for example, 0.1 µF) for AC-coupling capacitors must be used to maximize link signal quality and must conform to RT PolarFire FPGA Datasheet electrical specifications.

For lower data rates as per the data sheet, DC coupling is supported by RT PolarFire Transceiver Tx and Rx interfaces through a configuration option. If an RT PolarFire transmitter is used to drive an RT PolarFire receiver in DC-coupled mode, select the lowest common mode setting for the transmitter.

1.10 Brownout Detection

The RT PolarFire FPGA functionality is guaranteed only if VDD is above the recommended level specified in the Datasheet. Brownout detection occurs when VDD drops below the minimum recommended operating voltage. When this occurs, the device operation may not be reliable. The design might continue to malfunction even after the supply is brought back to the recommended values because parts of the device might have lost functionality during brownout. The VDD supply is protected by an built-in brownout detection circuit.

2. Board Design Checklist

This chapter provides a set of hardware board design checks for designing hardware using Microchip RT PolarFire FPGAs. The checklists provided in this chapter are a high-level summary checklist to assist the design engineers in the design process.

2.1 Prerequisites

Ensure that you have gone through the following chapters before reading this chapter:

- 1. Designing the Board
- 3. Appendix: General Layout Design Practices

This checklist is intended as a guideline only. The RT PolarFire FPGA consists of 500K logic elements (LEs) density.

2.2 Design Checklist

The following table lists the various checks that design engineers must take care while designing the system.

Table 2-1. Design Checklist

Guideline	Yes/No	Remarks
Prerequisites		
– See RT PolarFire FPGA Datasheet – See UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide – See CG1509 Package Pin Assignment Table		
See the board-level schematics of RT PolarFire Evaluation Kit		
Device Selection		
Check for available device variants for RT PolarFire FPGA – Select a device based on I/O pin count, transceivers, package, phase-locked loops (PLLs), and speed grade		
Check device errata in RT PolarFire FPGA Errata		
Design Checklist		
Power Analysis Download the UG0897: PolarFire and PolarFire SoC FPGA Power Estimator User Guide and check for the power budget.		
Power Supply Checklist See Figure 1-1 for used power rails, and Figure 1-3 and Figure 1-4 for unused rails.		
Decoupling Capacitors Follow 1.1.1. RT PolarFire Decoupling Capacitors. Perform PI Analysis for any deviation from the recommended capacitors.		
Clocks		
For more information about dynamic phase shift ports, see Table 6 of PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide. The XCVR reference clock ranges from 20 MHz to 400 MHz.		

.....continued		
Guideline	**Yes/No**	**Remarks**
The global clock network can be driven by any of the following: – Preferred clock inputs (CLKIN_z_w) – On-chip oscillators – CCC (PLL/DLL) – XCVR interface clocks For information about the preferred clock inputs connectivity to PLLs, DLLs, and global clock network, see the Packaging Pin Assignment Table (PPAT) on the RT PolarFire documentation web page. **High-Speed I/O Clocks** High-speed I/O clock networks can be driven by I/O or CCCs. The high-speed I/O clocks can feed reference clock inputs of adjacent CCCs through hardwired connections. **CCC** The CCC can be configured to have a PLL or DLL clock output, driving a high-speed I/O clock network.		
Global Buffer (GB) can be driven through the dedicated global I/O, CCC or fabric (regular I/O) routing. The global network is composed of GBs to distribute low-skew clock signals or high-fanout nets. Dedicated global I/O drive the GBs directly and are the primary source for connecting external clock inputs (to minimize the delay) to the internal global clock network. For more information about global clock network, see PolarFire FPGA and PolarFire SoC FPGA Clocking Resources User Guide.		
Reset		
For more information about DEVRST_N and user reset, see 1.5. Reset.		
DDR Interface		
For more information about DDR routing and topology, see RT PolarFire FPGA DDR Memory Controller User Guide (to be published).		
Programming and Debugging Scheme For programming and debugging information, see 1.7. Device Programming.		
XCVR		
For more information about XCVR, see UG0936: RT PolarFire FPGA Transceiver User Guide.		
For I/O gearing interfaces, place the clocks and data based on the defined requirements by selecting the correct I/O. For more information about the placement of User I/O, see UG0931: RT PolarFire FPGA User I/O User Guide.		
There is one IO_CFG_INTF pin available, which can be used as input.		
See the bank location diagrams in the UG0933: RT PolarFire FPGA Packaging and Pin Descriptions User Guide to assess the preliminary placement of major components on PCB.		

2.3 Layout Checklist

The following table lists the layout checklist.

Table 2-2. Layout Checklist

Guideline	Yes/No
Power	
Are the 0402 or lesser size capacitors used for all decapacitors?	
Is the required copper shape provided to core voltage?	
Are the required copper shape and sufficient vias provided to voltages?	
Are VREF planes for the DDRx reference supply isolated from the noisy planes?	
Are sufficient number of decoupling capacitors used for the DDRx core and VTT supply?	
Is one 0.1 µF capacitor for two VTT termination resistors used for DDRx?	
Is the VTT plane width sufficient?	
DDR Memories	
Are the length-match recommended by DDR manufacturer followed for DDR memories?	
XCVR	
Are the length-match recommendations for XCVR followed?	
Are DC blocking capacitors required for PCIe interface?	
Is tight-controlled impedance maintained along the XCVR traces?	
Are differential vias well designed to match XCVR trace impedance?	
Are DC blocking capacitor pads designed to match XCVR trace impedance?	
Dielectric Material	
Is proper PCB material selected for critical layers?	

3. Appendix: General Layout Design Practices

This chapter provides guidelines for the hardware board layout that incorporates RT PolarFire devices. Good board layout practices are essential to achieve the expected performance from PCBs and RT PolarFire devices. They help achieve high-quality and reliable results such as low-noise levels, signal integrity, impedance, and power requirements. The guidelines mentioned in this document act as a supplement to the standard board-level layout practices.

This chapter is intended for readers who are familiar with the RT PolarFire FPGA chip, experience in digital board layout, and know about line theory and signal integrity.

3.1 Transceiver

Collateral material of the RT PolarFire FPGA transceiver enables the system implementation easier for the designer by providing the system solution. Transceivers are high-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 10.3125 Gbps. For these transceiver-based interfaces, the system designer must be familiar with the industry specifications, transceivers technology, or RF/microwave PCB design. However, the PCB design can be evaluated by a knowledgeable high-speed digital PCB designer.

3.1.1 Layout Considerations

This section describes differential traces and skew matching, which must be taken care while designing the PCB layout.

3.1.1.1 Differential Traces

A well-designed differential trace must have the following qualities:

- No mismatch in impedance
- Insertion loss and return loss
- Skew within the differential traces

The following points must be considered while routing the high-speed differential traces to meet the previous qualities.

- The traces must be routed with tight length matching (skew) within differential traces. Asymmetry in length causes conversion of differential signals in common mode signals.
- The differential pair must be routed such that the skew within differential pairs is less than 5 mils. The length match must be used by matching techniques.

3.1.1.2 Skew Matching

The length of differential lanes must be matched within the TX and RX group. This applies only to specific protocols such as XAUI.

Differential pairs must be routed symmetrically in-to and out of structures, as shown in Figure 3-2.

The following figure shows the skew matching.

Figure 3-1. Skew Matching

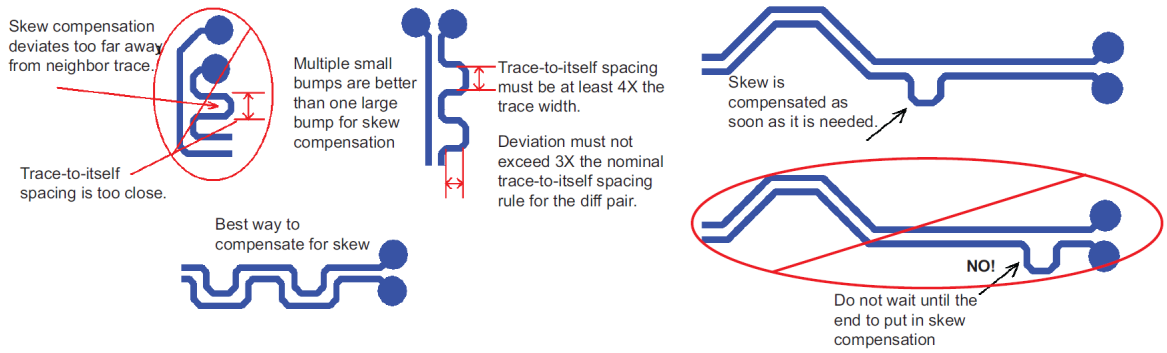


Figure 3-2. Example of Asymmetric and Symmetric Differential Pairs Structure

Skin effect dominates as the speed increases. To reduce the skin effect, the width of the trace must be increased (loosely coupled differential traces). Increase in trace width causes increase in dielectric losses. To minimize dielectric loss, use low dissipation factor (DF) PCB materials such as
Nelco 4000-13EP SI. Cost is significantly higher than FR4 PCB material, but FR4 PCB material cannot provide increased eye-opening when longer trace interconnections are required. Ensure that a 85 - 100Ω differential impedance is maintained. This is an important guideline to be followed if the data rate is 5 Gbps or higher.

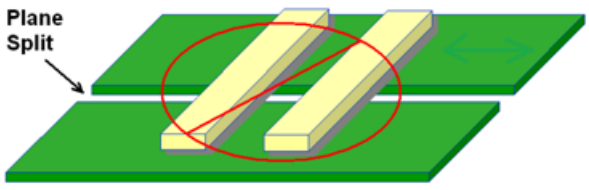
Far end crosstalk is eliminated by using stripline routing. However, this type of routing in stripline causes more dielectric loss. In order to minimize dielectric loss, it is better to route as a microstrip if there is enough space between differential pairs (>4 times the width of the conductor). Simulations are recommended to see the best possible routing.

Instruct the fabrication vendor to use these PCB materials before manufacturing.

Transceiver traces must be kept away from the aggressive nets or clock traces. For example, on RTPF500 devices, the transceiver and DDR traces must not be adjacent to each other. Trace stubs must be avoided.

It is recommended to use low roughness, that is, smooth copper. As the speed increases, insertion loss due to the copper roughness increases. The attenuation due to skin effect is increased proportional to the square root of frequency. Microchip recommends instructing the PCB fabrication house to use smooth copper, if the frequency exceeds 2 Gbps.

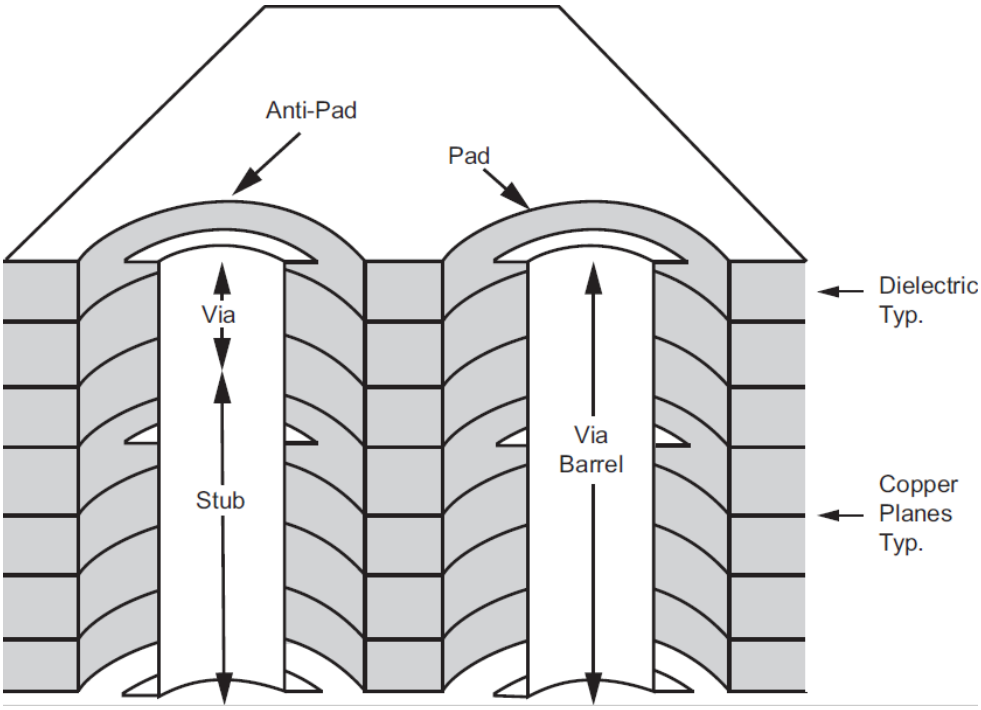
Split reference planes must be avoided. Ground planes must be used for reference for all transceiver lanes.



3.1.1.3 Via

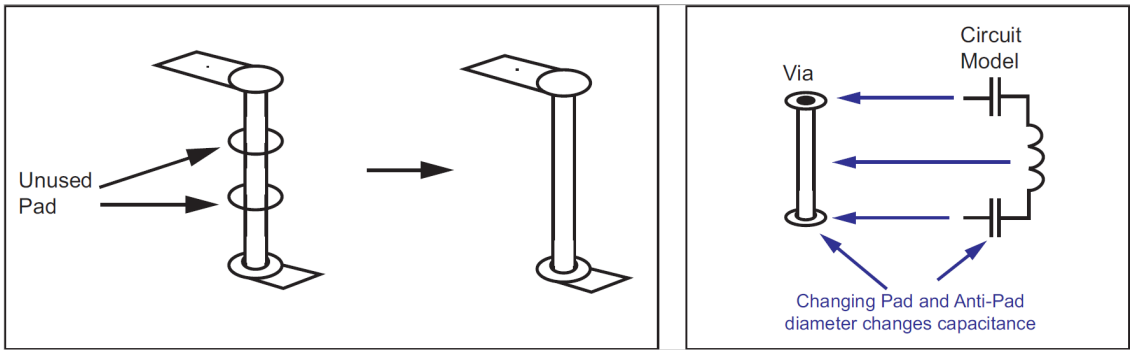
The target impedance of vias are designed by adjusting the pad clearance (anti-pad size). Field solver must be used to optimize the via according to the stack-up.

Figure 3-3. Via Illustration



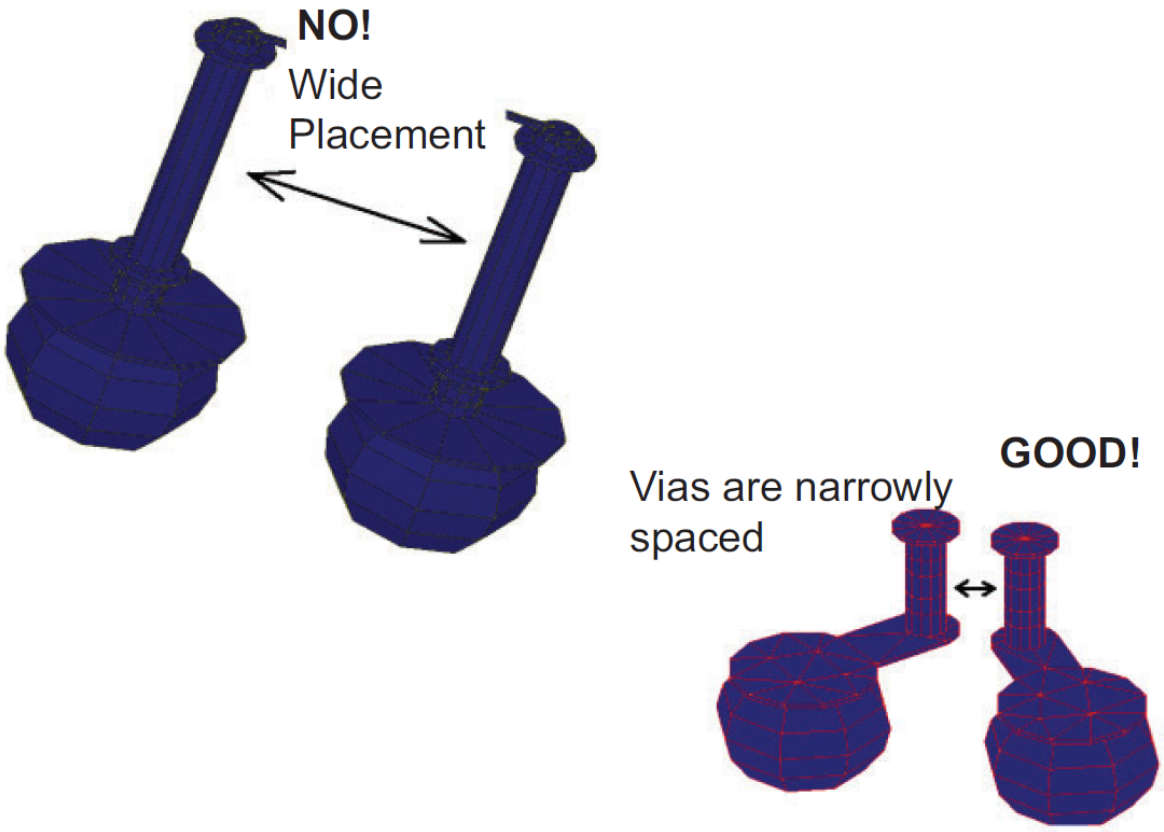
- Many vias on different traces must be avoided, or minimized as much as possible.
- The length of via stubs must be minimized by back-drilling the vias, routing signals from the near-top to the near-bottom layer, or using blind or buried vias. Using blind-vias and back drilling are good methods to eliminate via stubs and reduce reflections.
- If feasible, non-functional pads must be removed. Non-functional pads on-via are the pads where no trace is connected. This reduces the via capacitance and stub effect of pads.

Figure 3-4. Non-Functional Pads of Via



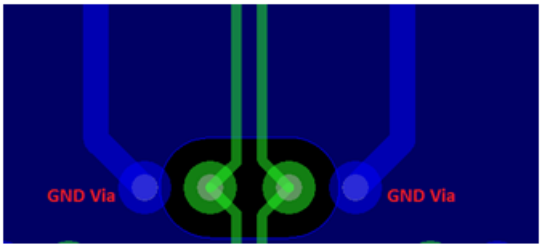
Using tight via-to-via pitches helps reducing the effect of crosstalk, as shown in the following figure.

Figure 3-5. Via-to-Via Pitch



Symmetrical ground vias (return vias) must be used to reduce discontinuity for Common mode signal components, as shown in the following figure. Common mode of part of the signal requires continuous return path for TX and RX to GND. Return vias help maintain the continuity.

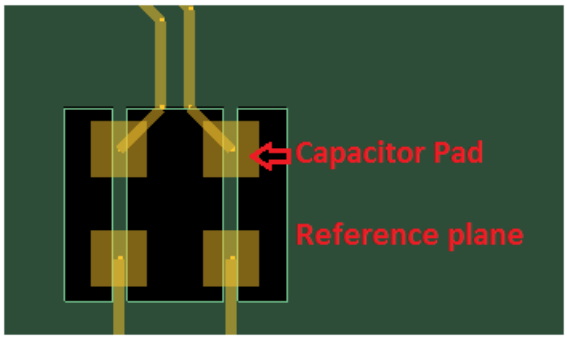
Figure 3-6. GND Via or Return Via



3.1.2 DC Blocking Capacitors

The plane underneath the pads of DC blocking capacitors should be removed, as shown in the following figure, to match the impedance of the pad to 50Ω.

Figure 3-7. Capacitor Pad Reference Plane



4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

Table 4-1. Revision History

Revision	Date	Description
A	12/2021	The first publication of this document.

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