AN4228

RT PolarFire® Lockstep Processor Application Note

Introduction

Embedded systems for aerospace applications are more susceptible to transient faults due to radiation, EMI, voltage fluctuations, and power supply failure. Transient faults are becoming a concern at the ground level due to low core voltage, decrease in transistor geometry, and increase in switching speeds. Transient faults are real at the ground level in nuclear, automotive, and communication equipment.

To mitigate the transient and intermittent faults, lockstep systems—which are fault-tolerant computer systems—run the same set of operations on two identical systems with a known delay between them. This application note demonstrates dual-core lockstep processor architecture using soft Mi-V processor, which uses redundancy to detect the transient faults. An error is introduced by interrupting a processor and a system Reset is asserted as a response to the lockstep error detection.

Dual-Core Lockstep Processor Architecture

The dual-core lockstep processor architecture provides real-time diagnostics using an additional processor and a comparator. Two identical processors run the same application in lockstep with a known time delay between them. Any differences between two processors outputs are flagged as an error by the comparator on cycle-by-cycle basis. A temporal delay of 0.5 to 2 clock cycles between processors is appropriate to detect most of the common errors.

Design Requirements

The following table lists the hardware and software requirements for this demo design.

Table 1. Design Requirements

Requirement	Description
Hardware	
RT PolarFire Evaluation Kit (RTPF500-CG1502) • 12V, 5A AC power supply adapter and cords • USB A to Mini-B cable	To be released
Software	
Libero® SoC	Refer to the readme.txt file provided in the design files for the software versions used with this reference design.

Note: Libero SmartDesign and configuration screenshots provided in this guide are for illustration purpose only. Refer to the provided Libero design to see the latest updates.

Prerequisites

Before you begin:

1. Download and install Libero SoC from the following location: https://www.microsemi.com/product-directory/design-resources/1750-libero-soc#downloads
2. For demo design files download: soc.microsemi.com/download/rsc/?f=rtpf_lockstep_df

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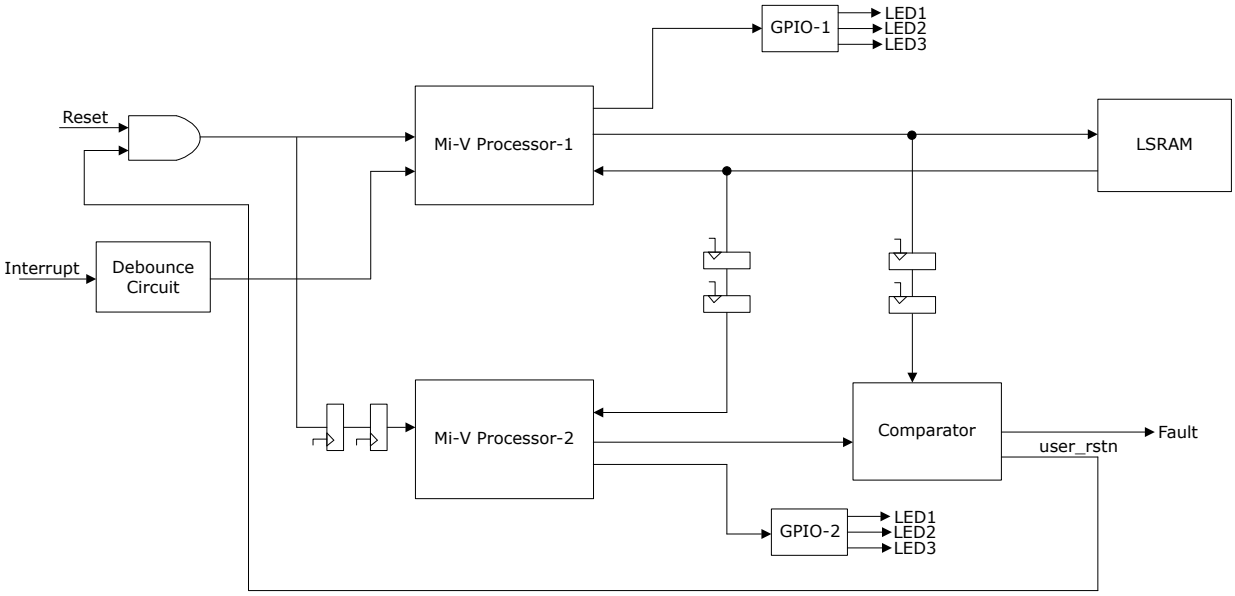
1. Design Description

The following figure shows high-level block diagram of the dual core lockstep design. The design has two Mi-V processor cores, LSRAM, comparator logic, GPIO IPs, and Debounce logic. Mi-V Processor-1 (Manager) is responsible for all the read or write transactions from or to the system memory (LSRAM) while Mi-V Processor-2 (Subordinate) executes the instructions fetched by Mi-V Processor-1.

A temporal delay of two clock cycles is introduced by releasing the Mi-V Processor-2 Reset two cycles after the Mi-V Processor-1 Reset. The processors execution is temporally separated to detect the faults which causes the same error on both the processors. Comparator logic is used to compare the read and write transactions from the two processors, and asserts a fault if there is a transaction mismatch. This fault bit is connected to the on-board LED. A sample GPIO application which blinks user LEDs on the board is used for testing the lockstep execution.

An external input with a Debounce logic is used to generate an interrupt to Mi-V Processor-1 for introducing a fault condition. As a fault recovery mechanism, a system Reset is applied after 30 seconds of detecting the fault. This 30 seconds timer is only used to visually see the fault LED glow before the system Reset is applied.

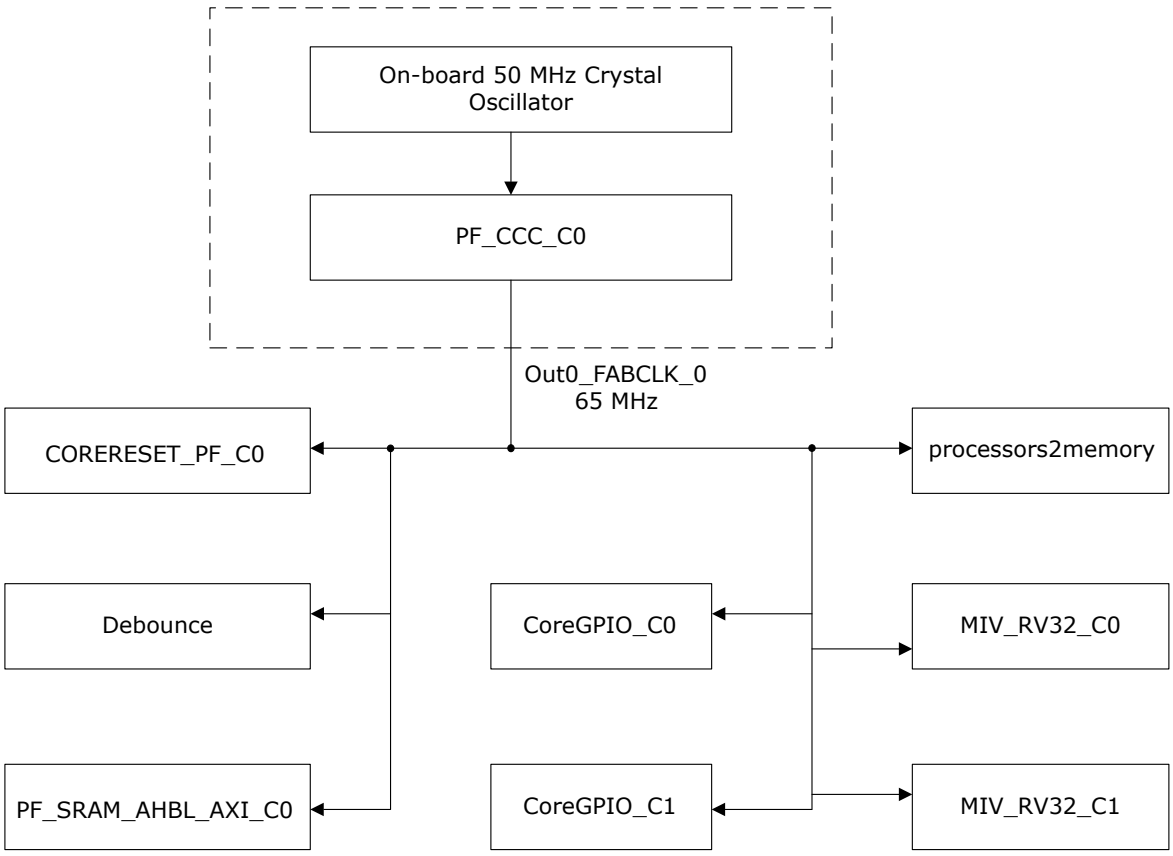
Figure 1-1. Lockstep Design High-level Block Diagram



1.1 Clocking Structure

In the design, there is a single clock domain. The on-board 50 MHz crystal oscillator is connected to the PF_CCC block, which generates 65 MHz system clock that is given to all the design blocks, as shown in following figure.

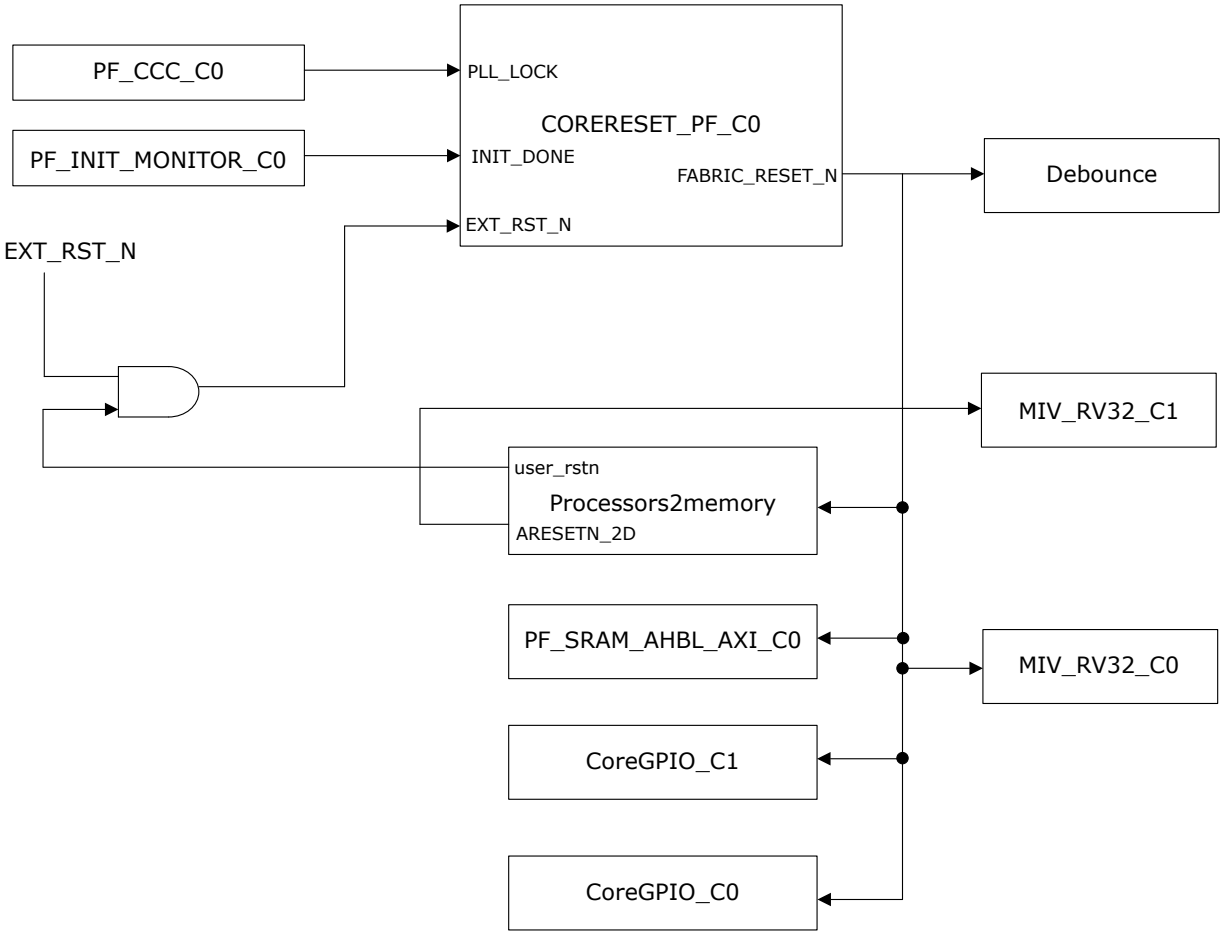
Figure 1-2. Clocking Structure



1.2 Reset Structure

In this design, the CORERESET_PF module generates the Reset signal as shown in the following figure. Reset signal to the MIV_RV32_C1 module is connected through ARESETN_2D port of the processors2memory module. This ensures MIV_RV32_C1 comes out of Reset state two clock cycles after MIV_RV32_C0. The user_rstn signal from the processors2memory module is ANDed with external Reset signal (EXT_RST_N) and the output is connected as an input to the CORERRESET_PF module. This is done to trigger user_rstn 30 seconds after an error is detected, which in-turn triggers a system Reset via the CORERESET_PF_C0. The following figure shows the Reset structure used in the design.

Figure 1-3. Reset Structure



1.3 Design Implementation

The following table lists the IP cores used in the reference design.

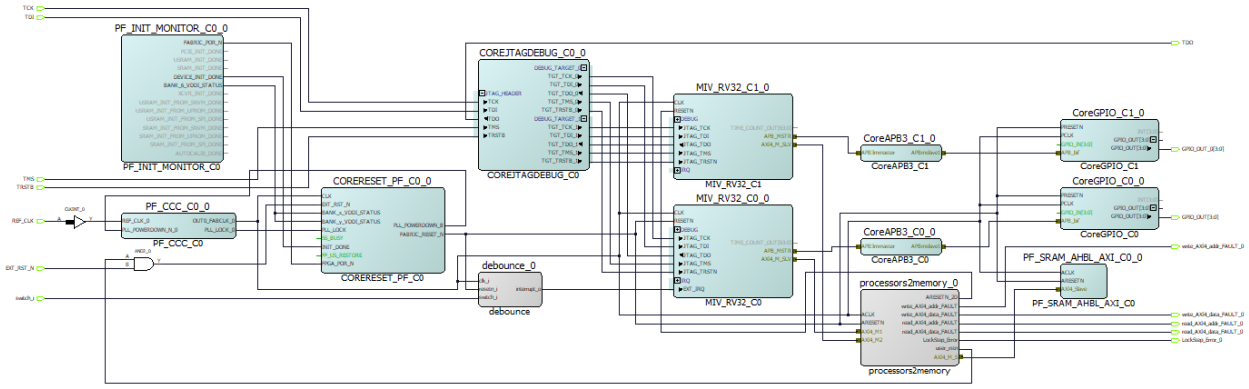
Table 1-1. IP Cores and Description

IP Core	Description
MIV_RV32	Mi-V soft processor
CoreJTAGDEBUG	Facilitates the connection of JTAG compatible soft core processors to the JTAG header for debugging. It provides fabric access to the JTAG interface using the UJTAG macro.
PF_INIT_Monitor	System controller uses this macro to check the status of device initialization. The device initialization includes SRAM initialization from µPROM/sNVM/SPI Flash. The DEVICE_INIT_DONE signal is used as a Reset.
PF_SRAM_AHBL_AXI	PolarFire LSRAM. Used as a system memory for the Mi-V processor.
PF_CCC	Macro to access PolarFire CCC block. It is used to synthesize 65 MHz clock frequency from the CCC with an on-board 50 MHz reference clock.
COREReset_PF	Generates a Reset, which is asserted asynchronously by one of the multiple potential sources and which negates synchronously to a specified clock.
CoreGPIO	Core GPIO provides an APB register-based interface with 32 GPIOs. It is used to check whether the application runs as expected.
CoreAPB3	Provides APB fabric for interconnecting an APB master and up to 16 APB slaves.

Configure two MIV_RV32 processors with Reset vector address (RSA) set to 0x8000_0000. In the Mi-V processors memory map, the 0x8000_0000 to 0x8001_FFFF range is defined for the AXI master interface, and the 0x6000_0000 to 0x6FFF_FFFF range is defined for the APB master interface. MIV-RV32_C0 processor accesses PF_SRAM_AHBL_AXI_C0 (processor main memory, where the application code (hex file) is stored) by sending transactions between addresses 0x8000_0000 to 0x8001_FFFF.

The following figure shows the SmartDesign view of the dual core lockstep design.

Figure 1-4. Smart Design Dual Core Lockstep Design



The processors2memory RTL module directs the MIV-RV32_C0 processor's read and write transactions to the PF_SRAM_AHBL_AXI and delays the read data transactions from the PF_SRAM_AHBL_AXI memory to MIV-RV32_C1 processor by two clock cycles. It also delays the read address, write address, and write data transactions from the MIV-RV32_C0 processor by two clock cycles to compare with MIV-RV32-C1 processor's read address, write address, and write data transactions. This RTL module also has comparison logic to compare the transactions from two processors on cycle-by-cycle basis and flags an error on Lockstep_Error output if there is a transaction mismatch. Lockstep_Error output gets asserted if there is a any mismatch on AXI address, AXI data, or AXI sideband/control signals. This Lockstep_Error output is mapped to an on-board LED.

MIV-RV32 processor's AXI master interface connects to processors2memory module's AXI slave interface while processors2memory module's AXI master interface connects to PF_SRAM_AHBL_AXI module's slave interface.

The APB interface of CoreGPIO IPs is connected to the master APB interface of MIV_RV32 processors through CoreAPB3. CoreGPIO is configured to have 32-bits APB width and four output ports. These output ports are mapped to the debug LEDs on the board to verify whether the application code works as expected.

An I/O pad with Debounce logic is used to introduce an error in the dual core lockstep design by asserting an interrupt (EXT_IRQ) to the MIV-RV32_C0 core. MIV-RV32_C0 core switches the execution to interrupt service routine (ISR) while MIV-RV32_C1 core continues executing its normal transactions. This leads to transactions mismatch and an error is detected.

As a fault recovery mechanism, system Reset is applied to the design after 30 seconds of detecting the fault. Here, the 30 seconds delay is used to prolong the LED glowing when the fault is detected. This is done through user RTL logic where user_rstn output from processors2memory module is ANDed with external Reset (EXT_RST_N).

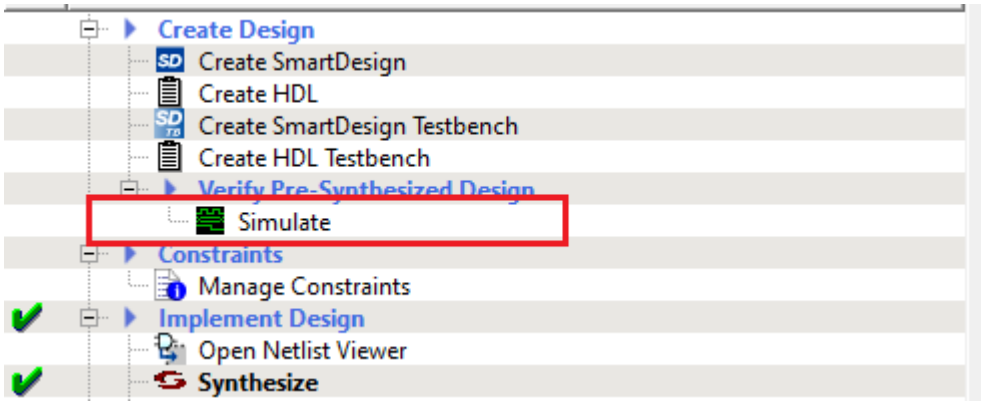
2. Dual Core Lockstep Simulation

There is a HDL testbench for running the simulation for the dual core lockstep design. Clock generator block generates 50 Mhz clock. Reset generator generates active-low Reset for the design and is asserted for initial 1000 ns of running simulation.

To run the simulation, go to **Stimulus Hierarchy** and verify if the `Lock_step_processor_tb` file is set as active stimulus. If not set, right-click on the file and select **Set as active stimulus**.

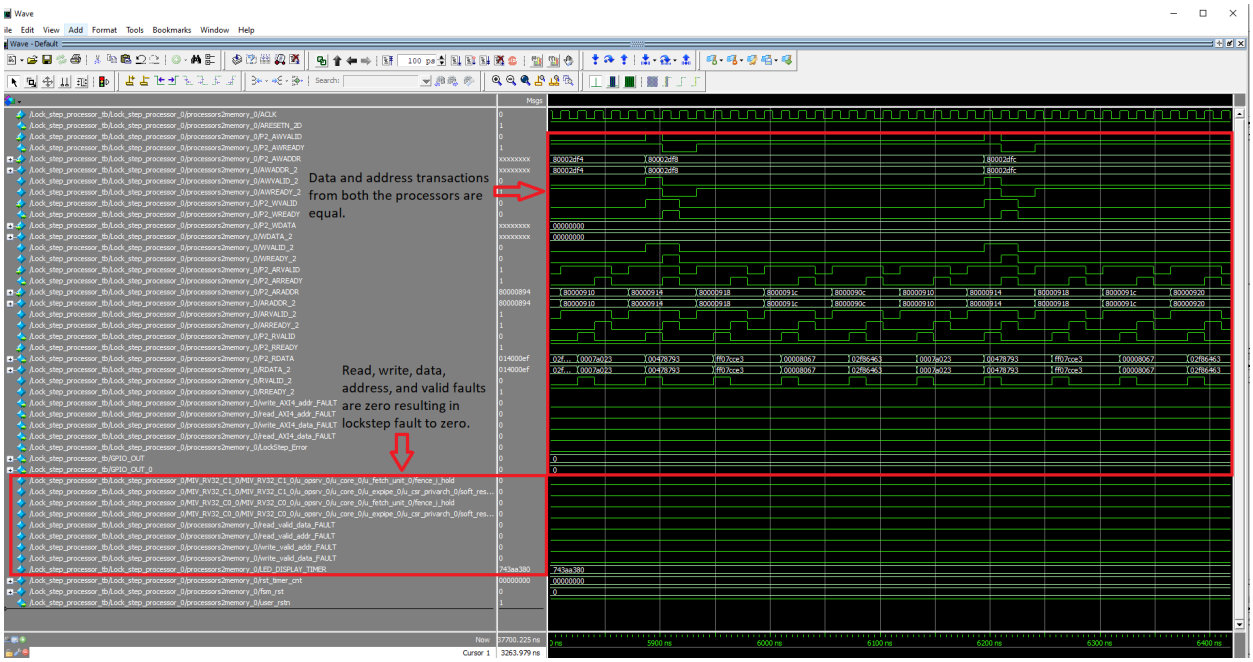
In the **Design Flow** tab, double-click **Simulate** under **Verify Pre-Synthesized Design** to simulate the design as shown in the following figure.

Figure 2-1. Run Simulation



The following figure shows the simulation waveform for the dual core lockstep design highlighting the data and address transactions from both the processors. The address, data, and control signals coming out from the two processors are matching and their corresponding faults are zero until the error is introduced as also highlighted. The design is kept in the Reset state for initial 1000 ns.

Figure 2-2. Dual Core Lockstep Simulation



3. Running the Demo

This chapter describe the steps to program the RT PolarFire device with the dual core lockstep design and detailed procedure to inject faults in the design through the SmartDebug tool.

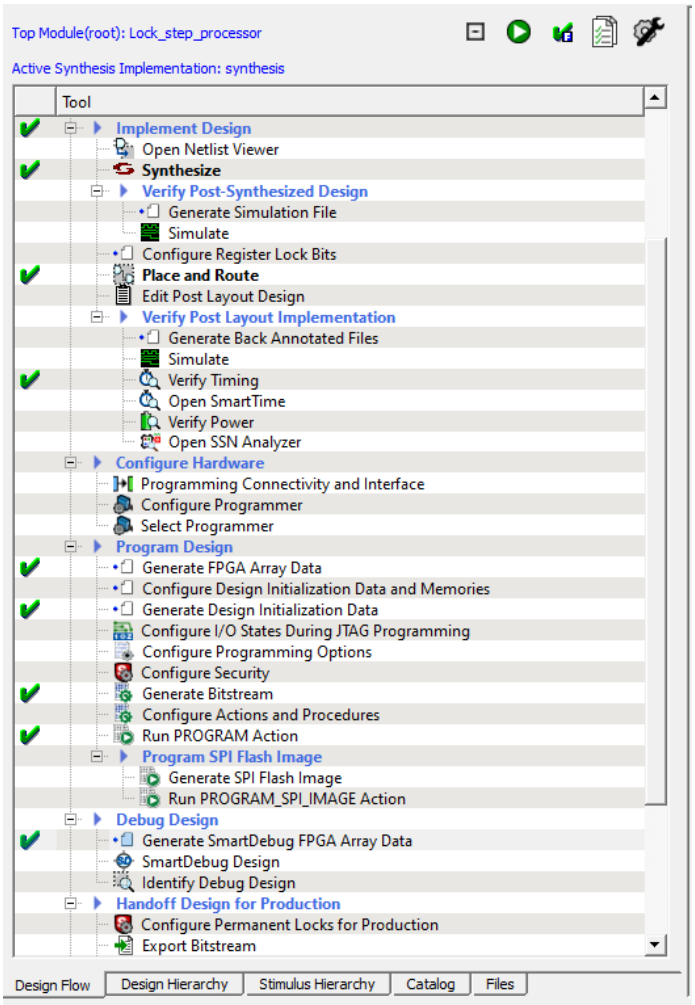
Before programming the RT PolarFire device, check the following:

- Ensure the jumper settings on the board is same as the default jumper settings specified in *RT PolarFire Evaluation Kit User Guide*.
- Connect the host PC to the J24 connector using the USB cable.
- Connect the power supply to the J19 connector and switch ON the power supply switch, SW7.

3.1 Programming the Device using Libero SoC

The RT PolarFire device can be programmed using the provided Libero SoC project. The following figure shows the Libero design flow.

Figure 3-1. Libero Design Flow Program Action

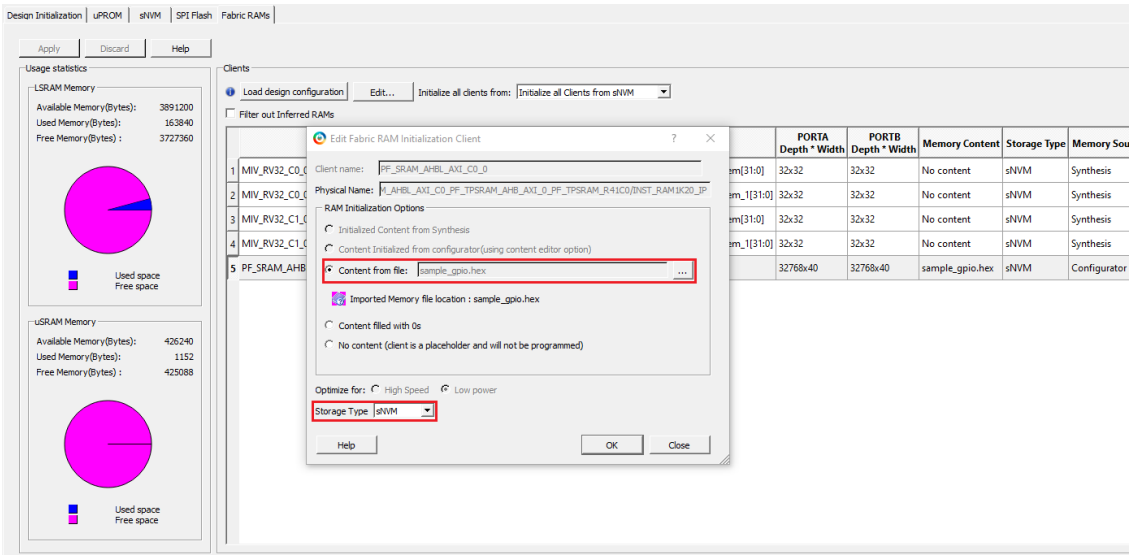


To program the device, follow these steps:

1. Open the design in Libero SoC. The Libero **Design Flow** window appears.
2. Double-click **Configure Design Initialization Data and Memories** on the **Design Flow** tab.

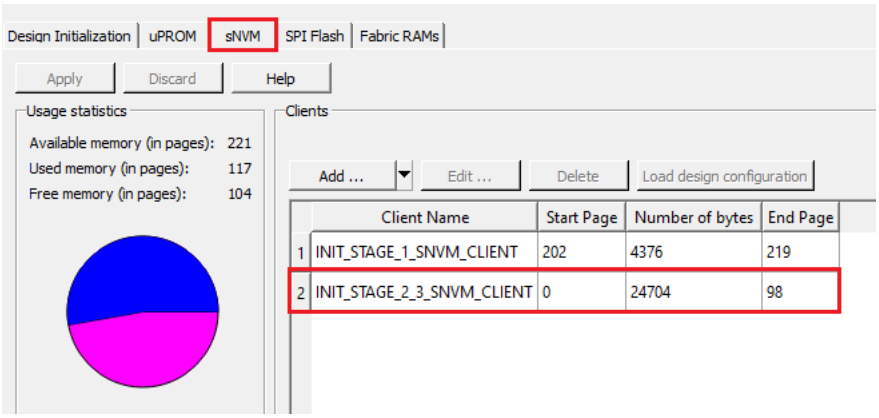
3. In the **Fabric RAMs** tab, double-click on **PF_SRAM_AHBL_AXI_C0_0** from the list of logical instances and click **Edit.**
4. In the **Edit Fabric RAM Initialization Client** window, ensure that the storage type is selected as sNVM and in the **Import Memory file location** dialog box, `sample_gpio.hex` is properly located as shown in the following figure. The system controller initializes the RAM instance with the sNVM client's content at power-up.

Figure 3-2. Edit Fabric RAM Initialization Client



5. In the **sNVM** tab, ensure that the sNVM client is added as shown in the following figure.

Figure 3-3. sNVM Tab



6. Double-click **Run PROGRAM Action.** Once the device is successfully programmed, a green tick appears on **Run PROGRAM Action**.

Note: To program the device using FlashPro Express, see 4. Appendix: Programming the Device using FlashPro Express.

3.2 Running the Design

Once the device is programmed, LED2, LED3, LED6, and LED7 continuously toggle which ensures that the MIV-RV32_C0 and MIV-RV32_C1 are in lockstep. To inject fault, follow these steps:

1. Press external push button, SW1.
2. LED8 on the board glows to show the lockstep error is introduced.
3. System Reset must be asserted after 30 seconds of detecting the fault. When the system Reset is released, application code restarts and lockstep error is zero. LED1, LED5, and LED8 stops glowing.

Note: LED1 glows as the interrupt service routine (ISR) is called after the external IRQ is triggered for MIV-RV32_C0. The same set of instructions to execute the ISR for MIV-RV32_C0 reaches MIV-RV32_C1 (via the read bus) which glows LED5.
When interrupt is asserted, there is a difference in MIV-RV32_C0 and MIV-RV32_C1 output ports for few clock cycles, which asserts the lockstep error, but the MIV-RV32_C1 might sync-up with MIV-RV32_C0 as the valid instructions are delivered to MIV-RV32_C1 as well. Hence, LED2, LED3, LED6, and LED7 continue to toggle. Ideally, there should be a system Reset or corrective action immediately after the lockstep error.

This concludes the demo.

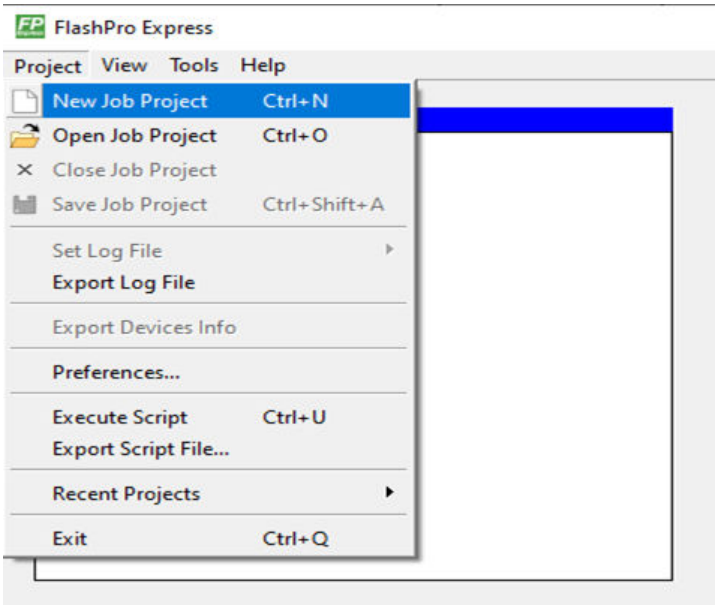
4. Appendix: Programming the Device using FlashPro Express

This section describes how to program the RT PolarFire device with the `.job` programming file using FlashPro Express. The `.job` file is available at the following design files folder location: <download_folder>\Programming_Job

To program the device, complete the following steps:

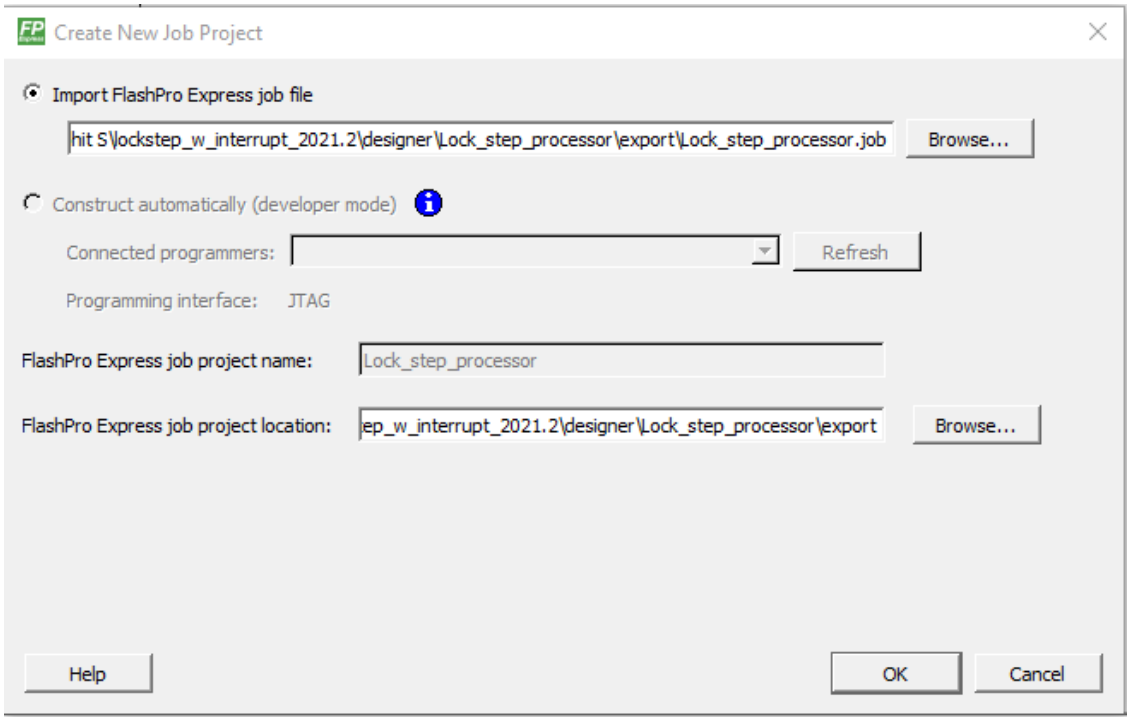
1. On the host PC, launch the **FlashPro Express** software.
2. Click **New** or select **New Job Project** from **Project** menu to create a new job project, as shown in the following figure.

Figure 4-1. New Job Project - FlashPro Express



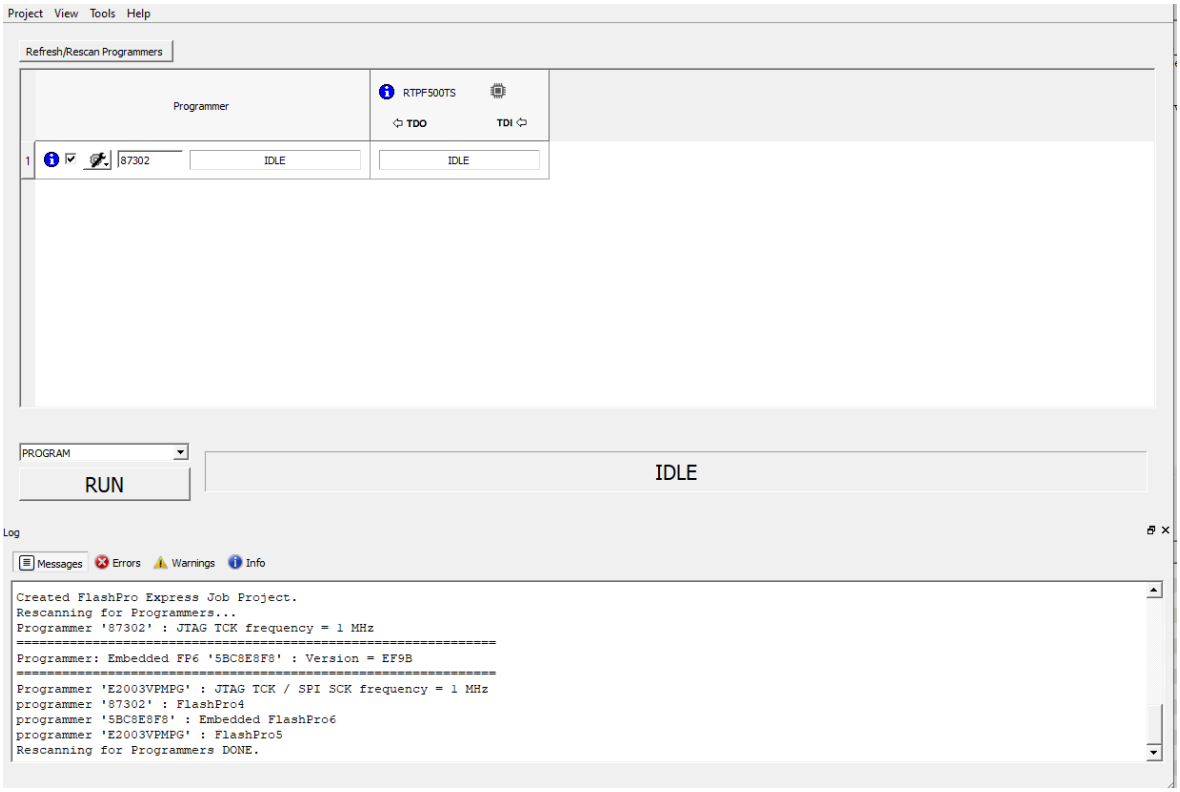
3. Enter the following in the **Create New Job Project** dialog box:
   - **Programming job file**: Click **Browse** and navigate to the location where the `.job` file is located and select the file. The default location is: <download_folder>\Programming_Job
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 4-2. Create New Job Project



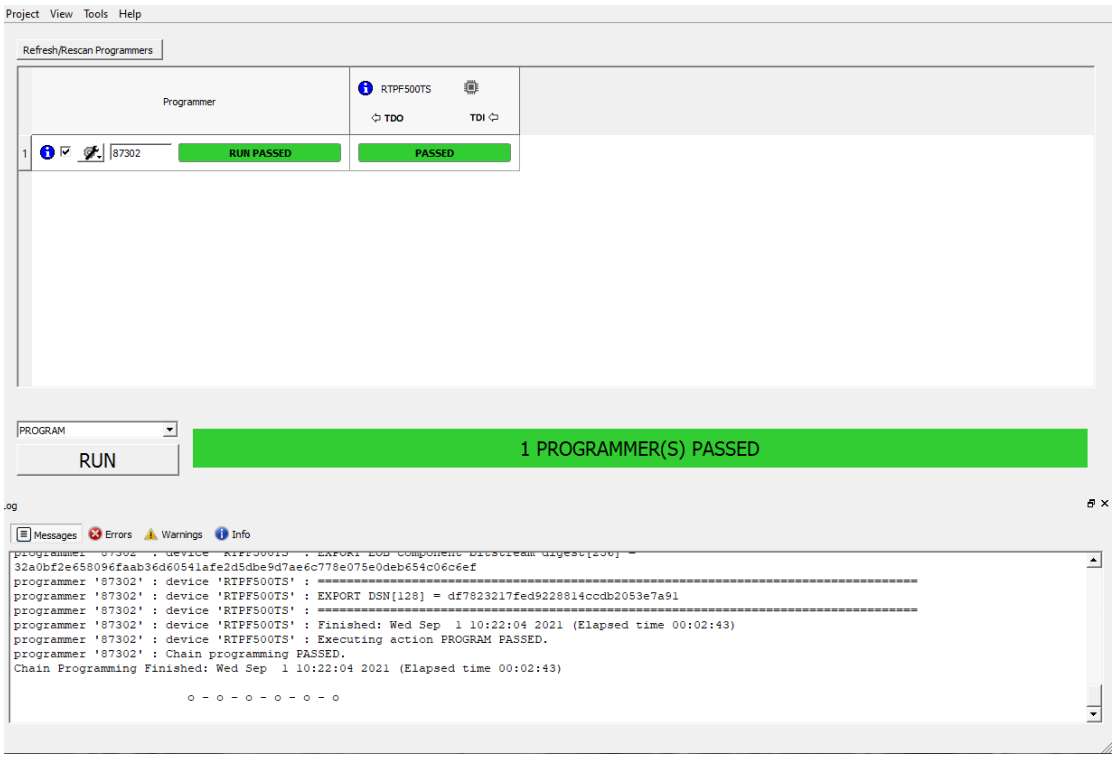
4. Click **OK**. The required programming file is selected and ready to be programmed in the device.
5. The **FlashPro Express** window appears as shown in the following figure. Confirm that a programmer number appears in the Programmer field. If it does not, confirm the board connections and click **Refresh/Rescan Programmers**.

Figure 4-3. Refresh/Rescan Programmers



6. Click **RUN** to program the device. When the device is programmed successfully, a **PROGRAMMER(S) PASSED** status is displayed as shown in the following figure.

Figure 4-4. Programming Successful



7. Close **FlashPro Express, Project** > **Exit**.

See 3. Running the Demo section to run the demo.

5. Appendix: Running the TCL Script

TCL scripts are provided in the design files folder under the directory **TCL_Scripts**. If required, the design flow can be reproduced from Design Implementation before the job file is generated.

To run TCL, follow these steps:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click **Browse** and select **script.tcl** from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of the TCL script, the Libero project is created within the **TCL_Scripts** directory.

For more information about TCL scripts, see **<design_name>/TCL_Scripts/readme.txt.**

See *Libero® SoC TCL Command Reference Guide* for more information about TCL commands. Contact Technical Support for any queries about running the TCL script.

6. Revision History

The revision history table describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	10/2021	The first publication of the document.

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