

Migrating RTG4 Designs from Plastic FC/FCG1657 Package to Ceramic CG/LG1657 Package

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1. Introduction

Microchip's RTG4 Sub-QML FPGA has been qualified to JEDEC standards in a flip-chip (FC/FCG) 1657 ball grid array plastic package, with 1.0 mm ball pitch. It is pin compatible with our QML Class V-qualified RTG4 FPGAs in ceramic packages CG/LG1657, making it easy for developers to migrate their designs between New Space and more rigorous Class-1 missions. This document describes the flow to migrate RTG4 designs between the plastic and ceramic package options.

Table 1-1. RTG4 Product Table

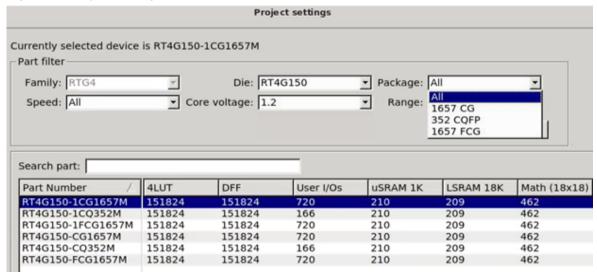
Resources	RT4G150			
	CG1657/LG1657	FCG1657/FC1657		
Logic Elements (TMR Register + 4-Input C Logic)	151,824	151,824		
18x18 Multiply-Accumulate Blocks	462	462		
RAM Mbits (1.5 Kbit and 24 Kbit Blocks, with ECC)	5.2	5.2		
UPROM Kbits	381	381		
DDR2/3 SDRAM Controller (with ECC)	2 × 32	2 × 32		
PCI Express Endpoints	2	2		
Globals	24	24		
PLLs (Rad Tolerant)	8	8		
SpaceWire Clock and Data Recovery Circuits	16	16		
User IO (excluding SERDES)	720	720		
SERDES lanes (3.125 Gbps)	24	24		
Packages				
CG1657 (Ceramic Column Grid Array, Six Sigma Columns)	QML-V Qualified	_		
LG1657 (Ceramic Land Grid Array, No Solder Termination)				
CB1657 (Ceramic Ball Grid Array, For Prototyping Only)				
FCG1657 (Ball Grid Array Plastic Package, Lead-free)	_	JEDEC Qualified		
FC1657 (Ball Grid Array Plastic Package, Leaded)				
Package Body Size	42.5 mm × 42.5 mm	42.5 mm × 42.5 mm		

2. Design Migration Flow

In Libero SoC software's project setting, changing between "1657 CG" (ceramic package) and "1657 FCG" (plastic package) options will invalidate the Synthesize and Compile steps in the existing design. This design migration flow is intended to help users migrate between RTG4 designs using FC/FCG1657 and CG/LG1657 packages.

- 1. Save a backup copy of the Libero project for the RTG4 design targeting FC/FCG1657 package.
- 2. Open the Libero project and make sure that the "Place and Route" design flow state is complete.
- 3. Invoke "Project Settings" from the "Project" menu and go to "Device selection".
- 4. Select the appropriate part number for the new design using "1657 CG" package option and Save.

Figure 2-1. Project Settings



- 5. Note that all the design flow states including "Synthesize" or "Compile Netlist" will be invalidated.
- 6. Right-click on "Place and Route" and choose "Configure Options". Select "Incremental Layout" to use previous placement data as the initial placement for the next run.
- 7. Complete the design flow.

3. Revision History

Revision	Date	Description
Α	09/2021	Initial Revision

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