UG0933
User Guide
RT PolarFire FPGA Packaging and Pin Descriptions

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

The first publication of this document.

2 RT PolarFire FPGA Packaging and Pin Descriptions

This guide provides pin and packaging information (such as bank assignments and mechanical information) for RT PolarFire® FPGAs.

RT PolarFire FPGAs feature a flexible I/O structure that supports a range of mixed voltages through bank selection. The HSIO and GPIO are configured as differential I/Os or two single-ended I/Os. For more information about HSIO, GPIO, and supported I/O standards, refer to *UG0931: RT PolarFire FPGA User I/O User Guide*.

2.1 Packaging Overview

RT PolarFire FPGAs are available in three variations of a hermetically sealed ceramic land grid array with 1509 contacts. For flight and engineering development applications, FPGAs are available with gold-plated land pads (LG1509) or with solder columns (CG1509). For engineering development applications only, FPGAs are available with solder balls (CB1509). Each package (device variant) has various I/O banks to allow the flexibility of using different I/O standards. This document refers to the CG1509 package designator. The information presented is also applicable to the LG1509 (ceramic land grid array with no solder termination) and the CB1509 (ceramic ball grid array with solder ball termination, for prototyping purposes).

The following table lists the RT PolarFire FPGA variant, with user I/O and XCVR lanes.

Table 1 • **RT PolarFire FPGA Product Family**

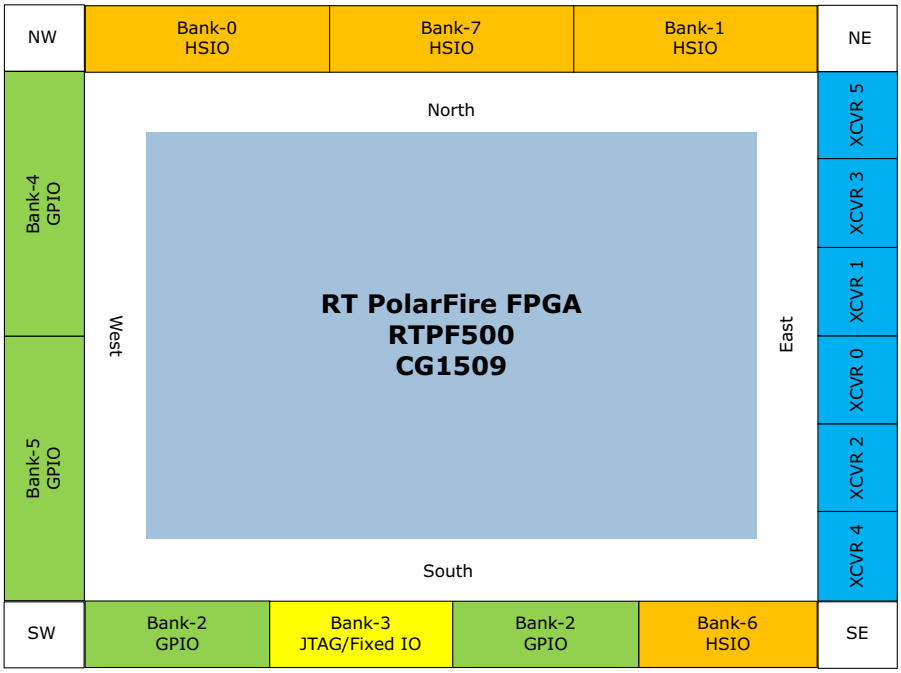
Features		RTPF500T
FPGA Fabric	Logic Elements (4 LUT + DFF)	481
	Math Blocks (18 × 18 MACC)	1480
	LSRAM Blocks (20 kbit)	1520
	µSRAM Blocks (64 × 12)	4440
	Total RAM (Mbits)	33
	µPROM (Kbits 9-bit bus)	513
	User DLLs/PLLs	8
High-Speed I/O	250 Mbps to 10.3125 Gbps Transceiver Lanes	24
	PCIe Gen2 End Points/Root Ports	2
Total I/Os	Total User I/Os	584
Packaging	Type/Size/Pitch	
	CG1509 (40 mm × 40 mm, 1.0 mm)	632(324/308)

2.2 Bank Locations

RT PolarFire FPGA I/O are grouped based on I/O voltage standards and I/O capabilities. Each I/O bank has dedicated I/O supplies and ground voltages. Because of these dedicated supplies, only I/O with compatible standards are assigned to the same I/O voltage bank.

The following illustrations show the bank locations for the RTPF500T device with available package combinations.

Figure 1 • **RT PolarFire RTPF500T-CG1509 I/O Bank Locations**



The following table lists the organization of the I/O banks in RT PolarFire FPGAs. Each XCVR supports four lanes in every package. In all the packages, PCIe is supported only in XCVR0.

Table 2 • **Organization of I/O Banks**

	CG1509
Bank Number	**RTPF500T**
Bank 0	HSIO
Bank 1	HSIO
Bank 2	GPIO
Bank 3	JTAG/FIXED I/O
Bank 4	GPIO
Bank 5	GPIO
Bank 6	HSIO
Bank 7	HSIO
XCVR 0	Included
XCVR 1	Included
XCVR 2	Included
XCVR 3	Included
XCVR 4	Included
XCVR 5	Included

Each I/O bank supports multiple DDR lanes. If CDR/SGMII interface is connected to the I/O bank, the Tx and Rx signal must be within the same DDR Lane. Only one CDR/SGMII is allowed per DDR lane.

For more information about DDR lanes for each package in Package Pin Assignment Table (PPAT), refer to *RT PolarFire FPGA Product Overview*.

The following table lists the XCVR channels for RT PolarFire device/package.

Table 3 • **Serial Transceiver Channels**

Device	CG1509
RTPF500T	24

2.3 Packaging Pin Assignment

The Package Pin Assignment Table, that is, PPAT information is available in the Packing section. For more information, refer to *RT PolarFire FPGAs Documentation web page*. PPAT contains information about recommended DDR pin-outs, PCI Express capability for XCVR-0, DDR Lane information for IO CDR, and generic IOD interface pin placement.

2.4 Pin Descriptions

RT PolarFire device has user I/O (GPIO/HSIO) pins, dedicated I/O bank pins, memory interface, XCVR interface, clocking pins, and supply pins.

2.4.1 User I/O

RT PolarFire FPGA I/Os are paired up to meet the differential I/O standards and grouped into lanes of 12 buffers with a lane controller for memory interfaces. For more information about the memory controller, refer to *RT PolarFire FPGA DDR Memory Controller User Guide* (To be published).

There are two types of I/O buffers—HSIO and GPIO. HSIO is optimized for 1.2 Gbps (DDR4) operation with operating supplies between 1.1 V and 1.8 V. GPIO buffers support a wider range of I/O interfaces with speeds of up to 1066 Mbps when using single-ended standards and 1.25 Gbps when using differential standards. GPIO supports multiple standards with an integrated clock data recovery (CDR) to high-speed serial interfaces such as 1GbE.

Each RT PolarFire FPGA user I/O uses an IOxyBz naming convention, where:

- **IO** = the type of I/O.
- **x** = the I/O pair number in bank z.
- **y** = P (positive) or N (negative). In single-ended mode, the I/O pair operates as two separate I/O—P and N. Differential mode is implemented with a fixed I/O pair and cannot be split with an adjacent I/O.
- **B** = bank (refer note in Supported I/O Features, page 5).
- **z** = bank number.

GPIOxyBz and HSIOxyBz are bi-directional user I/O pins that are capable of differential signaling.

2.4.1.1 Supported I/O Features

The following table lists the I/O features supported on HSIO and GPIO.

Table 4 • **Supported I/O Features**

I/O Feature	HSIO	GPIO	Additional Information
Programmable on/off clamp		Yes	
Hot-plug		Yes	
Cold sparing	Yes[1]	Yes	
True differential output driver		Yes	
Programmable on/off 100 Ω differential termination		Yes	
PVT-compensated output drive	Yes	Yes	
Programmable slew control		Yes	
PVT compensated slew control	Yes		
Programmable input hysteresis	Yes	Yes	
Mobile industry processor interface (MIPI) (input)		Yes	High-speed and low-power.
MIPI (output)		Yes	High-speed.

1. HSIO is **pseudo-cold spare** that is, it requires the spare device to have its HSIO VDDI banks powered-up to prevent I/O leakage through the ESD diodes.

2.4.2 Supply Pins

The following table lists multiple power supply pins required for proper device operation. For more information about unused conditions and power sequence, refer to *RT PolarFire FPGA Board Design User Guide* (To be published).

Table 5 • **Supply Pins**

Name	Description	Operating Voltage
XCVR_VREF[1]	Voltage reference for transceiver.	0.9 V/1.25 V
VDD_XCVR_CLK	Provides common power to all transceiver reference clock buffers.	2.5 V/3.3 V
VDDA25	Transceiver PLL power	2.5 V
VDDA	Power for transceiver Tx and Rx lanes 0, 1, 2, 3.	1.0 V/1.05 V
VSS	Core digital ground.	
VDD	Device core digital supply.	1.0 V/1.05 V
VDDIx (JTAG Bank)	Supply for I/O circuits in a bank.	1.8 V/2.5 V/3.3 V
VDDIx (GPIO Banks)[2]	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V/2.5 V/ 3.3 V
VDDIx (HSIO Banks)	Supply for I/O circuits in a bank.	1.2 V/1.5 V/ 1.8 V
VDD25	Power for corner PLLs and PNVM.	2.5 V
VDD18	Power for programming and HSIO receiver. HSIO auxiliary power supply.	1.8 V
VDDAUXx[2]	Auxiliary supply for I/O circuits. Auxiliary supply voltage must be set to 2.5 V or 3.3 V and must be always equal to or higher than VDDIx of GPIO banks.	Greater than or equal to VDDI

1. SSTL25 (stub series terminated logic) I/O standard for 1.25 V VREF, SSTL18 I/O standard for 0.9 V, and HSUL18 I/O standard for 0.9 V.
2. Designers should be familiar with the latest Single Event Latch-Up radiation test data before choosing GPIO supply voltages.

2.4.2.1 Packaging Decoupling Capacitors

RT PolarFire 1.0 mm pitch package contains decoupling capacitors to support high-speed I/O operation.

The following table lists the packaging decoupling capacitors contained in the LG1509/CB1509/CG1509 packages.

Table 6 • **Packaging Decoupling Capacitors**

Power Supply	1 mm Pitch	
	Caps available	**Value**
VDDI0	3	0.18 µF (x3)
VDDI1	2	0.18 µF (x2)
VDDI2	3	0.18 µF (x3)
VDDI4	4	0.18 µF (x4)
VDDI5	4	0.18 µF (x4)
VDDI6	3	0.18 µF (x3)
VDDI7	3	0.18 µF (x3)
VDD	7	0.18 µF (x7)
VDD18	2	0.18 µF (x2)
VDDA	4	4.7 nF (x1) 2.2 nF (x2) 1.0 nF (x1)

2.4.3 Memory Interface

Valid locations for DDR memory interfaces are shown in Package Pin Assignment Table (PPAT), refer to *RT PolarFire FPGA Product Overview*.

By using the Libero® SoC RT PolarFire configurator, all individual DDR interface pins are identified from the macro. For more information about the memory interface, refer to *RT PolarFire FPGA DDR Memory Controller User Guide* (To be published).

The following table lists the reference receiver modes of I/O standards.

Table 7 • **Reference Receiver Modes**

I/O Standard	V_{DDIx}	V_{REF}	On-die Termination (ODT) (in Ω)	Bank Type	Application
SSTL18	1.8 V	0.9 V	40/50/60/80/120/240	GPIO, HSIO	RLDRAM2
SSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	DDR3
SSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	DDR3L
HSTL15	1.5 V	0.75 V	40/50/60/80/120/240	GPIO, HSIO	QDRII+
HSTL135	1.35 V	0.68 V	20/30/40/60/120	HSIO	RLDRAM3
HSUL12	1.2 V	0.6 V	60/120/40	HSIO	LPDDR3
HSTL12	1.2 V	0.6 V	60/120/240	HSIO	QDRII+
POD12	1.2 V	0.6 V	20/30/40/60/120	HSIO	DDR4

2.4.4 DDR Interface

The DDR subsystems are hardened ASIC blocks for interfacing the LPDDR3, DDR3, and DDR4 memories. It supports 16-, 32-, and 64-bit data bus width modes with ECC support. The DDRIO uses fixed impedance calibration for different drive strengths. These values are programmed using Libero SoC RT PolarFire software for the selected I/O standard. The values are fed to the pull-up or pull-down reference network to match the impedance with an external resistor. For more information about DDR signals, refer to *RT PolarFire FPGA DDR Memory Controller User Guide* (To be published).

2.4.5 Clocking Pins

CCC blocks, located at each corner of the RT PolarFire FPGAs, contain two PLLs and two DLLs that provide flexible on-chip and off-chip clock management and synthesis capabilities. CCCs are labeled according to their locations in the core. For example, the CCC located in the northeast corner is labeled as CCC_NE. For more information about clocking pins, refer to *RT PolarFire FPGA Clocking Resources User Guide* (To be published). Preferred clock inputs (CLKIN) are located on three sides of the device, with eight preferred clock inputs on the west side, twelve on the north side, and either 12 or 16 inputs on the south side, depending on the package. The following table lists the clocking pin names and descriptions. For more information about CCC pin voltage, refer Table 5, page 6.

Table 8 • **Clocking Pins[1]**

Name	Description	When Unused
CCC_NW_PLL0_OUT[0:1]	Dedicated PLL output clock pins used to drive high-performance clocks in DDR3 and DDR4 applications located in the corners of RT PolarFire device to route the clocks to and from the PLLs and DLLs.	Do not connect (DNC)
CCC_NW_PLL1_OUT[0:1]		
CCC_NE_PLL0_OUT[0:1]		
CCC_NE_PLL1_OUT[0:1]		
CCC_SE_PLL0_OUT[0:1]		
CCC_SE_PLL1_OUT[0:1]		
CCC_SW_PLL0_OUT[0:1]		
CCC_SW_PLL1_OUT[0:1]		
CCC_SE_CLKIN_S_[8:15]	Preferred clock inputs that connect external clock signals to the CCCs and the global clock network through low-latency paths. It is recommended to use these preferred clock inputs for connecting external clocks to the clock inputs of PLLs, DLLs, and fabric logic.	DNC
CCC_SW_CLKIN_S_[0:3]		
CCC_SW_CLKIN_W_[0:3]		
CCC_NW_CLKIN_W_[4:7]		
CCC_NW_CLKIN_N_[0:3]		
CCC_NE_CLKIN_N_[8:11]		
CLKIN_S_[4:7]	Preferred clock inputs directly routed to internal global buffers through MUXes.	DNC
CLKIN_N_[4:7]		

1. Some of the preferred clock inputs have connections to feedback clock input of the PLL/DLL present in the CCC. It is required to choose a preferred clock input which has connection to the PLL reference clock input for clock frequency synthesis. Refer to *RT PolarFire FPGA Clocking Resources User Guide* (To be published) for preferred clock inputs connectivity to PLLs/DLLs and global clock network.

2.4.6 Dedicated I/O Bank Pins

JTAG, SPI, and DEVRST_N signals share the same bank 3 supply and are not directly available to the fabric. SPI I/O are, however, dynamically switched over to be used by the fabric whenever the RT PolarFire controller is not using them. Dedicated I/O bank supplies must be powered up above their operational threshold and enabled before the RT PolarFire controller negates the main power-on reset to the FPGA fabric. The following tables list the JTAG, SPI, and DEVRST_N pin names and descriptions. Libero configures unused user I/O as input buffer disabled, output buffer tri-stated with weak pull-up. For more information about unused conditions, refer to *RT PolarFire FPGA Board Design User Guide* (To be published).

The JTAG bank voltages can be set to operate at 1.8 V, 2.5 V, or 3.3 V. The following table lists the JTAG pins.

Table 9 • **JTAG Pins**

Pin Names	Direction	Weak Pull-Up/Unused Condition	Description
TMS	Input	Yes/DNC	JTAG test mode select.
TRSTB	Input	Yes[1]	JTAG test reset. Must be held low during device operation.
TDI	Input	Yes/DNC	JTAG test data in. In ATPG or test mode, when using a 4-bit tdi bus, this IO is used as tdi[0].
TCK	Input	No[2]	JTAG test clock
TDO	Output	No/DNC	JTAG test data out.

1. If FPGA is in System Controller Suspend Mode and TRSTB is unused, either an external 1 kΩ pull-down resistor should be connected to TRSTB to override the weak internal pull-up, or TRSTB should be driven low from the external source.
2. In unused condition, must be connected to VSS through 10 kΩ resistor.

Table 10 • **Device Reset Pins**

Name	Direction	Weak Pull-up	Description
DEVRST_N	Input	22 KΩ	Device reset (asserted low).

Table 11 • **SPI Interface Pins**

Name	Direction	Description
SCK	Bi-directional	SPI clock.
SS	Bi-directional	SPI slave select.
SDI	Input	SDI input for the shared SPI interface.
SDO	Output	SDO output for the shared SPI interface.
SPI_EN	Input	Pulled up or down through a resistor or driven dynamically from an external source to enable or tri-state the SPI I/O.
IO_CFG_INTF	Input	Pulled up or down through a resistor or driven dynamically from an external source to indicate whether the shared SPI interface is a master or a slave. Dedicated to the system controller. 0: SPI slave interface 1: SPI master interface

Table 12 • **Special Pins**

Name	Direction	Description	Unused Condition
NC	–	No connect pin. This pin indicates that it is not connected within the circuitry. NC pins can be driven by any voltage or can be left floating with no effect on the operation of the device.	–
DNC	–	Do not connect pin. DNC pins must not be connected to any signals on the PCB, and they must be left unconnected.	–
LPRB_A	Output	Specifies an internal signal for probing (oscilloscope-like feature). The two live probe I/O cells function as either of the following: – Live probe – User I/O (HSIO)	Libero-defined DNC.
LPRB_B	Output		Libero-defined DNC.
FF_EXIT_N	Input	RESERVED	–
Shield Signal	Output	Shield signal is required for each DDR data byte signal. It must be driven with maximum drive strength to improve the signal integrity.	Only when DDR controller is in use.

2.4.7 XCVR Interface

The transceiver I/O available in the RT PolarFire device is dedicated for high-speed serial communication protocols. Libero Defined DNC pins are pulled up internally when not used in the Libero design.

Table 13 • **XCVR Interface Pins**

Name	Direction	Description	Unused Condition
XCVR_xy_REFCLK_P XCVR_xy_REFCLK_N	Input	Differential serial reference clock xy - location x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	DNC.
XCVR_x_TXy_P XCVR_x_TXy_N	Output	Differential serial transmit pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC.
XCVR_x_RXy_P XCVR_x_RXy_N	Input	Differential serial receive pins. x - transceiver number (0, 1, 2, 3) y - lane number (0, 1, 2, 3)	Libero-defined DNC, refer to *UG0936: RT PolarFire FPGA Transceiver User Guide*.

2.5 Package Pin-outs

The following table lists packaging pin-outs of the RT PolarFire device. Detailed PPAT is available for download, and it contains revision history, device specification, power supplies, pin-outs, and BGA graphic. For more information about PPAT, refer to *RT PolarFire FPGAs Documentation web page*.

Table 14 • **Package Pin Outs**

	Package
Device	**CG1509**
RTPF500T	Yes

2.5.1 Pin Compatibility Between Devices

The following table lists the pin compatible packages of RT PolarFire device.

Table 15 • **Pin Compatible Packages**

Package	Devices
CG1509	RTPF500T
CB1509	
LG1509	

2.6 Mechanical Drawings

The following illustrations show the top, bottom, and side views and dimensions for the RT PolarFire FPGAs.

Figure 2 • **RTPF500T-CG1509 Package Top-View and Side-View**

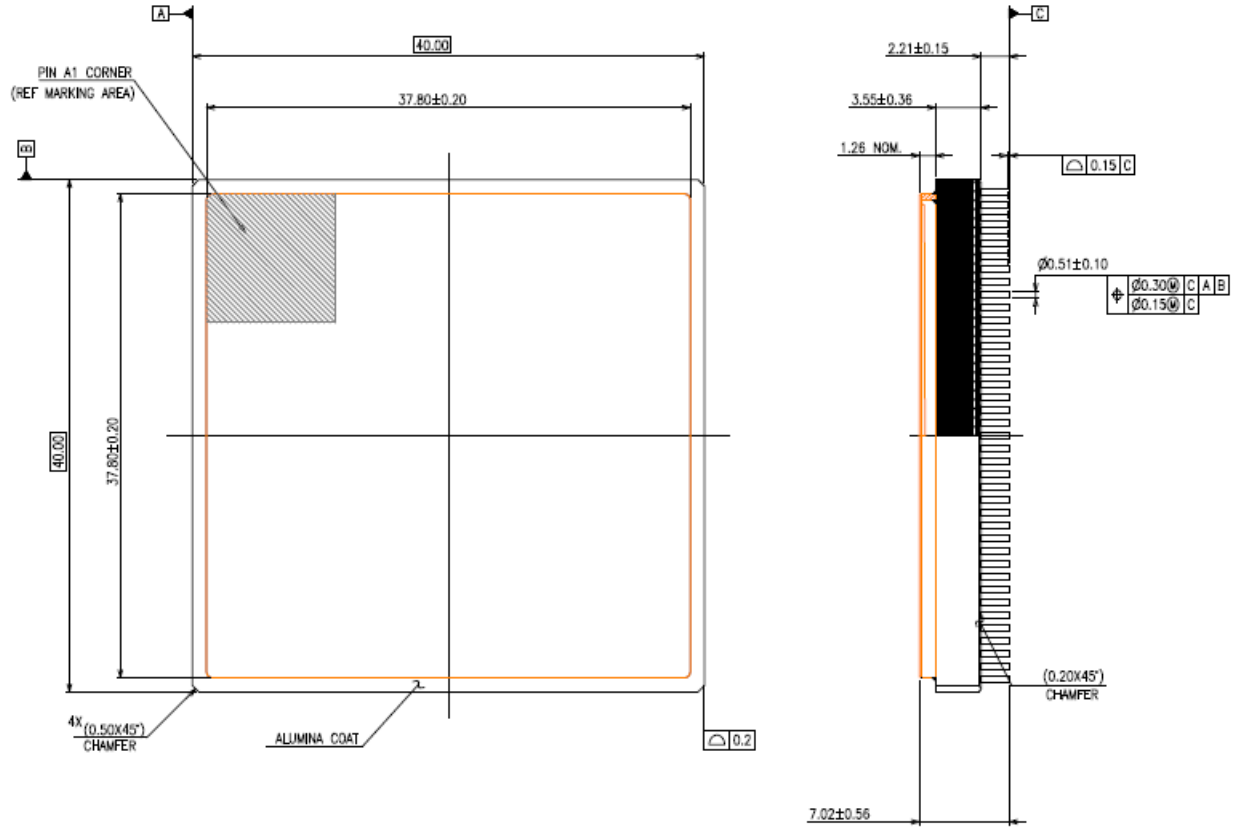
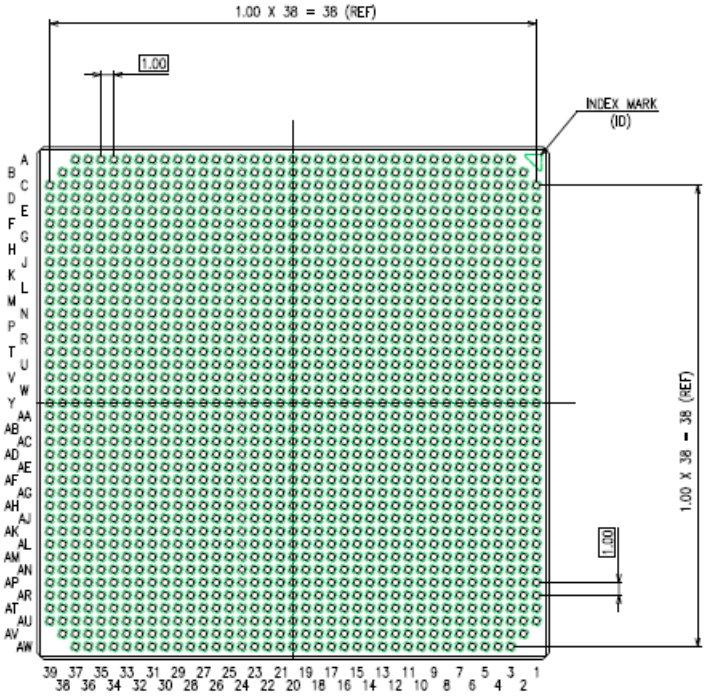


Figure 3 • **RTPF500T-CG1509 Package Bottom-View**



The following table lists the RT PolarFire FPGAs Package description and specification.

Table 16 • **RT PolarFire FPGAs Package Information**

		Package Specifications			
Package	**Description**	**Package type**	**Pitch (mm)**	**Size (mm)**	**Maximum I/Os**
CG1509	Flip-chip ceramic column grid array	Ceramic Column Grid Array (CCGA)	1	40 x 40	584 (HSIO 324 + GPIO 260)

2.7 Package Material Information

The following table lists the RT PolarFire ball grid array leaded packages.

Table 17 • **RT PolarFire Ball Grid Array Leaded Package**

Package	CB1509
Package Pitch	1 mm
Substrate Material	Alumina
Solder Ball Composition	Sn20/Pb80
Solder Bump Material	Sn98.2/Ag1.8

Table 18 • **RT PolarFire Column Grid Array Leaded Package**

Package	CG1509
Package Pitch	1 mm
Substrate Material	Alumina
Solder Column Composition	Sn20/Pb80 columns with copper spiral
Solder Bump Material	Sn98.2/Ag1.8

Table 19 • **RT PolarFire Land Grid Array Leaded Package**

Package	LG1509
Package Pitch	1 mm
Substrate Material	Alumina
Land Pad Composition	Gold Plated Land Pads
Solder Bump Material	Sn98.2/Ag1.8

2.8 Thermal Specifications

The following table lists the thermal resistances of the RT PolarFire FPGA package device.

Table 20 • **RT PolarFire Package Thermal Resistance**

Package	Environment	Theta-JA	Theta-JB	Theta-JC	Psi-JB	Psi-JT	Unit
RTPF500T-CG1509	Still Air	8.15 C/W	3.42 C/W	0.54 C/W	3.2 C/W	0.014 C/W	C/W
	1.0 m/s	5.81					
	2.5 m/s	4.98					

For more information about Thermal Management of RTG4 FPGAs in Space Applications, refer to *AC486: Thermal Management of RTG4 FPGAs in Space Applications*.

2.9 Package Mass

The following table lists the package mass information.

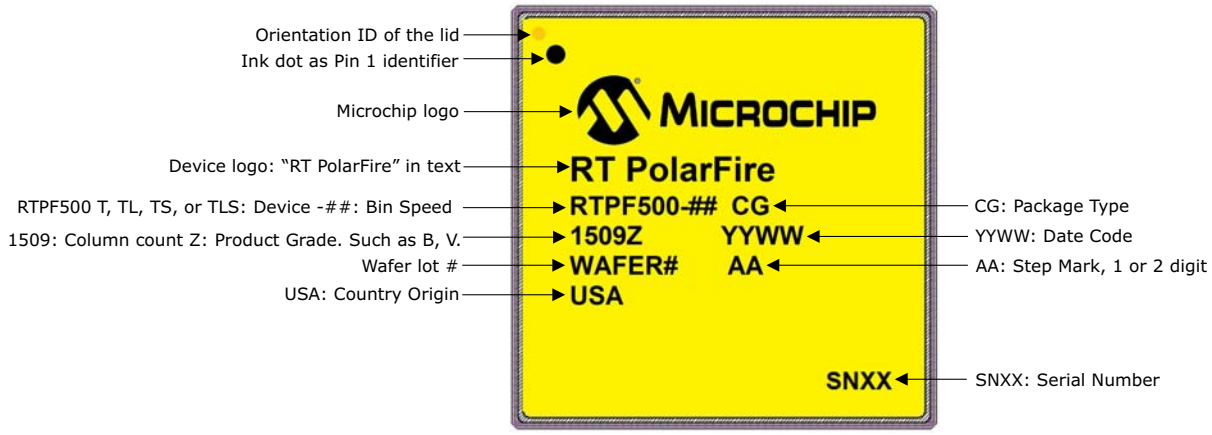
Table 21 • **Package Mass Information**

Package Name	Mass Value
LG1509	28.40 g
CB1509	32.71 g
CG1509	34.50 g

2.10 Package Marking

Microchip marks the full ordering part number on the top of each device. The following figure provides details for each character code present on Microchip's RT PolarFire FPGA device.

Figure 4 • **RT PolarFire LG1509/CG1509 Package Marking Format**



2.11 Packing and Shipping

The RT PolarFire series device is packed in trays, which are used to pack most of the Microchip surface-mount devices. Trays provide excellent protection from mechanical damage. In addition, they are manufactured using the anti-static material to provide limited protection against ESD damage.

Table 22 • **Standard Device Counts per Tray and Carton**

Package	Maximum Number of Devices Per Jewel Box
CG1509	1
CB1509	1
LG1509	1

2.12 PCB Design

For more information about PCB design rules for CCGA packages, refer to *AC190: Ceramic Column Grid Array Application Note*.