TR0066
Test Report
PolarFire FPGA CoreJESD204BRX Interoperability for ADC12DJ3200

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Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 1.0

The first publication of this document.

2 PolarFire FPGA CoreJESD204BRX Interoperability for ADC12DJ3200 Test Report

Microsemi provides solutions for interfacing with analog-to-digital converter (ADC) and digital-to-analog converter (DAC) devices using the JESD204B JEDEC standards. These solutions are provided as DirectCore soft IPs (CoreJESD204BRX and CoreJESD204BTX) and interfaced with the transceiver interface of PolarFire® FPGA devices. This report provides the interoperability test results performed on a third-party ADC. The interoperability test results describe the JESD204B link parameters, hardware test setup, equipment used, and final test report of Microsemi DirectCore—CoreJESD204BRX.

2.1 References

- *CoreJESD204BRX IP Handbook*
- *CoreJESD204BTX IP Handbook*
- *UG0677: PolarFire FPGA Transceiver User Guide*
- *ADC12DJ3200EVM*
- *Identify ME User Guide*

2.2 Scope

This report describes the hardware setup used for interoperability testing and reporting of the test results of JESD204B link. The following table shows the configuration of the tested device.

Table 1 • **Device Requirements**

Device	Link Rate (Gbps)	Link Width	Subclass
Texas Instruments - ADC12DJ3200	5	×4	0, 1

2.3 Test Requirements

The following are the hardware and software required for interoperability tests.

2.3.1 Hardware Requirements

- PolarFire Evaluation Kit
- Two USB A to mini-B cables
- ADC12DJ3200EVM Evaluation Board
- Function generator
- 110 V to 240 V AC to 12-V DC-Power adapter
- 110 V to 240 V AC to 5 V DC - Power adapter
- SMA cables

2.3.2 Software Requirements

- Libero® SoC PolarFire
- ADC12DJ320000EVM configuration GUI

2.3.3 Source Files

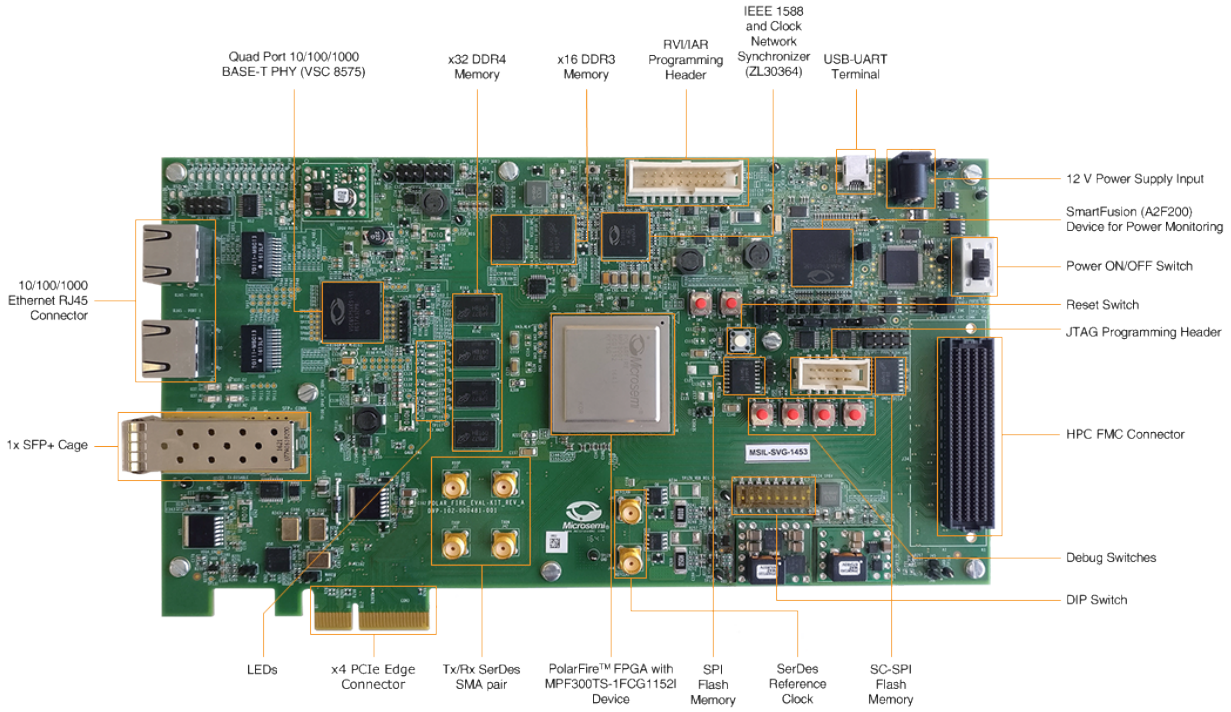
For design files, contact Microsemi Tech Support Team at *soc_tech@microsemi.com*.

2.4 Interoperability Test Setup

The interoperability test is performed on the PolarFire Evaluation Kit board with the MPF300T-1FCG1152I device as shown in Figure 1, page 3 and Texas instruments ADC12DJ3200 EVM as shown in Figure 2, page 4. The ADC12DJ3200 is a low-power, wide-bandwidth, 12-bit, dual 3.2-GSPS or single 6.4-GSPS, dual-channel, analog-to-digital converter (ADC). The device supports the JESD204B serial interface with data rates up to 12.8 Gbps, supporting two or four lanes per ADC. The design for the test is developed using the Libero SoC Polarfire software by instantiating the CoreJESD204BRX IP and other required IP cores in SmartDesign. The register configuration of ADC12DJ3200 is done using ADC12DJxxxx GUI by Texas instruments. ADC12DJ3200 EVM is used to evaluate the ADC12DJ3200. It is connected to the FPGA mezzanine card high pin count (FMC HPC) connector of the PolarFire Evaluation Kit.

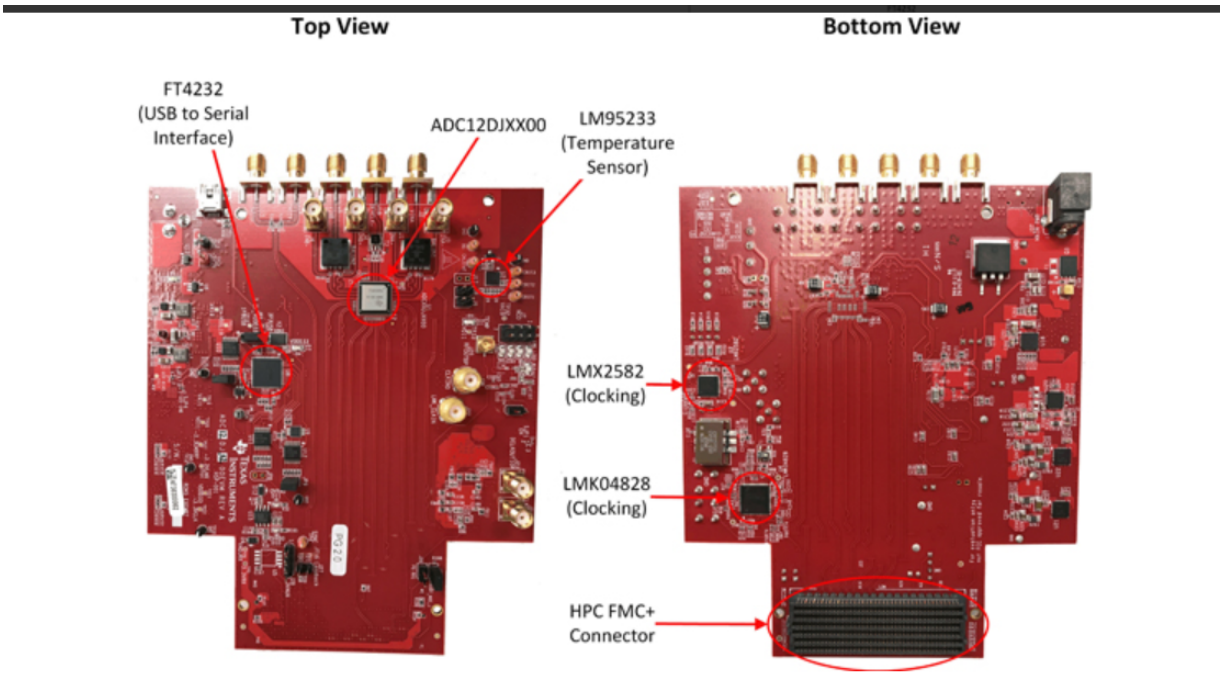
The following figure shows the hardware setup.

Figure 1 • **PolarFire Evaluation Kit**



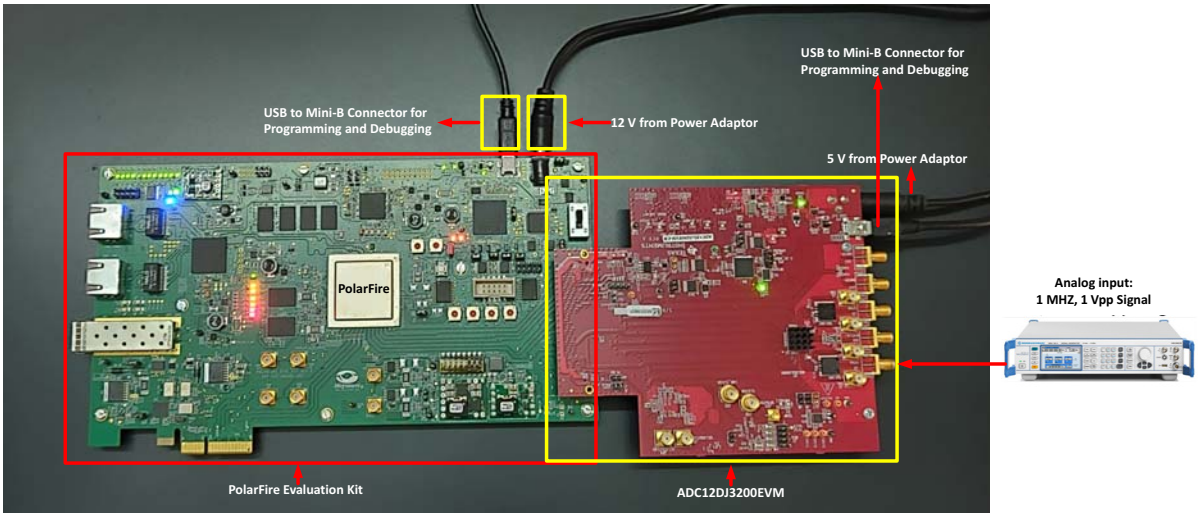
The following figure shows the ADC12DJ3200EVM evaluation board.

Figure 2 • **ADC12DJ3200EVM**



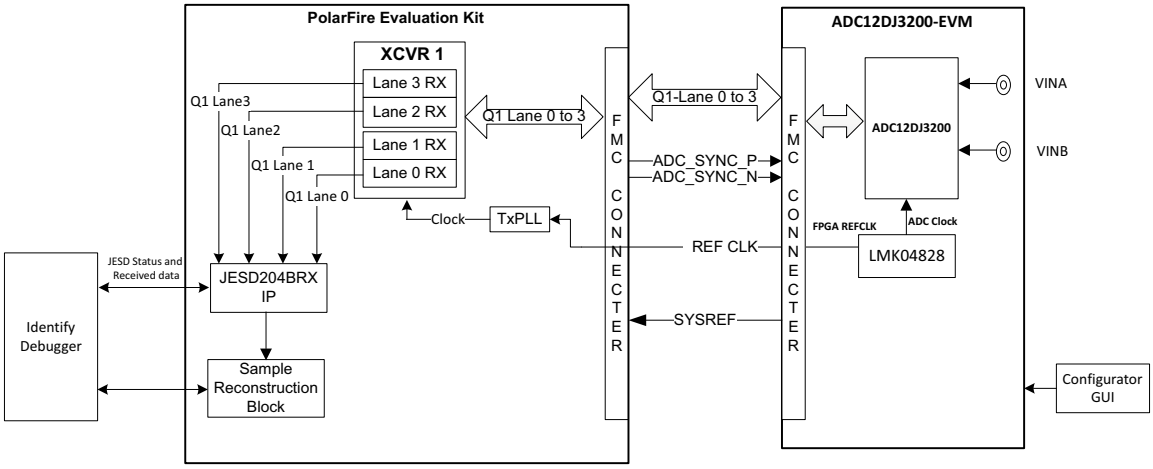
The following figure shows the hardware setup for interoperability tests.

Figure 3 • **Hardware Setup for Interoperability Testing with ADC12DJ3200EVM**



The following block diagram illustrates how signals flow in the hardware setup for interoperability tests.

Figure 4 • **Block Diagram of Interoperability Tests**



2.5 Interoperability Test Settings

CoreJESD204BRX and ADC12DJ3200 are configured, as shown in the following table.

Table 2 • **Configuring CoreJESD204BRX and ADC12DJ3200**

Parameter	CoreJESD204BRX	ADC12DJ3200	Description
SCR	0/1	0/1	Scramble enable/disable
L	4	4	Lanes
F	8	8	Octets per frame
K	4	4	Frames per multi-frame
M	4	4	Converters
CS	0	0	Control bits per sample
N	12	12	Sample resolution
N'	12	12	Sample envelope
S	5	5	Samples per converter per frame
HD	0	0	High density mode
CF	0	0	Control bits per frame
SUBCLASSV	0/1	0/1	0x0/0x1

2.6 ADC12DJ3200EVM Interoperability Tests

The following interoperability tests were performed on CoreJESD204BRX and ADC12DJ3200.

- Test 1: Data Link Layer—Code Group Synchronization, page 6
- Test 2: Data Link Layer—Initial Lane Alignment Sequence, page 7
- Test 3: Receiver Transport Layer, page 8
- Test 4: Descrambling, page 8
- Test 5: Deterministic Latency, page 9

2.6.1 Test 1: Data Link Layer—Code Group Synchronization

On link startup, the receiver issues a synchronization request and the transmitter emits comma characters /K/ = /K28.5/. Identify Debugger was used to monitor the operation of the receiver data link layer.

The following table shows the data link layer-code group synchronization (CGS) test results.

Table 3 • **Data Link Layer—Code Group Synchronization Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC1.1	Check if the receiver asserts SYNC_N signal when the link was down.	CoreJESD204BRX_0 -> SYNC_N signal was observed in Identify Debugger.	SYNC_N was low.	Passed
ADC1.2	Check if SYNC_N request was de-asserted on receiving at least four successive /K/ characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] and SYNC_N signals were observed in Identify Debugger.	K28.5 or /K/ character (0 ×BC) was observed on DATA_OUT, and SYNC_N was de-asserted on receiving at least four successive /K/ characters.	Passed
ADC1.3	Check the full code group synchronization at receiver on receiving another four successive 8B/10B characters.	CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] SYNC_N, and CGS_ERR[3:0] signals were observed in Identify Debugger.	CGS errors were not asserted.	Passed

2.6.2 Test 2: Data Link Layer—Initial Lane Alignment Sequence

The following table shows the data link layer—initial lane alignment sequence (ILAS) test results.

Table 4 • **Data Link Layer—Initial Lane Alignment Sequence Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC2.1	Check if the ILA phase starts after the CGS phase.	CoreJESD204BRX_0-> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0] SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0] signals were observed in Identify Debugger.	Multi-frame starts with 0×1C and was aligned to SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], and SOMF_3[3:0].	Passed
ADC2.2	Check the JESD configuration data in the second multi-frame	CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] SOMF_0[3:0], SOMF_1[3:0], SOMF_2[3:0], SOMF_3[3:0] SOF_0[3:0], SOF_1[3:0], SOF_2[3:0], SOF_3[3:0] and LINK_CD_ERROR[3:0] signals were observed in Identify Debugger.	Observe the second multi-frame that starts with 0x1C followed by 0x9C and JESD204B configuration data.	Passed

2.6.3 Test 3: Receiver Transport Layer

The following table shows the receiver transport layer test results.

Table 5 • **Receiver Transport Layer Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC3.1	Check data integrity in test mode	ADC was configured in long transport layer test pattern mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals were observed in Identify Debugger	Received signal correlates with the transport layer test pattern.	Passed
ADC3.2	Check data integrity in normal mode	ADC was configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals were observed in Identify Debugger.	Received signal correlates with the input signal given for ADC sampling.	Passed

2.6.4 Test 4: Descrambling

Scrambler is enabled in ADC and descrambler is enabled in CoreJESD204BRX IP. The following table shows the descrambling test results.

Table 6 • **Descrambling Test Results**

Test Case	Objective	Description	Passing Criteria	Results
ADC4.1	Check descrambler functionality	ADC was configured in normal mode. CoreJESD204BRX _0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals were observed in Identify Debugger.	Received signal (monitored in identify tool) correlates with the analog sine wave input given for ADC sampling.	Passed

2.6.5 Test 5: Deterministic Latency

CoreJESD204BRX IP and ADC12DJ3200 were configured in Subclass 1 mode. The following table shows the JESD204B deterministic latency measurement test results.

Table 7 • **JESD204B Deterministic Latency Measurement Test Results – Subclass 1 Mode**

Test Case	Objective	Description	Passing Criteria	Results
ADC5.1	Check local multi-frame counter (LMFC) alignment	CoreJESD204BRX_0 -> clkgen_lmfc and SYSREF_IN signals were observed in Identify Debugger.	SYSREF_IN aligned to clkgen_lmfc.	Passed
ADC5.2	SYSREF capture	CoreJESD204BRX _0 -> c2l_mf_phase, and SYSREF_IN signals were observed in Identify Debugger.	LMFC counter restarts after the SYSREF_IN capture.	Passed
ADC5.3	Check latency from start de-assertion of SYNC_N to first user data output.	Check Latency was fixed for every link reset/initialization.	Latency must be the same for link reset/initialization.	Passed
ADC5.4	Check the data latency during user data phase.	Check if the data latency was fixed during the user data phase. CoreJESD204BRX_0 -> DATA_OUT_0[31:0], DATA_OUT_1[31:0], DATA_OUT_2[31:0], DATA_OUT_3[31:0] signals were observed in Identify Debugger.	The user data is seen without distortion.	Passed