

# First Thursdays

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May 2 - Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

June 6 - Webinar 2: How to Get Started with Renode for PolarFire SoC

July 4 - Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

Aug. 1 - Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

**Sept. 5 - Webinar 5: Add and Debug PolarFire SoC Peripherals with Renode**

**Oct. 3 - Webinar 6: Add and Debug and Pre-Existing Peripheral in PolarFire SoC**

**Nov. 7 - Webinar 7: How to write custom models – filters, offloading, acceleration etc**

**Dec. 5 - Webinar 8: Handling Binaries**

Contd.

# Second Thursdays

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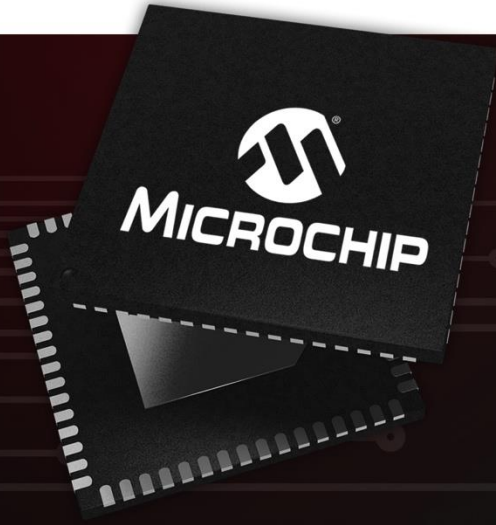
**Jan. 9 - Webinar 9: Run Linux on Renode (PolarFire SoC Model as a Quad-core SMP) – this is not a Linux / Buildroot tutorial**

**Feb. 13 - Webinar 10: Build applications for Linux on PolarFire SoC**

**Mar. 12 - Webinar 11: Introduction to PolarFire SoC MSS Configuration and Software Flow**

**Apr. 9 - Webinar 12: Two baremetal Applications on PolarFire SoC**

**May 14 - Webinar 13: Linux + Real-Time (AMP Mode) on PolarFire SoC**



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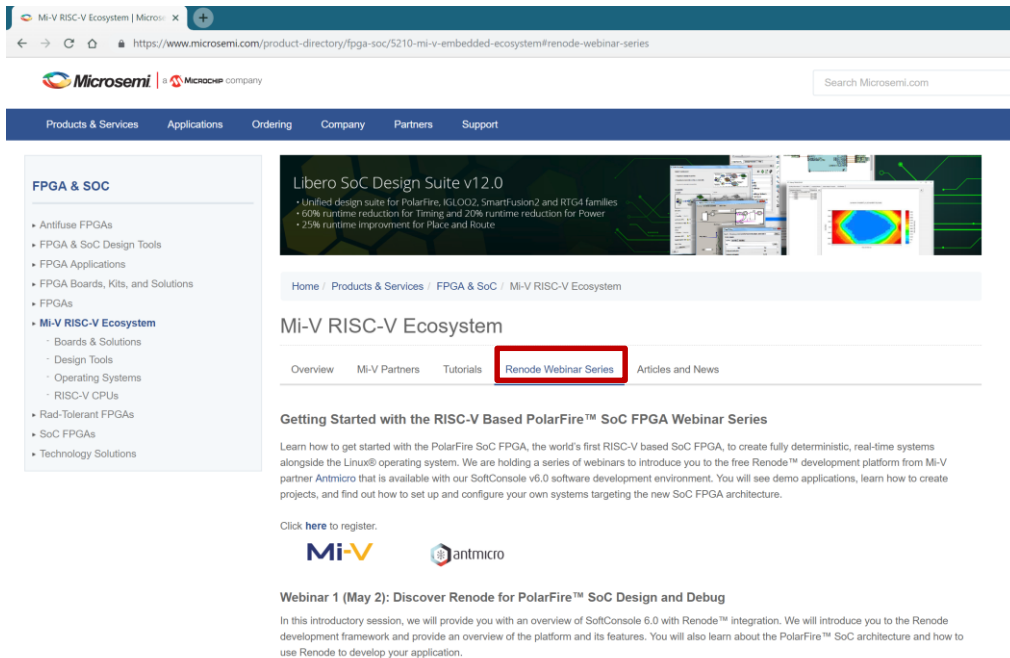


**Getting Started with the RISC-V Based PolarFire® SoC FPGA Webinar Series**  
**Session 5: “Add and Debug PolarFire SoC Peripherals with Renode”**

*Hugh Breslin, Embedded Linux Engineer*

*Thursday Sep. 5, 2019*

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**Libero SoC Design Suite v12.0**

- Unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 families
- 60% runtime reduction for Timing and 20% runtime reduction for Power
- 25% runtime improvement for Place and Route

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**Mi-V RISC-V Ecosystem**

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**Getting Started with the RISC-V Based PolarFire™ SoC FPGA Webinar Series**

Learn how to get started with the PolarFire SoC FPGA, the world's first RISC-V based SoC FPGA, to create fully deterministic, real-time systems alongside the Linux® operating system. We are holding a series of webinars to introduce you to the free Renode™ development platform from Mi-V partner Antmicro that is available with our SoftConsole v6.0 software development environment. You will see demo applications, learn how to create projects, and find out how to set up and configure your own systems targeting the new SoC FPGA architecture.

Click [here](#) to register.

**Mi-V** 

**Webinar 1 (May 2): Discover Renode for PolarFire™ SoC Design and Debug**

In this introductory session, we will provide you with an overview of SoftConsole 6.0 with Renode™ integration. We will introduce you to the Renode development framework and provide an overview of the platform and its features. You will also learn about the PolarFire™ SoC architecture and how to use Renode to develop your application.

[www.microsemi.com/Mi-V](https://www.microsemi.com/Mi-V) “Renode Webinar Series”

# Add and Debug PolarFire® SoC Peripherals with Renode

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- The files that make a Renode system
- The launch script
- CPU file
- Board file
- Summary
- Debugging a peripheral



# Learn to Debug a Bare-Metal PolarFire® SoC Application with Renode

---

## The Files That Make a Renode System

# The Files That Make a Renode System

---

- **We have two pre-configured systems:**

Mi-V Renode emulation platform (Mi-V system):

Configured to emulate the Mi-V soft CPUs (RV32G core with UART, GPIOs and Timers)

PolarFire SoC Renode emulation platform (PolarFire SoC system):

Configured to emulate PolarFire Soc and its peripherals

# The Files That Make a Renode System

- **3 files that can make up a Renode system**
  - Only the script file is passed as an argument when launching Renode
- **Script file:** Tells Renode to create a machine, load the board file and run commands
- **Board file:** Tells Renode to load the CPU file and describes the hardware connections for the system (e.g. GPIO connecting to an LED)
- **CPU file:** Describes the system (e.g. CPU and peripherals)

```
(monitor) 1 $CWD/./scripts/single-node/miv-basic.resc
Available peripherals:
```

```
sysbus (SystemBus)
├── clint (CoreLevelInterruptor)
│   └── <0x44000000, 0x4400FFFF>
├── cpu (RiscV32)
│   └── Slot: 0
├── ddr (MappedMemory)
│   └── <0x80000000, 0x83FFFFFF>
├── flash (MappedMemory)
│   └── <0x60000000, 0x6003FFFF>
├── gpioInputs (MiV_CoreGPIO)
│   └── <0x70002000, 0x700020A3>
│       ├── user_switch_0 (Button)
│       │   └── Address: 0
│       ├── user_switch_1 (Button)
│       │   └── Address: 1
│       └── user_switch_2 (Button)
│           └── Address: 2
├── gpioOutputs (MiV_CoreGPIO)
│   └── <0x70005000, 0x700050A3>
│       ├── led0 (LED)
│       │   └── Address: 0
│       ├── led1 (LED)
│       │   └── Address: 1
│       └── led2 (LED)
│           └── Address: 2
```

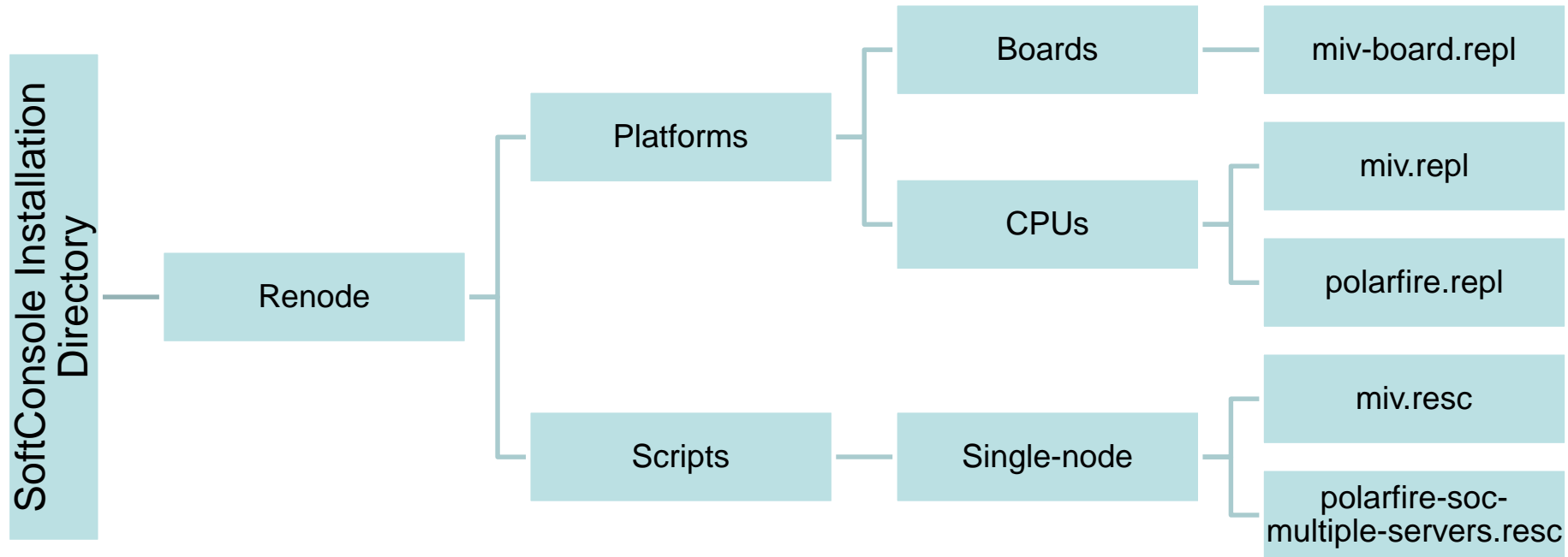
Launch Script

CPU File

Board File

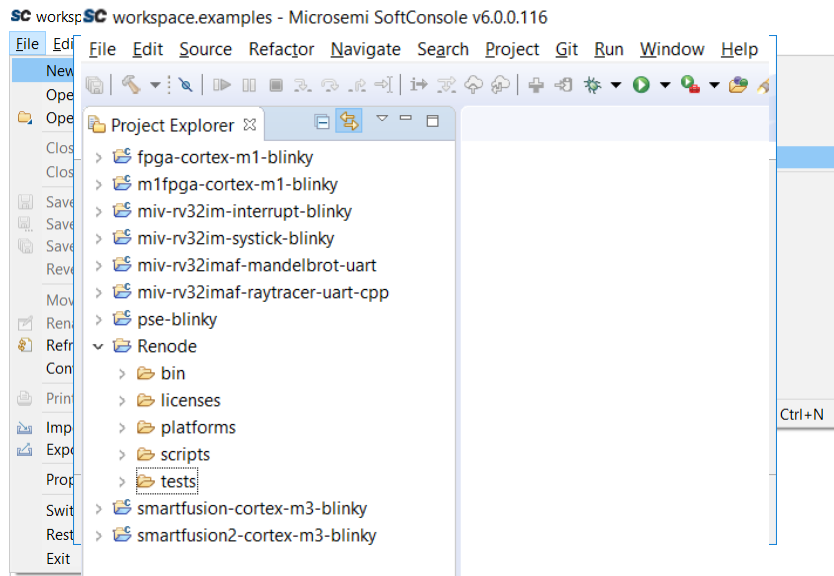


# The Files That Make a Renode System



# The Files That Make a Renode System

- **Easiest way to deal with the files and folder structure is to create a “Renode” project in SoftConsole**

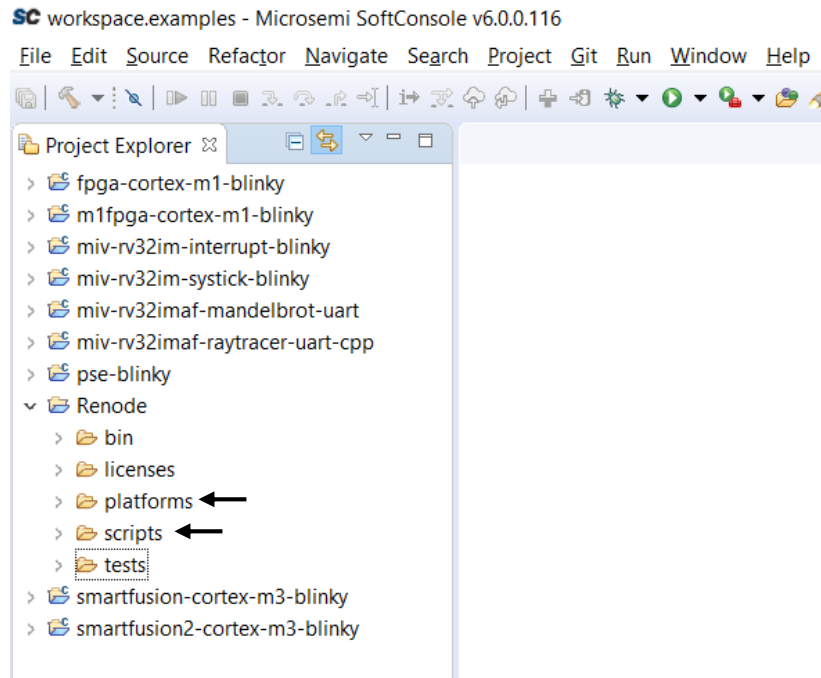


# The Files That Make a Renode System

SoftConsole  
Installation  
Directory

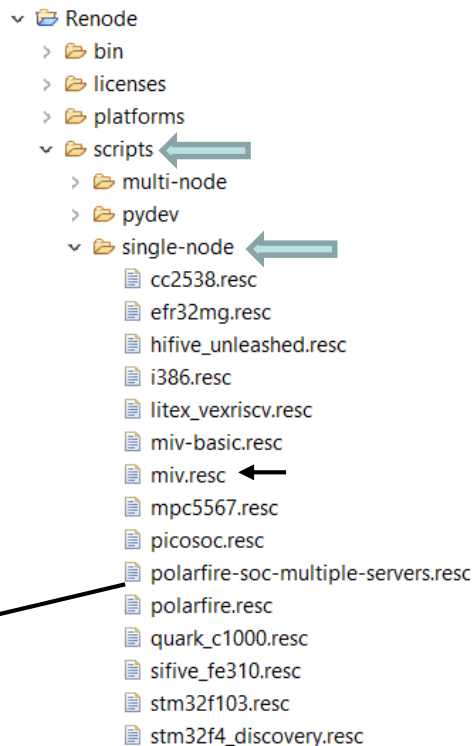
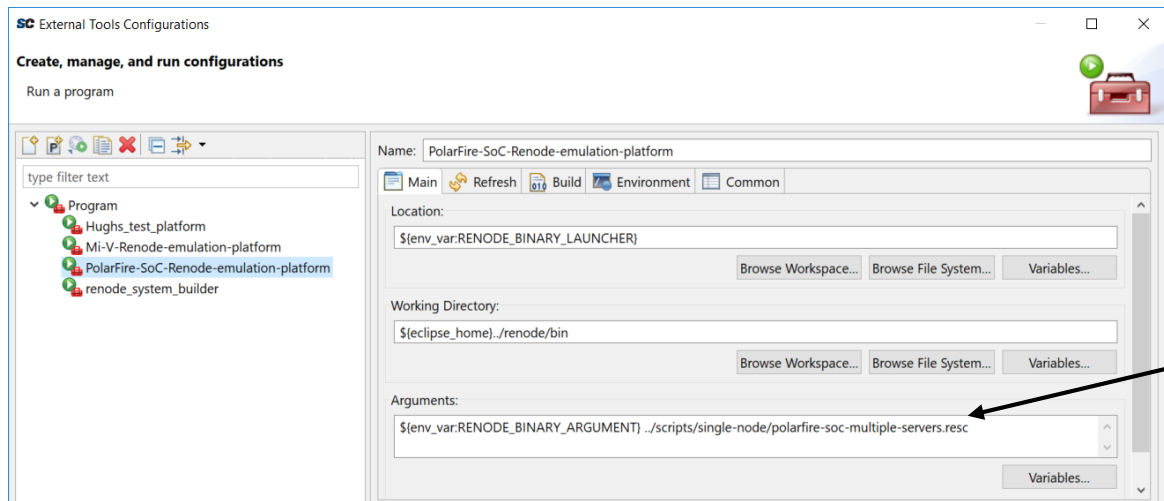
Renode

- **Platforms:** Contains configuration files for platforms (i.e. CPU and board files)
- **Scripts:** Contains launch files for different platforms (i.e. launch scripts)

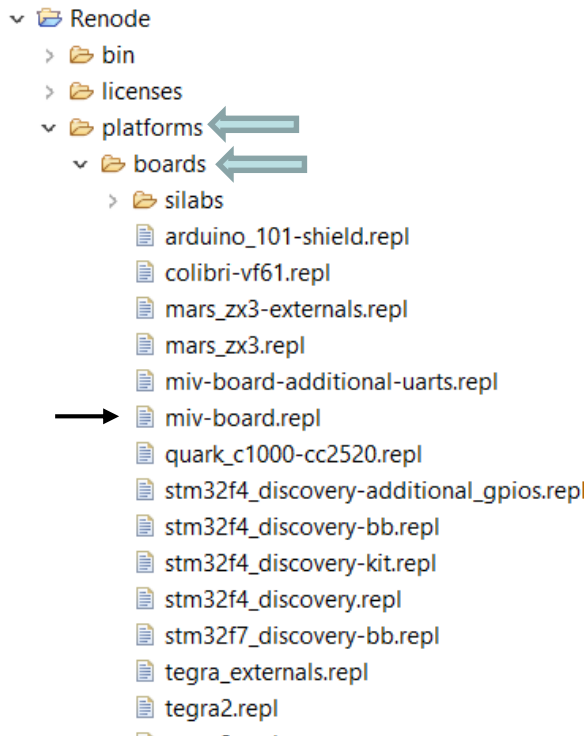


# The Files That Make a Renode System

- **miv.resc**: Launches the Mi-V system
- **polarfire-soc-multiple-servers.resc**: Launches the PolarFire SoC system



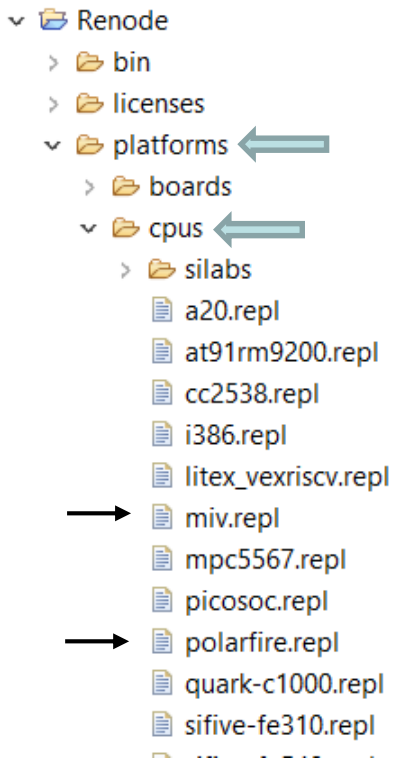
# The Files That Make a Renode System



## Board files

- PF SoC system: n/a
- Mi-V system: miv-board.repl

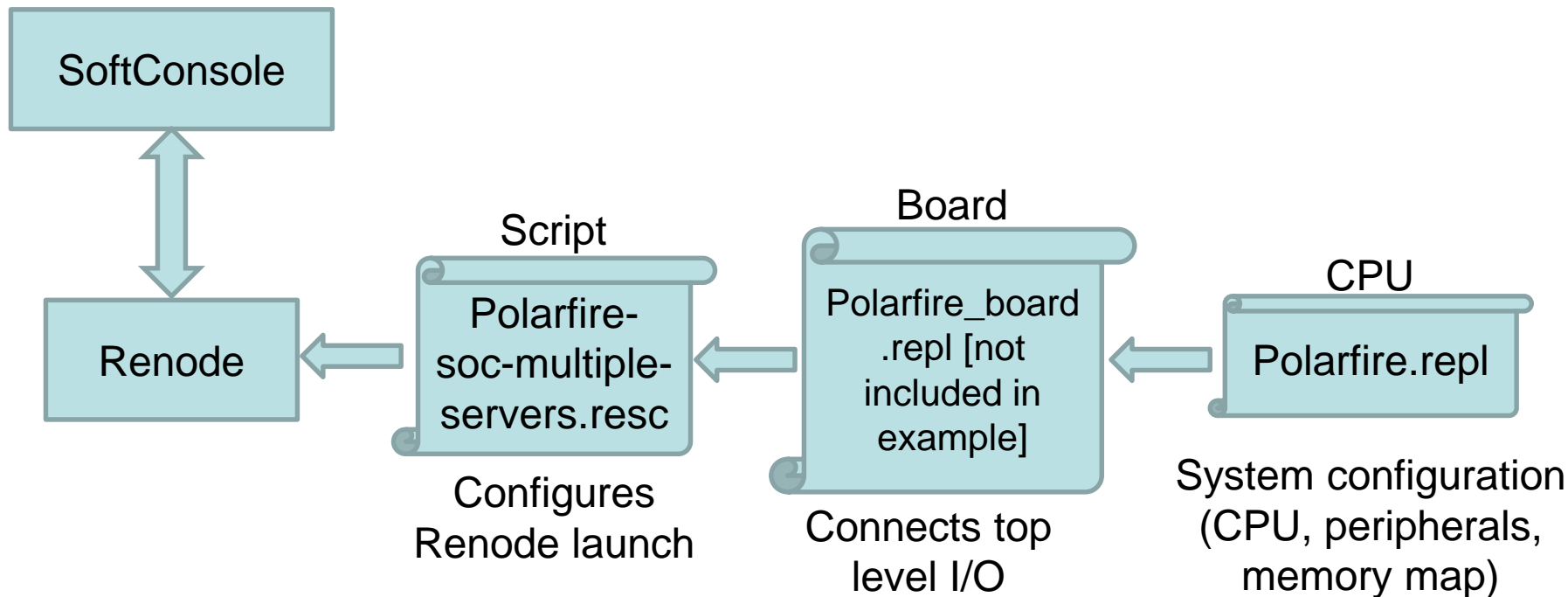
# The Files That Make a Renode System



## CPU files

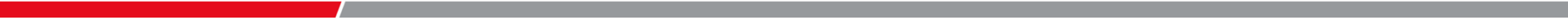
- **PolarFire SoC system: polarfire.repl**
- **Mi-V system: miv.repl**

# The Files That Make a Renode System





# The Launch Script





# The Launch Script

SC workspace.examples - Renode/scripts/single-node/polarfire-soc-multiple-servers.resc - Microsemi SoftConsole v6.0.0.116

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Project Explorer

- Renode
  - bin
  - licenses
  - platforms
  - scripts
    - multi-node
    - pydev
    - single-node
      - cc2538.resc
      - efr32mg.resc
      - hifive\_unleashed.resc
      - i386.resc
      - litex\_vexriscv.resc
      - miv-basic.resc
      - miv.resc
      - mpc5567.resc
      - picosoc.resc
      - polarfire-soc-multiple-servers.resc
      - polarfire.resc
      - quark\_c1000.resc
      - sifive\_fe310.resc
      - stm32f103.resc
      - stm32f4\_discovery.resc
      - stm32f746.resc
      - tegra3.resc
      - versatile.resc
      - vexpress.resc
      - vybrid.resc
      - zedboard.resc
      - monitor.py
- tests
- smartfusion-cortex-m3-blinkv

```

1:name: PolarFire SoC
2:description: This is a sample script prepared to create a PolarFire SoC platform
3
4:LogLevel 3
5
6:using sysbus
7:mach create
8
9:machine LoadPlatformDescription @platforms/cpus/polarfire.repl
10:machine LoadPlatformDescriptionFromString
11:""
12:button0: Miscellaneous.Button @ gpio0
13:    -> gpio0@0
14
15:button1: Miscellaneous.Button @ gpio0
16:    -> gpio0@1
17
18:button2: Miscellaneous.Button @ gpio0
19:    -> gpio0@2
20:""
21
22:LogLevel 3 sysbus.e51
23:LogLevel 3 sysbus.u54_1
24:LogLevel 3 sysbus.u54_2
25:LogLevel 3 sysbus.u54_3
26:LogLevel 3 sysbus.u54_4
27
28:showAnalyzer mmuart0
29
30:e51 StartGdbServer 3333 true
31:u54_1 StartGdbServer 3334 true
32:u54_2 StartGdbServer 3335 true
33:u54_3 StartGdbServer 3336 true
34:u54_4 StartGdbServer 3337 true
35
36:log "Renode has been started successfully and is ready for a gdb connection. (This is not an error)" 3

```

1. Create a new machine

2. Load the platform

3. Connect buttons to GPIOs \* Could be done in the board file \*

4. Configure logging

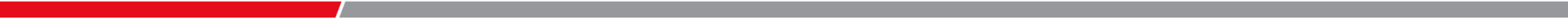
5. Show UART analyser

6. Start a GDB server on each hart

7. Print message to allow SC to start GDB



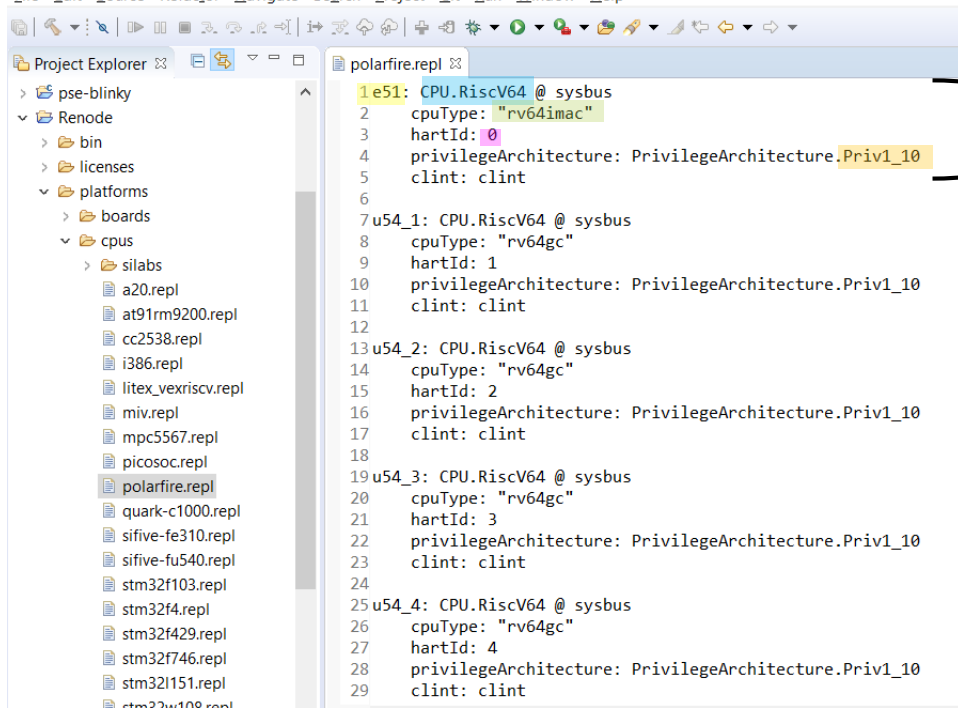
# The CPU File



# The CPU File

SC workspace.examples - Renode/platforms/cpus/polarfire.repl - Microsemi SoftConsole v6.0.0.116

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ADD CPU to the system

## Connecting a CPU:

[name]: [path\_to\_cpu] @ sysbus

cpu\_Type: "[cpu\_type]"

hartId: [ID]

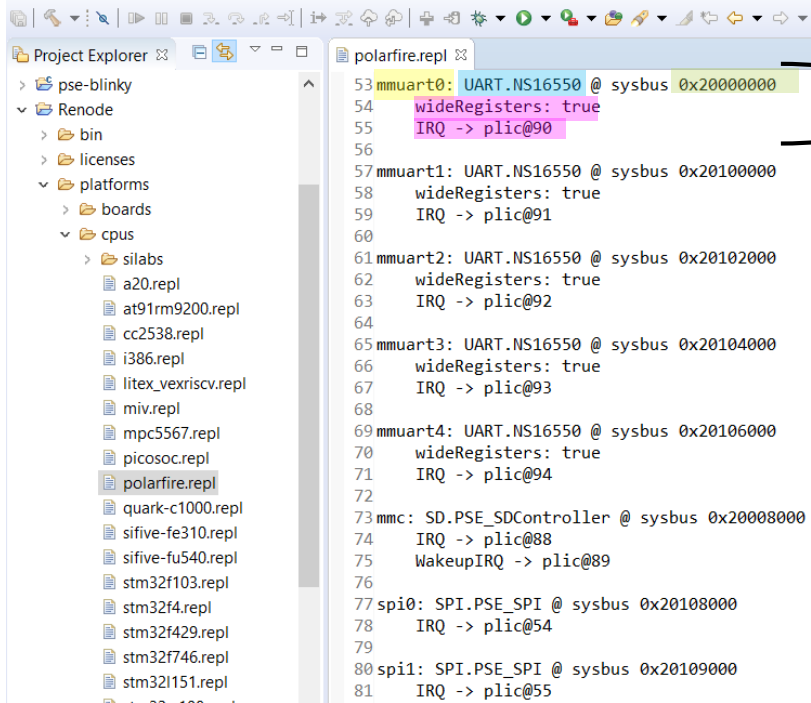
privilegeArchitecture: PrivilegeArchitecture.[version]

clint: clint

# The CPU File

SC workspace.examples - Renode/platforms/cpus/polarfire.repl - Microsemi SoftConsole v6.0.0.116

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ADD UART to the system

## Connecting a peripheral:

It depends on the peripheral!

[name]: [path\_to\_peripheral] @ sysbus [address]  
[parameters0]  
[parameters1]  
etc.

# The CPU File

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer

- Renode
  - bin
  - licenses
  - platforms
    - boards
    - cpus
      - silabs
        - a20.repl
        - at91rm9200.repl
        - cc2538.repl
        - i386.repl
        - litex\_vexriscv.repl
        - miv.repl**
        - mpc5567.repl
        - picosoc.repl
        - polarfire.repl
        - quark-c1000.repl
        - sifive-fe310.repl
        - sifive-fu540.repl
        - stm32f103.repl
        - stm32f4.repl
        - stm32f429.repl
        - stm32f746.repl
        - stm32l151.repl
        - stm32w108.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress.repl
        - vybrid.repl
        - zynq-7000.repl

```

1 flash: Memory.MappedMemory @ sysbus 0x60000000
2   size: 0x40000
3
4 ddr: Memory.MappedMemory @ sysbus 0x80000000
5   size: 0x4000000
6
7 uart: UART.MiV_CoreUART @ sysbus 0x70001000
8   clockFrequency: 66000000
9
10 cpu: CPU.RiscV32 @ sysbus
11   cpuType: "rv32g"
12   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
13   clint: clint
14
15 plic: IRQControllers.PlatformLevelInterruptController @ sysbus 0x40000000
16   [0-3] -> cpu@[8-11]
17   numberOfSources: 31
18   prioritiesEnabled: false
19
20 // Power/Reset/Clock/Interrupt
21 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
22   frequency: 66000000
23   [0, 1] -> cpu@[3, 7]
24
25 gpioInputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70002000
26   -> plic@29
27
28 gpioOutputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70005000
29
30 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
31   -> plic@30
32   clockFrequency: 66000000
33
34 timer1: Timers.MiV_CoreTimer @ sysbus 0x70004000
35   -> plic@31
36   clockFrequency: 66000000
  
```

```

sysbus (SystemBus)
├── clint (CoreLevelInterruptor)
│   └── <0x44000000, 0x4400FFFF> 6
├── cpu (RiscV32)
│   └── Slot: 0 4
├── ddr (MappedMemory)
│   └── <0x80000000, 0x83FFFFFF> 2
├── flash (MappedMemory)
│   └── <0x60000000, 0x6003FFFF> 1
├── gpioInputs (MiV_CoreGPIO)
│   └── <0x70002000, 0x700020A3> 7
│       ├── user_switch_0 (Button)
│       │   └── Address: 0
│       ├── user_switch_1 (Button)
│       │   └── Address: 1
│       └── user_switch_2 (Button)
│           └── Address: 2
├── gpioOutputs (MiV_CoreGPIO) 8
│   └── <0x70005000, 0x700050A3>
│       ├── led0 (LED)
│       │   └── Address: 0
│       └── led1 (LED)
│           └── Address: 1
├── plic (PlatformLevelInterruptController)
│   └── <0x40000000, 0x43FFFFFF> 5
├── timer0 (MiV_CoreTimer)
│   └── <0x70003000, 0x7000301B> 9
├── timer1 (MiV_CoreTimer)
│   └── <0x70004000, 0x7000401B> 10
└── uart (MiV_CoreUART)
    └── <0x70001000, 0x70001017> 3
  
```

# The CPU File

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer

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    - boards
    - cpus
      - silabs
        - a20.repl
        - at91rm9200.repl
        - cc2538.repl
        - i386.repl
        - litex\_vexriscv.repl
        - miv.repl**
        - mpc5567.repl
        - picosoc.repl
        - polarfire.repl
        - quark-c1000.repl
        - sifive-fe310.repl
        - sifive-fu540.repl
        - stm32f103.repl
        - stm32f4.repl
        - stm32f429.repl
        - stm32f746.repl
        - stm32l151.repl
        - stm32w108.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress.repl
        - vybrid.repl
        - zynq-7000.repl
- scripts
- tests

miv.repl

```

1 flash: Memory.MappedMemory @ sysbus 0x60000000
2   size: 0x40000
3
4 ddr: Memory.MappedMemory @ sysbus 0x80000000
5   size: 0x4000000
6
7 uart: UART.MiV_CoreUART @ sysbus 0x70001000
8   clockFrequency: 66000000
9
10 cpu: CPU.RiscV32 @ sysbus
11   cpuType: "rv32g"
12   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
13   clint: clint
14
15 plic: IRQControllers.PlatformLevelInterruptController @ sysbus 0x40000000
16   [0-3] -> cpu@[8-11]
17   numberOfSources: 31
18   prioritiesEnabled: false
19
20 // Power/Reset/Clock/Interrupt
21 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
22   frequency: 66000000
23   [0, 1] -> cpu@[3, 7]
24
25 gpioInputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70002000
26   -> plic@29
27
28 gpioOutputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70005000
29
30 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
31   -> plic@30
32   clockFrequency: 66000000
33
34 timer1: Timers.MiV_CoreTimer @ sysbus 0x70004000
35   -> plic@31
36   clockFrequency: 66000000
37
38 uart2: UART.MiV_CoreUART @ sysbus 0x70006000
39   clockFrequency: 66000000
40

```

Add a second UART

Current UART:

**uart:** UART.MiV\_CoreUART @ sysbus **0x70001000**  
clockFrequency: 66000000

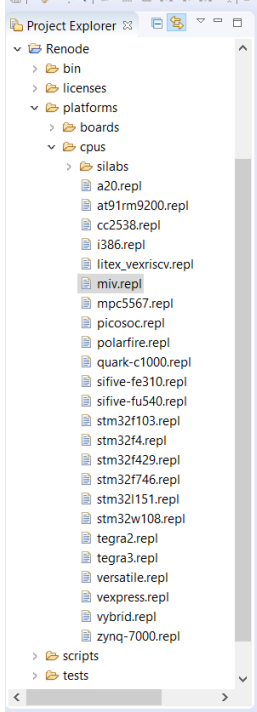
Second UART:

**uart2:** UART.MiV\_CoreUART @ sysbus **0x70006000**  
clockFrequency: 66000000

# The CPU File

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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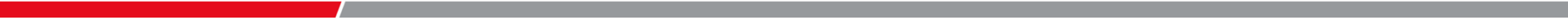


1	flash: Memory.MappedMemory @ sysbus 0x60000000	1
2	size: 0x400000	
3		
4	ddr: Memory.MappedMemory @ sysbus 0x80000000	2
5	size: 0x4000000	
6		
7	uart: UART.MiV_CoreUART @ sysbus 0x70001000	3
8	clockFrequency: 66000000	
9		
10	cpu: CPU.RiscV32 @ sysbus	
11	cpuType: "rv32g"	
12	privilegeArchitecture: PrivilegeArchitecture.Priv1_09	4
13	clint: clint	
14		
15	pllc: IRQControllers.PlatformLevelInterruptController @ sysbus 0x40000000	5
16	[0-3] -> cpu@[8-11]	
17	numberOfSources: 31	
18	prioritiesEnabled: false	
19		
20	// Power/Reset/Clock/Interrupt	
21	clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000	6
22	frequency: 66000000	
23	[0, 1] -> cpu@[3, 7]	
24		
25	gpioInputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70002000	7
26	-> plic@29	
27		
28	gpioOutputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70005000	8
29		
30	timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000	
31	-> plic@30	9
32	clockFrequency: 66000000	
33		
34	timer1: Timers.MiV_CoreTimer @ sysbus 0x70004000	
35	-> plic@31	10
36	clockFrequency: 66000000	
37		
38	uart2: UART.MiV_CoreUART @ sysbus 0x70006000	11
39	clockFrequency: 66000000	
40		

sysbus (SystemBus)	
clint (CoreLevelInterruptor)	6
<0x44000000, 0x4400FFFF>	
cpu (RiscV32)	4
Slot: 0	
ddr (MappedMemory)	2
<0x80000000, 0x83FFFFFF>	
flash (MappedMemory)	1
<0x60000000, 0x6003FFFF>	
gpioInputs (MiV_CoreGPIO)	7
<0x70002000, 0x700020A3>	
user_switch_0 (Button)	
Address: 0	
user_switch_1 (Button)	
Address: 1	
user_switch_2 (Button)	
Address: 2	
gpioOutputs (MiV_CoreGPIO)	8
<0x70005000, 0x700050A3>	
led0 (LED)	
Address: 0	
led1 (LED)	
Address: 1	
plic (PlatformLevelInterruptController)	5
<0x40000000, 0x43FFFFFF>	
timer0 (MiV_CoreTimer)	9
<0x70003000, 0x7000301B>	
timer1 (MiV_CoreTimer)	10
<0x70004000, 0x7000401B>	
uart (MiV_CoreUART)	3
<0x70001000, 0x70001017>	
uart2 (MiV_CoreUART)	11
<0x70006000, 0x70006017>	



# The Board File





# The Board File

SC workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer

- Renode
  - bin
  - licenses
  - platforms
    - boards
      - silabs
        - arduino\_101-shield.repl
        - colibri-vf61.repl
        - mars\_zx3-externals.repl
        - mars\_zx3.repl
        - miv-board-additional-uc
        - miv-board.repl**
        - quark\_c1000-cc2520.repl
        - stm32f4\_discovery-addit
        - stm32f4\_discovery-bb.re
        - stm32f4\_discovery-kit.re
        - stm32f4\_discovery.repl
        - stm32f7\_discovery-bb.re
        - tegra\_externals.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress-externals.repl

miv-board.repl

```
1 using "platforms/cpus/miv.repl"
2
3 gpioOutputs:
4     0 -> led0@0
5     1 -> led1@0
6
7 led0: Miscellaneous.LED @ gpioOutputs 0
8     invert: true
9
10 led1: Miscellaneous.LED @ gpioOutputs 1
11     invert: true
12
13 user_switch_0: Miscellaneous.Button @ gpioInputs 0
14     invert: true
15     -> gpioInputs@0
16
17 user_switch_1: Miscellaneous.Button @ gpioInputs 1
18     invert: true
19     -> gpioInputs@1
20
21 user_switch_2: Miscellaneous.Button @ gpioInputs 2
22     invert: true
23     -> gpioInputs@2
24
25
26
27
```

1. Load the CPU file

2. Connect GPIO outputs to LEDs

3. Create LEDs

4. Create switches

5. Connect switch to GPIO

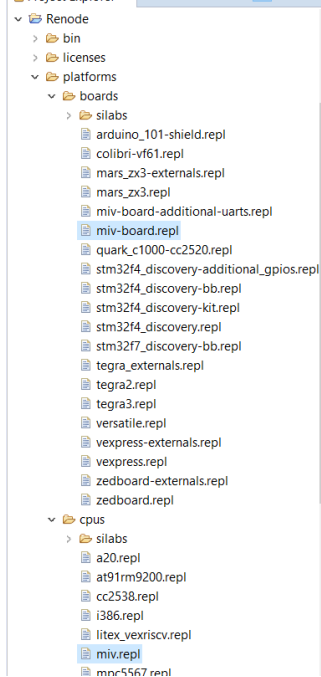
# The Board File

SC workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer



miv.repl

```
1 flash: Memory.MappedMemory @ sysbus 0x60000000
2   size: 0x400000
3
4 ddr: Memory.MappedMemory @ sysbus 0x80000000
5   size: 0x40000000
6
7 uart: UART.MiV_CoreUART @ sysbus 0x70001000
8   clockFrequency: 66000000
9
10 cpu: CPU.RiscV32 @ sysbus
11   cpuType: "rv32g"
12   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
13   clint: clint
14
15 plic: IRQControllers.PlatformLevelInterruptController @ sysbus 0x40000000
16   [0-3] -> cpu@[8-11]
17   numberOfSources: 31
18   prioritiesEnabled: false
19
20 // Power/Reset/Clock/Interrupt
21 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
22   frequency: 66000000
23   [0, 1] -> cpu@[3, 7]
24
25 gpioInputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70002000
26   -> plic@29
27
28 gpioOutputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70005000
29
30 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
31   -> plic@30
32   clockFrequency: 66000000
33
34 timer1: Timers.MiV_CoreTimer @ sysbus 0x70004000
35   -> plic@31
36   clockFrequency: 66000000
37
38 uart2: UART.MiV_CoreUART @ sysbus 0x70006000
39   clockFrequency: 66000000
```

miv-board.repl

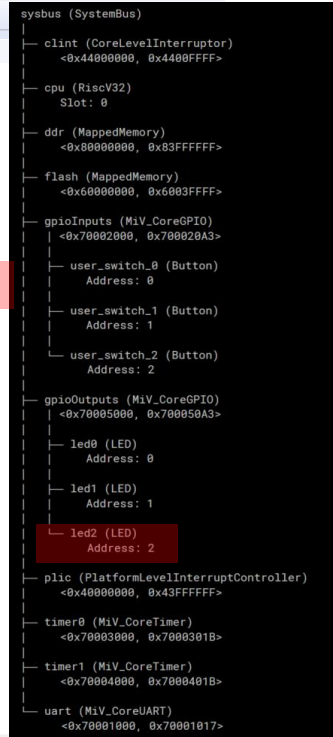
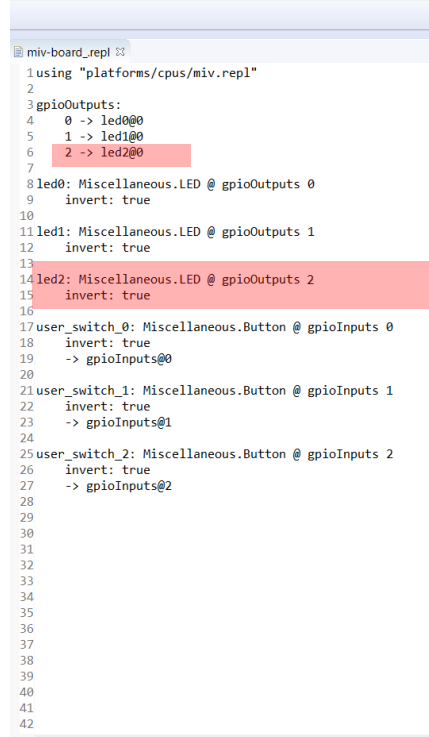
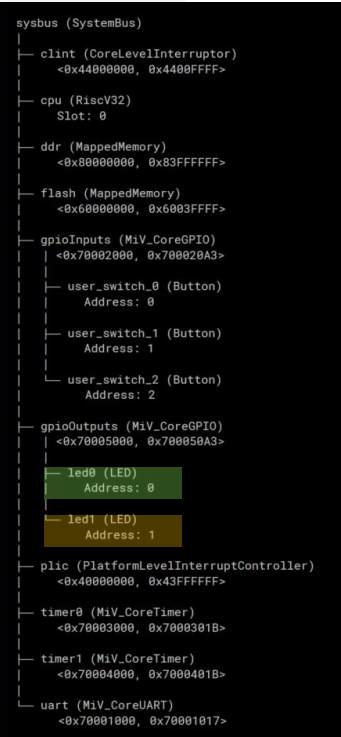
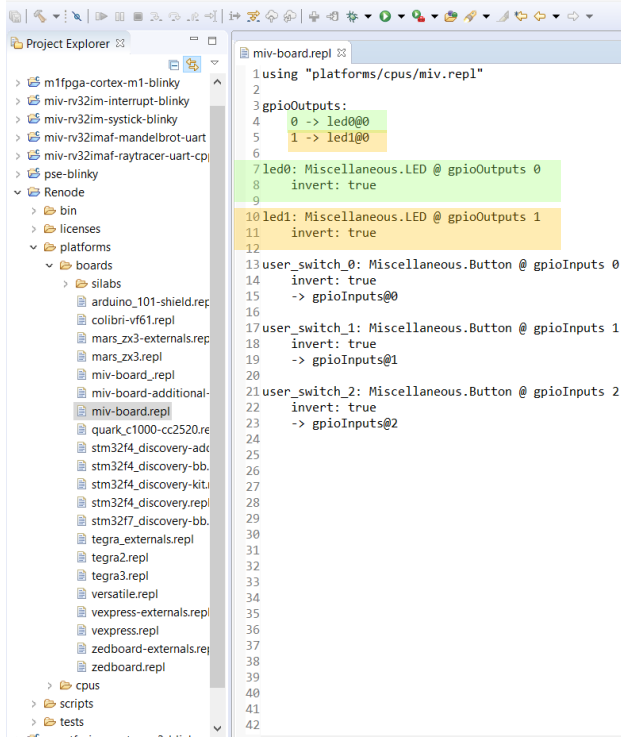
```
1 using "platforms/cpus/miv.repl"
2
3 gpioOutputs:
4   0 -> led0@0
5   1 -> led1@0
6
7 led0: Miscellaneous.LED @ gpioOutputs 0
8   invert: true
9
10 led1: Miscellaneous.LED @ gpioOutputs 1
11   invert: true
12
13 user_switch_0: Miscellaneous.Button @ gpioInputs 0
14   invert: true
15   -> gpioInputs@0
16
17 user_switch_1: Miscellaneous.Button @ gpioInputs 1
18   invert: true
19   -> gpioInputs@1
20
21 user_switch_2: Miscellaneous.Button @ gpioInputs 2
22   invert: true
23   -> gpioInputs@2
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
```

```
sysbus (SystemBus)
├── clint (CoreLevelInterruptor)
│   └── <0x44000000, 0x4400FFFF>
├── cpu (RiscV32)
│   └── Slot: 0
├── ddr (MappedMemory)
│   └── <0x80000000, 0x83FFFFFF>
├── flash (MappedMemory)
│   └── <0x60000000, 0x603FFFFF>
├── gpioInputs (MiV_CoreGPIO)
│   └── <0x70002000, 0x700020A3>
│       ├── user_switch_0 (Button)
│       │   └── Address: 0
│       ├── user_switch_1 (Button)
│       │   └── Address: 1
│       └── user_switch_2 (Button)
│           └── Address: 2
├── gpioOutputs (MiV_CoreGPIO)
│   ├── <0x70005000, 0x700050A3>
│   │   ├── led0 (LED)
│   │   │   └── Address: 0
│   │   └── led1 (LED)
│   │       └── Address: 1
│   └── <0x70003000, 0x7000301B>
├── plic (PlatformLevelInterruptController)
│   └── <0x40000000, 0x43FFFFFF>
├── timer0 (MiV_CoreTimer)
│   └── <0x70003000, 0x7000301B>
├── timer1 (MiV_CoreTimer)
│   └── <0x70004000, 0x7000401B>
└── uart (MiV_CoreUART)
    └── <0x70001000, 0x70001017>
```

# The Board File

SC workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

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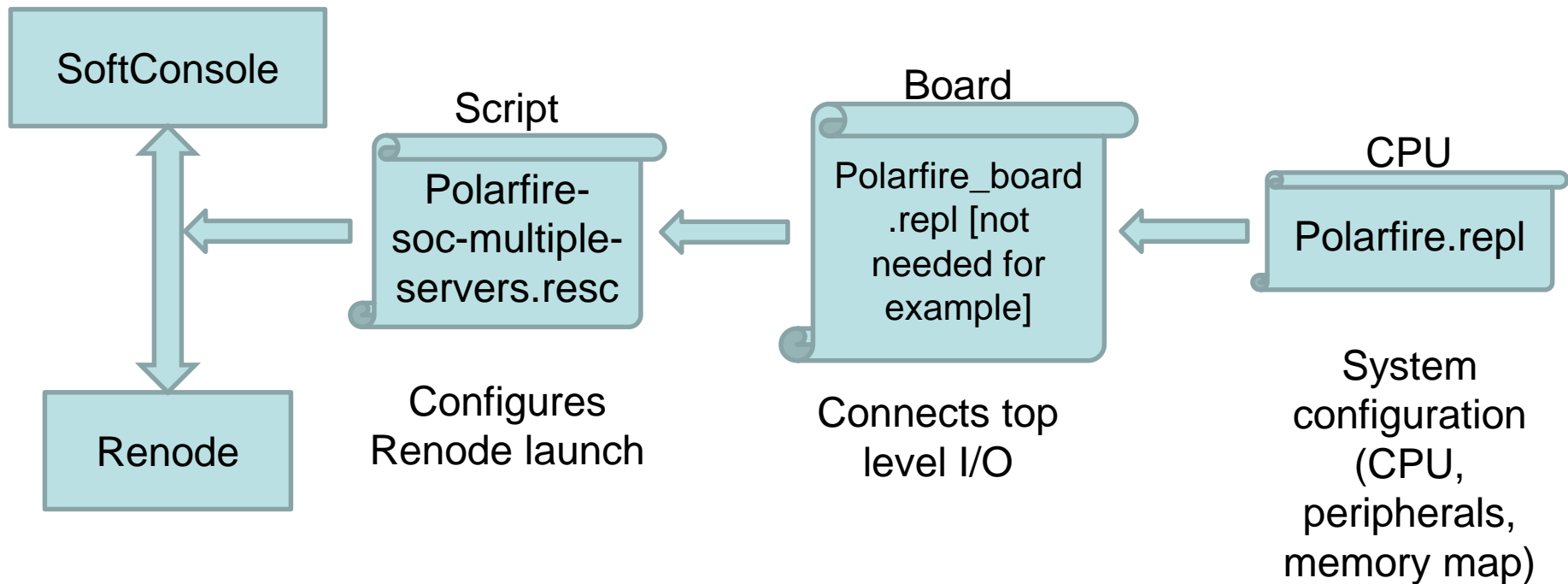




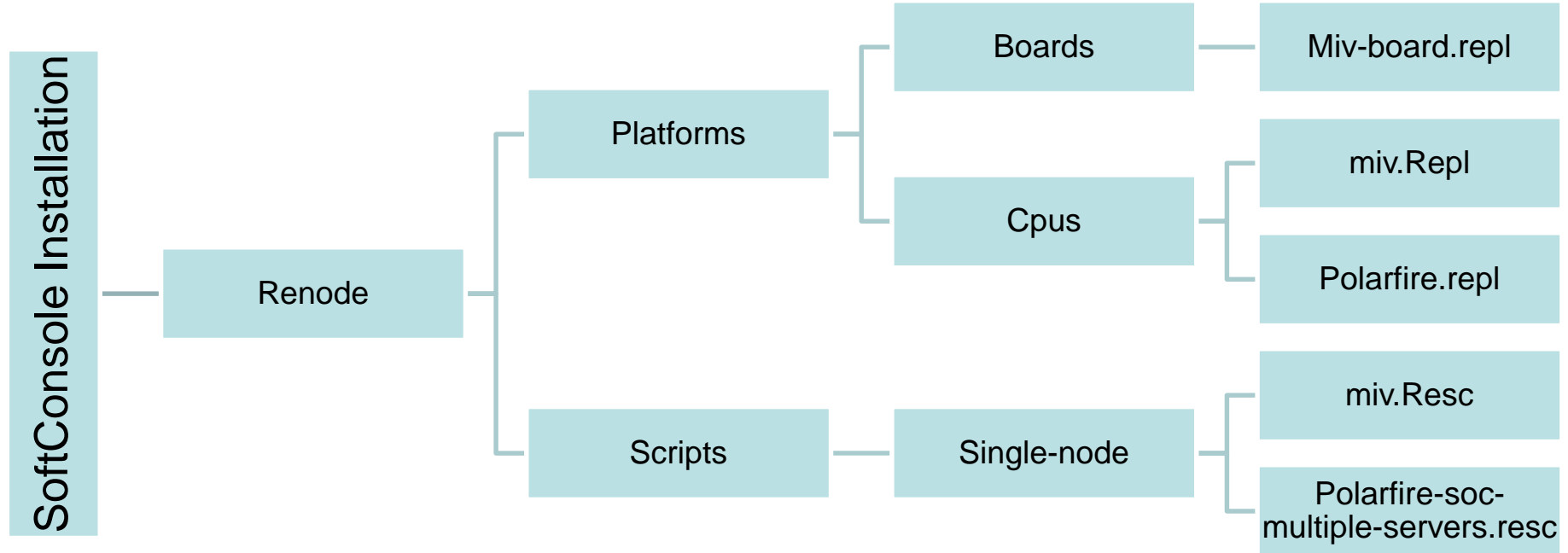
# Summary



# Summary



# Summary



# Summary

1. **Launch the Renode external tool configuration**
2. **Renode starts**
  - A. Loads the script file passed to it as an argument
  - B. Script creates a machine
  - C. Script tells Renode to load a board file
  - D. Board file tells Renode to load a CPU file
  - E. Renode loads the CPU file
  - F. Renode loads the board file
  - G. Script tells Renode to start the GDB server
  - H. Script tells Renode to print the started message in the console
3. **SoftConsole starts GDB**

```
(monitor) 1 $CWD/./scripts/single-node/miv-basic.resc
Available peripherals:

sysbus (SystemBus)
├─ clint (CoreLevelInterruptor)
│   <0x44000000, 0x4400FFFF>
├─ cpu (RiscV32)
│   Slot: 0
├─ ddr (MappedMemory)
│   <0x80000000, 0x83FFFFFF>
├─ flash (MappedMemory)
│   <0x60000000, 0x6003FFFF>
├─ gpioInputs (MiV_CoreGPIO)
│   <0x70002000, 0x700020A3>
│   └─ user_switch_0 (Button)
│       Address: 0
│   └─ user_switch_1 (Button)
│       Address: 1
│   └─ user_switch_2 (Button)
│       Address: 2
├─ gpioOutputs (MiV_CoreGPIO)
│   <0x70005000, 0x700050A3>
│   └─ led0 (LED)
│       Address: 0
│   └─ led1 (LED)
│       Address: 1
│   └─ led2 (LED)
│       Address: 2
```

Launch Script

CPU File

Board File

# Summary: Available Peripherals Mi-V system

---

Memory	Cores	Peripherals
DDR	RV32G	CoreUART
Flash		PLIC
		CLINT
		CoreGPIO
		CoreTimer



# Summary: Available Peripherals PolarFire SoC system

Cores	Memory	Peripherals	Peripherals contd.
RV64IMAC	DDR	CLINT	Cadence GEM (MAC)
RV64GC	Flash	PLIC	PSE GPIO
	PSE eNVM	NS16550 UART	PSE RTC
		PSE SD Controller	PSE Timer
		PSE SPI	PSE USB
		PSE I2C	PSE PCI
		PSE CAN	



# **Debugging Adding Peripherals**



# Debugging Adding Peripherals

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer

- Renode
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    - boards
      - silabs
        - arduino\_101-shield.repl
        - colibri-vf611.repl
        - maris\_zx3-externals.repl
        - maris\_zx3.repl
        - miv-board.repl
        - miv-board-additional-
        - miv-board.repl
        - quark\_c1000-cc2520.repl
        - stm32f4\_discovery-adv
        - stm32f4\_discovery-bb
        - stm32f4\_discovery-kit
        - stm32f4\_discovery.repl
        - stm32f7\_discovery-bb
        - tegra\_externals.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress-externals.repl
        - vexpress.repl
        - zedboard-externals.repl
        - zedboard.repl
      - cpus
        - silabs
          - a20.repl
          - at91rm9200.repl
          - cc2538.repl
          - i386.repl
          - litex\_vexriscv.repl
          - miv.repl
          - mpc5567.repl

miv.repl

```

1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x40000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x40000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16
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42

```

miv-board.repl

```

1 using "platforms/cpus/miv.repl"
2
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42

```

Renode

**RENODE™**

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

(monitor) i \$CWD/./scripts/single-node/miv-basic.resc

Available peripherals:

```

sysbus (SystemBus)
├── clint (CoreLevelInterruptor)
│   └── <0x40000000, 0x4000FFFF>
├── cpu (RiscV32)
│   └── Slot: 0
├── ddr (MappedMemory)
│   └── <0x80000000, 0x83FFFFFF>
└── uart (MiV_CoreUART)
    └── <0x70001000, 0x70001017>

```

(Mi-V) □

# Debugging Adding Peripherals

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer

Renode

bin

licenses

platforms

boards

silabs

arduino\_101-shield.repl

colibri-v61.repl

mars\_zx3-externals.repl

mars\_zx3.repl

miv-board\_repl

miv-board-additional-

miv-board.repl

quark\_c1000-cc2520.re

stm32f4\_discovery-ack

stm32f4\_discovery-bb.

stm32f4\_discovery-kit

stm32f4\_discovery.repl

stm32f7\_discovery-bb.

tegra\_externals.repl

tegra2.repl

tegra3.repl

versatile.repl

vexpress-externals.repl

vexpress.repl

zedboard-externals.re

zedboard.repl

cpus

silabs

a20.repl

at91rm9200.repl

cc2538.repl

i386.repl

lites\_vexriscv.repl

miv.repl

mpc5567.repl

miv.repl

```
1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x40000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
```

miv-board.repl

```
1 using "platforms/cpus/miv.repl"
2
3
```

```
Renode

RENODE™

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

(mon) i $CWD/./scripts/single-node/miv-basic.resc
There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\boards\miv-board.repl'
Error E25: Could not find suitable constructor for type 'Antmicro.Renode.Peripherals.Timers.MiV_CoreTimer'.
Constructor selection report:

Considering ctor Antmicro.Renode.Peripherals.Timers.MiV_CoreTimer with the following parameters: [Antmicro.Renode.Core.Machine, System.Int64].
Parameter 'machine' of type 'Antmicro.Renode.Core.Machine' filled with default value = 'Mi-V'.
Could not find corresponding attribute for parameter 'clockFrequency' of type 'System.Int64' and it is not a default parameter. Rejecting constructor.
At C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\cpus\miv.repl:17:9:
timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000

(Mi-V)
```

# Debugging Adding Peripherals

1. There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\boards\miv-board.repl'
2. Error E25: Could not find suitable constructor for type 'Antmicro.Renode.Peripherals.Timers.MiV\_CoreTimer'.
  - A. Constructor selection report:
  - B. Considering ctor Antmicro.Renode.Peripherals.Timers.MiV\_CoreTimer with the following parameters: [Antmicro.Renode.Core.Machine, System.Int64].
  - C. Parameter 'machine' of type 'Antmicro.Renode.Core.Machine' filled with default value = 'Mi-V'.
  - D. Could not find corresponding attribute for parameter 'clockFrequency' of type 'System.Int64' and it is not a default parameter. Rejecting constructor.
  - E. At C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\cpus\miv.repl:17:9:
  - F. timer0: Timers.MiV\_CoreTimer @ sysbus 0x70003000

SC workspace.examples - Renode/platforms/cpus/miv\_repl - Microsemi SoftConsole v6.0.0.116

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```
Project Explorer
└─ Renode
  └─ platforms
    └─ boards
      └─ cpus
        └─ silabs
          └─ miv_repl
            └─ miv.repl

miv.repl
1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x4000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
17
18
```

```
miv_repl
1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x4000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
17   clockFrequency: 66000000
18
```

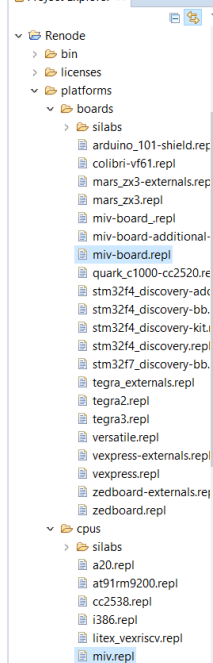
# Debugging Adding Peripherals

workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

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Project Explorer



miv-board.repl

```
1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x40000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
17   clockFrequency: 66000000
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
```

miv-board.repl

```
1 using "platforms/cpus/miv.repl"
```

```
2
3
4
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8
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38
39
40
41
```

Renode

## RENODE™

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

(monitor) i \$CWD/./scripts/single-node/miv-basic.resc  
Available peripherals:

sysbus (SystemBus)

├ clint (CoreLevelInterruptor)

└ <0x44000000, 0x4400FFFF>

├ cpu (RiscV32)

└ Slot: 0

├ ddr (MappedMemory)

└ <0x80000000, 0x83FFFFFF>

├ timer0 (MiV\_CoreTimer)

└ <0x70003000, 0x7000301B>

└ uart (MiV\_CoreUART)

└ <0x70001000, 0x70001017>

(Mi-V) █

# Debugging Adding Peripherals

SC workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

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Quick Access

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        - colibri-v61.repl
        - mars\_zx3-externals.repl
        - mars\_zx3.repl
        - miv-board.repl
        - miv-board-additional-uart.repl
        - miv-board.repl
        - quark\_c1000-cc2520.repl
        - stm32f4\_discovery-additional\_gp.repl
        - stm32f4\_discovery-bb.repl
        - stm32f4\_discovery-kit.repl
        - stm32f4\_discovery.repl
        - stm32f7\_discovery-bb.repl
        - tegra\_externals.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress-externals.repl
        - vexpress.repl
        - zedboard-externals.repl
        - zedboard.repl
      - cpus
        - silabs
          - a20.repl
          - at91rm9200.repl
          - cc2538.repl
          - i386.repl
          - litex\_vexriscv.repl
          - miv.repl
          - mpc5567.repl

```

1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x4000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x40000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70001000
17   clockFrequency: 66000000
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41

```

miv-board.repl

```

1 using "platforms/cpus/miv.repl"
2

```

Renode

RENODE™

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

```

(monitor) i $CWD/./scripts/single-node/miv-basic.resc
There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\boards\miv-board.repl'
Error E39: Exception was thrown during registration of 'timer0 in 'sysbus':
Could not register Given address <0x70001000, 0x7000101B> for peripheral Antmicro.Renode.Peripherals.Timers.MiV_CoreTimer conflicts with address <0x70001000, 0x70001017> of peripheral Antmicro.Renode.Peripherals.UART.MiV_CoreUART in address.
At C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\cpus\miv.repl:17:32:
timer0: Timers.MiV_CoreTimer @ sysbus 0x70001000
^
(Mi-V)

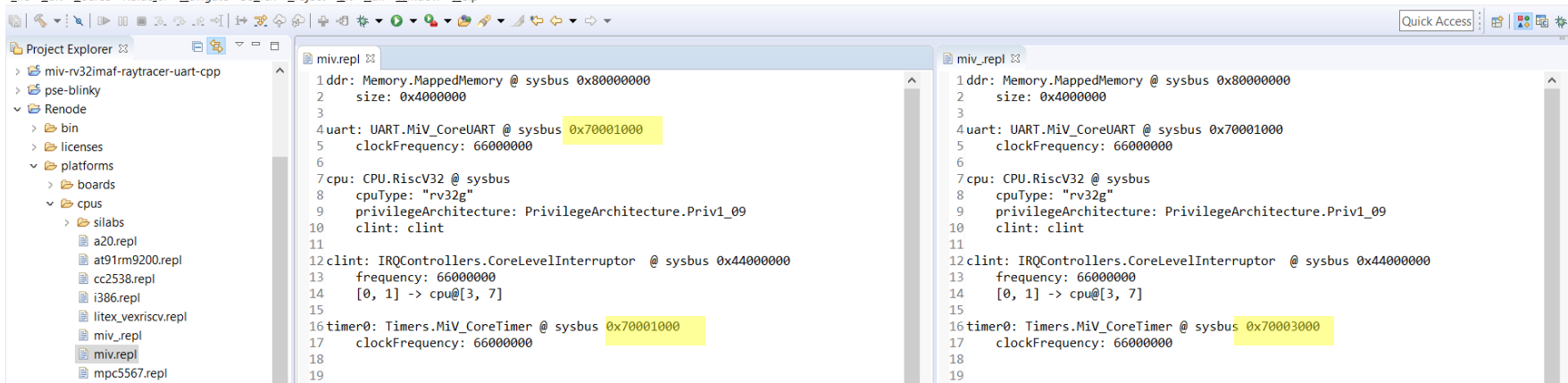
```

# Debugging Adding Peripherals

1. There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\boards\miv-board.repl'
2. Error E39: Exception was thrown during registration of 'timer0 in 'sysbus':
  1. Could not register Given address <0x70001000, 0x7000101B> for peripheral Antmicro.Renode.Peripherals.Timers.MiV\_CoreTimer conflicts with address <0x70001000, 0x70001017> of peripheral Antmicro.Renode.Peripherals.UART.MiV\_CoreUART in address.
  2. At C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\cpus\miv.repl:17:32:
  3. timer0: Timers.MiV\_CoreTimer @ sysbus 0x70001000

SC workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

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The screenshot shows the Renode IDE interface. On the left is the Project Explorer showing the file structure. The main editor displays the content of 'miv.repl'. Two instances of the file are open, showing the same code. The code defines hardware components for a system. The conflict highlighted in the error message is visible in both files: the UART peripheral is located at 0x70001000, and the timer0 peripheral is also located at 0x70001000.

```

1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x4000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70001000
17   clockFrequency: 66000000
18
19
  
```



# Debugging Adding Peripherals

workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

File Edit Source Refactor Navigate Search Project Git Run Window Help

Project Explorer

- Renode
  - bin
  - licenses
  - platforms
    - boards
      - silabs
        - arduino\_101-shield.repl
        - colibri-vf61.repl
        - mars\_zx3-externals.repl
        - mars\_zx3.repl
        - miv-board.repl
        - miv-board-additional-
        - miv-board.repl
        - quark\_c1000-cc2520.re
        - stm32f4\_discovery-adv
        - stm32f4\_discovery-bb
        - stm32f4\_discovery-kit
        - stm32f4\_discovery.repl
        - stm32f7\_discovery-bb
        - tegra\_externals.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress-externals.repl
        - vexpress.repl
        - zedboard-externals.re
        - zedboard.repl
      - cpus
        - silabs
          - a20.repl
          - at91rm9200.repl
          - cc2538.repl
          - i386.repl
          - litex\_vexriscv.repl
          - miv.repl

```

1 ddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x40000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu@[3, 7]
15
16 timer0: Timers.MiV_CoreTimer @ sysbus 0x70003000
17   clockFrequency: 66000000
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
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37
38
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40
41

```

```

1 using "platforms/cpus/miv.repl"
2
3
4
5
6
7
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11
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```

Renode

## RENODE™

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

(monitor) i \$CWD/./scripts/single-node/miv-basic.resc  
Available peripherals:

sysbus (SystemBus)

├ clint (CoreLevelInterruptor)

├─ <0x44000000, 0x4400FFFF>

├ cpu (RiscV32)

├─ Slot: 0

├ ddr (MappedMemory)

├─ <0x80000000, 0x83FFFFFF>

├ timer0 (MiV\_CoreTimer)

├─ <0x70003000, 0x7000301B>

└ uart (MiV\_CoreUART)

└─ <0x70001000, 0x70001017>

(Mi-V) □

# Debugging Adding Peripherals

SC workspace.examples - Renode/platforms/boards/miv-board.repl - Microsemi SoftConsole v6.0.0.116

File Edit Source Refactor Navigate Search Project Git Run Window Help

Project Explorer

- Renode
  - bin
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  - platforms
    - boards
      - silabs
        - arduino\_101-shield.repl
        - colibri-vf61.repl
        - mars\_zx3-externals.repl
        - mars\_zx3.repl
        - miv-board.repl
        - miv-board-additional-uart.repl
        - miv-board.repl
        - quark\_c1000-cc2520.repl
        - stm32f4\_discovery-bb.repl
        - stm32f4\_discovery-kit.repl
        - stm32f4\_discovery.repl
        - stm32f7\_discovery-bb.repl
        - tegra\_externals.repl
        - tegra2.repl
        - tegra3.repl
        - versatile.repl
        - vexpress-externals.repl
        - vexpress.repl
        - zedboard-externals.repl
        - zedboard.repl
      - cpus
        - silabs
          - a20.repl
          - at91rm9200.repl
          - cc2538.repl
          - i386.repl
          - litex\_vexriscv.repl
          - miv.repl
          - mpc5567.repl

```
miv.repl
1 lddr: Memory.MappedMemory @ sysbus 0x80000000
2   size: 0x4000000
3
4 uart: UART.MiV_CoreUART @ sysbus 0x70001000
5   clockFrequency: 66000000
6
7 cpu: CPU.RiscV32 @ sysbus
8   cpuType: "rv32g"
9   privilegeArchitecture: PrivilegeArchitecture.Priv1_09
10  clint: clint
11
12 clint: IRQControllers.CoreLevelInterruptor @ sysbus 0x44000000
13   frequency: 66000000
14   [0, 1] -> cpu[3, 7]
15
16 gpioOutputs: GPIOPort.MiV_CoreGPIO @ sysbus 0x70005000
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
32
33
34
35
36
37
38
39
40
41
```

```
miv-board.repl
1 using "platforms/cpus/miv.repl"
2
3 gpioOutputs:
4   0 -> led0@0
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
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```

Renode

RENODE™

Renode, version 1.6.0.30082 (3b6a18a4-201811221641)

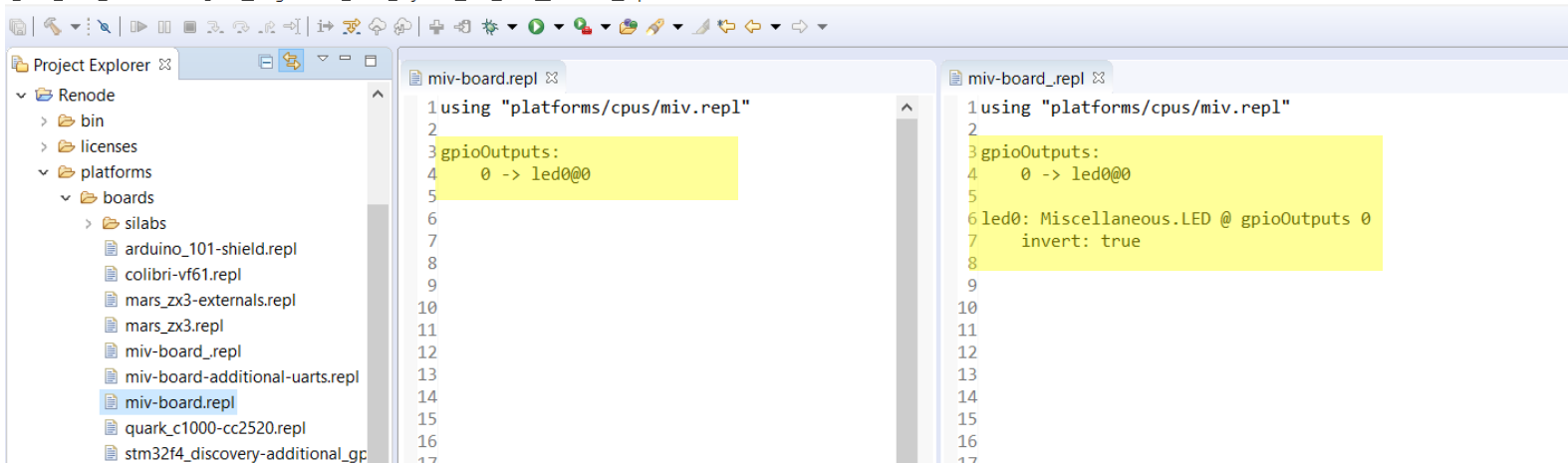
```
(monitor) i $CWD/./scripts/single-node/miv-basic.resc
There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\boards\miv-board.repl'
Error E11: Irq destination 'led0' does not exist.
At C:\Microsemi\SoftConsole_v6.0.0.0\renode\platforms\boards\miv-board.repl:4:10:
    0 -> led0@0
    ****
(Mi-V)
```

# Debugging Adding Peripherals

1. There was an error executing command 'machine LoadPlatformDescription C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\boards\miv-board.repl'
2. **Error E11: Irq destination 'led0' does not exist.**
  1. At C:\Microsemi\SoftConsole\_v6.0.0.0.0\renode\platforms\boards\miv-board.repl:4:10:
  2. 0 -> led0@@
  3. ^^^

SC workspace.examples - Renode/platforms/boards/miv-board\_repl - Microsemi SoftConsole v6.0.0.116

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The screenshot shows the Renode IDE interface. On the left is the Project Explorer showing the file structure: Renode > bin, licenses, platforms > boards > silabs > miv-board.repl. The main editor displays the contents of miv-board.repl. The code is as follows:

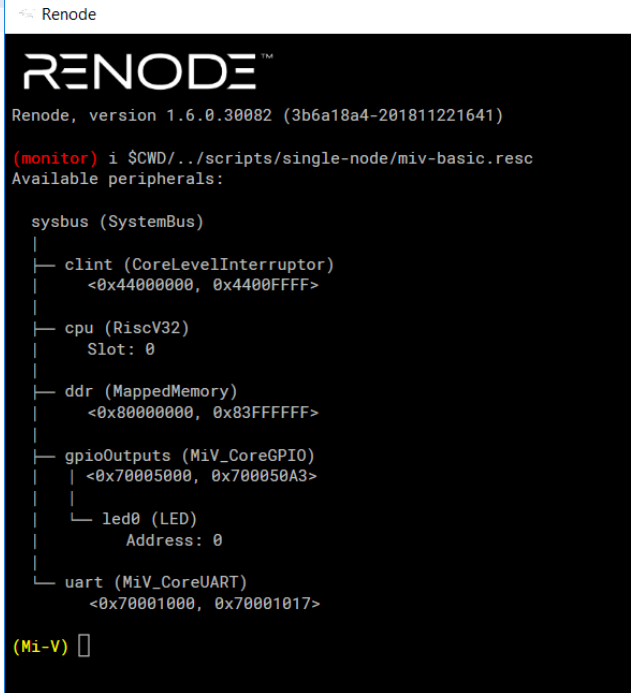
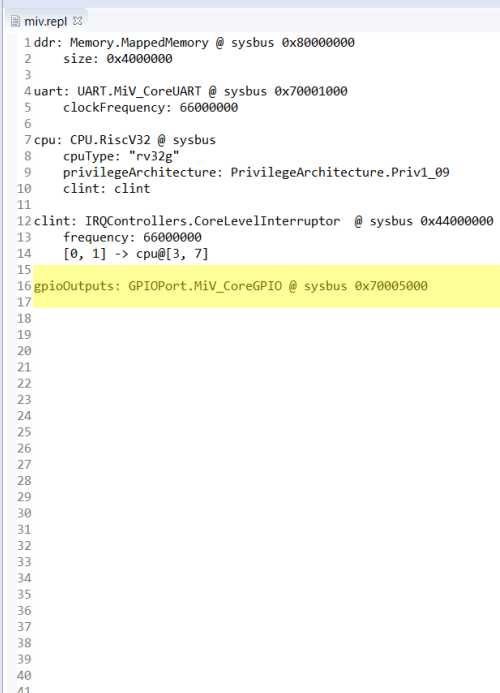
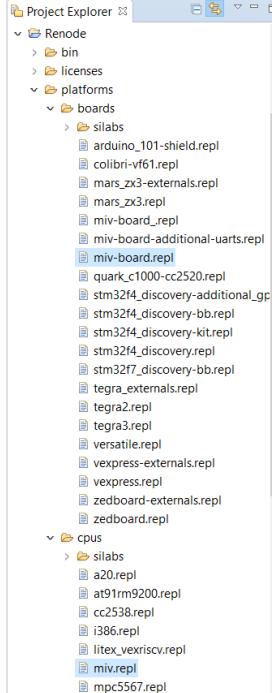
```
1 using "platforms/cpus/miv.repl"
2
3 gpioOutputs:
4   0 -> led0@@
5
6 led0: Miscellaneous.LED @ gpioOutputs 0
7   invert: true
8
9
10
11
12
13
14
15
16
17
```

Yellow highlights in the original image mark the error location: line 4 (0 -> led0@@), line 6 (led0: Miscellaneous.LED @ gpioOutputs 0), and line 7 (invert: true).

# Debugging Adding Peripherals

workspace.examples - Renode/platforms/cpus/miv.repl - Microsemi SoftConsole v6.0.0.116

File Edit Source Refactor Navigate Search Project Git Run Window Help



# First Thursdays

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May 2 - Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

June 6 - Webinar 2: How to Get Started with Renode for PolarFire SoC

July 4 - Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

Aug. 1 - Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

Sept. 5 - Webinar 5: Add and Debug PolarFire SoC Peripherals with Renode

**Oct. 3 - Webinar 6: Add and Debug and Pre-Existing Peripheral in PolarFire SoC**

**Nov. 7 - Webinar 7: How to write custom models – filters, offloading, acceleration etc**

**Dec. 5 - Webinar 8: Handling Binaries**

**Contd.**

# Second Thursdays

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**Jan. 9 - Webinar 9: Run Linux on Renode (PolarFire SoC Model as a Quad-core SMP) – this is not a Linux / Buildroot tutorial**

**Feb. 13 - Webinar 10: Build applications for Linux on PolarFire SoC**

**Mar. 12 - Webinar 11: Introduction to PolarFire SoC MSS Configuration and Software Flow**

**Apr. 9 - Webinar 12: Two baremetal Applications on PolarFire SoC**

**May 14 - Webinar 13: Linux + Real-Time (AMP Mode) on PolarFire SoC**



**Thank You**

