Sub-QML FPGAs Screening Flows

Sub-QML FPGAs are Microchip's radiation-tolerant FPGAs with reduced screening flows available in various packaging options including ceramic and plastic for the most cost-optimized space-flight solutions.

The following table shows all available screening flows for Microchip's RT FPGAs including traditional QML flows: V, E, B, and Sub-QML screening flows: R, Mil-Ceramic, and Mil-Plastic.

Table 1: Sub-QML FPGA Screening Flows

Flow	Purpose	Package	Qualification	Screening			
				Burn-In	Temp Test	Life Test	DPA
V	NSS, NASA Class1	Hermetic Ceramic	QML-V	Static Dynamic	-55°C – 125°C	Wafer-Lot	Assy Lot
E	Advanced Traditional Space	Hermetic Ceramic	QML-Q	Static Dynamic	-55°C – 125°C	Generic Group C	Optional
B	Entry Level Traditional Space	Hermetic Ceramic	QML-Q	Dynamic	-55°C – 125°C	Generic Group C	None
R	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	Dynamic	-55°C – 125°C	None	None
Mil Ceramic	New Space, Strategic Programs	Hermetic Ceramic	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
PROTO	Prototyping	Ceramic (Hermeticity not Guaranteed)	MIL-STD-883 Class B	None	-55°C – 125°C	None	None
Mil Plastic	New Space, Strategic Programs	Plastic Non-Hermetic	JEDEC	None	-55°C – 125°C	None	None

Sub-QML FPGA screening flow options are available for all Microchip radiation-tolerant FPGA families: RTSX-SU, RTAX-S/SL/DSP, RT ProASIC3, RTG4, RT PolarFire, with the exception of the Mil-Plastic flow availability for RTG4 family only. Please note that minimum order quantity (MOQ) and non-cancelable, non-returnable (NCNR) will apply for all Sub-QML devices. The following sections describe each of the Sub-QML screening flow in details:

Reduced Flow, or R-Flow

1. Same test and screening flow as B-flow (no test elimination).
2. TID will be performed on each wafer lot.
3. Solder column testing for Ceramic Column Grid Array (CCGA) packages:
    - Solder column visual inspection criteria is less strict than MIL-STD-883 Class B.
    - Solder column rework is allowed up to 3 times, compared to zero for QML flows.
4. Parts will not be QML compliant and will not be marked with the SMD part number.
5. Requests for Single Lot Date Code (SLDC), specific date codes, single wafer lot, date code restrictions, or specific wafer lots will not be accepted.

6. R-flow paperwork:
    - A system-generated Certificate of Compliance (C of C), which is not hand-signed by Quality Assurance, will ship with the order.
    - No datapack, assembly lot group B data, generic group C nor group D data will be available.
    - No attribute sheet will be available.
7. Terms and Conditions:
    - MOQ of 25 units applies. The entire quantity must be on one line of the PO with one delivery date.
    - Order is non-cancelable and non-returnable.
    - No customer QA or Purchase Order clauses will be reviewed/accepted.
    - No FARs/DFARs will be reviewed/accepted.
    - If programming at the factory is required, the programming files must be supplied at the time of order placement; Microchip cannot reserve inventory or units from lots in process pending receipt of customer programming files.
    - Parts are under the same export control as QML RT FPGAs.

Mil-Ceramic Flow

1. Mil-Ceramic FPGAs are offered in ceramic packages. The hermeticity of the lid seal is guaranteed by Fine and Gross Leak testing, unlike RT PROTO FPGAs which hermeticity is NOT guaranteed.
2. Test and screening for Mil-Ceramic:
    - Parts are tested across the full military temperature range (-55°C to 125°C).
    - No MIL-STD-883 Class B testing is performed.
    - Parts are not subjected to burn-in, temperature cycling, X-ray inspection, PIND testing, assembly lot Group B testing, generic group C, or generic group D.
3. TID will be performed on each wafer lot.
4. Parts will not be QML compliant and will not be marked with the SMD part number.
5. Requests for Single Lot Date Code (SLDC), specific date codes, single wafer lot, date code restrictions, or specific wafer lots will not be accepted.
6. Mil-Ceramic paperwork:
    - A system-generated C of C, which is not hand-signed by Quality Assurance, will ship with the order.
    - No datapack will be available.
    - No attribute sheet will be available.
7. Terms and Conditions:
    - MOQ of 25 units applies. The entire quantity must be on one line of the PO with one delivery date.
    - Order is non-cancelable and non-returnable.
    - No customer QA or Purchase Order clauses will be reviewed/accepted.
    - No FARs/DFARs will be reviewed/accepted.
    - If programming at the factory is required, the programming files must be supplied at the time of order placement; Microchip cannot reserve inventory or units from lots in process pending receipt of customer programming files.
    - Parts are under the same export control as QML RT FPGAs.

Mil-Plastic Flow for RTG4

1. RTG4 plastic FPGAs are offered in a non-hermetic flip-chip plastic package with solder balls, FC1657 (lead solder) and FCG1657 (lead-free solder).
2. RTG4 plastic is qualified under JEDEC, and not MIL-STD-883 Class B. Once qualification completes, a qualification summary can be provided upon request.
3. Test and screening for RTG4 plastic:
    - Parts are tested across the full military temperature range (-55°C to 125°C).
    - No MIL-STD-883 Class B testing is performed.
    - Parts are not subjected to burn-in, temperature cycling, X-ray inspection, PIND testing, fine and gross leak, assembly lot Group B testing, generic group C, or generic group D.
2. TID will be performed on each wafer lot.
4. Parts will not be QML compliant and will not be marked with the SMD part number.
5. Requests for Single Lot Date Code (SLDC), specific date codes, single wafer lot, date code restrictions, or specific wafer lots will not be accepted.
6. RTG4 plastic paperwork:
    - A system-generated C of C, which is not hand-signed by Quality Assurance, will ship with the order.
    - No datapack will be available.
    - No attribute sheet will be available.
7. Terms and Conditions:
    - MOQ of 100 units applies. Lower quantity available for engineering models and PROTO version of RTG4 plastic. The entire quantity must be on one line of the PO with one delivery date.
    - Order is non-cancelable and non-returnable.
    - No customer QA or Purchase Order clauses will be reviewed/accepted.
    - No FARs/DFARs will be reviewed/accepted.
    - If programming at the factory is required, the programming files must be supplied at the time of order placement; Microchip cannot reserve inventory or units from lots in process pending receipt of customer programming files.
    - Parts are under the same export control as QML RTG4 FPGAs.

Revision History

Revision 2.0

Revision 2.0 was published in October 2020.
Removed the RGA criteria for RTG4 in R-flow.
Updated the statement about hermeticity of the lid seal for Mil-Ceramic flow.
Updated Mil-Ceramic and Mil-Plastic flows to state that TID will be performed on each wafer lot.
Added NCNR to terms and conditions for each of the Sub-QML screening flows.

Revision 1.0

Revision 1.0 was published in February 2020. It is the first publication of this document.