PO0145

Product Overview

Radiation-Tolerant PolarFire FPGA

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in October 2019. It was the first publication of this document.

2 Overview

Radiation-Tolerant (RT) PolarFire FPGAs are derived from PolarFire, the fifth-generation family of non-volatile FPGA devices from Microchip, built on 28nm process technology. RT PolarFire FPGAs deliver the lowest power at high density, and integrate the industry's lowest power FPGA fabric. RT PolarFire also provides the lowest power transceiver lanes in the 10 Gbps range, built-in low power dual PCI Express Gen2 (EP/RP), and an integrated low-power crypto coprocessor. RT PolarFire FPGAs can operate at 1.0 V and 1.05 V core voltage, offering the end user the ability to trade off power and performance to match the application requirements.

RT PolarFire uses the same silicon design as commercial PolarFire FPGAs, with modifications to the flip-chip bump spacing to facilitate integration into hermetically-sealed ceramic packages. The choice of a hermetically-sealed ceramic package enables a path to QML class Q and QML class V qualification.

This document describes the features of the RT PolarFire FPGAs. Please refer to the datasheet for current silicon status and electrical characteristics.

2.1 Summary of Features

- 481K logic elements consisting of a 4-input look-up table (LUT) with a fractureable D-type flip-flop
- 20 Kb dual- or two-port large static random access memory (LSRAM) block with built-in single error correct double error detect (SECDED)
- 64 × 12 two-port µRAM block implemented as an array of latches
- 18 × 18 math block with a pre-adder, a 48-bit accumulator, and an optional 16 deep x 18 coefficient ROM
- Built-in µPROM, modifiable at program time, readable at run time for user data storage
- High-speed serial connectivity with built-in, multi-gigabit, multi-protocol transceivers from 250 Mbps to 10.3125 Gbps
- Integrated dual PCIe for up to ×4 Gen2 endpoint (EP) and root port (RP) designs
- High-speed I/O (HSIO) supporting up to 1333 Mbps DDR4, 1067 Mbps DDR3L, and 1067 Mbps DDR3 memories with integrated I/O digital logic
- General purpose I/O (GPIO) supporting 2.5 V, built-in CDR for serial gigabit Ethernet, 800 Mbps DDR3, and 1250 Mbps LVDS I/O speed with integrated I/O digital logic
- Low-power phase-locked loops (PLLs) and delay-locked loops (DLLs) for high precision and low jitter
- 1.0 V and 1.05 V operating modes
- Hermetically-sealed flip-chip ceramic column grid array and ceramic land grid array packages
- Path to Mil Std 883 class B, QML class Q, and QML class V qualification

2.1.1 Radiation Features

- Maintains datasheet parameters at 100 krad total ionizing dose
- Total ionizing dose test reports available for each wafer lot
- Immune to radiation-induced configuration upsets to beyond 80 MeV.cm^2/mg
- Single-event latch-up threshold >80 MeV.cm^2/mg (1.8 V I/Os), >60 MeV.cm^2/mg (2.5 V I/Os)
- Single-event upset protection in fabric flip-flops can be instantiated by synthesis tools
- Built-in SECDED and memory interleaving on LSRAMs
- System controller suspend mode protects against radiation single-event upsets

2.1.2 Low-Power Features

- Low device static power
- Low inrush current
- Low power transceivers

2.1.3 Security Features

- Cryptography Research Incorporated (CRI) patented differential power analysis (DPA) bitstream protection
- Integrated physically unclonable function (PUF)
- 56 KB of secure non-volatile memory (sNVM)
- Built-in tamper detectors and countermeasures
- Digest integrity check for FPGA, µPROM, and sNVM
- Data security features in S devices—true random number generator, integrated Athena TeraFire EXP5200B crypto coprocessor, suite B capable, and CRI DPA countermeasure pass-through license

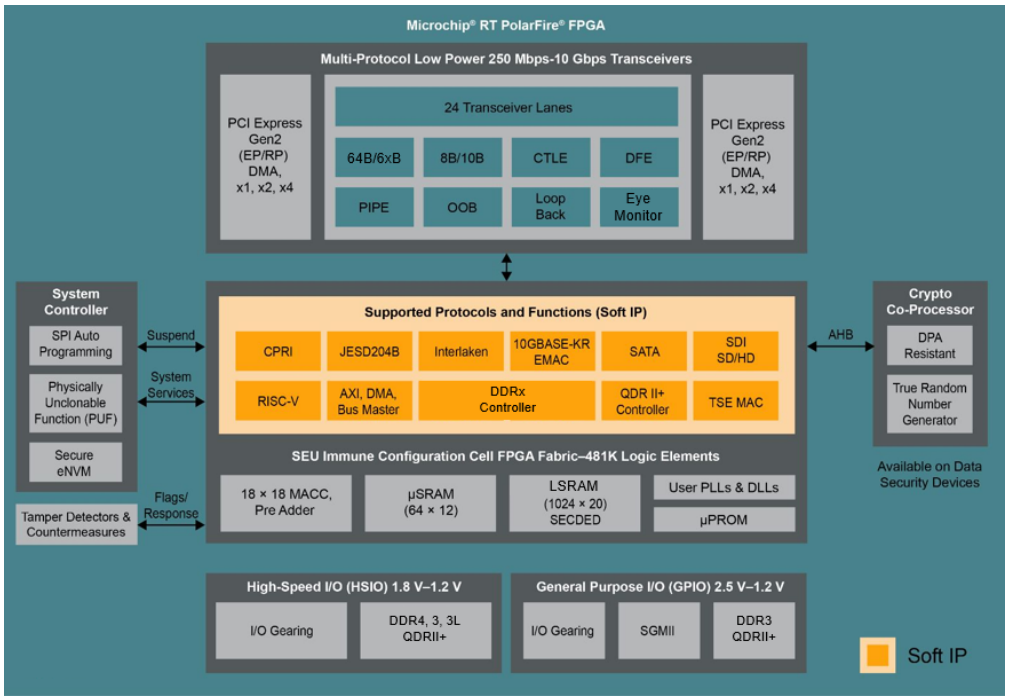
2.1.4 Libero ® SoC FPGA Toolset

- Complete FPGA and embedded software development environment
- Includes Synplify Pro synthesis and Mentor ModelSim ME simulation

2.2 Block Diagram

The following illustration shows the functional blocks of the RT PolarFire FPGA.

Figure 1 • RT PolarFire FPGA Block Diagram



2.3 Product Family Table

The following table lists the product and packaging overview of the RT PolarFire FPGA product family.

Table 1 • RT PolarFire FPGA Product Family

Features		RTPF500T, RTPF500TL, RTPF500TS, RTPF500TLS
FPGA fabric	K Logic elements (4 LUT + DFF)	481
	Math blocks (18 x 18 MACC)	1480
	LSRAM blocks (20 kb)	1520
	µSRAM blocks (64 x 12)	4440
	Total RAM (Mb)	33
	µPROM (Kb 9-bit bus)	513
	sNVM (KB)	56
	User DLLs/PLLs	8
High-speed I/O	250 Mbps to 10.3125 Gbps transceiver lanes	24
	PCIe Gen2 endpoints/ root ports	2
Total I/Os	Total user I/Os	584
	HSIO	324
	GPIO	260
Packaging	CG1509, LG1509 1.0 mm 40 mm x 40 mm	584

Notes:

- TS and TLS FPGAs contain an Athena™ TeraFire F5200B crypto coprocessor.

3 Non-Volatile FPGA Fabric

The non-volatile FPGA fabric is built on a 28nm low-power, non-volatile process technology. The RT PolarFire FPGA fabric is composed of the following building blocks:

- Logic element
- On-chip memory (LSRAM, µSRAM, sNVM, and µPROM)
- Math block

The FPGA fabric configuration cells are SEU immune, and are used to configure I/Os and other aspects of the device. Non-volatile FPGAs do not require the configuration process inherent in SRAM FPGAs. Non-volatile FPGAs power up quickly like an ASIC with minimal inrush current, and are ideal for root-of-trust, first-up functionality in any system.

3.1 Logic Element

The 4-input LUT can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with a carry input to generate the sum output.

The logic element has the following features:

- A fully permutable 4-input LUT optimized for lowest power
- A dedicated carry chain based on a carry look-ahead technique
- A separate flip-flop that can be used independently from the LUT

3.2 On-Chip Memory

RT PolarFire FPGAs integrate four different types of memories that allow the designer to optimize for power, functionality, and area. Two memory types are volatile, and two memory types are non-volatile.

Volatile memories include:

- LSRAM
- µSRAM

The LSRAMs are 20 Kb SRAMs with a built-in SECDED and interleaving to prevent multi-bit upsets (MBUs). The µSRAMs are small distributed 64 x 12 RAMs, well suited for efficient implementation of small buffers, thereby reserving LSRAM usage for the wider and deeper memories.

Non-volatile memories (NVMs) include:

- µPROM
- sNVM

The µPROM, constructed of SEU-immune FPGA configuration non-volatile cells, is readable at runtime and writable during device programming. It provides users with SEU-immune parameters, constants, IDs, and parametric or initialization data. The sNVM is accessible through system service calls. Data written to the sNVM can be protected by the PUF. The sNVM is readable and writable by the designer's application during runtime and is an ideal storage location for the boot code for soft processors and user keys.

3.3 LSRAM

Each LSRAM block consists of 20,480 bits of RAM and includes functionality to support dual-port and two-port modes. There are numerous configurations and features for each block. The Libero SoC toolset has an LSRAM configurator that provides automated combining and cascading of several LSRAM blocks into larger memories.

LSRAM features include:

- Up to 385 MHz operation
- True dual-port memory
- Two-port memory (one dedicated write port, one dedicated read port)
- Data widths of ×1, ×2, ×5, ×10, ×20, ×40, and ×33 with SECDED enabled
- Multi-bit upset mitigation
- Synchronous operation
- Independent port clocks
- Byte enables
- Registered inputs
- Output registers with separate enables and synchronous resets
- Read enables to conserve power while retaining output data
- Power switch to minimize static power when the LSRAM is not used
- Fast zeroization mode

3.3.1 Dual-Port Mode

In dual-port mode, the width of both ports is less than 33 and the ports are independent of each other. The write and read operations can occur independently of each other, at any location. On write collisions, while the write operations occur correctly, the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data correctly.

3.3.2 Two-Port Mode

In two-port mode, at least one port has a width of 32 or 40 (or 33 with SECDED). Port A is dedicated for reads and port B for writes.

The following illustration shows port widths in various modes.

Figure 2 • LSRAM Dual- and Two-Port Configurations

	Port A Width						
Port B Width	x1/x1	x1/x2	x1/x4	x1/x8	x1/x16	W1/R32	N/A
	x2/x1	x2/x2	x2/x4	x2/x8	x2/x16	W2/R32	N/A
	x4/x1	x4/x2	x5/x5	x5/x10	x5/x20	W5/R40	N/A
	x8/x1	x8/x2	x10/x5	x10/x5	x10/x20	W10/R40	N/A
	x16/x1	x16/x2	x20/x5	x20/x10	x20/x20	W20/R40	N/A
	W32/R1	W32/R2	W40/R5	W40/R10	W40/R20	W40/R40	N/A
	N/A	N/A	N/A	N/A	N/A	N/A	Wx33/R33

Dual Port
Two Port
Two Port SECDED

3.4 µSRAM

The µSRAM is a two-port memory embedded in the FPGA fabric, which is provided for an efficient low-power implementation for small buffers. On write collisions, the write operations occur correctly, while the read operations can return ambiguous results while the write completes. After completing the write operation, the read data reads the newly written write data.

The following are key features of the µSRAM block:

- Up to 430 MHz operation
- Two-port memory with 64 words of 12 bits
- The write port operates synchronously
- The write port has a fixed width
- The read port operates asynchronously and supports synchronous and pipeline operations with the FPGA fabric flip-flops
- The Libero SoC toolset provides automated combining and cascading for larger memories
- Multiple memory blocks can be combined to extend the depth or width
- Provides a state-keeping, low-power suspend mode
- Implemented as an array of latches

3.5 µPROM

The µPROM is a single monolithic non-volatile memory that provides a PROM-like storage for a variety of purposes, including but not limited to: initialization data for other memories, user calibration data, and so on. The memory cells are constructed from the FPGA configuration cells and are updated when the device is programmed.

The following are key features of the µPROM:

- 10 ns read access time
- Programmed with the FPGA bitstream
- Asynchronous or synchronous read access mode from the FPGA fabric

3.6 sNVM

Each RT PolarFire FPGA has 56 KB of sNVM. The sNVM is organized into 221 pages of 236 or 252 bytes, depending on whether the data is stored as plain text or encrypted/authenticated data. It is accessible to users through system services calls to the RT PolarFire FPGA system controller. Pages within the sNVM can be marked as ROM during bitstream programming. The sNVM content can be used to initialize LSRAM and µSRAMs with secure data. The sNVM is only accessible through system service calls. Data written to the sNVM can be protected by the PUF.

3.7 Math Block

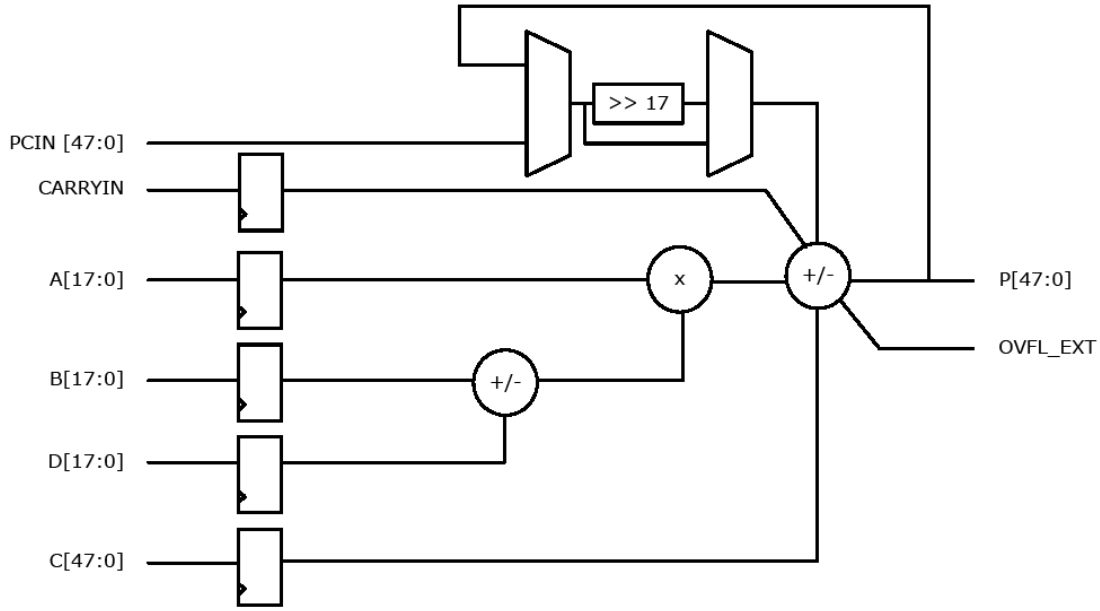
The fundamental building block in any digital signal processing algorithm is the multiply-accumulate (MACC) operation. RT PolarFire FPGAs implement a custom 18 x 18 MACC block for an efficient low-power implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast fourier transform (FFT) for filtering and image processing applications. An optional 16-word coefficient ROM can be constructed from logic elements located near the math block.

The following are key features of the math block functionality:

- Up to 450 MHz operation
- 18 × 18 two's complement multiplier accumulator with an output width of 48 bits
- Power-saving pre-adder to optimize linear phase FIR filter applications and reduce the math block usage
- Optional pipelining and dedicated buses for cascading
- Dot-product mode for complex multiplies

The following illustration shows the functional blocks of the math block.

Figure 3 • Math Block



4 Clock Management

In each RT PolarFire FPGA, there are eight DLLs and eight PLLs to provide flexible clock generation and management capabilities. In addition to these DLLs and PLLs, up to 15 transceiver lane transmit PLLs are also available.

The following are key highlights of the clock management architecture:

- High-speed buffers and routing for low-skew clock distribution
- Frequency synthesis and phase shifting
- Low-jitter clock generation and jitter filtering

4.1 DLL

The DLL provides a calculated PVT compensated delay to the I/O's digital delay lines as well as delay or phase-shifted clocks to the FPGA fabric.

The following are the major modes to which the DLL can be configured.

- Time reference mode—the DLL takes a single clock as an input and determines how many delay line buffer taps are required for a signal to pass through them to rotate a signal. The main use of time reference mode is to know how many delay taps are needed to delay the clock by 90 degrees. The value is then provided to the data strobe signal (DQS)/DQSn input signals for double data rate (DDR) memory controllers to delay all DQS/DQSn signals by the required 90-degree phase shift to capture the data from the memory devices. Multiple memory interfaces of the same clock rate can reuse the same DLL with lane level controls for PVT updates.
- Clock injection delay mode—the DLL can be used to compensate for the clock injection delay associated with the source synchronous receive interfaces. The DLL can match delays for the global, regional, and high-speed bank clocks. There are two outputs from the DLL in this mode: a x1 output fixed in time and another output that can be divided by x1, x2, or x4 and can be phase shifted.

4.2 PLL

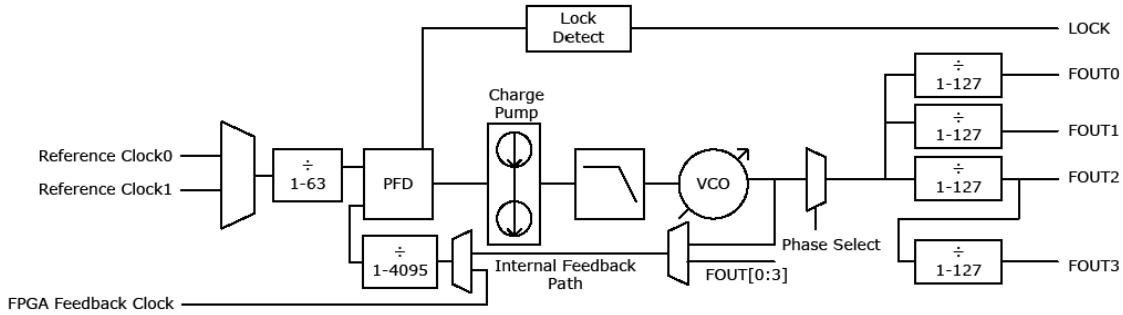
The programmable delta-sigma low-jitter fractional PLLs are multi-function and general purpose frequency synthesizers, as shown in the following illustration. Wide input and output ranges along with the best-in-class jitter performance allow these PLLs to be used for almost any clocking application. With excellent supply noise immunity, the PLL is ideal for use in noisy FPGA environments.

- The PLL output clock is available in eight phases with 45-degree phase differences. All eight phases are selectable to drive four separate outputs from the PLL, where each output can select any of the eight phases independent of other output selections and that each output can also be driven to a zero output when not used.
- Each of the four outputs from the PLL can then be divided independently for any value from 1 to 127. Each of the PLL outputs can have the output divider released by up to seven VCO/4 cycles. The delayed outputs can be set independently for each output clock.
- Fractional-N (24-bit accuracy) capability is added to the feedback divider to have the VCO frequency be a non-integer divide of the reference clock input frequency. The base frequency is applied to all PLL outputs.
- The PLL supports glitch-free start and stop on any one of the four outputs independently by either a register map or a fabric control. This capability also allows the output divider values and the VCO/4 phase selection to be modified glitch-free during the time that the clock is stopped.

- For fine granularity phase control of the PLLs, they can be cascaded with DLLs located near the PLLs, whereby the DLL delay lines can be used in a process, voltage, and temperature (PVT) compensated or non-PVT compensated mode to provide the phase control needed.

The following illustration shows the flow of the PLL functionality.

Figure 4 • PLL Block Diagram



4.3 Clock Network

The clock network is designed to route clocks and asynchronous reset signals to large sections of the fabric with limited skew. On occasion, the network can also be used for other high fanout signals that can tolerate long delays, such as non-timing-critical synchronous enables or resets. There are two main clock networks for the FPGA fabric, global and regional clocks.

4.3.1 Global Clocks

There are 24 clocks on the device with global low skew scope to all synchronous elements. The global can be divided into left and right sides of the device. Thus, the number of globals can increase to 48 total clocks with 24 in the left and 24 in the right.

4.3.2 Regional Clocks

There are up to 38 regional clock domains that interface to the edges of the device. The regional clocks provide a fixed number of logic elements based on the size of the device. Up to 14 clocks are available for the FPGA I/Os and up to 24 clocks for the transceiver lanes, one for each lane direction. These are the fast insertion clock networks used to move data in and out of the fabric.

5 I/Os

RT PolarFire device user I/Os support multiple I/O standards while providing the high bandwidth needed to maximize the internal logic capabilities of the device and achieve the required system-level performance.

5.1 Low-Power High-Speed Transceiver Lane

All RT PolarFire FPGAs contain state-of-the-art low-power transceiver lane capabilities from speeds as low as 250 Mbps up to 10.3125 Gbps. The PMA is designed to support multiple protocols (as listed in the following table) with state-of-the-art control and debug features. PCI Express Gen1 or Gen2 support is provided by a hard macro. All other protocols are implemented with a soft IP. Serial Gigabit Ethernet is also supported with GPIO 2.5 V LVDS differential pairs. A single transmit PLL can provide a high-speed clock up to four transceiver lanes.

Table 2 • Transceiver Lane Protocol Support

Protocol	Data Rate (Gbps)	Channels Bonded
PCIe	2.5, 5	1, 2, 4
Interlaken	6.375	1–16
10GBASE-R/KR	10.3125	1
SGMII/QSGMII	1.25–5	1
XAUI	3.125	4
RXAUI	6.25	2, 3, 4, 6
HiGig/HiGig+/HiGiGII	3.75–4.065	4
CPRI	0.6144–9.83	1
Fiber channel	0.6144–8.5	1
SRIO	1.25–6.3	1, 2, 4, 8
SATA	1.5–6	1
JESD204B	0.5–10.3125	1–4
Display port	2, 5, 8	4
SDI	0.277–6	1

5.1.1 Low-Power Transceiver Lane Features

The following are low-power transceiver lane features:

- Advanced low-power modes
- Programmable transmit amplitude and emphasis control
- Low-speed CDR operation with support for 270 Mbps SMPTE serial line rates
- Continuous time linear equalization (CTLE) and decision feedback equalization (DFE) for long-reach or backplane applications
- Auto-adaption at receiver equalization and integrated eye monitor feature for easy serial link tuning
- Eye monitor and/or equalization can be powered down to reduce power if not needed
- Out-of-band, electrical idle signaling capability for SAS, SATA, and PCIe
- Multiple loopback modes for test and debug
- Transmit jitter attenuation for loop timing applications (SyncE compatible)

- Hot-socketing capable
- IEEE 1149.6 AC JTAG
- Adjacent channel loopback modes allow transceiver lane data streams to remain active during FPGA fabric programming

5.1.2 Transmitter

The transmitter is fundamentally a parallel-to-serial converter with a conversion ratio of 8, 10, 16, 20, 32, 40, 64, or 80 bits. It allows the designer to trade-off data path width for timing margin in high-performance designs. These transmitter outputs drive the PC board with a differential output signal. TX_CLK is the appropriately divided serial data clock available to the fabric, and can be used directly to register the parallel data coming from the internal logic. The transmit parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. The bit-serial output signal drives two package pins with differential signals. The output signal pair supports a wide variety of serial protocols and has programmable signal swing as well as programmable pre- and post-emphasis to compensate for PC board losses and other interconnect characteristics. For shorter channels, the swing can be reduced to lower power consumption. Each transmit lane can be sourced by one of two transmit PLLs. Each transmit PLL can drive up to four transceiver lanes. Transmitter PLLs are state-of-the-art fractional frequency synthesizers with integrated jitter attenuation.

5.1.3 Receiver

The receiver is fundamentally a serial-to-parallel converter with clock recovery changing the incoming bit-serial differential signal into a parallel stream of words of 8, 10, 16, 20, 32, 40, 64, or 80 bits. This allows the FPGA designer to trade off the internal data path width versus logic timing margin. The receiver takes the incoming differential data stream, feeds it through programmable linear and decision feedback equalizers (to compensate for PC board and other interconnect characteristics), and uses the reference clock input to initiate clock recognition. The data pattern uses non-return-to-zero (NRZ) encoding and optionally guarantees sufficient data transitions by using the selected encoding scheme. The outgoing parallel data has additional hardware support for the 8b/10b, 64b/66b, or 64b/67b encoding schemes to provide a sufficient number of transitions. Parallel data is transferred into the FPGA logic using the recovered clock (RX_CLK).

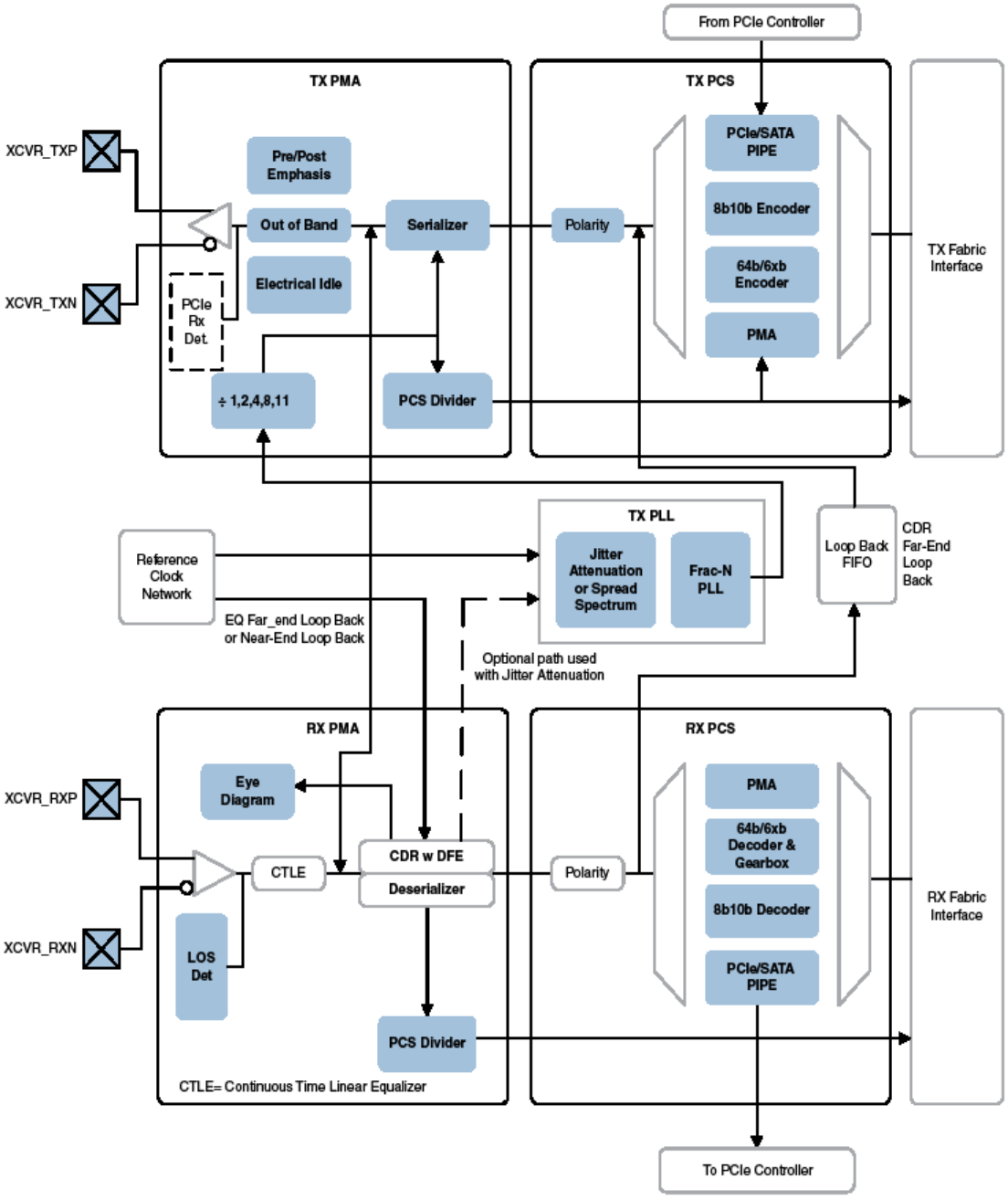
5.1.4 Transceiver Lane Modes

The transceiver lane supports five different modes of operations:

- PMA—direct access to the PMA without any encoding
- 8b/10b—8b/10b encoding/decoding is provided
- 64b/6xb—64b/66b or 64/67b encoding/decoding with gearbox logic is provided
- PIPE—a PIPE interface supporting both PCIe Gen2 and SATA 3.0
- PCIe—direct connection to the embedded PCIe Gen2 controller

The following illustration shows the collaboration of five modes that transceiver lanes support.

Figure 5 • Transceiver Lane Modes

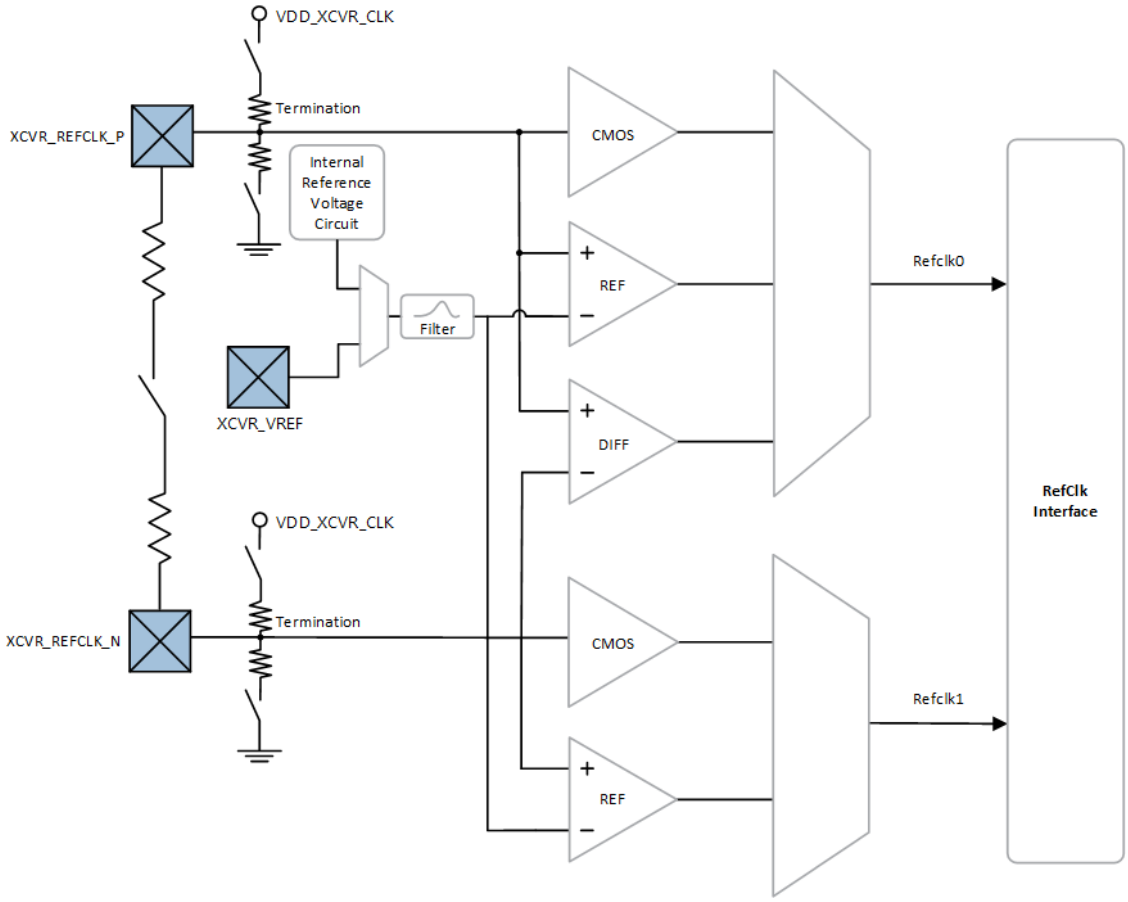


5.1.5 Reference Clock

The reference clock pins allow connections directly with the transceiver lane quads. The reference clock inputs provide flexibility to interface with both single-ended and differential clocks, and can drive up to two independent clocks per transceiver lane quad. These reference clocks can also be sources for the global and regional clock networks in the FPGA fabric of the device.

The following illustration shows the connectivity between the reference clock and transceiver lane quads.

Figure 6 • Reference Clock



5.1.6 Quad Lane Overlay Assignments

The transceiver lane either connects the parallel side of the interface to the PCIe Gen2 controller or to the fabric. The PCIe connections are fixed in the hardware and have a dedicated number of combinations between the two controllers. The fabric interface is used to support the PMA, 8b/10b, 64b/6xb, and PIPE modes and have complete flexibility into the fabric connections.

The following table lists the combinations between the PCIe and fabric controllers.

Table 3 • Quad0 Lane Assignments

PCIe_0 Controller	Quad0 Lane 0	Quad0 Lane 1	Quad0 Lane 2	Quad0 Lane 3	PCIe_1 Controller
x1	PCIe_0	Not available	Not available	PCIe_1	x1
x1	PCIe_0	Unused	PCIe_1	PCIe_1	x2
x2	PCIe_0	PCIe_0	Not available	PCIe_1	x1
x2	PCIe_0	PCIe_0	PCIe_1	PCIe_1	x2

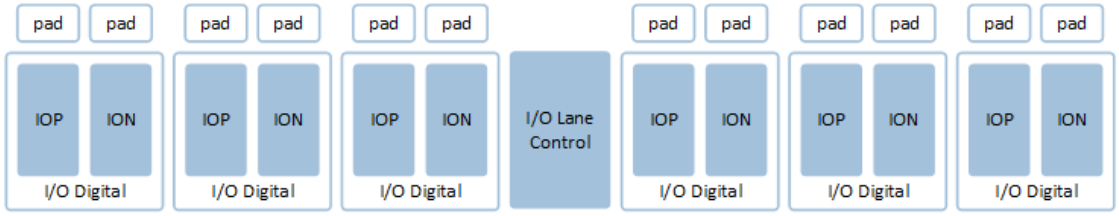
PCIe_0 Controller	Quad0 Lane 0	Quad0 Lane 1	Quad0 Lane 2	Quad0 Lane 3	PCIe_1 Controller
x4	PCIe_0	PCIe_0	PCIe_0	PCIe_0	Unused
x1	PCIe_0	Not available	Fabric	Fabric	Unused
x2	PCIe_0	PCIe_0	Fabric	Fabric	Unused
Unused	Fabric	Fabric	Not available	PCIe_1	x1
Unused	Fabric	Fabric	PCIe_1	PCIe_1	x2
Unused	Fabric	Fabric	Fabric	Fabric	Unused

Note: Fabric includes PMA, 8b/10b, 64b/66b, 64b/67b, and PIPE modes.

5.2 Inputs/Outputs

RT PolarFire FPGA I/Os are grouped into pairs to meet the differential I/O standards. Additionally, they are grouped in lanes of 12 buffers with a lane controller for memory interfaces, as shown in the following illustration.

Figure 7 • I/O Topology



The number of I/O pins varies depending on the device and package size. The persistent I/O feature preserves a state on an I/O without user intervention during programming mode. The RT PolarFire FPGA I/O buffers are constructed from the following main sub modules.

- Transmit buffer (PVT compensated)
- Receive buffer
- Termination (Thevenin, Differential, Up, and Down)
- Weak pull mode logic (Up, Down, and Bus-Hold)

Each I/O is configurable and can comply with a large number of I/O standards. There two types of user I/Os in RT PolarFire FPGAs:

- High-speed I/O (HSIO) optimized for DDR4 memories at speeds up to 1333 Mbps and a maximum voltage of 1.8 V nominal
- GPIO capable of supporting multiple standards up to 2.5 V with an integrated CDR to support SGMII Ethernet applications

5.2.1 Input Buffer Speed

The following tables provide information about input buffer speed.

Table 4 • HSIO Maximum Input Buffer Speed (TBD)

Standard	STD	–1	Unit
LVDS18			Mbps
RSDS18			Mbps
MINILVDS18			Mbps
SUBLVDS18			Mbps
PPDS18			Mbps
SLVS18			Mbps
SSTL18I			Mbps
SSTL18II			Mbps
SSTL15I			Mbps
SSTL15II			Mbps
SSTL135I			Mbps
SSTL135II			Mbps
HSTL15I			Mbps
HSTL15II			Mbps
HSTL135I			Mbps
HSTL135II			Mbps
HSUL18I			Mbps
HSUL18II			Mbps
HSUL12			Mbps
HSTL12			Mbps
POD12I			Mbps
POD12II			Mbps
LVCMOS18 (12 mA)			Mbps
LVCMOS15 (10 mA)			Mbps
LVCMOS12 (8 mA)			Mbps

1. Performance is achieved with VID ≥200 mV.

Table 5 • GPIO Maximum Input Buffer Speed (TBD)

Standard	STD	–1	Unit
LVDS25/LVDS33/LCMDS25/LCMDS33[3]			Mbps
RSDS25/RSDS33[3]			Mbps
MINILVDS25/MINILVDS33[3]			Mbps
SUBLVDS25/SUBLVDS33[3]			Mbps
PPDS25/PPDS33[3]			Mbps
SLVS25/SLVS33[3]			Mbps
SLVSE15			Mbps
HCSL25/HCSL33[3]			Mbps
BUSLVDSE25			Mbps
MLVDSE25			Mbps
LVPECL33[3]			Mbps
SSTL25I			Mbps
SSTL25II			Mbps
SSTL18I			Mbps
SSTL18II			Mbps
SSTL15I			Mbps
SSTL15II			Mbps
HSTL15I			Mbps
HSTL15II			Mbps
HSUL18I			Mbps
HSUL18II			Mbps
PCI			Mbps
LVTTL33[3] (20 mA)			Mbps
LVCMOS33[3] (20 mA)			Mbps
LVCMOS25 (16 mA)			Mbps
LVCMOS18 (12 mA)			Mbps
LVCMOS15 (10 mA)			Mbps
LVCMOS12 (8 mA)			Mbps
MIPI25/MIPI33[3]			Mbps

1. All SSTLD/HSTLD/HSULD/LVSTLD/POD type receivers use the LVDS differential receiver.
2. Performance is achieved with VID ≥200 mV.
3. Designers should familiarize themselves with Single Event Latch-Up risks before selecting 3.3V I/Os. Refer to latest RT PolarFire radiation test data.

5.2.2 Output Buffer Speed

Table 6 • HSIO Maximum Output Buffer Speed (TBD)

Standard	STD	–1	Unit
SSTL18I			Mbps
SSTL18II			Mbps
SSTL18I (differential)			Mbps
SSTL18II (differential)			Mbps
SSTL15I			Mbps
SSTL15II			Mbps
SSTL15I (differential)			Mbps
SSTL15II (differential)			Mbps
SSTL135I			Mbps
SSTL135II			Mbps
SSTL135I (differential)			Mbps
SSTL135II (differential)			Mbps
HSTL15I			Mbps
HSTL15II			Mbps
HSTL15I (differential)			Mbps
HSTL15II (differential)			Mbps
HSTL135I			Mbps
HSTL135II			Mbps
HSTL135I (differential)			Mbps
HSTL135II (differential)			Mbps
HSUL18I			Mbps
HSUL18II			Mbps
HSUL18II (differential)			Mbps
HSUL12			Mbps
HSUL12I (differential)			Mbps
HSTL12			Mbps
HSTL12I (differential)			Mbps
POD12I			Mbps
POD12II			Mbps
LVCMOS18 (12 mA)			Mbps
LVCMOS15 (10 mA)			Mbps
LVCMOS12 (8 mA)			Mbps

Table 7 • GPIO Maximum Output Buffer Speed (TBD)

Standard	STD	–1	Unit
LVDS25/LCMDS25			Mbps
LVDS33/LCMDS33[1]			Mbps
RSDS25			Mbps
MINILVDS25			Mbps
SUBLVDS25			Mbps
PPDS25			Mbps
SLVSE15			Mbps
BUSLVDSE25			Mbps
MLVDSE25			Mbps
LVPECLE33[1]			Mbps
SSTL25I			Mbps
SSTL25II			Mbps
SSTL25I (differential)			Mbps
SSTL25II (differential)			Mbps
SSTL18I			Mbps
SSTL18II			Mbps
SSTL18I (differential)			Mbps
SSTL18II (differential)			Mbps
SSTL15I			Mbps
SSTL15II			Mbps
SSTL15I (differential)			Mbps
SSTL15II (differential)			Mbps
HSTL15I			Mbps
HSTL15II			Mbps
HSTL15I (differential)			Mbps
HSTL15II (differential)			Mbps
HSUL18I			Mbps
HSUL18II			Mbps
HSUL18I (differential)			Mbps
HSUL18II (differential)			Mbps
PCI			Mbps
LVTTL33[1] (20 mA)			Mbps
LVCMOS33[1] (20 mA)			Mbps
LVCMOS25 (16 mA)			Mbps
LVCMOS18 (12 mA)			Mbps
LVCMOS15 (10 mA)			Mbps
LVCMOS12 (8 mA)			Mbps
MIPIE25			Mbps

1. Designers should familiarize themselves with single event latch-up risks before selecting 3.3 V I/Os. Refer to latest RT PolarFire radiation test data.

5.2.3 Maximum PHY Rate for Memory Interface IP

The following tables provide information about the maximum PHY rate for memory interface IP.

Table 8 • Maximum PHY Rate for Memory Interfaces IP for HSIO Banks (TBD)

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR4	8:1	1.8 V	1.2 V				
DDR3	8:1	1.8 V	1.5 V				
DDR3L	8:1	1.8 V	1.35 V				
QDRII+	8:1	1.8 V	1.5 V				
RLDRAM3[1]	8:1	1.8 V	1.35 V				
RLDRAM3[1]	4:1	1.8 V	1.35 V				
RLDRAM3[1]	2:1	1.8 V	1.35 V				
RLDRAM2[1]	8:1	1.8 V	1.8 V				
RLDRAM2[1]	4:1	1.8 V	1.8 V				
RLDRAM2[1]	2:1	1.8 V	1.8 V				

1. RLDRAM2 and RLDRAM3 are not supported with a soft IP controller currently.

Table 9 • Maximum PHY Rate for Memory Interfaces IP for GPIO Banks (TBD)

Memory Standard	Gearing Ratio	V_{DDAUX}	V_{DDI}	STD (Mbps)	–1 (Mbps)	Fabric STD (MHz)	Fabric –1 (MHz)
DDR3	8:1	2.5 V	1.5 V				
QDRII+	8:1	2.5 V	1.5 V				
RLDRAM2[1]	4:1	2.5 V	1.8 V				
RLDRAM2[1]	2:1	2.5 V	1.8 V				

1. RLDRAM2 is currently not supported with a soft IP controller.

The following table lists the GPIO LVTTL or LVCMOS receivers that are also designed to support a limited mixed mode of operation to provide greater board I/O design flexibility. For example, if VDDIO is set to 3.3 V, the I/O receivers can operate at the lower voltage of JEDEC standards.

Table 10 • GPIO Mixed Receiver Mode Operation Capability

VDDIO (V)	LVCMOS33	LVCMOS25	LVCMOS18	LVCMOS15	LVCMOS12
3.3[1]	Yes	Yes	Yes	Not available	Yes
2.5	Yes	Yes	Yes	Yes	Yes
1.8	Yes	Yes	Yes	Yes	Yes
1.5	Yes	Yes	Yes	Yes	Yes
1.2	Yes	Yes	Not available	Yes	Yes

1. Designers should familiarize themselves with single event latch-up risks before selecting 3.3 V I/Os. Refer to latest RT PolarFire radiation test data.

The following table lists the HSIO mixed receiver mode capability.

Table 11 • HSIO Mixed Receiver Mode Capability

VDDIO (V)	LVCMOS18	LVCMOS15	LVCMOS12
1.8	Yes	Yes	Yes
1.5	Yes	Yes	Yes
1.2	Not available	Yes	Yes

5.3 I/O Digital

The RT PolarFire FPGA I/O digital logic is used to interface between the FPGA fabric and the I/O buffers. It interfaces between the high-speed I/O buffers and lower-speed FPGA fabric. The I/O digital block consists of the following:

- A delay chain, for input or output delay
- Registers and control logic for input modes and output modes

The I/O digital registers can be configured for both input and output DDR and shift register modes and combined DDR-shift register modes. It allows gearing up the output data rate and gearing down the input data rate. The RT PolarFire FPGA I/O digital logic works in conjunction with fast and low-skew clock distributions that are optimized for DDR applications, special clock dividers, and other support circuits to guarantee clock domain crossings.

5.3.1 I/O Digital Features

The following are the I/O digital features:

- Programmable input and/or output delay chain
- Data eye monitor for detecting margin to clock edges
- Data eye position optimizer
- Up to 10:1 input deserialization
- Up to 10:1 output serialization
- Support for DDR and SDR interfaces
- Receive slip control to facilitate word alignment
- Fast and low-skew lane clocks per 12 I/Os
- Clock recovery for SGMII and similar interfaces (one per 12 I/Os)

5.3.2 I/O Digital Modes

The following table lists the associated memory interface, I/O data rate, FPGA clock rate, and its applications.

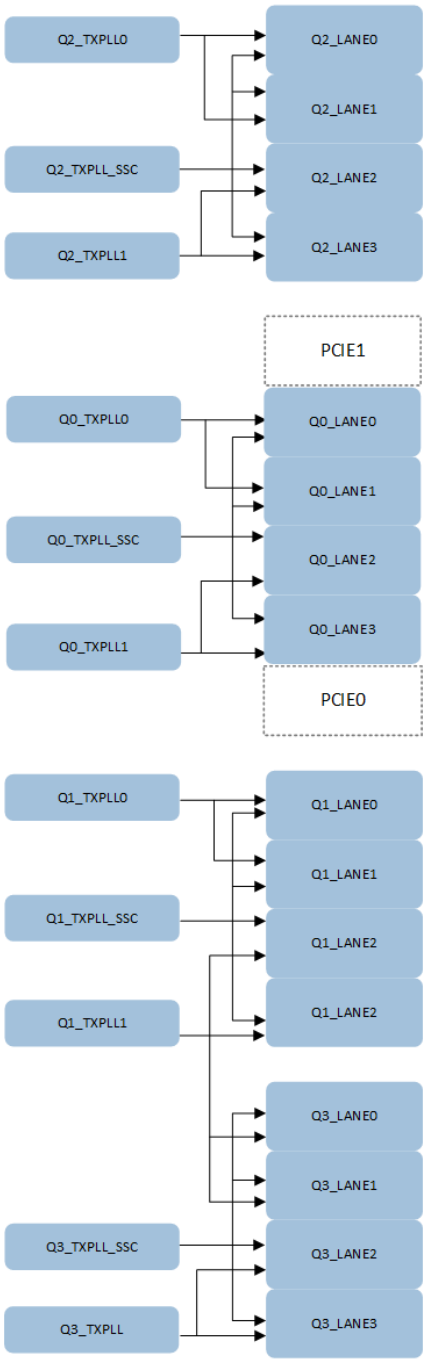
Table 12 • I/O Digital Modes (TBD)

Interface	Direction	I/O Data Rate	I/O Clock Rate (MHz)	Gear Ratio	FPGA Clock Rate (MHz)	Applications
DDR4	BiDir			8:1		Memory interface
DDR3 (L)	BiDir			8:1		Memory interface
QDRII+	Input/ Output			8:1		Low-latency memory interface
RLDRAM3	Input/ Output			8:1		Low-latency memory interface
7:1 LVDS	Input			7:1		Flatlink, Cameralink
CDR	Input			10:1		1000BASE-T, SGMII
MIPI-DPHY	Input/ Output			2:1		MIPI CSI, DSI

6 PCI Express

Each PolarFire FPGA integrates two low-power built-in PCIe Gen2 controllers, allowing seamless and easy connectivity to one or more host processors. The two PCIe controllers are shared across two quads, as shown in the following illustration. All PLLs are jitter attenuation-capable, while the SSC label indicates spread spectrum clock (SSC) capability.

Figure 8 • PCI Express Hard Macro Lane Sharing



6.1 PCI Express Features

The following are PCIe features:

- ×1, ×2, and ×4 lane support
- Suitable for root port, native endpoint
- PCI Express base specification revision 2.0 and 1.1 compliant
- AXI4 master and slave interfaces to the FPGA fabric
- Single function capability
- Advanced error reporting (AER) support
- Integrated clock domain crossing (CDC) to support user-selected AXI4 frequency
- Lane reversal support
- Legacy PCI power management support
- Native active state power management L0s and L1 state support
- Power management event (PME message)
- MSI and legacy INT message support
- Latency tolerance reporting (LTR)
- L1 PM sub-states with CLKREQ
- Address translation tables between the PCIe and AXI4 domains

6.2 PCI Express DMA Engines

Each PCIe controller supports the following built-in DMA modes, enabling low-power and efficient data transfer into the FPGA fabric.

- Two DMA channels
- Eight outstanding read and write requests
- Completion reordering support
- Flexible scatter-gather DMA modes, including dynamic DMA control per descriptor
- Optional DMA engine reporting to the descriptor to ease software management
- Fetching of up to three descriptors to optimize throughput

7 System Controller

The Radiation-Tolerant PolarFire FPGA system controller is based on the industry-standard ARM Cortex-M3 and is only used for FPGA powerup, secure DPA safe FPGA programming, and executing and responding to system services. All internal memories are SECDED protected with background scrubbing capabilities to remove single bit errors.

7.1 System Services

System services provide the user with information about the state of the FPGA and allow the user to request the system controller to perform predefined functions using a standard Application Programming Interface (API).

Design services

- Initialize fabric RAM
- Bitstream authentication
- IAP image authentication

Data services

- sNVM read/write
- PUF emulation service
- Nonce service

Device services

- Serial number
- JTAG user code
- Design version number
- Device certificate

FPGA fabric services

- In-application programming
- Digest check

8 Debug Probe System

Two specified user I/Os can be configured (at design capture stage) as either two single-ended live probes or one differential live probe. These live probes can provide read access to any register in the FPGA fabric, to the output pipeline registers in the LSRAMs, and to all the registers in the math block in real-time without having to re-instrument the code. A snapshot of all internal probe points can be created and read out asynchronously. The live-probe feature can be considered like a two-channel oscilloscope, whose two channels can be routed out to I/Os for external observation, and to internal ports to allow fabric design observation. Selecting different probe points within the RT PolarFire FPGA occurs dynamically through commands over the JTAG port using SmartDebug. Reprogramming of the FPGA is not required.

The debug probe system includes the following:

- Active probe allows dynamic asynchronous read and write to a flip-flop or a probe point. This enables quick internal observation of the logic output or experimentation on how the logic will be affected by writing to a probe point.
- Memory debug allows dynamic asynchronous read and write to a µSRAM or a large SRAM block to quickly verify if the content of the memory is changing as expected.
- Probe insertion allows routing of nodes or debug points in the FPGA design externally through unused I/Os. An oscilloscope/logic analyzer can be attached to monitor them as live signals.

9 Programming

Microsemi's RT PolarFire FPGAs have multiple programming modes designed to enable various use models. All bitstreams are always encrypted and DPA safe. Each RT PolarFire FPGA can be programmed using a dedicated SPI peripheral and JTAG port. All RT PolarFire FPGAs are typically reprogrammed in less than 60 seconds. For device specific programming timings, see DSxxxx: RT PolarFire FPGA Datasheet (TBD).

The following programming modes are supported:

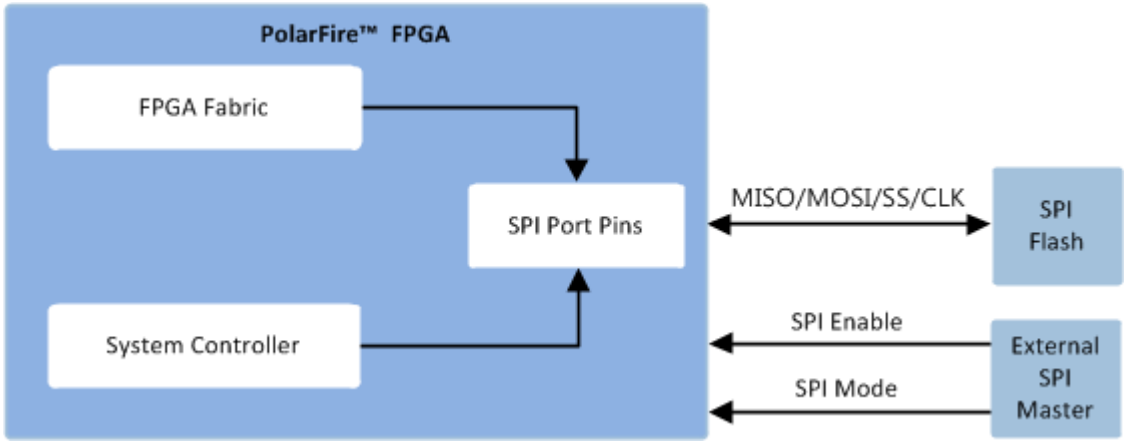
- Slave Programming
  - JTAG
  - Slave SPI—an external SPI master programs the FPGA
- SPI Master Programming—In-Application Programming (IAP)
  - Auto update feature—the system controller on power-up checks for a new bitstream in an external SPI flash and programs the FPGA.
  - Auto programming feature—on a blank device, the system controller on power-up checks for a bitstream in an external SPI flash and programs the FPGA.
  - Programming recovery feature—if remote programming fails due to a power interruption, the system controller reprograms the FPGA on the next power-up cycle from a golden bitstream (located in an external SPI flash).

9.1 Dedicated SPI Programming Port

To facilitate the use of various programming modes RT PolarFire FPGAs share dedicated SPI port pins between the system controller and user logic embedded in the FPGA. User logic must instantiate the User SPI macro to gain access to the pins from their design. The SPI port pins can be used as a master or slave programming port based on the signal level on the dedicated SPI mode pin. The dedicated SPI Enable pin also allows an external SPI master to program the on-board SPI flash without an external MUX by tri-stating the SPI MOSI/MISO/SS/CLK pins on the RT PolarFire FPGA.

The following illustration shows the SPI port facilitating the use of various programming modes.

Figure 9 • SPI Programming Port



10 Low Power

RT PolarFire FPGAs offer a variety of techniques and capabilities to lower the total application power. Users can take advantage of these features to lower both capital and operational expenditures with smaller or no heat sinks, smaller or fewer fans, lower cooling costs, and so on. Additionally, the lower total power advantage can also allow the user to pack more compute operations into an existing thermal budget.

10.1 Non-Volatile Technology

Using a non-volatile complementary metal–oxide semiconductor (CMOS) technology for the FPGA configuration cells offers several power advantages over SRAM FPGA technology.

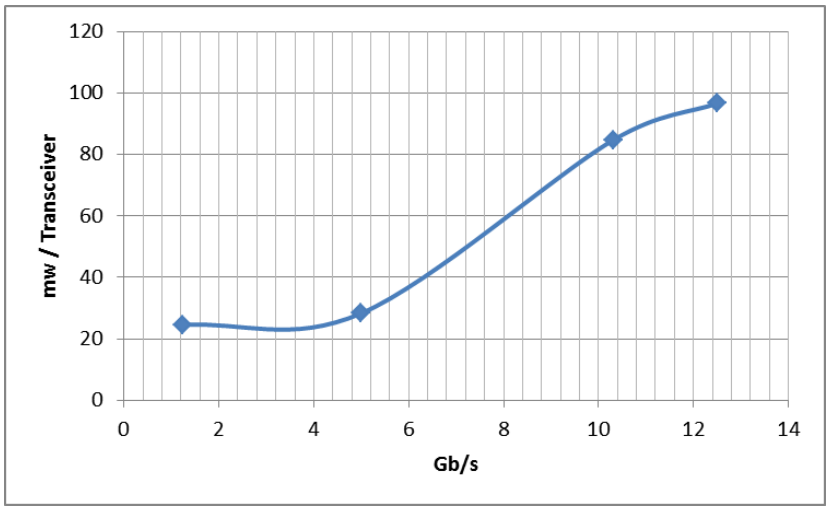
- A non-volatile configuration cell has lower power than a SRAM configuration cell, leading to lower static power consumption
- No SRAM configuration in-rush currents
- An external configuration component is not necessary

10.2 Low-Power Transceiver Lane

RT PolarFire FPGAs' low-power capability is also extended to the industry's most power efficient transceiver lane, enabling 10GBASE-KR applications at less than 100 mW of power per lane. The transceiver lane has comprehensive power-down controls to optimize power consumption, including programmable amplitude and edge rate control.

The following illustration shows the connection between transceiver power and data rate.

Figure 10 • Transceiver Power versus Data Rate



10.3 Lower Power "L" Devices

Low power (L) devices provide up to 35 percent lower static power with identical electrical specifications to the standard speed grade device. For more information, see Ordering Information (see page 35).

11 Reliability

Microsemi continues to offer the industry's most reliable FPGAs for mission and safety critical applications.

11.1 FPGA Fabric

PolarFire FPGA configuration cells are inherently immune to SEUs caused by heavy ions, protons, and neutrons, without requiring scrubbing of the configuration cells. The configuration of the RT PolarFire FPGA fabric provides worry-free operation against random loss of configuration caused by SEUs.

11.2 LSRAM

LSRAMs have built-in SECDED capability on a 32-bit word boundary. Seven additional bits are used for error correction. Two flags are provided to the user to indicate SECDED. Mitigation against multi-bit upsets is provided by keeping all cells in a word separated by a minimum distance. Applications that require scrubbing need to be accomplished with user logic. The error correction logic can be turned ON and OFF by the user to enable easy validation of the error correction operation.

11.3 µSRAM

The 64 × 12 µSRAMs are constructed from latches and are not as sensitive to SEUs as SRAMs are.

11.4 Digests

Digests verify the integrity of the programmed non-volatile data. Digests are a cryptographic hash of various data areas. Any digest that reports back an error raises the digest tamper flag.

The following are digestible non-volatile areas:

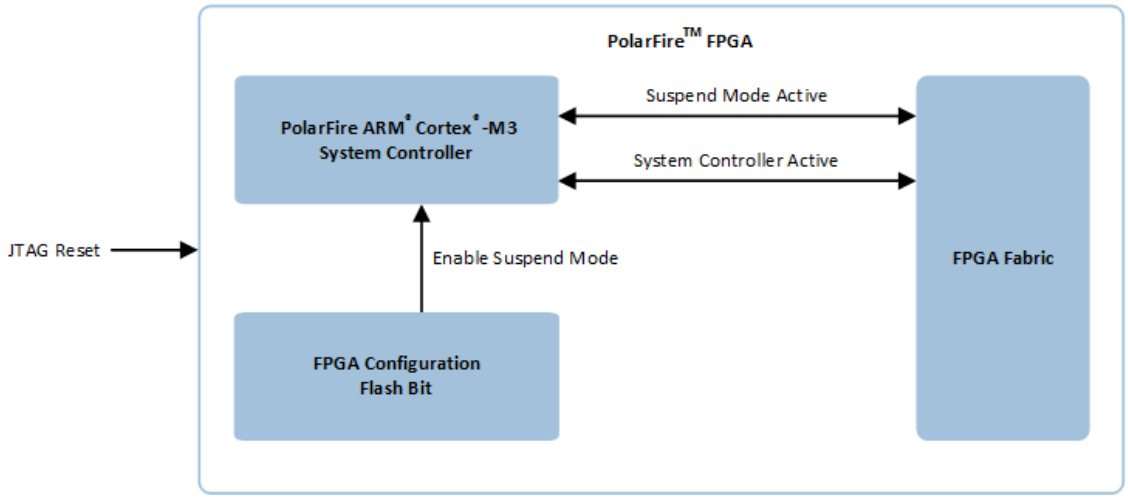
- The FPGA fabric and consequently the µPROM
- sNVM marked as ROM
- User key 1
- User key 2
- Factory parametric and key storage

11.5 System Controller Suspend Mode

For safety critical applications, RT PolarFire FPGAs allow the user to place the Cortex-M3-based system controller in a reset state after the FPGA has powered up. By programming an SEU configuration non-volatile bit, the Cortex-M3 is placed in reset by a TMRed SEU immune reset latch after FPGA power-up. User logic can monitor if the suspend mode command is active and if the system controller cannot fetch instructions while in the reset state. The FPGA can be re-programmed after disabling the suspend mode by asserting the appropriate JTAG signals. The JTAG TRSTB signal must be asserted low for suspend mode to remain active.

The following illustration shows how to activate and deactivate suspend mode.

Figure 11 • RT PolarFire



12 Security

Today's demanding applications not only have to meet the functional requirements, but also to meet them in a secured way. Security starts during silicon manufacturing and continues through system deployment and operations. Microsemi's RT PolarFire FPGAs represent the industry's most advanced, secure programmable FPGAs.

12.1 Design Security

Protecting your design starts with wafer manufacturing and continues through the deployment of the end product. The following are key features that provide state-of-the-art supply chain assurance and IP protection benefits in all RT PolarFire FPGA devices:

- Secure supply chain management through the use of hardware security modules (HSMs) during wafer test and packaging
- Supply chain assurance through the use of a 768-byte digitally signed x.509 FPGA certificate embedded in every FPGA
- AES256-encrypted CRI DPA countermeasures patent protected, bitstream, and key management protocols
- Built-in tamper detectors: voltage monitors, temperature monitor, clock glitch detectors, protective meshes, and bus scrambling
- Data integrity through built-in cryptographic digest capabilities
- Zeroization capabilities for all on-chip memories and the FPGA fabric
- Integrated PUF for the ultimate in key storage
- 56 KB of PUF protected sNVM
- Secure reprogrammable keys using non-volatile memory

12.1.1 Tamper Detectors

Microsemi's RT PolarFire FPGAs integrate numerous on-chip tamper detectors, enabling users to monitor the environment and the operating parameters of the design. The user can respond to the events that are determined to be out-of-scope for proper operation. Tamper flags indicate that a tamper event has occurred and are available as signals to the FPGA fabric for users to process and respond. The following is a partial list of tamper detectors:

- Clock glitch detectors
- Clock frequency detectors
- Voltage monitor detectors
- Temperature sensor
- JTAG active detector
- Mesh active detector

12.1.2 Tamper Responses

After processing a detected event, the user can perform one of the following actions.

- Disable I/Os—configurable on a per I/O basis
- Security lockdown
- Reset
- Zeroize

12.2 Data Security

Select Microsemi RT PolarFire FPGAs (TS and TLS FPGAs) build on the design security capabilities in all PolarFire FPGAs by enabling high-speed DPA safe cryptographic protocols at wire-line speeds. PolarFire data security FPGAs include the following additional features.

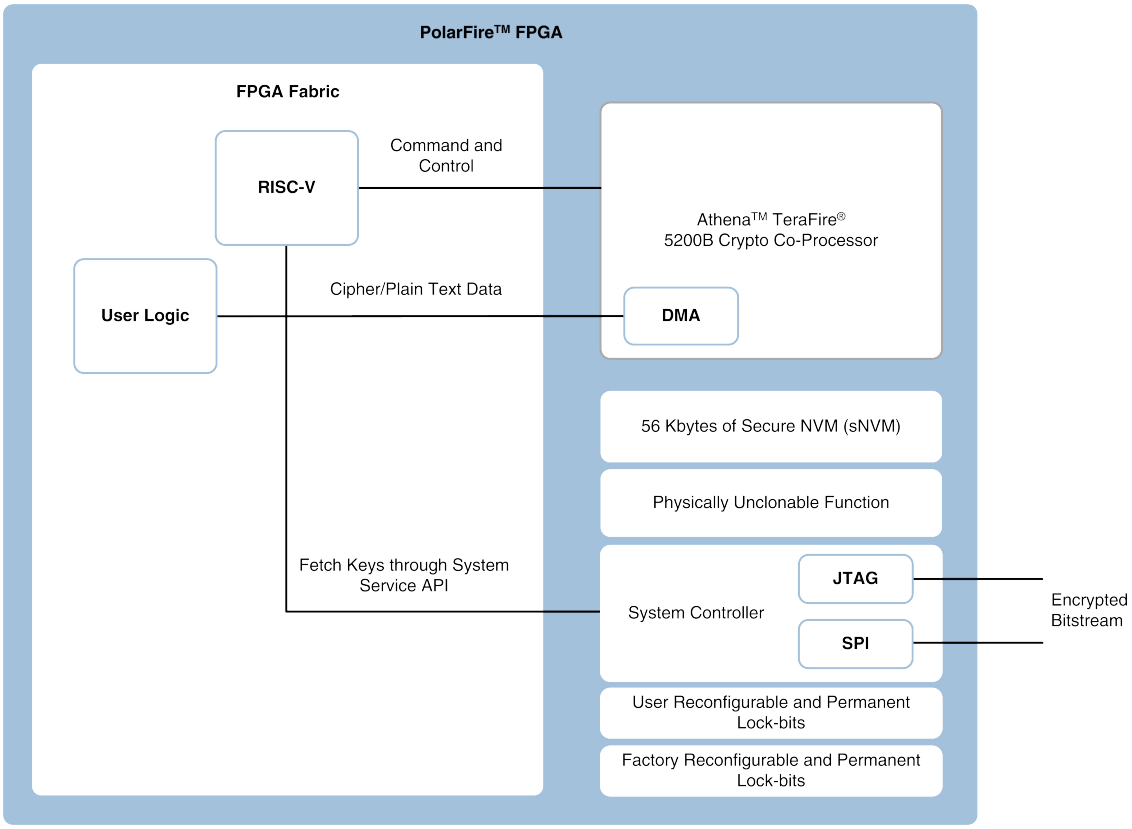
- Integrated true random number generator for enabling modern cryptographic protocols capable of generating random numbers at greater than 100 Mbps
- 189 MHz Athena TeraFire 5200B DPA safe crypto coprocessor capable of implementing Suite-B+ algorithms
- CRI DPA pass-through licensing enabling DPA safe high-speed cryptographic designs in the FPGA fabric. A CRI license is included in the purchase price of the TS FPGA. There is no need to negotiate a separate license.
- NIST-certified protocols

The following are TeraFire EXP-F5200B supported protocols/features:

- TRNG (integrated): SP800-90A CTR_DRBG-256, and SP800-90B(draft) NRBG
- AES-128/192/256 E/D (ECB, CBC, CTR, OFB, CFB, CCM, GCM, KeyWrap)
  Note: AES GCM mode is implemented through an application note.
- SHA-1/224/256/384/512
- HMAC-SHA-256/384/512; GMAC; CMAC
- SHA-256 Key Tree
- ECC-NIST P192/224/256/384/521 and Brainpool P256/384/512 curves with: KAS-ECC CDH; ECDSA-SigGen, SigVer, PKG, and PKV
- FFC: 1024/1536/2048/3072/4096-bits with: DSA SigGen and SigVer; and KAS-DH
- IFC: 1024/1536/2048/3072/4096/8192-bits with: RSA E/D; SSA_PKCS1_V1_5 SigGen and SigVer; and ANSI X9.31 SigGen and SigVer

The following illustration shows a typical use model for using the Athena crypto coprocessor.

Figure 12 • Using the Athena TeraFire 5200B Crypto Coprocessor



Users instantiate a RISC-V CPU for command and control, including fetching keys from the system controller through a system service API, initializing the Athena core, and setting up DMA to perform the desired function. The TeraFire core comes with a complete firmware driver library for all supported protocols. These driver libraries are delivered to the designer's desktop through our Firmware Catalog within Libero SoC.

13 Device Offerings

Radiation-Tolerant PolarFire FPGAs offer low-power transceivers, design security, data security, and low power. All RT PolarFire FPGAs are integrated with multi-protocol industry-leading low-power transceivers. Low power (L) devices provide up to 35 percent lower static power with identical electrical specifications to the standard speed grade device. Also, data security (S) devices integrate a DPA-resistant crypto accelerator.

The following table lists the RT PolarFire FPGA device options. Temperatures listed are junction temperatures.

Table 13 • RT PolarFire FPGA Offerings

Device Options	Military Temperature –55 °C–125 °C	Standard Speed Grade	–1 Speed Grade	Transceivers (T)	Lower Static Power (L)	Data Security (S)
RTPF500T	Yes	Yes	Yes	Yes		
RTPF500TL	Yes	Yes		Yes	Yes	
RTPF500TS	Yes	Yes	Yes	Yes		Yes
RTPF500TLS	Yes	Yes		Yes	Yes	Yes

The following table lists the temperature offerings for the RT PolarFire FPGA device.

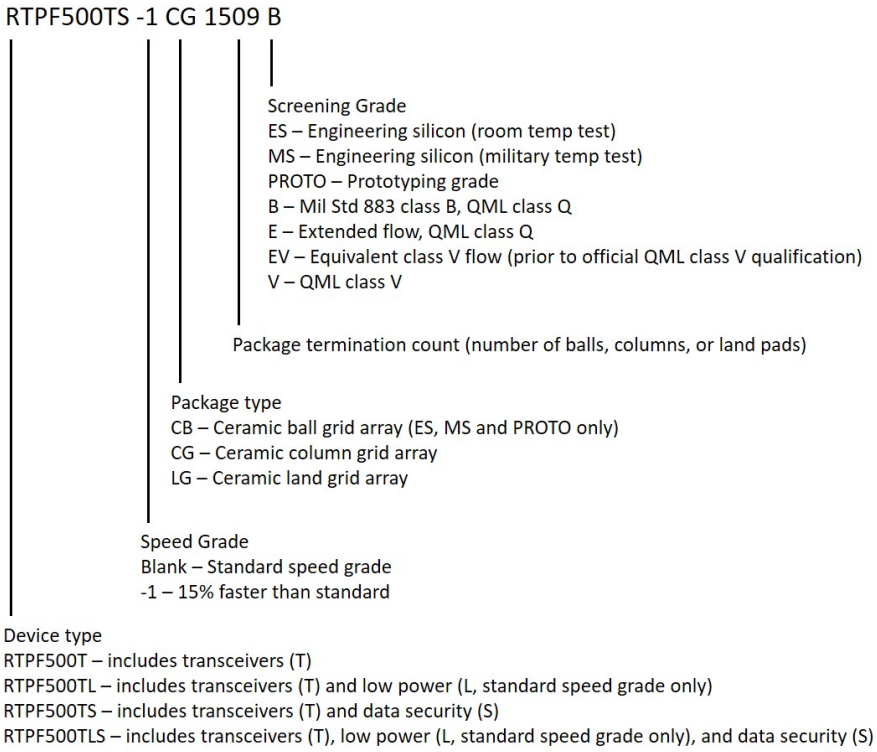
Table 14 • RT PolarFire Temperature Rating

Screening Level	Junction Temperature Range
ES	0 °C to 100 °C (room temp test only)
MS	–55 °C to 125 °C (tested at 125 °C)
PROTO	–55 °C to 125 °C
B	–55 °C to 125 °C
E	–55 °C to 125 °C
EV	–55 °C to 125 °C
V	–55 °C to 125 °C

14 Ordering Information

RT PolarFire FPGAs are offered with multiple speed grades, screening levels, and package combinations. All FPGAs are equipped with low-power transceivers.

Figure 13 • Ordering Information



15 Export Classification

The following table lists the RT PolarFire FPGA export classification.

Table 15 • RT PolarFire FPGA Export Classification

Device Options	Data Security (S)	ECCN
RTPF500T	No	TBD
RTPF500TL	No	TBD
RTPF500TS	Yes	TBD
RTPF500TLS	Yes	TBD

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