UG0872

User Guide

PolarFire MPF300T FPGA Video Kit

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Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was the first publication of this document

2 Introduction

The Microsemi PolarFire® FPGA Video Kit (POLARFIRE VIDEO KIT), which is RoHS-compliant, enables you to evaluate the PolarFire MPF300T-1FCG1152E FPGA for the following interfaces:

- MIPI CSI-2 RX interface
- HDMI2.0
- HDMI1.4
- DDR4 memory
- FMC HPC with 8 Transceiver lanes
- UART Interface to the FTDI device
- SPI Interface to the SPI Flash device

2.1 Kit Contents

The following table lists the contents of the PolarFire Video Kit.

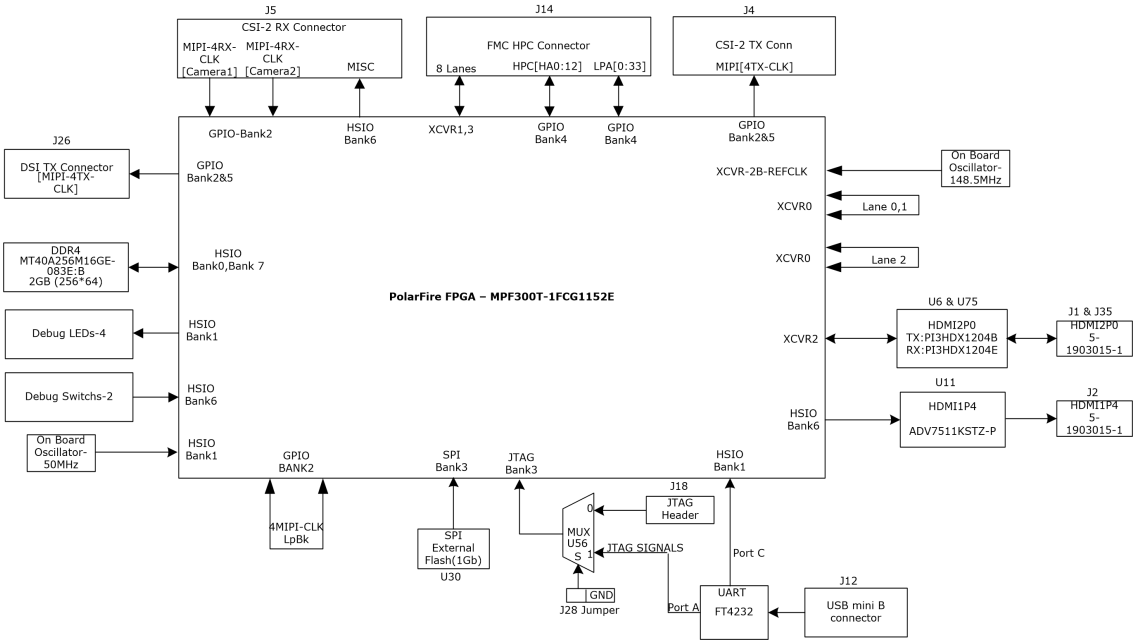
Table 1 • Kit Contents

Item	Quantity
Dual Camera Sensor Module	1
PolarFire Video Board featuring the MPF300T-1FCG1152E device with 300K logic elements	1
12 V, 5 A AC power adapter and cord	1
USB 2.0 A-male to mini-B cable programming	1
Quickstart card	1
Free one-year Libero Gold software license	1

2.2 Block Diagram

The following figure shows the block diagram of the video kit.

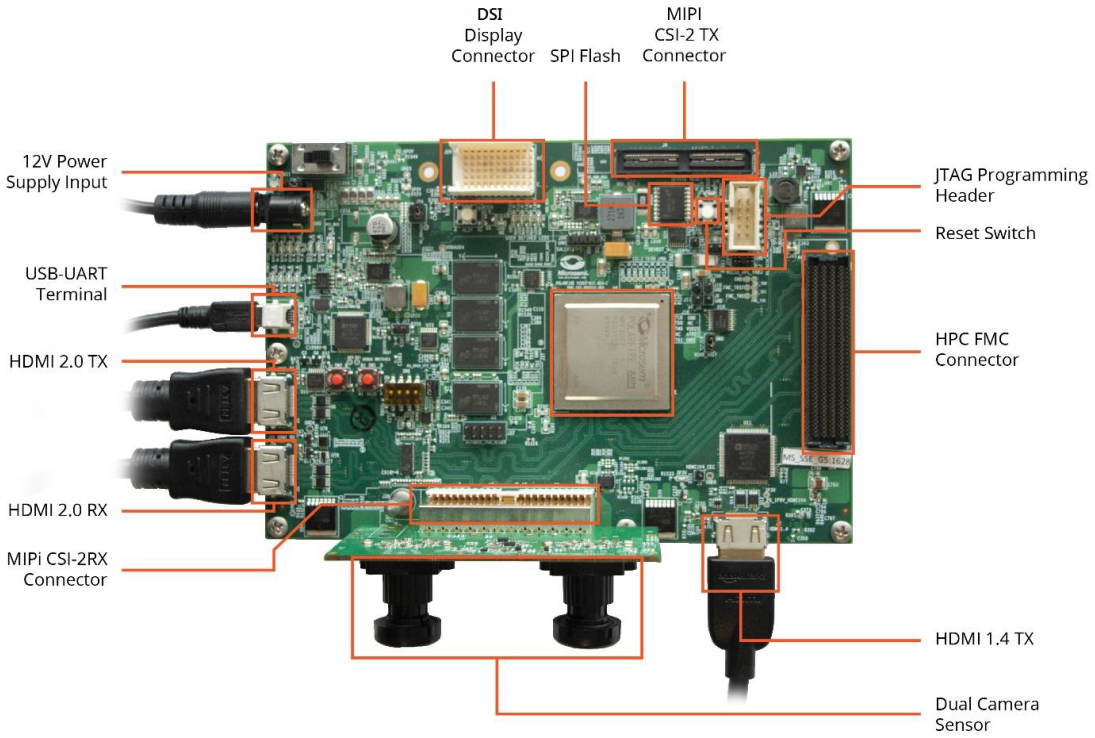
Figure 1 • Block Diagram



2.3 Board Overview

The following figure shows a labeled image of the video board highlighting its components.

Figure 2 • Board Callout



The following table lists the components of the video board.

Table 2 • Board Components

Component	Label on Board	Description
Featured Device		
PolarFire FPGA		MPF300T-1FCG1152E FPGA
Power Supply		
12 V power supply	J20	The board is powered by a 12 V power source using an external +12 V/5 A DC jack
ON/OFF switch	SW4	Power ON/OFF switch from +12 V external DC jack
Clocks		
On-board 50 MHz clock oscillator	X3	50 MHz clock oscillator with single-ended output
XCVR reference clock	Y5	148.5 MHz oscillator (differential LVDS output) that provides reference clock (REFCLK) via PolarFire device pins AF29 and AF30. These pins are connected to the XCVR
Clock Synthesizer	U15	CDCEL913PWR Clock Synthesizer for HDMI1.4 clocks and programmable through the I2C
FPGA Programming and Debugging		
FT4232H	U70	USB-to-quad serial ports in various configurations
JTAG programming header	J18	This header is used to program and debug the PolarFire device using FlashPro4 or FlashPro5. In the FlashPro software, the appropriate programmer (FlashPro4 orFlashPro5) must be selected.
SPI flash	U30	One 1 Gb SPI Flash from Micron MT25QL01GBBB8ESF-0SIT (P/N) connected to SPI pins on bank 3 of the PolarFire device
Memory Chips		
DDR4 Memory	U1,U2, U3 and U4	Four 4 Gb (MT40A256M16GE-083E:B) chips are connected in Fly-by topology with a 64-bit data bus for storing data bits
FMC HPC connector	J14	FMC connector with eight XCVR lanes and 13 Differential pairs HPC[HA0:12] and LPC [0:33])
Video Interfaces		
CSI-2 RX connector	J5	MIPI data and clock signals are received from Camera sensor board
DSI TX connector	J26	MIPI data and clock signals are transmitted to Display daughter board through the connector
CS-2 TX connector	J4	MIPI data and clock signals are transmitted to Display daughter board through the connector
General Purpose I/O		
Switches	SW1 and SW2	Push-button switches for user-interface debugging applications
DIP Switches	SW6	Four DIP switches for testing
Light-emitting diodes (LEDs)		Four active-high LEDs connected to some of the user I/Os for debugging, and twelve active high LEDs used for indicating power supply

Component	Label on Board	Description
USER Reset switch	SW3	Push-button system reset for the PolarFire device Users must program this HSIO for PolarFire logic reset function
Device reset	SW5	Device reset

3 Hardware Settings

This section provides information about jumper settings, switches, LEDs, and DIP switches on the PolarFire video board.

3.1 Jumper Settings

Connect the jumpers according to the settings specified in the following table.

Table 3 • Jumper Settings

Jumper	Description	Pin(s)	Default
J15	SPI Slave and Master mode selection. By Default SPI master	1-2	Closed
J19	XCVR_VREF is connected to GND	1-2	Closed
J28	Close pin 1-2 to program through the FTDI Open pin 1-2 to program the external Flash pro5	1-2	Closed
J24	Jumper to select the PolarFire VDDAUX4 for Bank4 voltage	Close pin2-4 for 3V3	Closed
		Close pin2-4 for 2V5	Open
J25	Jumper to select the PolarFire VCCIO voltage (VCCIO_HPC_VADJ)	Close pin 1 and 2 for 3.3 V	Open
		Close pin 3 and 4 for 2.5 V	Open
		Close pin 5 and 6 for 1.8 V	Closed
		Close pin 7 and 8 for 1.5 V	Open
		Close pin 9 and 10 for 1.2 V	Open
J36	Jumper to select the SW3 input or the ENABLE_FT4 232 signal from the FT4232H chip	Close pin 1 and 2 for manual power switching using SW3	Close
		Close pin 2 and 3 for remote power switching using the GPIO capability of the FT4232 chip	Open

3.2 LEDs

The following table lists the power supply LEDs.

Table 4 • LEDs

LED	Description
DS14-Green	12 V voltage rail
DS20-Green	5 V voltage rail
DS21-Green	3.3V voltage rail
DS5-Green	1.0V voltage rail
DS4-Green	1.8V voltage rail
DS3-Green	VDD25 Voltage rail
DS2-Green	VDDAUX2_5 Voltage rail

LED	Description
DS9-Green	VDDA(1V05) Voltage rail
DS8-Green	VDDAUX4 Voltage rail
DS7-Green	1.2V voltage rail
DS6-Green	VCCIO_HPC_VADJ voltage rail
DS12-Green	1.8V HDMI1V4 voltage rail
DS13-Green	0.6V VTT voltage rail

3.3 Power Sources

The PolarFire video board uses Microchip power supply devices. For more information about these power supply devices, see: https://www.microchip.com/design-centers/power-management/dc-dc-converters-regulators.

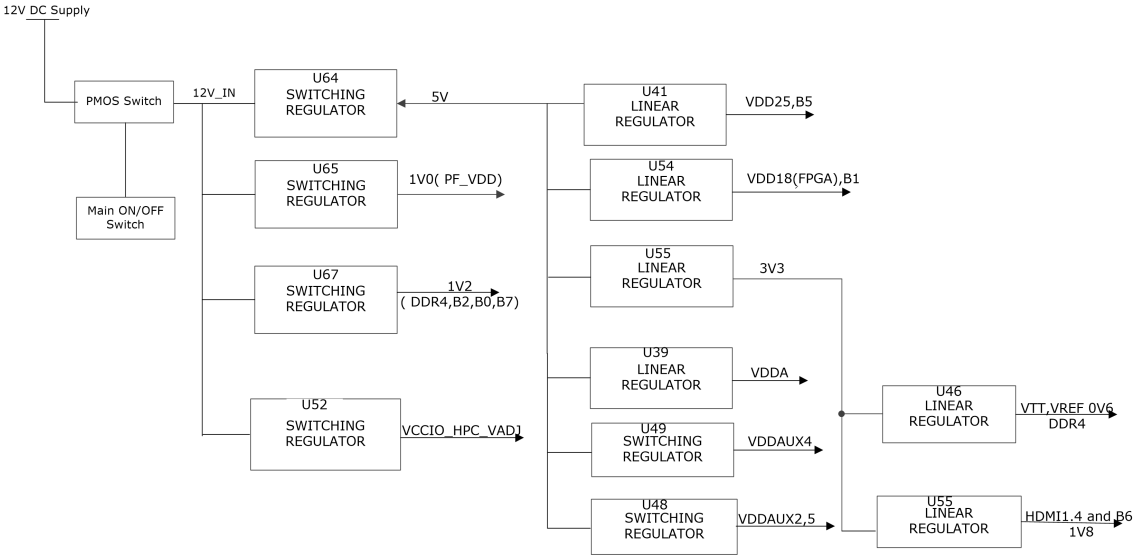
The following table lists the key power supplies required for normal operation of the PolarFire video board.

Table 5 • Voltage Rails in PolarFire Video Board

PolarFire Bank	I/O Rail	Voltage
Bank 0	1P2V	1.2V
Bank 1	1P8V	1.8V
Bank 2	1P2V_B2	1.2V
Bank 3	VDD25	2.5V
Bank 4	VCCIO_HPC_VADJ	1.8V
Bank 5	VDD25	2.5V
Bank 6	1P8V_HDMI1V4	1.8V
Bank 7	1P2V	1.2V

The following figure shows the power supply scheme used in the PolarFire video board.

Figure 3 • Power Supply Scheme



The following table lists the suggested Microchip power regulators for PolarFire FPGA voltage rails.

Table 6 • Power Regulators

Voltage Rail	Part Number	Description	Current
5V	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12A
1V	MIC24055YJL-TR	IC REG BUCK ADJ 12A SYNC 28QFN	12A
1V2	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5A
VDDAUX2&5	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3A
VDDAUX4	MIC23303YML-T5	IC REG BUCK ADJ 3A SYNC 12DFN	3A
VCCIO_HPC_VADJ	MIC24046YFL-TR	IC REG BUCK PROG 5A SYNC 20VQFN	5A
VREF,VTT	MIC5166YML-TR	IC PWR SUP 3A HS DDR TERM 10MLF	3A
HDMI1.4	MCP1726T-ADJE/MF	IC REG LINEAR POS ADJ 1A 8DFN	1A
VDD25	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
3V3	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
VDD18	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A
1V05	MIC69502WR	IC REG LINEAR POS ADJ 5A SPAK-7	5A

Note: These regulators are not pin compatible with the existing video kit schematics. Use these regulators for new board.

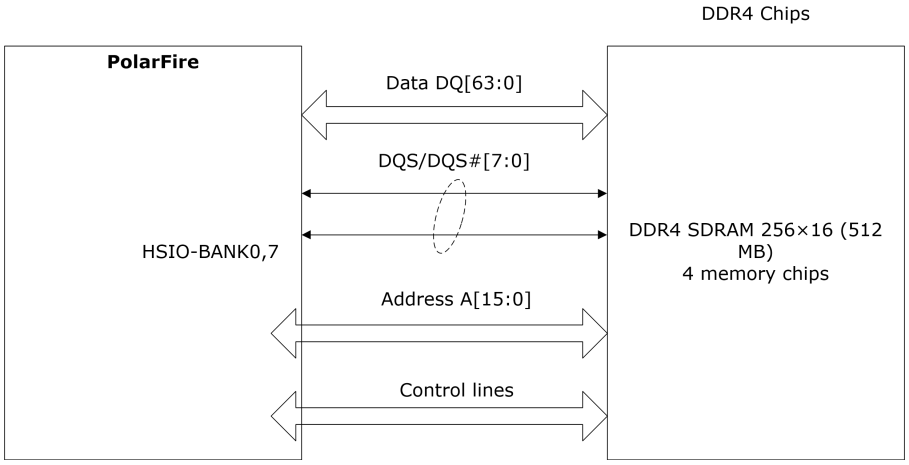
4 Board Components and Operations

This section describes the key components of the PolarFire Video board and important board operations.

4.1 Memory Interface

The following figure shows the memory interface scheme.

Figure 4 • Memory Interface



As shown in the preceding figure, Four 4 Gb DDR4 SDRAM chips are used as flexible volatile memory for user applications. The DDR4 interface is implemented in the HSIO Bank 0 and Bank 7.

The DDR4 SDRAM specifications are as follows:

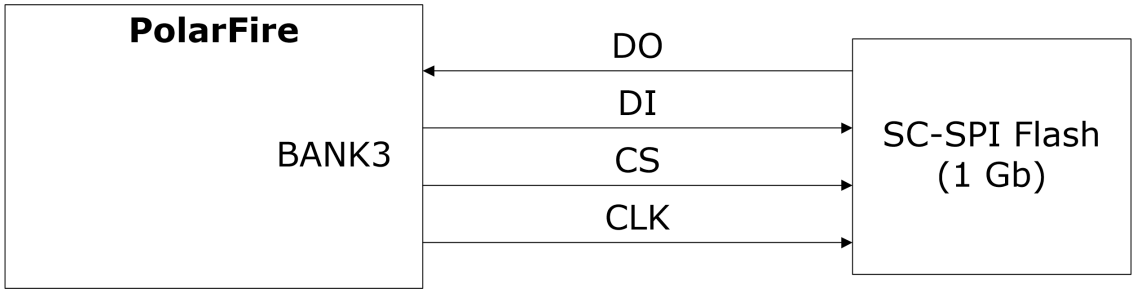
- MT40A256M16GE-083E:B
- Quantity: Four chips are connected in Fly-by topology
- Density: 16 Gb
- Data rate: DDR4 64-bit at 166 MHz clock rate

The PolarFire video board design uses the DDR4 and POD12 standards for the DDR4 interface. The default board assembly for the DDR4 standard uses RC terminations.

4.2 SPI Serial Flash

The following figure shows the SPI Flash and its interface with the PolarFire device.

Figure 5 • SPI Flash Interface



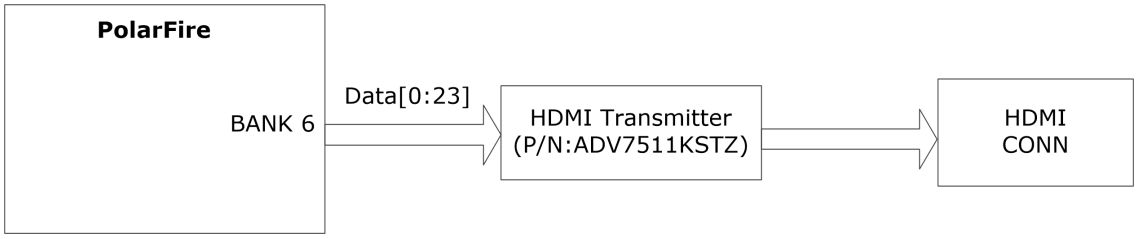
The SPI flash specifications for the PolarFire device are:

- Density: 1 Gb
- Voltage: 2.7 V to 3.6 V (MT25QL01GBBB8ESF-0SIT)
- Frequency: 90 MHz
- Quantity = 1
- SPI mode support: Modes 0 and 3

4.3 HDMI1.4 Interface

One HDMI1.4 Transmitter is connected to the PolarFire device to support the HDMI1.4 standard as shown in the following figure.

Figure 6 • HDMI1.4 Interface



The HDMI interface is implemented in Bank6.

The HDMI1.4 transmitter specifications for the PolarFire device are:

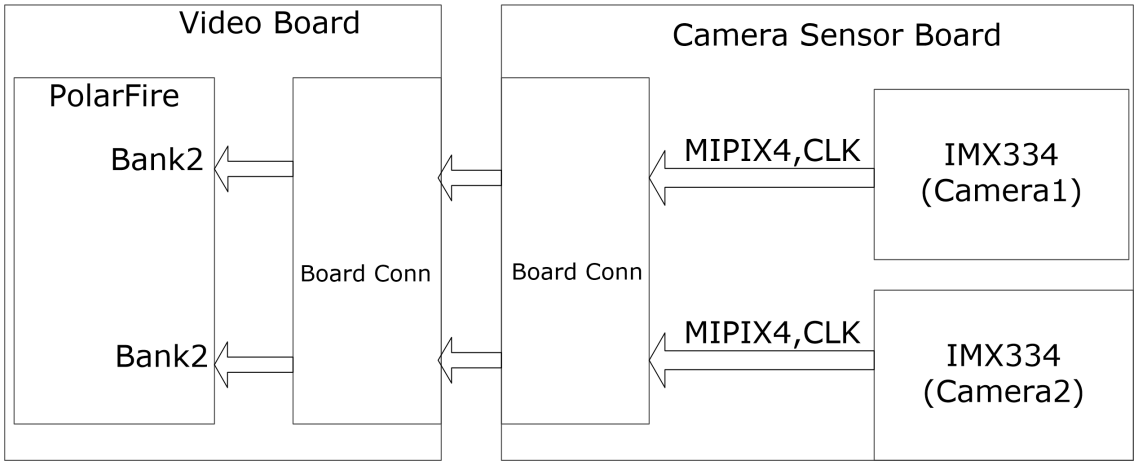
- Part Number of the HDMI Transmitter: ADV7511KSTZ
- Operating frequency: up to 225 MHz

4.4 MIPI-RX Connector (CSI-2 Application)

The video board supports a dual Camera image sensor daughter card that can be connected using the CSI-2 RX interface (J5) for CSI-2 RX applications. The daughter card includes two IMX334 cameras. Each image sensor supports a four-lane MIPI interface. The daughter card is connected to the video board via the board to board connector as shown in the following figure. (see page)The MIPI output signals are connected to Bank 2.

The image sensor supports maximum 1782 Mbps.

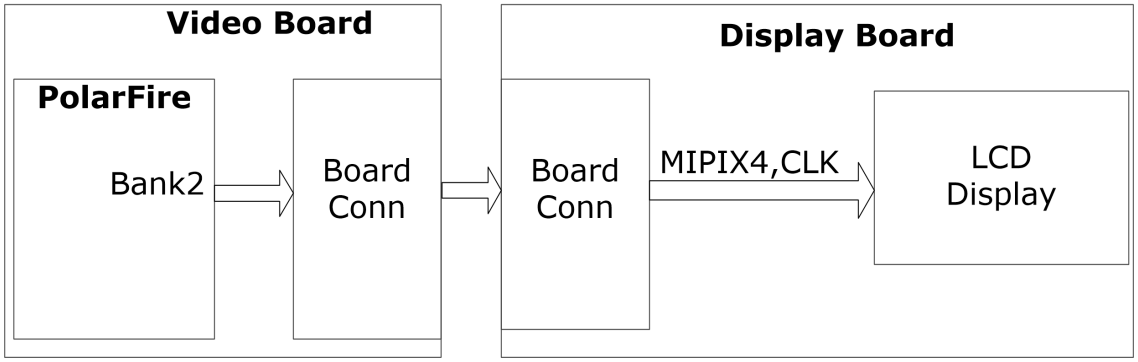
Figure 7 • MIPI-RX Connection



4.5 MIPI-TX Connector (DSI Application)

The video board supports the MIPI transmitter X4 lanes and clock for DSI application, as shown in the following figure. MIPI TX signals are interfaced to the LCD display. An adaptor board for the LCD display can be connected through the J26 connector on the video board. This adaptor board contains the LCD mating connector and the auxiliary circuit required for the display. For more information, see the video board schematics.

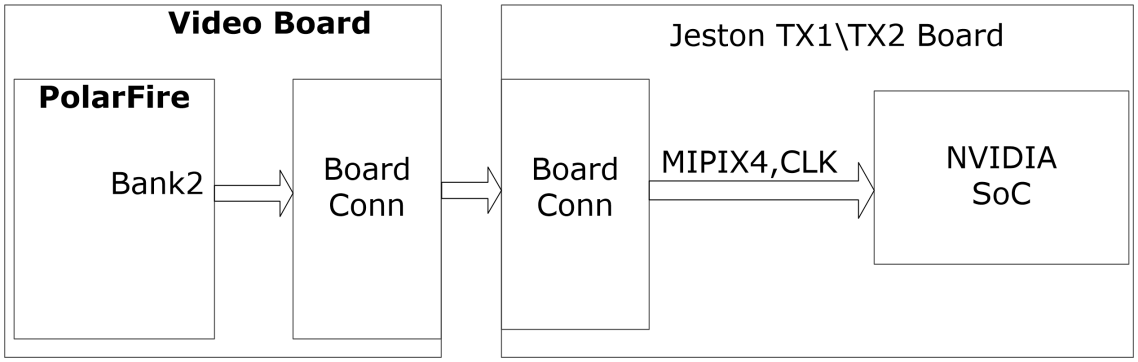
Figure 8 • MIPI-TX Connection (DSI Application)



4.6 MIPI-TX Connector (CSI-2 Application)

The video board supports the MIPI X4 lanes and clock for the CSI-2 transmitter application, as shown in the following figure. For testing, the video board can be can be interfaced with Nvidia's Jetson TX1\TX2 development board using a mating connector cable.

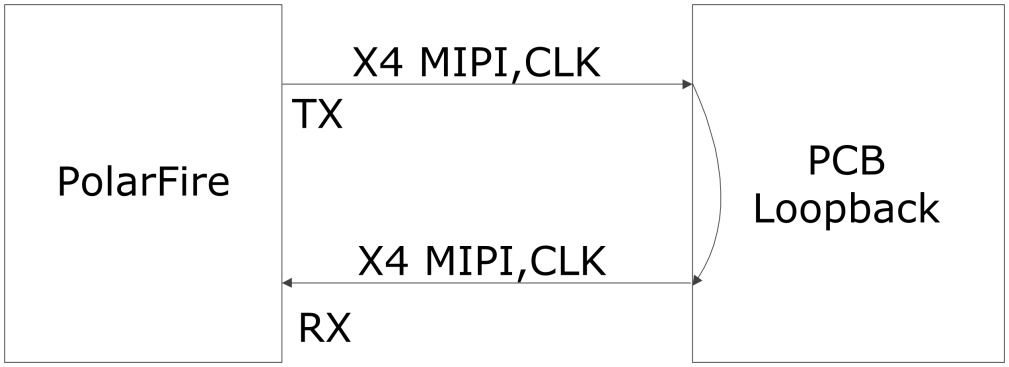
Figure 9 • MIPI-TX Connection (CSI-2 Application)`



4.7 MIPI-TX and RX PCB Loopback

The video board supports the on-board PCB trace loopback of MIPI X4 lanes and clock, as shown in the following figure.

Figure 10 • MIPI-TX and RX Loopback



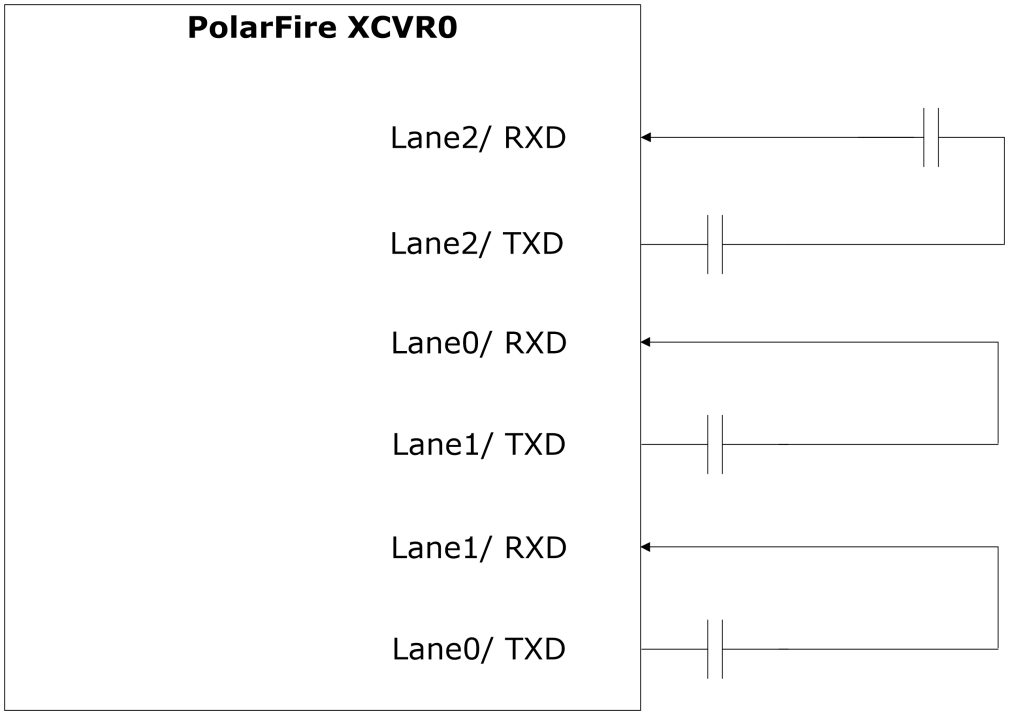
4.8 Transceivers

The PolarFire MPF300T-1FCG1152E FPGA device has 4 XCVR blocks and each block contains 4 transceiver lanes. These lanes can be accessed through the HDMI2.0 and FMC connectors on the board. The following sections describe these blocks and the lanes used.

4.8.1 XCVR0 Block

Lanes 0, 1, and 2 of the XCVR0 block are looped back, as shown in the following figure .

Figure 11 • XCVR0 Interface



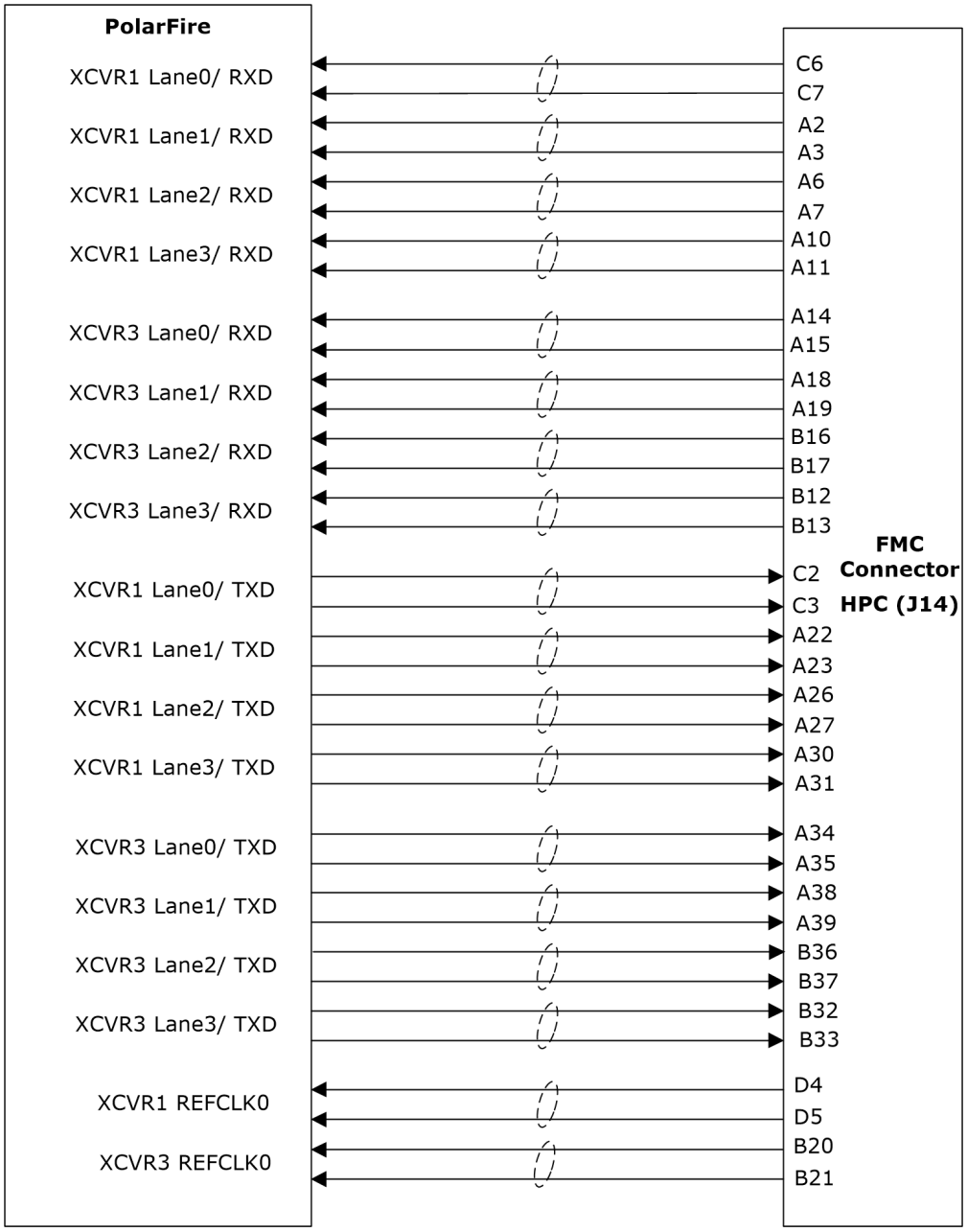
4.8.2 XCVR1 and XCVR3 Blocks

XCVR1 and XCVR3 blocks have four lanes each. These lanes are connected to the FMC HPC connector and the signals are routed on the PCB as follows:

- Lanes 0 to 7 are directly routed to the FMC HPC
  - TX pad > trace > via (to bottom layer) > trace > FMC HPC connector pad
  - RX pad > trace > via (to Top layer) > trace > PolarFire device pad

The XCVR1 and XCVR3 reference clock is routed directly from the HPC connector to the PolarFire device. The following figure shows the XCVR1 and XCVR3 and their interfaces.

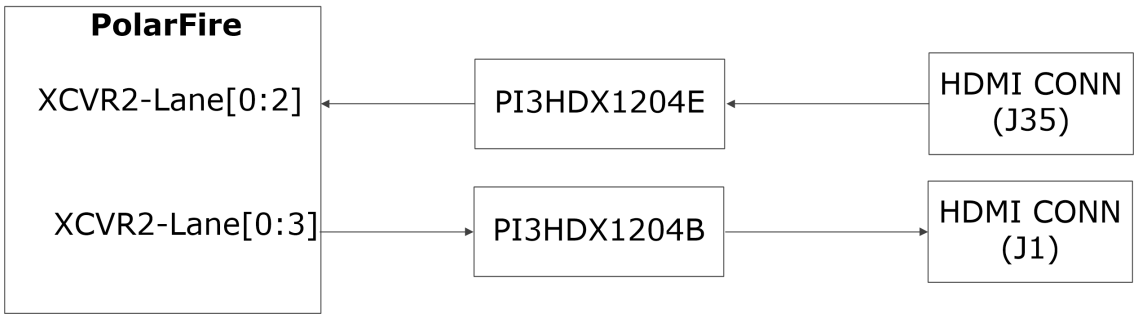
Figure 12 • XCVR1 and XCVR3 Interface



4.8.3 XCVR2 Block

The lanes of the XCVR2 block are connected to HDMI2.0 TX and RX chips via the line drivers chips, as shown in the following figure. This interface can operate up to 6 Gbps.

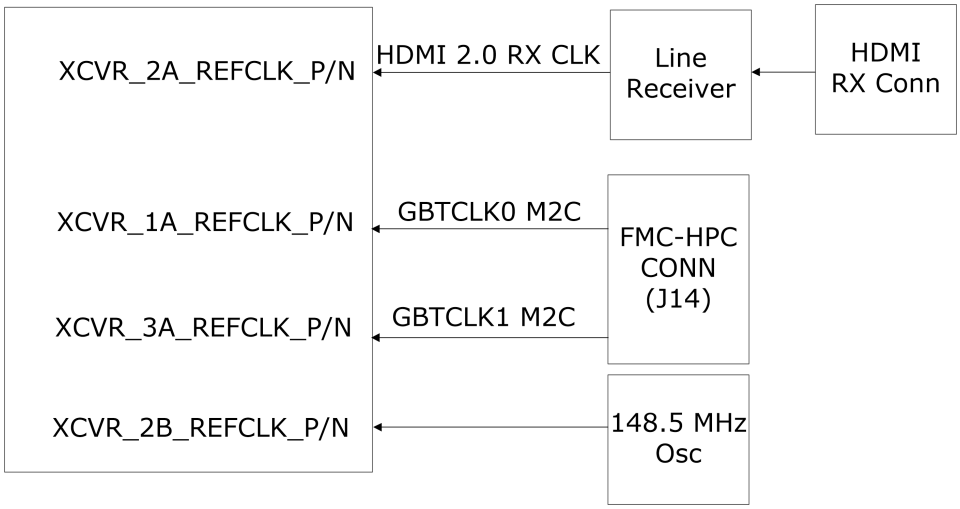
Figure 13 • XCVR2 Interface



4.8.4 XCVR Reference Clock

The following figure shows the clock sources for XCVR blocks.

Figure 14 • XCVR Reference Clocks



- XCVR 1A, 3A reference clocks are sources from FMC HPC connector(J14).
- XCVR 2B reference clock is sourced from the on-board 148.5 MHz
- XCVR 2A reference clock is sourced from the on-board HMDI2.0 TX

4.9 Programming

The PolarFire device is programmed using the on-board FlashPro5 programmer or through the JTAG Header. For more information about programming, see the video board schematics.

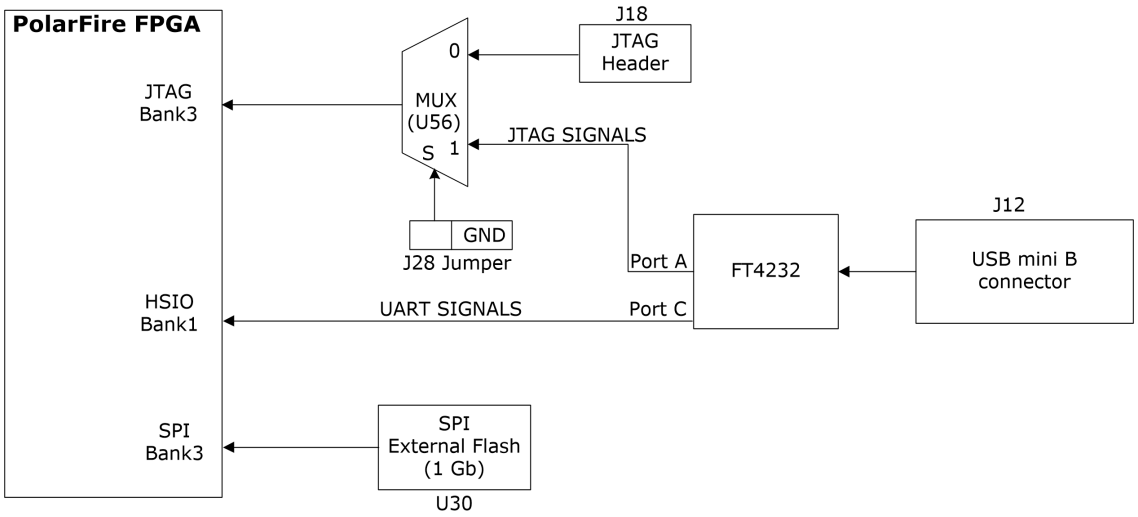
The following section describes the FTDI and JTAG Header programming schemes used on the board.

4.9.1 FTDI and JTAG Header Scheme

The PolarFire device can be programmed using the on-board JTAG Header or FTDI. By default, the FTDI programming mode is enabled. The programming mode can be changed based on the Jumper settings. For more information, see Table 3.

The following figure shows how the JTAG Header interfaces with the PolarFire Device.

Figure 15 • JTAG Header Interface



Note: By default, the FTDI programming mode is enabled. Remove J28 jumper to enable programming through JTAG header.

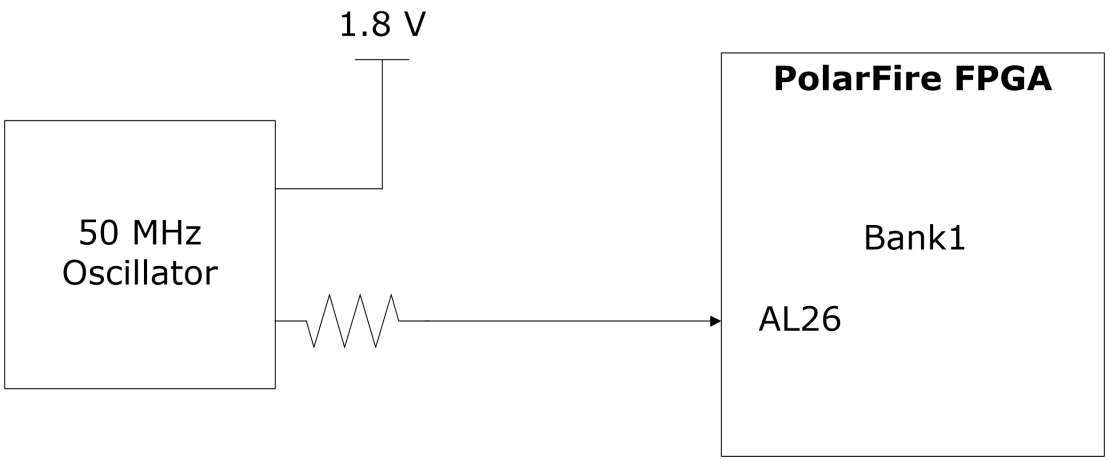
4.10 50 MHz Oscillator

A 50 MHz clock oscillator with an accuracy of +/-50 ppm is available on the board. This clock oscillator is connected to the FPGA fabric to provide a system reference clock. An on-chip PolarFire PLL can be configured to generate a wide range of high-precision clock frequencies.

The package and pin details of the 50 MHz oscillator are as follows:

- Pin Number: AL26
- Pin Name: HSIO72PB1/CCC_NE_CLKIN_N_11 shows the 50 MHz clock oscillator interface.

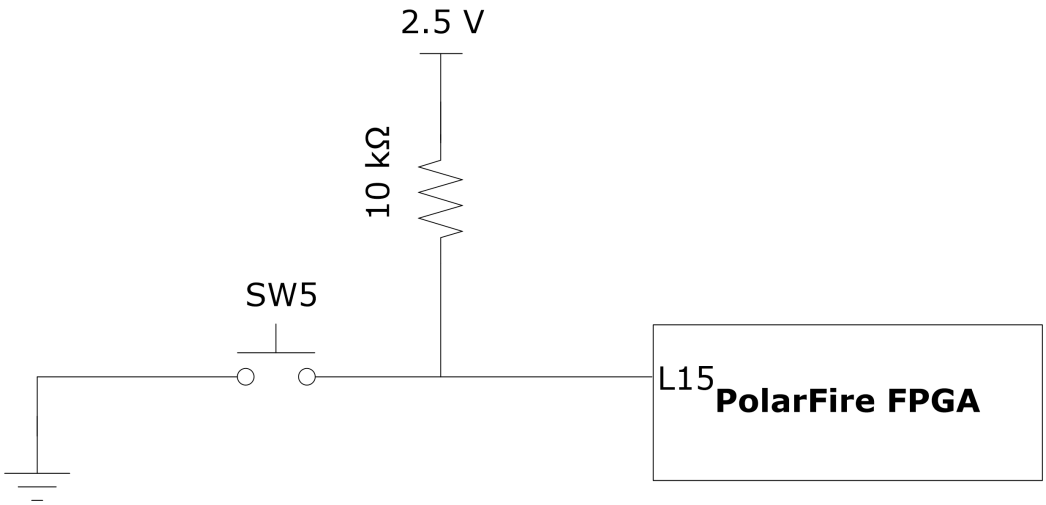
Figure 16 • 50 MHz Oscillator Interface



4.11 Device Reset

As shown in the following figure, DEVRST_N (SW5 push button) is an input-only reset switch that allows assertion of a full reset of the chip at any time. The DEVRST_N signal is an active-low signal.

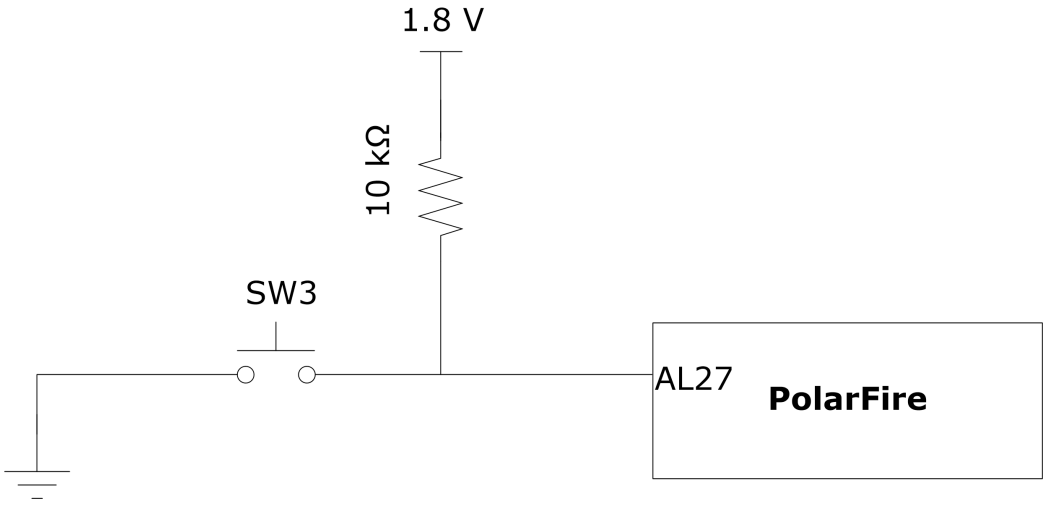
Figure 17 • Device Reset



4.12 User Reset

As shown in the following figure, (see page)the user reset (SW3 push button) is an input-only reset switch that allows assertion of a reset of the fabric logic.

Figure 18 • User Reset



4.13 User Interface

LEDs and push-button switches are available on the board for the user interface.

4.13.1 User LEDs

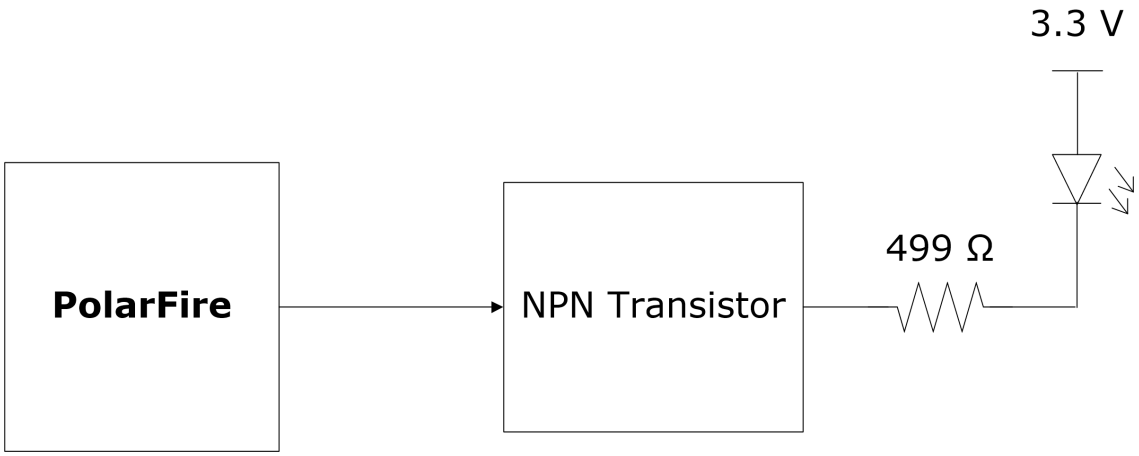
Four active-high LEDs are connected to the PolarFire device. The following table (see page)lists the on-board label of these switches, the associated PolarFire pin number, name, and Bank.

Table 7 • User LEDs

Label On Board	PolarFire Pin Number	PolarFire Pin Name	PolarFire Bank
LED1	G17	HSIO37NB6	Bank 6
LED2	K23	HSIO54PB6	Bank 6
LED3	L23	HSIO54NB6	Bank 6
LED4	B25	HSIO68NB6/DQS	Bank 6

The following figure (see page)shows how each user LED interfaces with the PolarFire device.

Figure 19 • User LED Interface



4.13.2 Push-Button Switches

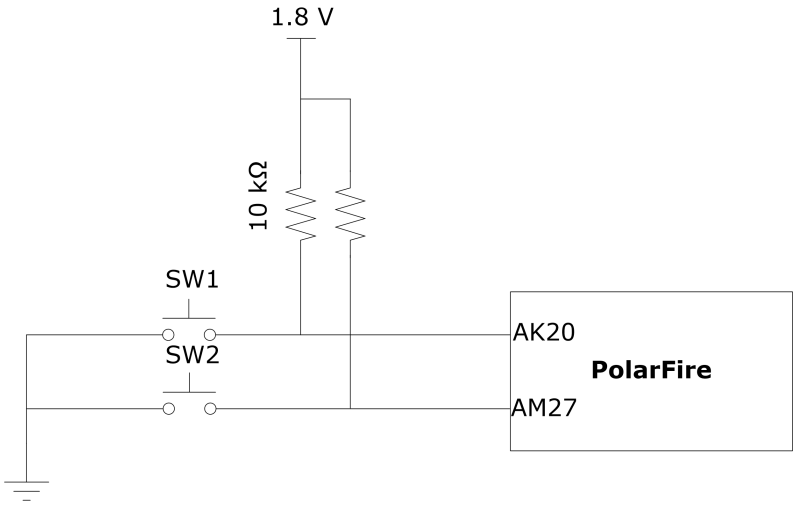
Two push-button tactile switches are connected to the PolarFire device. The following table lists the on-board label of these switches, the associated PolarFire pin number, name, and Bank.

Table 8 • Push-Button Switches

Label On Board	PolarFire Pin Number	PolarFire Pin Name	PolarFire Bank
SW1	AK20	HSIO98NB1	Bank 1
SW2	AM27	HSIO73NB1	Bank 1

The following figure shows how these push-button switches interface with the PolarFire Device.

Figure 20 • Push-Button Interface



4.13.3 Slide Switches (DPDT)

The SW4 slide switch powers the device ON or OFF.

4.13.4 DIP Switches (SPST)

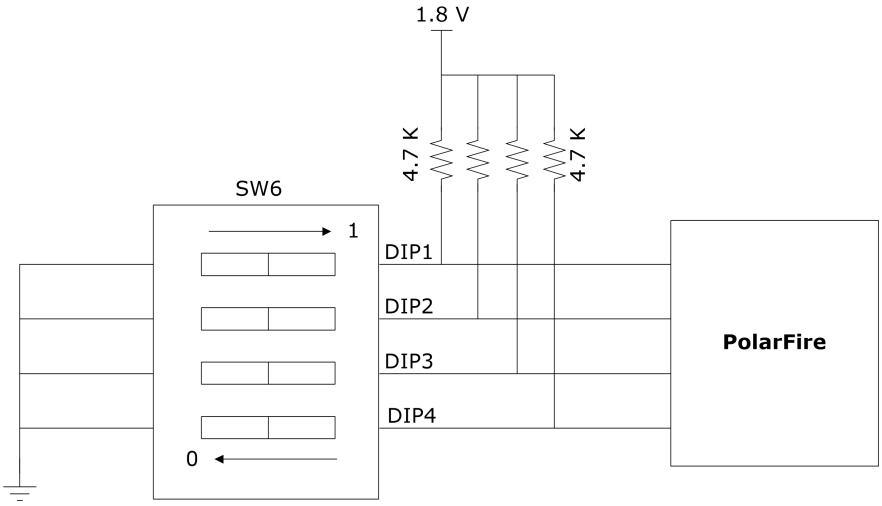
The SW6 DIP switch includes 8 connections to the PolarFire device. The following table lists on-board label of these switches, the associated PolarFire pin number, name, and Bank.

Table 9 • DIP Switch

Label On Board	PolarFire Pin Number	PolarFire Pin Name	PolarFire Bank
DIP1	AH22	HSIO99PB1/DQS	Bank1
DIP2	AJ21	HSIO99NB1/DQS	Bank1
DIP3	AG21	HSIO100PB1	Bank1
DIP4	AH21	HSIO100NB1	Bank1

The following figure shows how the DIP switch interfaces with the PolarFire device.

Figure 21 • DIP Switch Interface



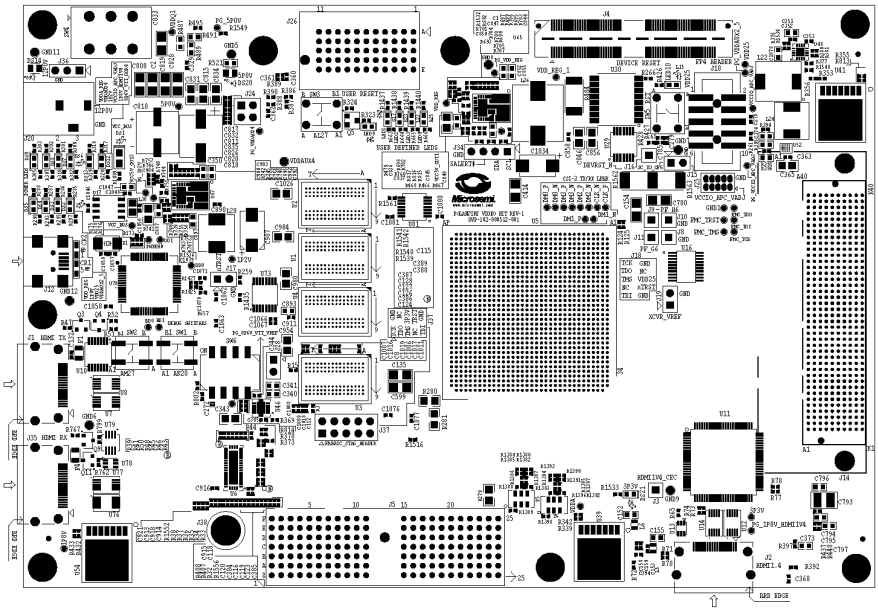
4.13.5 FMC HPC Connector (J14)

An HPC (J14) FMC connector is available for future expansion of interfaces. This FMC connector is compliant with the VITA 57.1 specification. The PolarFire Bank4, XCVR1, and XCVR3 signals are routed to the FMC connector (J14) for user application development. For more information, see the video board schematics.

4.14 Board Components Placement

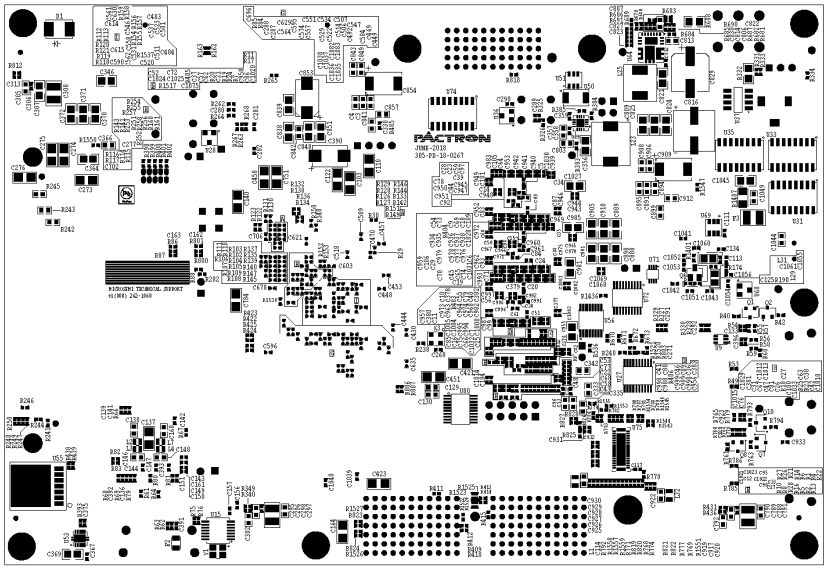
The following figure shows the top view of the placement of board components.

Figure 22 • Silkscreen Top View



The following figure shows the bottom view of the placement of board components.

Figure 23 • Silkscreen Bottom View



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