Application Note

AN-211 Designing an IEEE 802.3af/802.3at/802.3bt-Compliant PD69208 48-Port PoE System

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a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 of this document was published in June 2018. The following is a summary of the changes:

- Introductory text was updated.
- The latest Microsemi formatting was imported.
- Hot-swap information was added.
- Schematics were updated.

1.2 Revision 1.2

Revision 1.2 of this document was published in November 2016. The following is a summary of the changes:

- General updates
- Added a 4.7 µF capacitor between V_{AUX5} to V_{AUX3P3} to minimize the time delay between the 5 V and 3.3 V rise.

1.3 Revision 1.1

Revision 1.1 of this document was published in February 2016. The following is a summary of the changes:

- Broken links and paragraphs were fixed.
- The reference to communication protocol “PD69200_UG_COMM_PROT” was updated.

1.4 Revision 1.0

Revision 1.0 of this document was published in January 2015. The following is a summary of the changes:

- General structural changes.
- PD69204 was added.
- A comment was added that an output capacitor can be from 22 nF to 220 nF.

1.5 Revision 0.5

Revision 0.5 of this document was published in November 2014. In revision 0.5 of the document, a recommendation for V_{MAIN} capacitors was added.

1.6 Revision 0.4

Revision 0.4 of this document was published in May 2014. In revision 0.4 of the document, a note was added that the precision resistor should be 0.1% in a PoH system.

1.7 Revision 0.3

Revision 0.3 of this document was published in March 2014. In revision 0.3 of the document, output capacitors were changed to 220 nF.

1.8 Revision 0.2

Revision 0.2 of this document was published in March 2014. In revision 0.2 of the document, R_{REF} was changed to 28.7 kΩ.

1.9 Revision 0.1

Revision 0.1 of this document was published in December 2013. This was the preliminary release version.

2 Overview

This application note provides detailed information about and circuitry design guidelines for the implementation of a 48-port Power over Ethernet (PoE) system, based on Microsemi's PoE manager and PD69200 PoE controller. This document enables designers to integrate PoE capabilities (as specified in IEEE 802.3af, IEEE 802.3at, IEEE 802.3bt, and PoH standards) into an Ethernet switch.

The PoE manager can be 8 channels or 4 channels. The 8-channel PoE manager, PD69208M, supports up to type-3 PSE, 60 W. The 4-channel PoE manager, PD69204T4, supports up to type-4.

The PD69208/4 PoE manager implements real-time functions as specified in the standards (including detection, classification, and port-status monitoring) and system-level activities such as power management and management information base (MIB) support for system management. The PoE manager is designed to detect and disable disconnected powered devices (PDs) using DC disconnection methods, as specified in the standards.

The PD69208/4 provides real-time PD protection through the following mechanisms: overload, underload, over voltage, and short-circuit. The PD69208/4 share the same design, package, and features. The only difference between the PD69208 and PD69204 is the number of ports.

An evaluation board (part number: PD-IM-7648) can be ordered. A layout guideline for a PoE system based on PD69208/4 is also included in this document.

2.1 Features

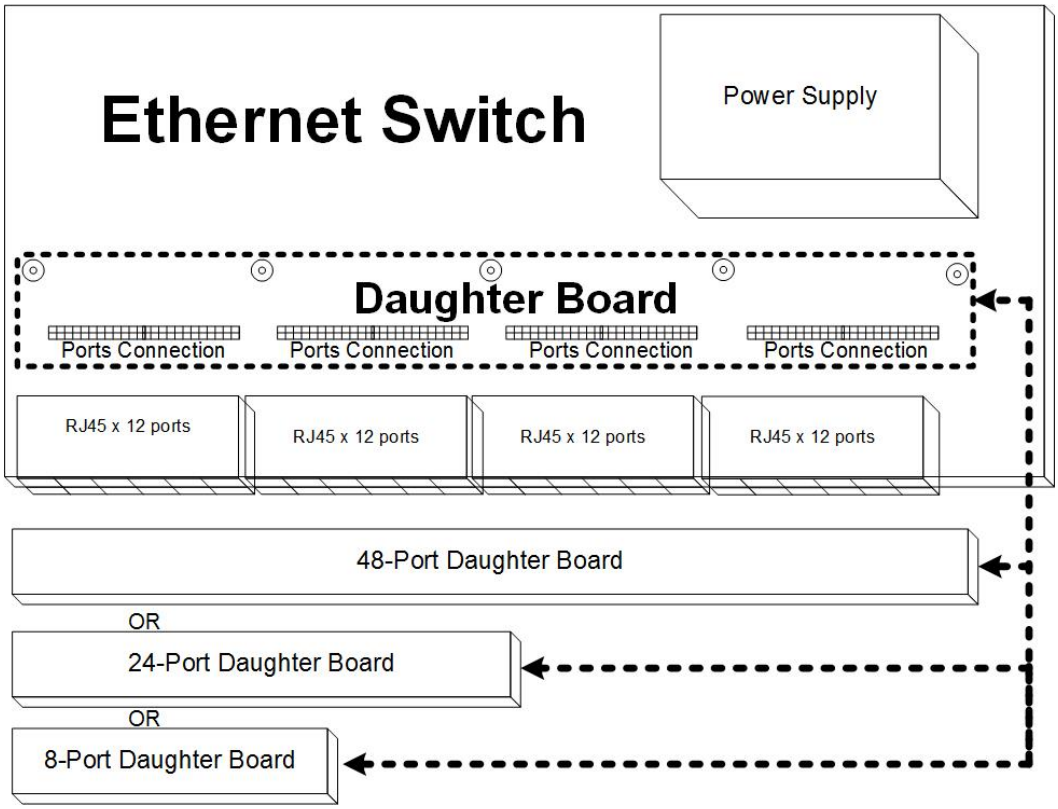
- IEEE 802.3af-2003 standard compliant
- IEEE 802.3at-2009 standard compliant
- Power over HDBaseT standard compliant (60 W/95 W)
- Configurable AT/AF modes
- Configurable standard/reduced capacitor detection mode
- Supports pre-standard PD detection
- Supports Cisco devices detection
- Single DC voltage input (44 V_{DC}–57 V_{DC})
- Two- and three-event classification
- Voltage monitoring/protection
- Low power dissipation
- Internal sense resistor (0.1 Ω)
- Internal MOSFET with low R_{DS_ON} (~0.24 Ω)
- Internal power on reset
- Only one external front-end component per port
- Includes reset input from hosting system
- Four direct address configuration pins
- Continuous port monitoring and system data
- Configurable load current setting
- On-chip thermal protection
- Built-in 3.3 V_{DC} and 5 V_{DC} regulators
- Emergency power management supporting sixteen configurable power banks
- Can be cascaded to up to 12 PoE devices (48 logical ports in 4 pairs configuration)
- Supports 4-pair connection (PD69208T4)
- Wide temperature range: –40 ° to 85 °C
- MSL3
- RoHS compliant
- Supports I^2C and UART communication and software update

2.2 Integration

The system described is destined for a 48-port switch, feeding power over two pairs for each port. Any combination of PD69208 and PD69204 can be implemented with up to 12 chips. The same design can be applied to 1–12 PoE managers controlling eight ports each (from 8 ports to 96 ports in multiples of 8) or with PD69204 in multiples of 4 ports.

The PoE system board can easily be integrated on top of a switch, providing the capability to add any PoE application while using different daughter applications.

Figure 1 • PoE Daughter Board Integration



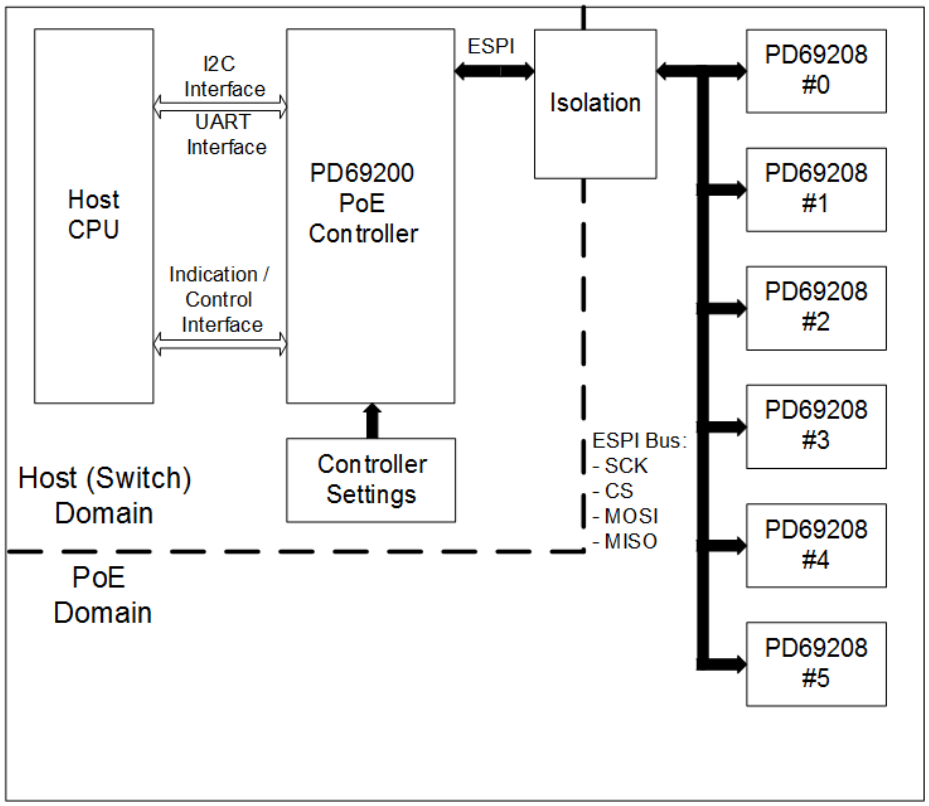
3 Functional Descriptions

A typical application includes the following blocks:

- PoE circuit for 48 ports, based on six PD69208.
- Controller circuit, used to initialize, control, and monitor each of the PD69208 through an internal enhanced serial peripheral interface (ESPI) isolated bus. The PoE controller communicates with the host CPU through a non-isolated UART or an I²C interface.
- Isolation circuit for ESPI bus.

This is shown in the following illustration.

Figure 2 • 48-port Configuration Block Diagram



3.1 General Circuit Description

The 48-port configuration for a PoE system shown in the previous illustration (see page 5) is comprised of six PoE manager circuits (PD69208) controlled by a PoE controller (PD69200). The PoE controller utilizes the ESPI bus to control the PoE managers. PoE operations are automatically performed by PoE manager circuits, while the PoE controller performs power management and other tasks. A configuration of 96 ports (over two pairs of wires per port) or 48 ports (over four pairs of wires per port) is also possible using 12 PoE manager circuits (PD69208) controlled by a single PoE controller (PD69200).

3.1.1 Communication Interfaces

Communication between the host CPU and the local PoE controller is performed through an UART or an I²C interface. For more information, refer to the *Serial Communication Protocol* User Guide (PD69200_UG_COMM_PROT), document number PD-000300095.

3.1.2 Communication Flow

The host CPU issues commands, utilizing a dedicated serial communication protocol to the PoE controller.

The PoE controller converts the serial communication protocol to ESPI communication and sends it through isolated ESPI lines to the appropriate PD69208. This isolation is a basic requirement of IEEE PoE standards.

3.1.3 ESPI Bus

The ESPI bus, used for internal communication, includes the following lines:

- Master out/slave in (MOSI) provides communication from the PoE controller to the PD69208.
- Master in/slave out (MISO) provides communication from the PD69208 to the PoE controller.
- SCK is the serial clock generated by the controller.
- Chip select (CS) is utilized by the PoE controller to transmit data simultaneously to all PD69208 ICs, while only the chosen PoE manager responds back.

3.1.4 Control

An xReset_IN control signal driven by the host CPU is used to reset the PoE system. An xDisable_ports control signal driven by the host CPU is used to disable all PoE ports at once.

For more information, see Control and Indication Signals (see page 8).

3.1.5 Indications

An xSystem_ok signal is generated by the PoE controller, indicating that the main input voltage is within range. This pin is determined by a 15-byte serial communication protocol.

An xInt_out interrupt signal is designed to indicate PoE events such as port on, port off, port fault, PoE manager fault, voltage out of range, and so on.

An xI2C_Message_Ready indicates a signal message is ready to be read by the host.

For the full list of interrupt events, refer to the *Serial Communication Protocol* User Guide (document number PD-000300095).

3.1.6 Main Supply

The PoE system operates within a range of 44 V_{DC} to 57 V_{DC} (IEEE 802.3at port's range is 50 V_{DC} to 57 V_{DC}). To comply with UL SELV regulations, the maximum output voltage should not exceed 60 V_{DC}.

3.1.7 Hot-swap Circuit

The hot-swap circuit is crucial for applications where DC hot plug is present because the absence of such a circuit will cause the DC voltage to oscillate (ring), which leads to application malfunctions. The selected MOSFET is rated for 80 A and the R_{DS} is 10 mΩ. For more information, see Hot-swap Circuit (see page 18).

For more information on timing and power loss in the MOSFET, refer to the hot-swap test report (PD-000308569).

3.1.8 Grounds

Several grounds are utilized in the system: PoE domain analog, PoE domain digital, chassis, and host domain floating.

Digital and analog grounds are the same ground, electrically. However, to reduce noise coupling, grounds are physically separated and connected only at a single point.

The chassis ground is connected to the switch's chassis ground. This ground plane should be 1500 V_{rms} isolated from PoE circuitry.

The PoE controller relates to the host domain floating ground, which is isolated from the PoE domain grounds.

3.1.9 5 V DC and 3.3 V DC Regulators

Each PD69208 has a 5 V_{DC} and a 3.3 V_{DC} regulator for internal IC circuitry and can provide up to 6 mA to be utilized for powering components in the PoE domain. The 5 V has been powered from V_{MAIN} by an internal regulator and the 3.3 V has been powered from the 5 V with another internal regulator. In order to minimize time between the 5 V and 3.3 V rise during the first system power up, a 4.7 µF capacitor should be placed between those pins (pins 20 and 22).

An external boost transistor can be added to the 5 V_{DC} regulator's output (instead of R166) to increase the current, as shown in Boost Transistor to the 5 V_{DC} Regulator (see page 18). The transistor can provide a total of 30 mA to the PoE controller and to the isolation circuits. This total current is the sum of the 5 V and 3.3 V currents. All external components in this circuitry must also be isolated from the switch circuitry by 1500 V_{rms}.

Using a boost transistor reduces the internal heat generated by the PD69208.

3.2 Detailed Circuit Description

The following sections provide a detailed description of the circuit.

3.2.1 Communication Interfaces/Isolation

There are two communication interfaces in this circuitry.

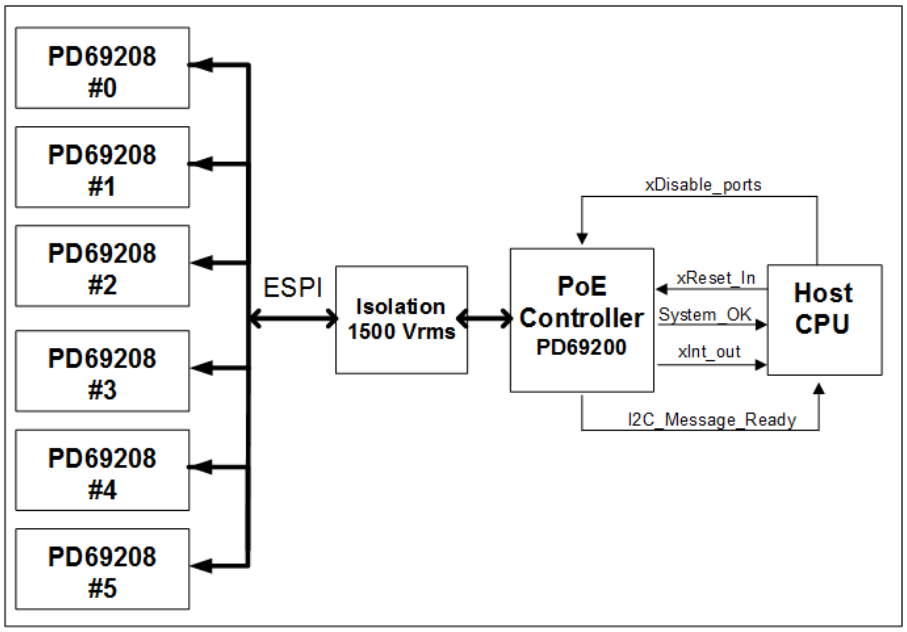
- An interface between the Ethernet switch and the PoE controller; this interface is an I^2C or an UART interface and does not require isolation.
- An interface between the PoE controller and PoE managers with 1500 V_{rms} isolation; this interface is a standard SPI.

The isolation circuit is comprised of a digital isolator, as shown in Digital Isolator (see page 17). Each side of the isolator circuitry is fed by a separate power supply.

3.2.2 Control and Indication Signals

Control/indication signals are of the single hardware lines type, running between the host CPU and PoE controller, as the following illustration shows.

Figure 3 • Control and Indication Signals



3.2.2.1 Control Signals

There are two control lines driven by the host CPU to the PoE controller.

- xDisable_ports: Disables all PoE ports. When the PoE controller detects low level voltage at PD69200 pin #31, it sends a disable command through ESPI to all PoE manager ports.
- xReset_In: Resets the PoE controller and all PoE managers. When the PoE controller detects low level voltage at PD96200 pin #19, it enters reset mode and all of its output pins switch to tri-state mode. When xReset_In line returns to high, the PoE controller initializes and sends a RESET command to the PoE managers through the ESPI bus. xReset_In is also used by the PoE controller watchdog to reset itself, and so the host should drive a reset using an open-drain output and a pull up to eliminate conflict.

In case the host drives the reset pin from a push-pull output, a 1 KΩ resistor should be located between the host's output to the PD69200's xReset_in pin.

3.2.3 PoE Controller Circuitry

The following section describes the PD69200 PoE controller circuitry, which is shown in PD69200 PoE Controller Circuitry (see page 16).

3.2.3.1 Interface to PoE Manager

The PoE controller features 1 Mbps ESPI for each of the PoE managers, and a communication interface with host CPU through UART or I²C protocol.

3.2.3.2 Interface to Host

UART (set to 19200 bps) or I²C (up to 400 KHz) communication between the host CPU and PoE controller are managed by setting the PoE controller's address, pin #22 (I2C_ADDR). For the UART and I²C communication address table, see Serial Communication Configuration (see page 12).

3.2.3.3 Clock

The PoE controller runs at 47.972 MHz, facilitated by an internal clock.

3.2.3.4 Supply

The PoE controller requires stable, filtered power for its operation coming from the host (3_3V_iso), so a number of decoupling capacitors are included in the design (C56, C71, C92). The expected current consumption of the PoE controller circuitry should be below 20 mA.

3.2.3.5 Self Reset

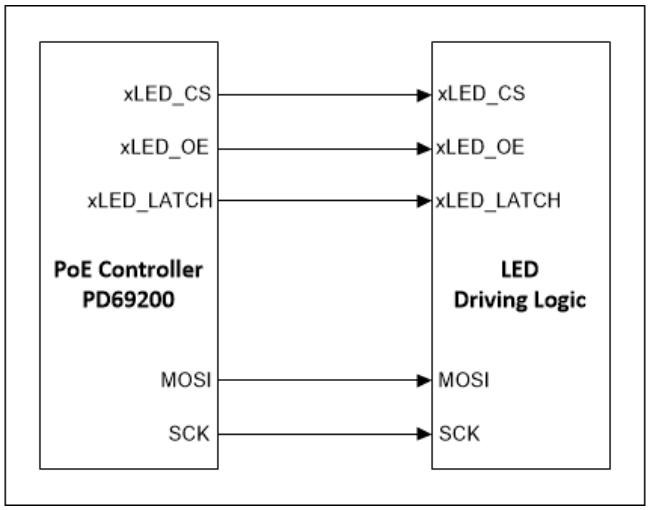
As required by the application, the PoE controller can reset itself. This reset can also be performed by an external source utilizing the xReset_In signal (usually by the host controller). If the host utilizes XReset_in, it should drive a reset using an open-drain output and a pull up to eliminate conflict.

3.2.3.6 LED Support

LED support for port status indication is accomplished by utilizing the ESPI bus (SCK and MOSI), xLED_CS, xLED_OE, and xLED_Latch signals. Bus behavior is 1 Mhz synchronous serial communication (clock and data) in one direction (write only) that transmits the status of up to 96 ports. For more details, refer to Technical Note 218 (catalog number PD69200_TN_218).

The following illustration shows the SPI bus and LED support.

Figure 4 • SPI Bus and LED Support



3.2.3.7 Emergency Power Management

PoE circuits can be powered by up to four separate power supplies. It is recommended that each power supply be capable of generating a logic signal, indicating its operate/fail status. For more information, see Power Good (see page 10).

The following table lists the pins used for emergency power management.

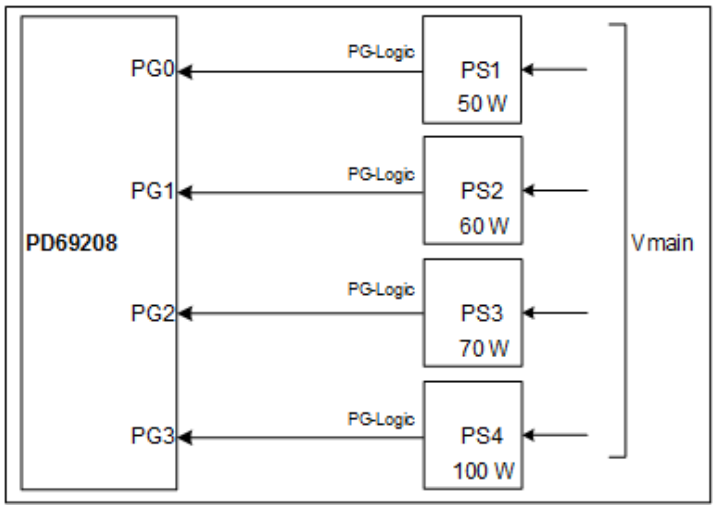
Table 1 • Emergency Power Management Pins

PD69208 Pin Number	Signal	Description
56	PG0	Power Good 0
41	PG1	Power Good 1
46	PG2	Power Good 2
47	PG3	Power Good 3

The PoE circuit allocates power to the system in 16 power levels (power banks) programmed by users. Power bank values are based on each supplies' available power and on the state of the logic signals PG[0..3] coming from power supplies. If PG pin is not used, the pin must be connected to GND or VDD.

The following illustration shows the connections between the power supplies' logic signals and the PoE manager.

Figure 5 • Power Good



3.2.4 PoE Manager Circuitry

The PD69208 performs a variety of internal operations and PoE functions, requiring a minimal number of external components. Each PD69208 handles up to 8 ports.

The PoE manager #0 with its related components for an 8-port configuration is shown in PD69208 Circuitry for PoE Manager #0 (6 PL) (see page 17). For 48 ports, this is circuitry is duplicated 6 times.

3.2.4.1 Reference Current Source

The reference for internal voltages within the PD69208 is set by a precision resistor (R60), 28.7 kΩ 1%.

In a PoH and IEEE 802.3bt system, the precision resistor should be 0.1%.

3.2.4.2 Sense Resistors

The PD69208 provides an internal sense resistor of 100 mΩ to each port sense pin. This resistor is utilized to measure port current.

3.2.4.3 Front-End Components

A single capacitor per port is the only external front-end component used. The capacitor value can be between 22 nF and 220 nF.

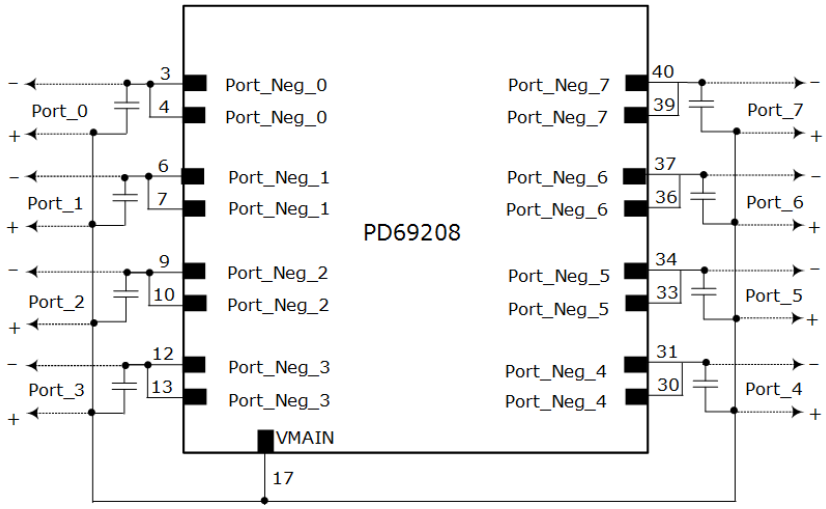
Using 220 nF is recommended in order to improve the PSE immunity to 50 Hz/60 Hz noise, which might influence the IEEE detection.

All other components (such as reverse diode, port protection, sense resistor, and switching MOSFET) are internal.

Fuses per port are not required for use in circuits with a total power level of up to 3 kW, as the PD69208 is designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1.

The following illustration shows the front-end components of an 8-port configuration.

Figure 6 • 8-Ports Front End Components



3.2.4.4 Line Transformer

A line transformer that is dedicated to PoE (with the desired PoE current for the specific applications in mind) should be used.

3.2.5 Serial Communication Host-Controller

The PoE controller can communicate with the hosting system using UART or I²C communication. The PoE controller may be one of few controlled devices on the I²C communication bus reporting to the host, requiring the user to configure a dedicated address for the PoE controller. This is done by selecting a value for R93 (see PD69200 PoE Controller Circuitry (see page 16) for more information). This resistor sets the analog level into pin #22 (I2C_ADDR_Meas_ADC0), as specified in the following table.

Table 2 • Serial Communication Configuration

I²C Address	Address (Hex)	R93 (Ω)
#0	UART	
#1	0x4	97600
#2	0x8	53600
#3	0xC	35700
#4	0x10	25500
#5	0x14	19100
#6	0x18	14700
#7	0x1C	11300
#8	0x20	8870
#9	0x24	6810
#10	0x28	5230
#11	0x2C	3920
#12	0x30	2800
#13	0x34	1870
#14	0x38	1020
#15	0x3C	324

3.2.5.1 UART

An Rx signal should be connected to pin #11 of the PoE controller.

A Tx signal should be connected to pin #12 of the PoE controller.

A pull-up resistor is required on the UART communication line (for more information, see PD69200 PoE Controller Circuitry (see page 16)).

3.2.5.2 I 2 C

An SDA signal should be connected to pin #21 of the PoE controller.

An SCL signal should be connected to pin #20 of the PoE controller.

A pull-up resistor is required on the I²C communication line (pins 20 and 21).

3.2.6 Ground Interface Connection (AGND)

The power supplies' ground connector enables the current a path back to the power supply. The ground connection should be capable of carrying all current back to power supplies.

3.2.7 Four-Pair Connectivity

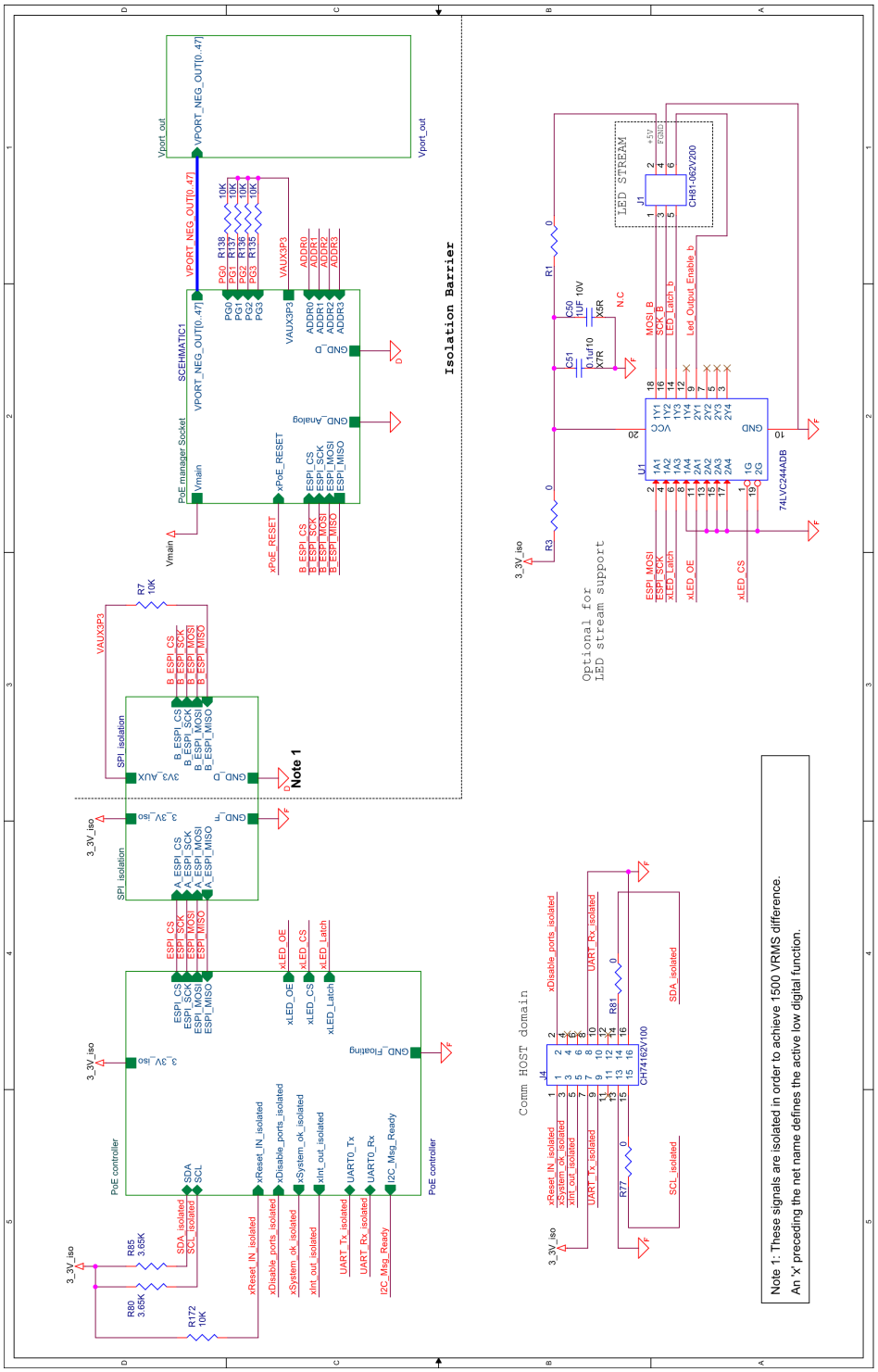
Designing a PoE port delivering power to over RJ45 four pairs of wires is quite easy by utilizing the PD69208T4. Just connect any two ports of the PD69208T4 to a single RJ45 connector and configure the PD69200 accordingly. The two ports utilized for the the four-pair output terminal can be taken from the same PD69208T4 or from any two PD69208T4 ICs in the system. The PD69208T4 can deliver AT power (enabling delivery of 60 W over 4 pairs) or IEEE 802.3bt type 4/PoH power (delivering 95 W over 4 pairs).

The PD69200 configuration process is further explained in the *Serial Communication Protocol* User Guide (document number PD-000300095).

4 Schematics

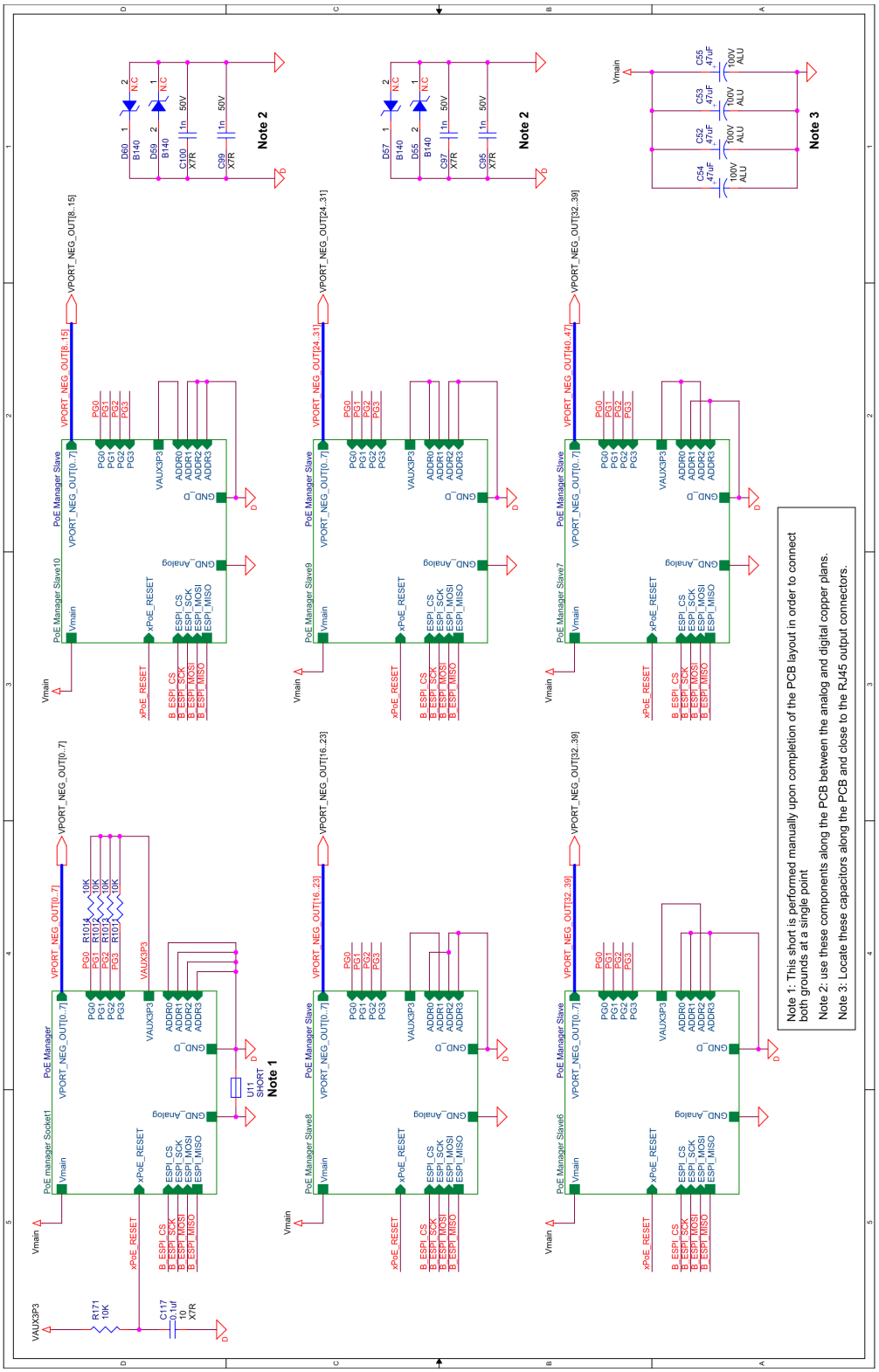
The following illustration shows the main blocks of a 48-port system. For descriptions and more information, see Vmain Capacitors (see page 30).

Figure 7 • 48-port System Main Blocks



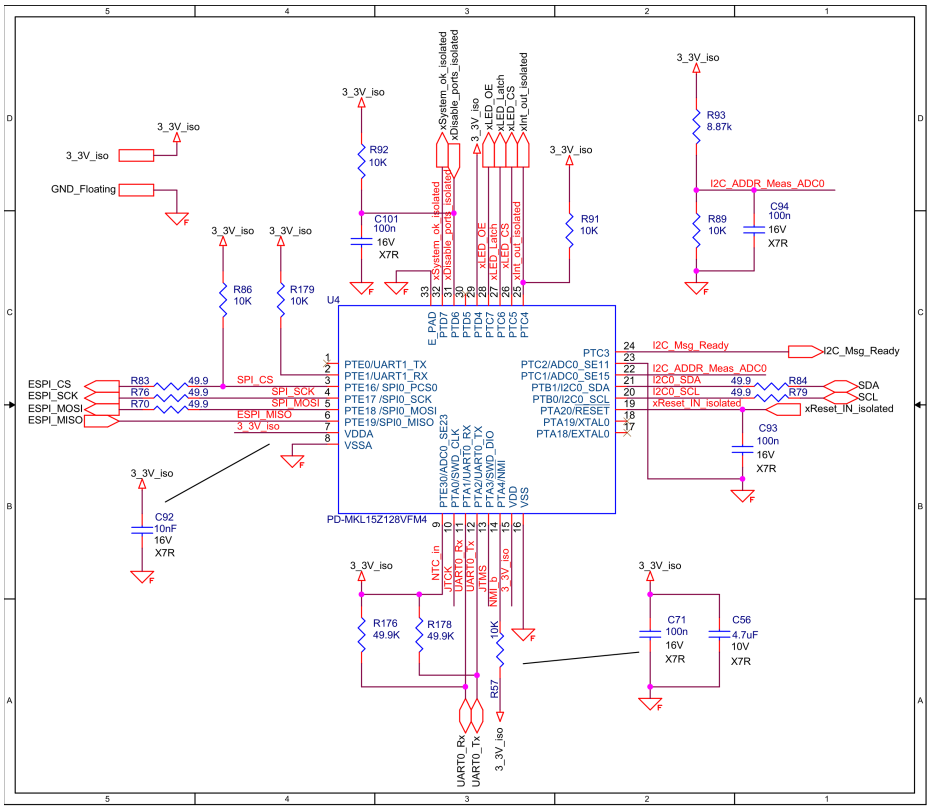
The following illustration shows the 6 PD69208 PoE manager circuitry. For descriptions and more information, see Vmain Capacitors (see page 30).

Figure 8 • 48-port PoE Manager Blocks



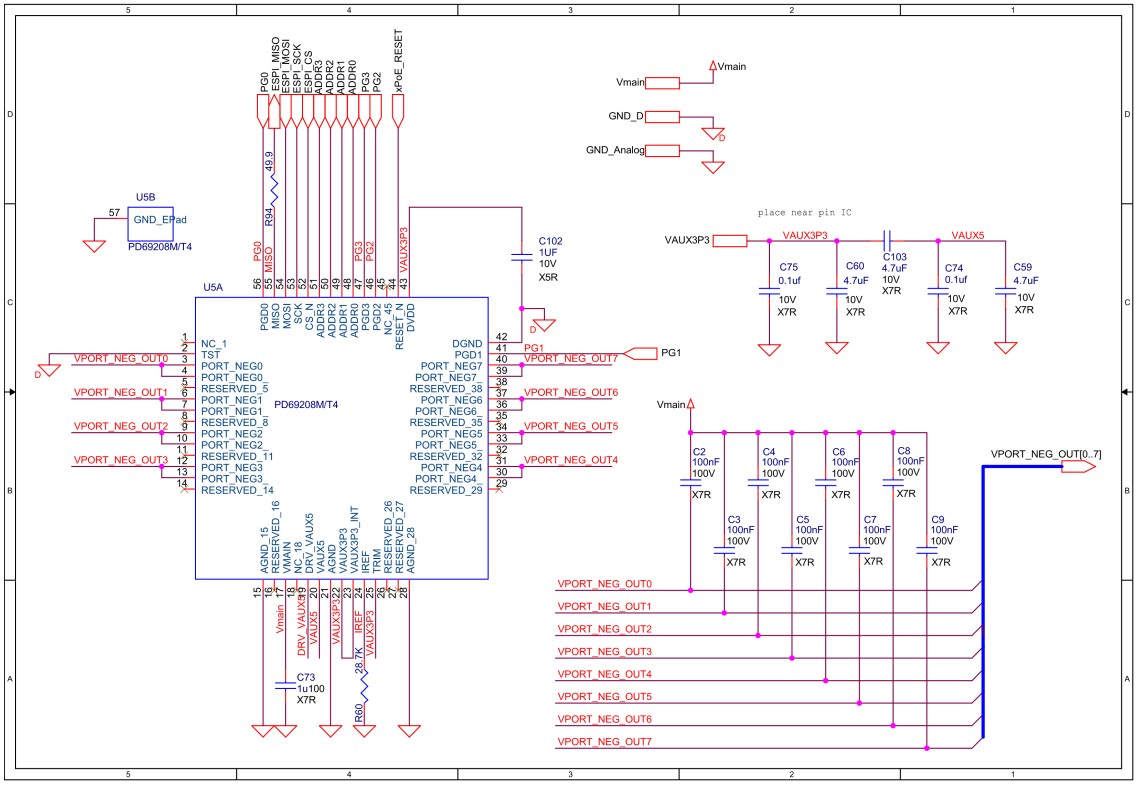
The following illustration shows the PD69200 PoE controller circuitry. For descriptions and more information, see PoE Controller Circuitry (see page 8).

Figure 9 • PD69200 PoE Controller Circuitry



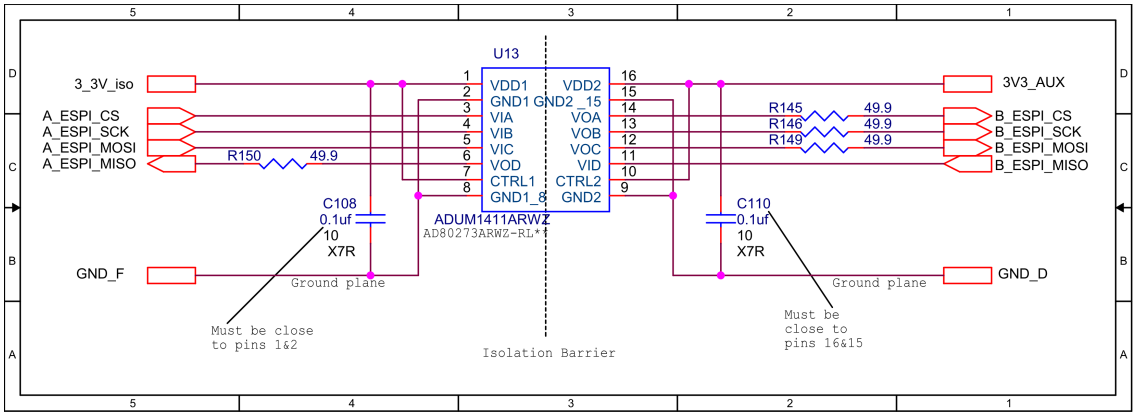
The following illustration shows the PD69208 circuitry for PoE manager #0. For descriptions and more information, see PoE Manager Circuitry (see page 10).

Figure 10 • PD69208 Circuitry for PoE Manager #0 (6 PL)



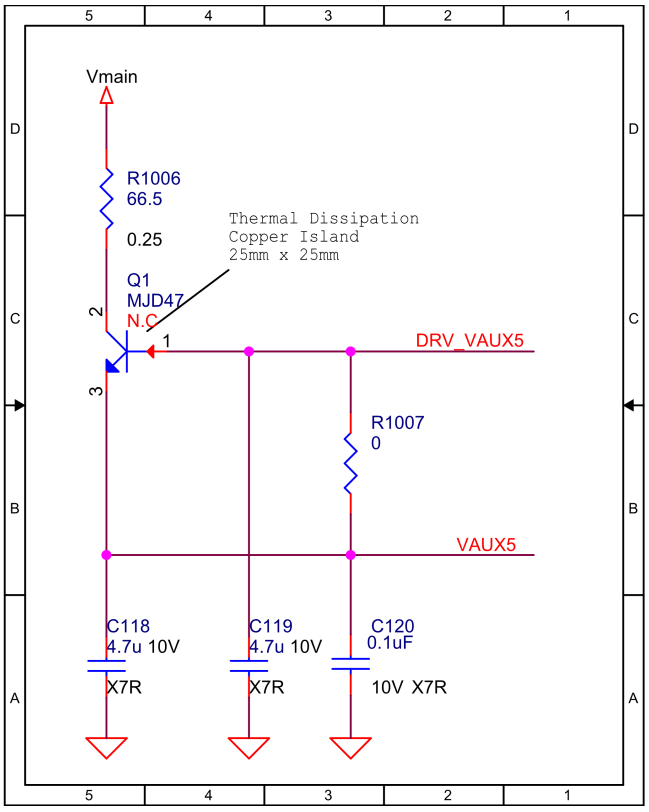
The following illustration shows the digital isolator. For descriptions and more information, see Communication Interfaces/Isolation (see page 7).

Figure 11 • Digital Isolator



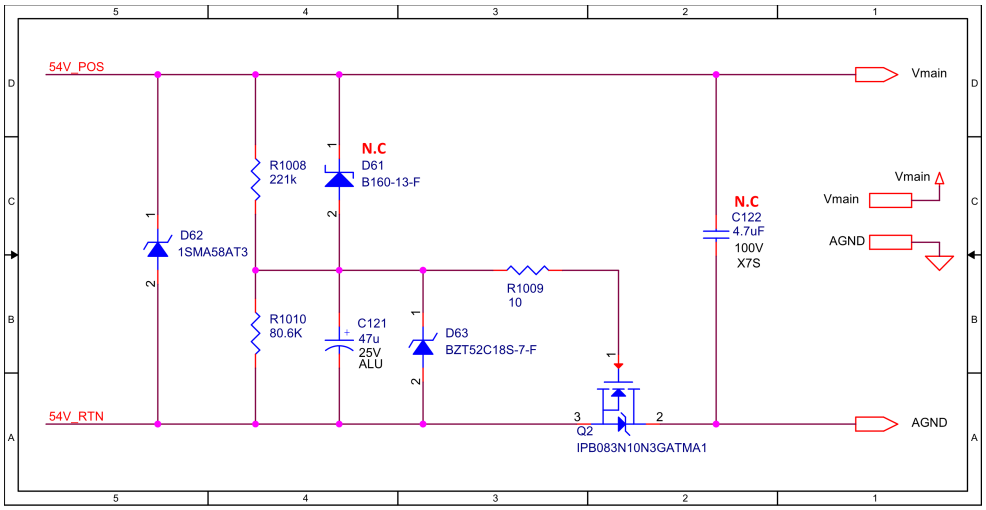
The following illustration shows the boost transistor to the 5 V_{DC} regulator. For descriptions and more information, see 5 V_{DC} and 3.3 V_{DC} Regulators (see page 7).

Figure 12 • Boost Transistor to the 5 VDC Regulator



The following illustration shows the hot-swap circuit. For descriptions and more information, see Hot-swap Circuit (see page 6).

Figure 13 • Hot-swap Circuit



5 Bill of Materials for a PoE System

The following tables list the bill of materials for a PoE system.

Table 3 • Main Block Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C52, C53, C54, C55	47 µF	Capacitor ALU 47 µF 100 V 20% 8 x 11.5 105 °C	Rubycon	100PX47M T7 8X11.5
4	C95, C97, C99, C100	1 nF	Capacitor X7R, 1 nF 50 V 10% 0402	Murata	GRM155R71H102KA01D
2	C51, C117	0.1 µF	Capacitor 0.1 µF 10 V X7R 10% 0402	Murata	GRM155R71A104KA01J
4	D55, D57, D59, D60	B140	Schottky diode 40 V 1 A SMAT	Diodes Inc.	B140
2	R80, R85	3.65 KΩ	3.65K 62.5 mW 1% 0402	Yageo	RC0402FR-073K65L
3	R171, R151, R172	10 KΩ	10K 1% 62.5 mW 0402	Vishay	CRCW040210K0FKED
2	C108, C110	0.1 µF	Capacitor 0.1 µF 10 V X7R 10% 0402	Murata	GRM155R71A104KA01J
4	R145, R146, R149, R150	49.9 Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L
1	U13	AD80273ARWZ	IC digital isolator SO16	Analog Devices	AD80273ARWZ-RL**

**Special part number for Microsemi PoE applications; preferential pricing for Microsemi customers.

Table 4 • PoE Controller Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
4	C71, C93, C94, C101	100 nF	Capacitor 100 nF 16 V 10% X7R 0603	Samsung	CL10B104KO8NNNC
1	C56	4.7 µF	Capacitor 4.7 µF 10 V 10% X5R 0805	Taiyo Yuden	LMK212BJ475KD-T
1	C92	10 nF	Capacitor X7R 10 nF 16 V 10% 0402	Samsung	CL05B103KO5NCNC
6	R57, R86, R89, R91, R92, R179	10 KΩ	10K 100 mW 1% 0603	Samsung	RC1608F1002CS
2	R176, R178	49.9 KΩ	49.9K 125 mW 1% 0805	Samsung	RC2012F4992CS
5	R70, R78, R83, R79, R84	49.9 Ω	49.9R 1% 62.5 mW 0402	Yageo	RC0402FR-0749R9L

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	R93	8.87 KΩ	8.87K 125 mW 1% 0805	Yageo	RC0805FR-078K87-L
1	U4	PD69200	PoE PSE controller	Microsemi	PD69200X-GGGG

Table 5 • PoE Manager Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
8	C2–C9	100 nF	Capacitor 100 nF 100 V 10% X7R 0805	Samsung	CL21B104KCFSFNE
3	C59, C60, C103	4.7 µF	Capacitor 4.7 µF 10 V 10% X5R 0805	Murata	GRM219R61A475KE19D
2	C74, C75	0.1 µF	Capacitor 0.1 µF 10 V X7R 10% 0402	Murata	GRM155R71A104KA01J
1	C102	1.0 µF	Capacitor 1.0 µF 10 V X5R 10% 0402	Panasonic	ECJ-0EB1A105M
1	C73	1 µF	Capacitor 1 µF 100 V X7R 1210 10 %	AVX	12101C105K4T2A
1	R60	28.7 KΩ	28.7K 125 mW 1% 0805 (For PoH and IEEE 802.3bt, 99 W should be 0.1%)	Vishay	CRCW080528K7FKEA
1	R94	49.9 Ω	49.9R 1% 62.5 mW 0402	Bourns	CR0402-FX-49R9-ELF
1	U5	PD69208	8 Port PSE PoE Manager SMT	Microsemi	PD69208M/T4

Note: Fuses per port are not required for use in circuits with a total power level of up to 3 kW. This is because PD69208 is a UL 2367 (category QVRQ2)-recognized component and fulfills limited power source (LPS) requirements of the latest editions of IEC60950-1 and EN60950-1.

Table 6 • Hot-swap circuit Components

Quantity	Reference	Value	Description	Manufacturer	Manufacturer's Part Number
1	Q2	IPB083N10N3	MOSFET N-CH 100 V 80 A 8.3 mΩ TO263-3	Infineon	IPB083N10N3GATMA1
1	C121	47 µF	Capacitor ALU 47 µF 25 V 20% SMT	SUNCON	25CE47FS
1	R1008	221 KΩ	221K 1% 1/10 W 0603	Yageo	RC0603FR-07221KL
1	R1010	80.6 KΩ	80.6K 125 mW 1% 0603	ASJ	CR16-8062FL
1	D63	BZT52C18S-7-F	Diode Zener, 18 V 200 mW SOD323	Diodes Inc.	BZT52C18S-7-F
1	D62	1SMA58AT3	DIO TVS 58 V 40 A SRG400WPK SMA SMT	ON Semiconductor	1SMA58AT3

6 Layout Guidelines

This section provides detailed information and PCB design guidelines for the implementation of a 48-port PoE system, based on Microsemi's PD69208 8-channel PoE manager.

6.1 Isolation and Termination

According to the IEEE 802.3af and the IEEE802.3at standard, certain isolation requirements need to be met in all PoE equipment. In addition, EMI limitations should be considered, as specified in the FCC and European EN regulations. These requirements are taken into account by PoE switch vendors while designing the switch circuitry. However, when a PoE manager is integrated into a switch, special design considerations must be met due to the unique combination of data and power circuitries.

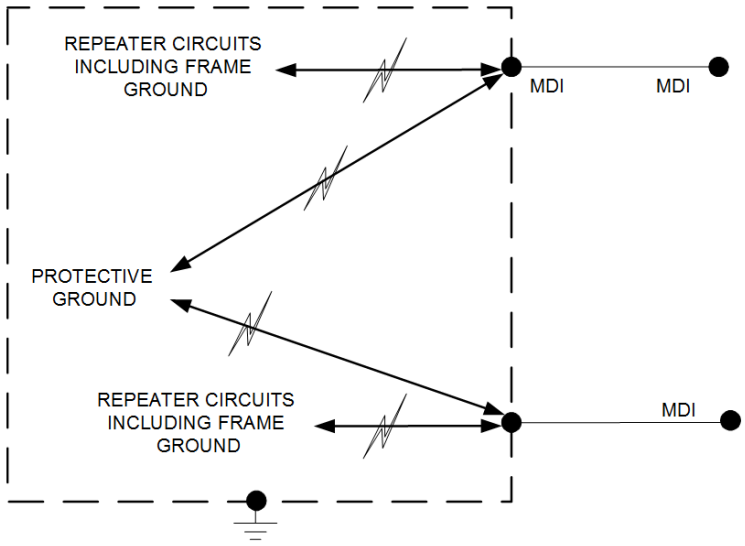
The following sections define these requirements and provide recommendations for their implementation in an effort to assist designers in meeting those requirements, while also integrating Microsemi's PoE chipset and its daughter boards.

6.1.1 Isolation

As specified in the IEEE PoE standards, 1500 V_{RMS} isolation is required between the switch's main board circuitry (including protective and frame ground) and the media dependent interface (MDI).

The following illustration shows the overall isolation requirements.

Figure 14 • Isolation Requirements



Reference to environment A

1. IEEE 802.3 Repeater 500 Vrms min. (27.5.3.1 ;9.7.1)
2. IEEE 802.3 Repeater, PMA to MDI 1500 Vrms min. (23.5.1.1)
3. UL1950: 1500 Vrms

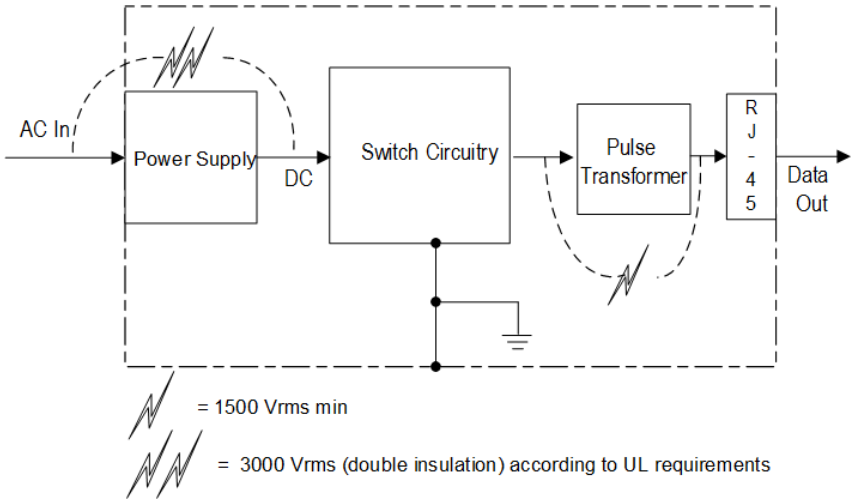
1500 =Vrms min.

PMA :Physical Medium Attachment
MDI :Media Dependent Interface

6.1.2 High Voltage Isolation

For a switch with no PoE circuitry, isolation requirements between the physical inputs and the data connectors are met by using an isolated AC/DC power supply and isolated pulse transformers, as shown in the following illustration.

Figure 15 • Standard Switch Circuitry

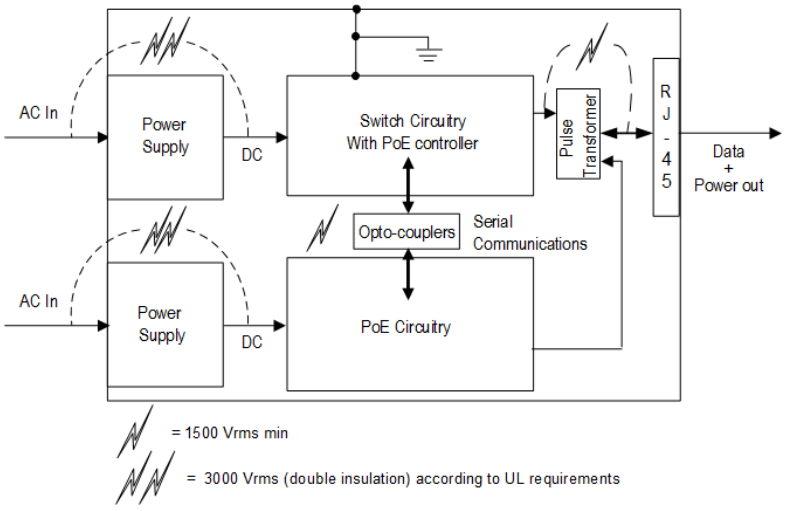


When integrating PoE circuitry into a switch, the output power can be supplied through the central tap of the pulse transformer's secondary side (unless power is provided over the spare pairs). This connectivity can bypass the pulse transformer's isolation if the PoE ground or DC input is connected to the switch's circuitry/ground.

To comply with these isolation requirements, the PoE managers must be isolated in regards to all other switch circuitries. Use one of the following methods:

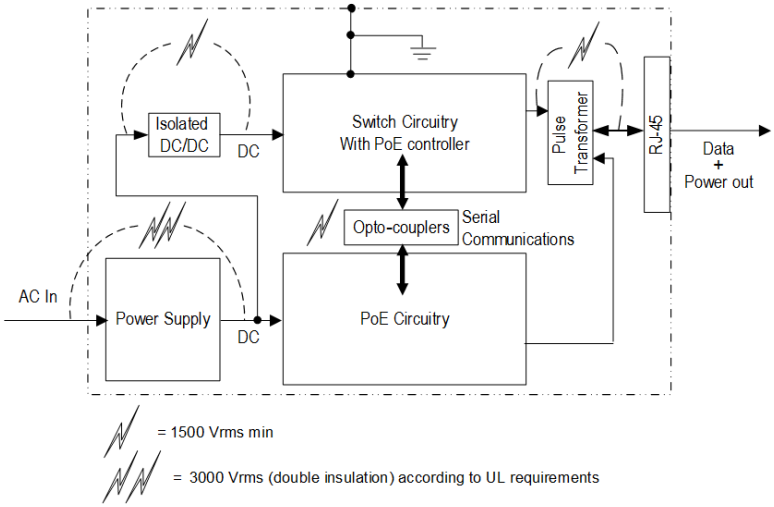
- A separate DC input for the switch and the PoE circuitry and isolated serial communication between the PoE circuitry and the switch circuitry, as shown.

Figure 16 • Switch Circuitry with Two DC Source



- A single DC input (separate power supplies) for both the switch and PoE circuit as well as additional or integrated isolated DC/DC circuitry for the switch input and isolated serial communication port between the PoE circuitry and the switch's circuitry, as shown.

Figure 17 • Switch Circuitry with a Single DC Source

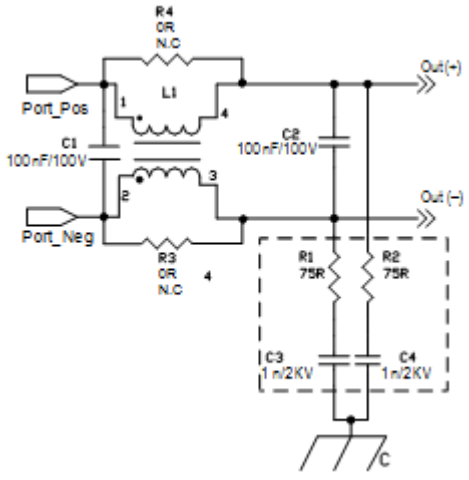


To maintain 1500 V_{RMS} isolation between two adjacent layers of a NEMA FR-4 multi-layer PCB, a minimum of 15 mils isolation thickness is recommended to provide a safe margin for hi-pot requirements.

6.1.3 PoE Output Ports Filtering and Terminations

A switch normally creates a noisy environment. To meet EMI requirements, high filtering and line terminations may be needed when connecting the PoE circuit outputs to the switch circuitry, as shown in the following illustration.

Figure 18 • Recommended EMI Filter



Note that in most PoE systems, it is recommended to use 0 Ω resistors for R1 and R2. However, certain systems may benefit from 75 Ω resistors. Filtering provisions should be made. In quiet PoE systems, the EMI filter can be replaced (bypassed) using R3 and R4.

A circuitry for the recommended filter includes:

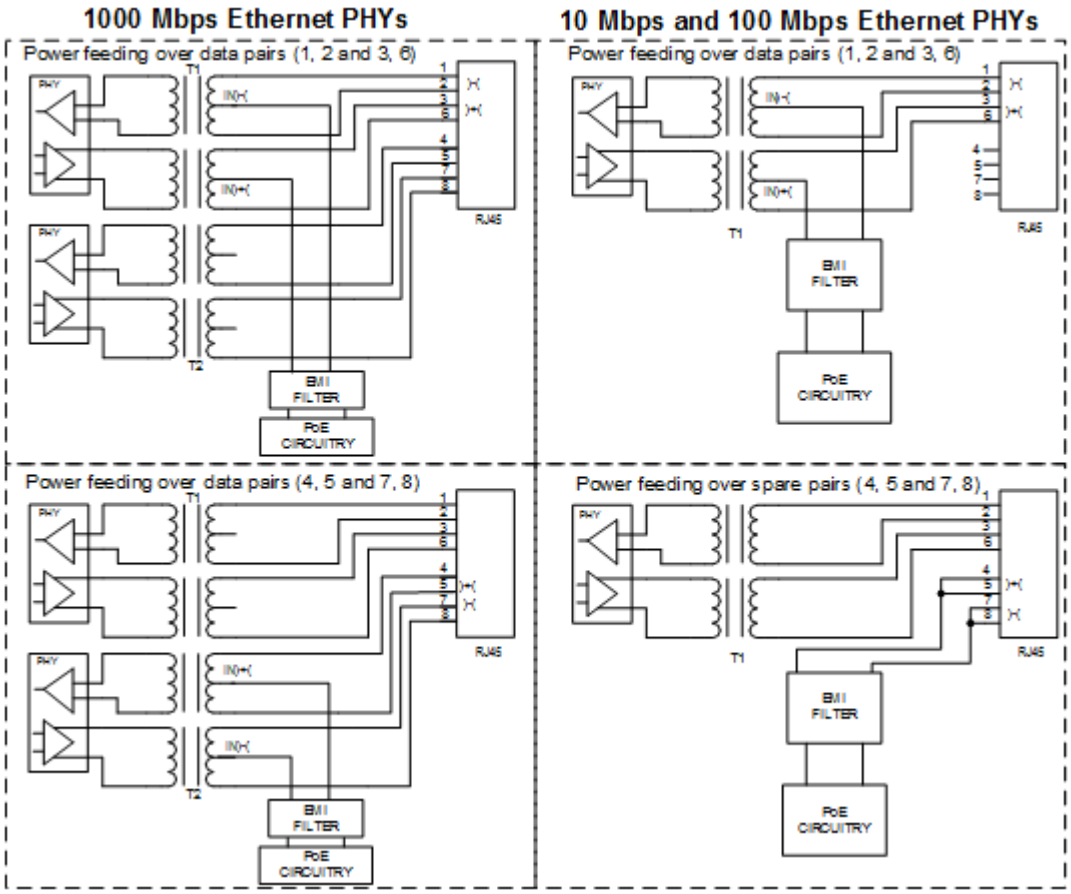
- A common mode choke for conducted EMI performances (such as ICE CS01 series)
- Output differential cap filter for radiated EMI performances
- Y-capacitive/resistive network to chassis

Because each system is a unique EMI case, this circuit is a good starting point for EMI suppression.

Note: For best EMI performance and to avoid additional noise accumulated on the lines between the filter and the port connectors, it is recommended to implement this circuitry on the switch's main board, located as close as possible to the port connectors.

As specified in the IEEE PoE standards, PoE output power can be supplied over the data pairs or the spare pairs. Both methods are shown in the following illustration, which shows an MDI-X (or Auto MDI-X) connection, associated with the switch.

Figure 19 • Output Ports Design Details



6.1.4 Isolating the Stacked Modular Jack Assembly

The IEEE PoE standards require 1500 V_{RMS} isolation between PoE voltages and frame ground (EGND). Note that RJ45 jack assemblies have a metal cover of 80 mils that almost reaches to the PCB surface. Maintain an 80 mils traces clearance between EGND traces for the RJ45 modular jack assembly metal covering and adjacent circuit paths and components. To prevent 1500 V_{RMS} isolation violation, it is necessary to provide layout clearances of PoE traces on the top layer, in the vicinity of the RJ45 connector assemblies.

PoE technology involves voltages as high as VDC. Thus, plan adjacent traces for 100 VDC operational creepage. Operational creepage should be maintained to prevent breakdown between traces carrying these potentials.

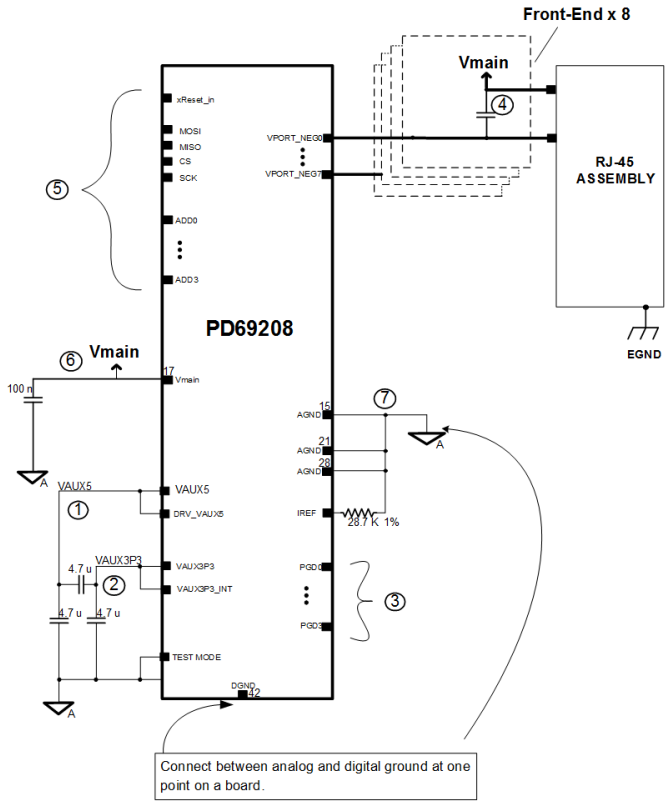
6.2 Guidelines

Microsemi's PD69208 PoE manager is designed to simplify the integration of PoE circuitry into switches based on the IEEE PoE standards. The pinout arrangement has been configured for optimal PCB routing.

The following illustration shows the various circuits and elements surrounding the PD69208 PoE manager. This block diagram includes the following peripheral elements, identified by numbers:

- 5 V voltage source (VAUX5) (1)
- 3.3 V voltage source (VAUX3P3) (2)
- Power good inputs (3)
- Output capacitor used for filtering (4)
- ESPI bus, ESPI address lines (5)
- Vmain input (6)
- Analog ground/AGND (7)

Figure 20 • Component Identification for PD69208 Circuitry



Note: The VAUX5 supply may include an external transistor connected to pin 20, to increase current drive for external circuitry. To prevent heat from being transferred to the PD69208, place this transistor away from the PoE managers.

6.2.1 Locating PoE Circuitry in a Switch

To minimize the length of high current traces as well as RFI pick-up, place the PoE circuitry as close as possible to the switch's pulse transformers. The circuit can be fully integrated into the switch's PCB, or can be easily placed on top of the switch's using a daughter board. Typical integration of PoE modules inside a switch is shown in the following illustrations.

Figure 21 • PoE Circuitry Inside the Switch

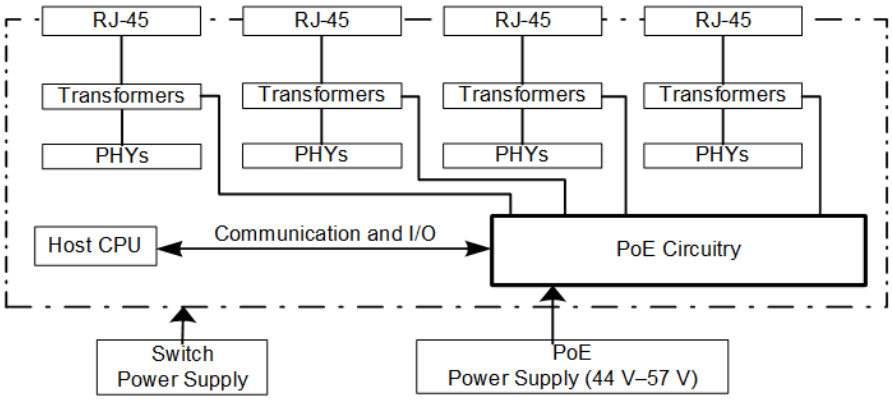
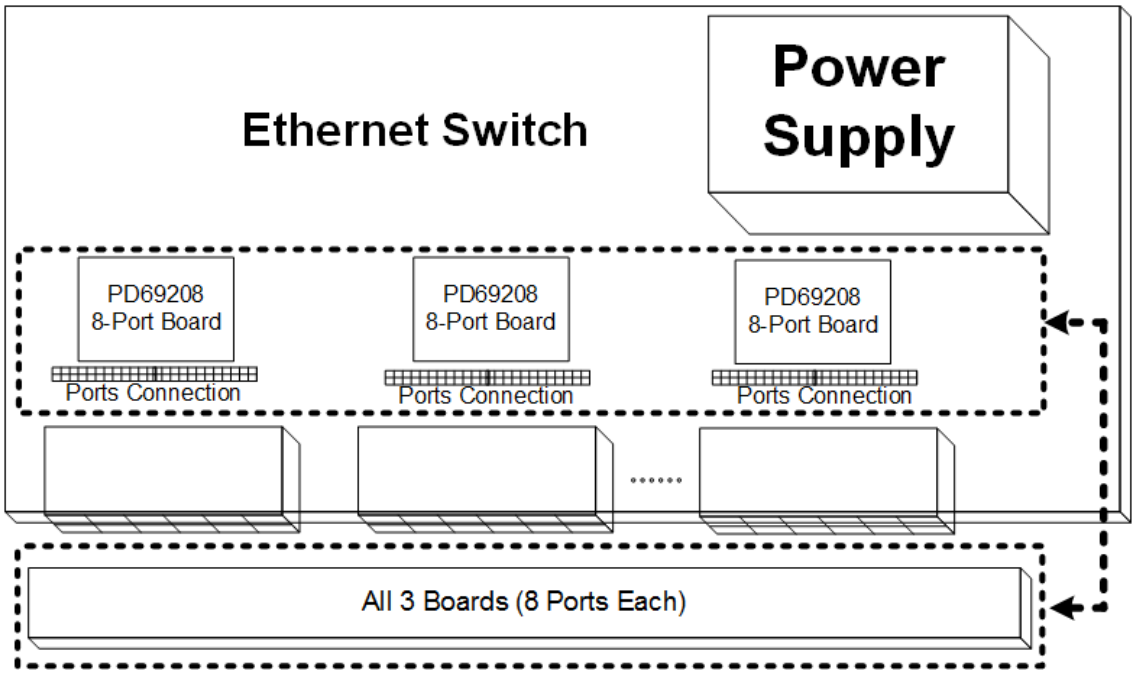


Figure 22 • PoE DB Circuitry Inside the Switch



6.2.2 Ground and Power Planes

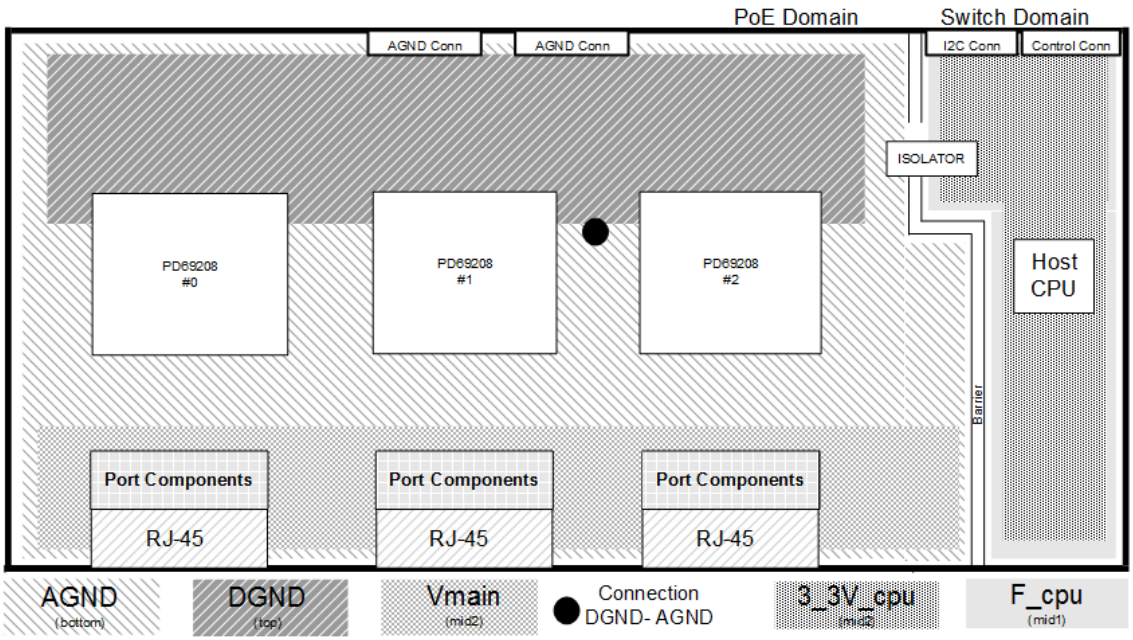
Because the PoE solution is a mixed-signal (analog and digital) circuitry, special care must be taken when routing the ground and power signals lines.

The reference design assumes a four-layer board: top, mid1, mid2, and bottom. The main planes are Vmain/AGND and DGND.

Ground planes are crucial for proper operation and should be designed in accordance with the following guidelines.

- Separate analog and digital grounds, with a gap of at least 40 mils.
- Analog ground plane (AGND) is utilized to transfer the heat generated by the PD69208.
- The AGND should be located on external layer.
- Earth ground is used to tie in the metal frame of the RJ45 connectors. This ground is to be routed separately and connected to the switch's metal chassis/enclosure.
- To prevent ground loop currents, use only a single connection point between the digital and analog grounds, as the following illustration shows.

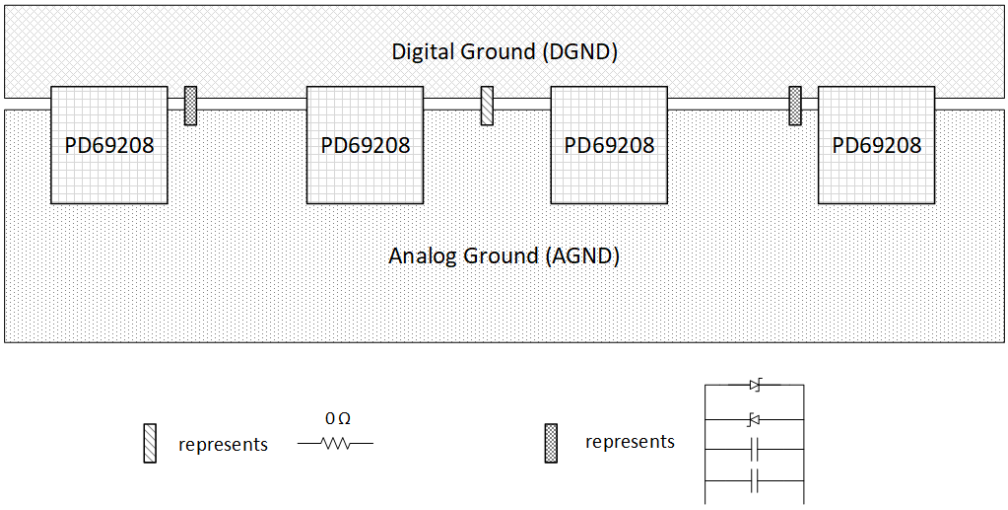
Figure 23 • Ground and Power Planes



- To connect various digital ground (DGND) points and to enable stable impedance to the ESPI bus traces, extend the DGND surface under pins 41–56 of the PD69208 managers.

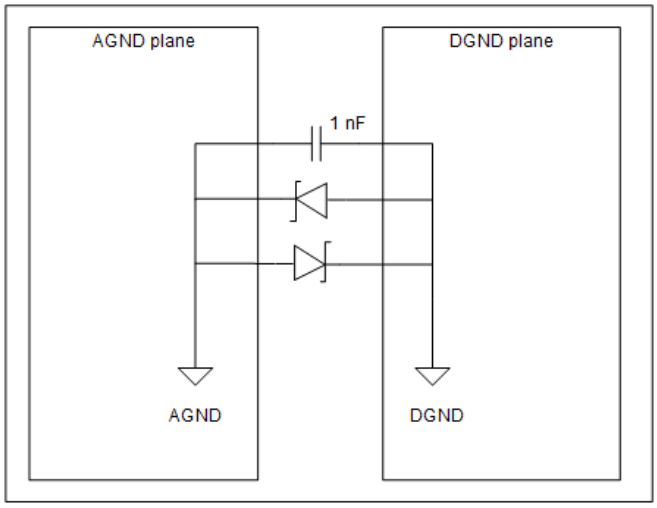
- A focal interconnection point for the digital and analog grounds should be located at about the middle of the overlapping section, as the following illustration shows.

Figure 24 • Single-Point Connection Between DGND and AGND



- Leave spacing for a ceramic 1 nF bypass capacitor and two parallel and inversed Schottky diodes near each PoE manager between the analog and digital layers, as shown. The capacitors form low impedance paths for digital driving signals.

Figure 25 • Grounding Scheme

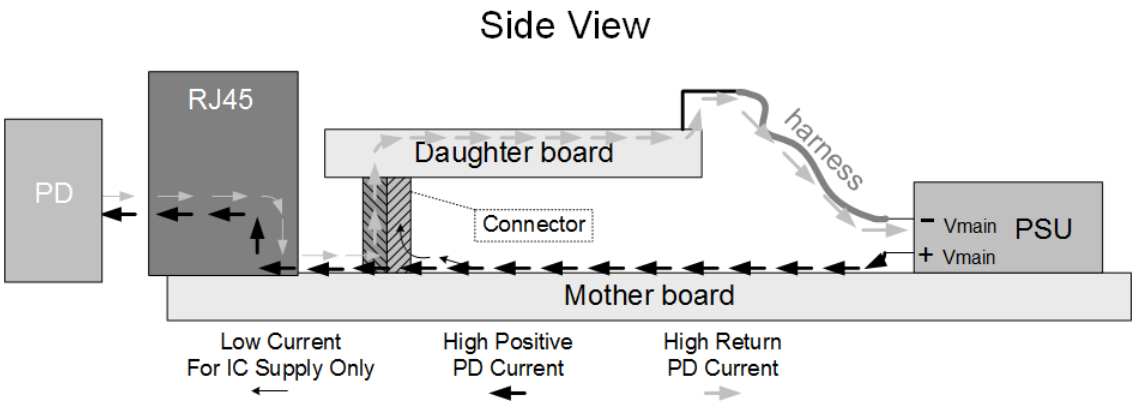


- The power and return (ground) planes for the 48 V supply must be designed to carry the system maximum continuous current, based on the design capacity. Minimize DC power losses on these planes by using wide copper lands. When implementing the PoE circuitry on a daughter board, the high current does not have to be routed through the daughter board but only the return path, as seen in Component Identification for PD69208 Circuitry (Side View) (see page 29).

6.2.3 Current Flow through the PoE Application

The current flow through the PoE application is shown in the following illustration.

Figure 26 • Component Identification for PD69208 Circuitry (Side View)



The port's DC current flows in an application utilizing a PoE daughter board (DB) as follows:

1. Coming from the switch's power supply positive to the center taps of the line transformer through a mother board wide trace (not through the DB)
2. From the center tap of the line transformer through the switch's RJ45 to the PD side
3. The return current from the PD flows through the RJ45 and the line transformer to the DB PoE circuitry
4. From the DB analog ground (AGND), the current flows back to the switch's power supply negative through harness.

Note: The positive port's heavy current flows directly to the PD side without going through the PoE managers on the DB.

6.3 Specific Component Placement

The following section provides placement details for specific components.

6.3.1 Peripheral Components

To minimize heat transfer among various components, a gap between them should be maintained. The following are suggested gaps, but any gap can be used as long as the designer monitors the thermal performance during the design and follows the maximum temperatures allowed at the various components.

- Minimum gap between the PD69208 ICs should be 50 mm.
- Minimum gap between the PD69208 and the PoE controller should be 30 mm.
- Minimum gap between the PD69208 and the NPN transistor regulator (if used) should be 50 mm.

6.3.2 PoE Controller and Peripherals

Refer to the Freescale Semiconductor MKL15Z128VFM4 datasheet for recommendations related to the PoE controller layout guidelines.

The following guidelines are for the integration of the PoE controller into a PoE circuit.

- Locate the filtering capacitors for VDD and for VDDA close to power and ground pins.
- Termination resistors for the outgoing ESPI digital lines should be located close to the respective driving pins.

6.3.3 PD69208 PoE Manager and Peripherals

- The side of the PoE manager that includes pins 41–56 should face the DGND plane. The pins function as communication and control pins for the manager; connect between the PoE manager and the PoE controller through isolation circuitry.
- Locate the bypass capacitors for the PoE manager supply input close to the relevant pin. In cases where two bypass capacitors are placed on the same line, locate the lower valued capacitor closer to the pin on the same layer and place the higher valued capacitor at a more distant location.
- Locate the VAUX5 and VAUX3P3 0.1 µF and 4.7 µF filtering capacitors as close as possible to the PoE manager's pins 20 and 22, respectively.

6.3.4 Vmain Capacitors

It is a good design practice to have three 47 µF capacitors over Vmain in order to prevent noise and spikes events to penetrate into the Vmain rail. Review note 4 of 48-port System Main Blocks (see page 14).

6.4 Conductor Routing

The following sections describe conductor routing guidelines.

6.4.1 General Guidelines

Conductor (or printed lands) routing is to be performed as practiced in the general layout guidelines, specifically:

- Conductors that deliver a digital signal are to be routed between the analog and the digital ground planes.
- Avoid routing analog signals above the digital ground.

6.4.2 Specific Requirements for Clock and Sensitive Signals

Issues that require special design considerations:

- The IREF resistor (connects to pin 24), used for current reference, must be directly connected to AGND and pin 24 using the shortest path.
- Carefully route the ESPI communication clock (SCK) line coming from the PoE controller so that it will not disturb other lines. Two ground lines (connected to DGND) could be routed alongside the clock line to isolate it from the rest of the lines.

6.4.3 Port Outputs

For robust design, the port output traces are to be 45-mil wide in order to handle maximum current and port power. However, to obtain a 10 °C (maximum) copper rise under 1 A per port, set the minimum width for traces in accordance with the layer location and copper thickness, as listed:

- For two ounce copper, external layer: 15 mils
- For two ounce copper, internal layer: 20 mils
- For one ounce copper, external layer: 25 mils
- For one ounce copper, internal layer: 40 mils
- For 1/2 ounce copper, external layer: 30 mils
- For 1/2 ounce copper, internal layer: 55 mils (20 °C copper rise)

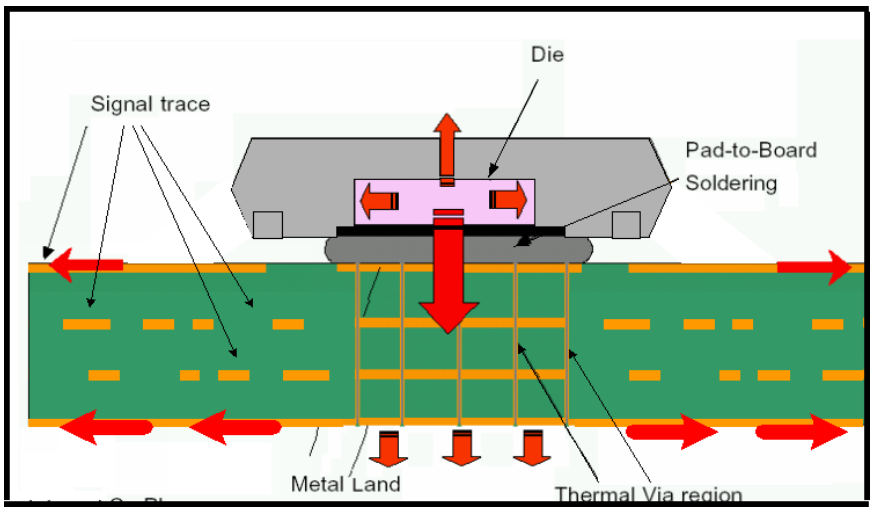
Additionally, the following port output guidelines should be considered.

- The port output traces must be short and parallel to each other in order to reduce RFI pickup and keep the series resistance low.
- The PoE port outputs must be connected to the switch’s pulse transformers as shown in Output Ports Design Details (see page 24). The common mode choke and Bob Smith termination (resistor-capacitor) to chassis ground are optional, and used to reduce RFI noise. The circuit is to be located as close as possible to the pulse transformer.

7 Thermal Pad Design

The PD69208 exposed pad is a metal substrate on the bottom of the package. The attachment process for the exposed pad package is equivalent to standard surface mount packages.

Figure 27 • Heat Dissipation in PCB



For proper heat dissipation, the following footprint/layout guidelines must be followed.

- All thermal vias are to be connected to the AGND area under the PD69208
- Via diameter should be approximately 0.3 mm with one-ounce copper barrel plating. Solder flow into the vias from the component side can result in voids during the solder process and this must be avoided.
- If copper plating does not plug the vias, apply stencil print solder paste onto the printed circuit side. This provides sufficient solder paste, filling those vias to avoid the above mentioned voids. Top solder mask layer and bottom and internal layers copper plane show the associated solder printing masks (CS and PS). The solder mask openings are lined up in respect to the 7×7 thermal via array. Because large solder printing mask openings may result in poor release, the opening should be subdivided as shown.
- For a nominal package standoff of 0.1 mm, a solder mask stencil thickness of 5 mils should be considered.

Refer to the device datasheet for package footprint guidelines.

8 References

The following documents can be obtained from our website, http://www.microsemi.com.

- PD69204T4 datasheet (PD000303601)
- PD69208M datasheet (PD000303451)
- PD69208T4 datasheet (PD000303603)
- Serial Communication Protocol user guide (PD-000300095)
- PoE LED Stream Interface (PD69200_TN_218)
- 6 kV Surge Protection (TN_205)
- Emergency Power Management (TN_134)

In addition, the following non-Microsemi documents can be consulted.

- IEEE 802.3af-2003 Standard, DTE Power via MDI
- IEEE 802.3at-2009 Standard, DTE Power via MDI
- IEEE 802.3bt, Draft 3.0

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