PD69208/4_TN_205

Design for surge immunity within PSE system

Introduction

This document provides detailed design guidelines to sustain extreme high voltage/current surges per few of the most popular immunity standards using Microsemi PD69208/4 IC for PoE functionality.

Overview

Surge immunity is a basic feature required within telecommunication systems in order to increase system reliability when exposed to a surge event. When designing surge protection it is common to check if the required installation of the telecommunication cable is located indoor or outdoor. Surge protection is usually divided to two protection stages:

- Primary protection, deals with high energy surge and is usually located between EUT (Equipment Under Test) and external cable subjected to surge event, however it can be implemented at the EUT front end.
  Used mostly for outdoor cable installation.
- Secondary protection deals with lower surge energy and is usually located within the EUT front end.
  Used mostly for indoor cable installation.

None of the above protection stages intends to protect from direct lightning strike events but a surge event occurs near the telecommunication line. This design guide is intended to assist the designer to implement primary protection mechanisms for protection from outdoor surge events.

Disclosure: an outdoor surge event in this document points to equipment that whose telecommunication cables are located outdoor but the equipment itself is located indoor. For equipment that is located totally outdoor additional regulations must be complied with such as waterproof, AC input line protection, etc.

Immunity requirements

Many standards around the world define different surge voltage levels, source impedance and maximum current. This document deals with a few of the most severe surge events. In most of the cases, a system sustaining the following events will sustain the following standards:

- EN 61000-4-5:2006
- GR-1089-core 2011
- ITU-T K.21 2011

The following tests were analyzed:

#	standard	wave shape	voltage	Port status [1]	Line under test	resistance	Type	Figure
1.	EN55024(2010) +EN61000 4-5 (Europe)	10/700us	+4KV	ON	All lines	Common 15Ω and n x 25Ω + 90V gas arristor per line (n is the number of lines) (Port ON and Port OFF)	All Line to Earth	1
				OFF				
			-4KV	ON				
				OFF				
2.	GR-1089 (USA)	1.2/50us	+800V	OFF	Vmain	6 Ω	Line to line (differential)	2
					Vp_neg			
			-800V	OFF	Vmain			
					Vp_neg			
3.		1.2/50us	+1.5KV	OFF	All lines	2 pair - 10Ω on each out of 4 lines	Line to Earth (common)	3
			-1.5KV	OFF				
4.		2/10us We do 1.2/50us	+1KV	OFF	Vmain	200A (3 Ω)	Line to All lines	2
					Vp_neg			
			-1KV	OFF	Vmain			
					Vp_neg			
5.		2/10us We do 1.2/50us	+1KV	OFF	All lines	200A (3 Ω)	All Lines to Earth	4
			-1KV	OFF				
6.		10/700us	+4KV	OFF		25Ω per line (+15Ω generator internal)	Line to Earth (common)	5 (no need for GDT)
			-4KV	OFF				
7.	ITU-T K21 (International)	10/700us	+1.5KV	OFF	Vmain	25 Ω (+15Ω generator internal)	Line to line (differential)	2
					Vp_neg			
			-1.5KV	OFF	Vmain			
					Vp_neg			
8.		10/700us	+6KV	OFF	All lines	25 Ω per line (+15Ω generator internal)	Line to earth (common)	5
				ON				
			-6KV	OFF				
				ON				

[1] – Port status during the test

- Criteria A - Port stays on during the event
- Criteria B - port is turned-off during the surge, after the event turned-on automatically recovered.

- During all tests, the Criteria for the “neighbors” ports next to the tested port is **A**.
  In tests with tested port ON: The tested port meets criteria **A.**

Surge protection circuit design

Setup Figures:

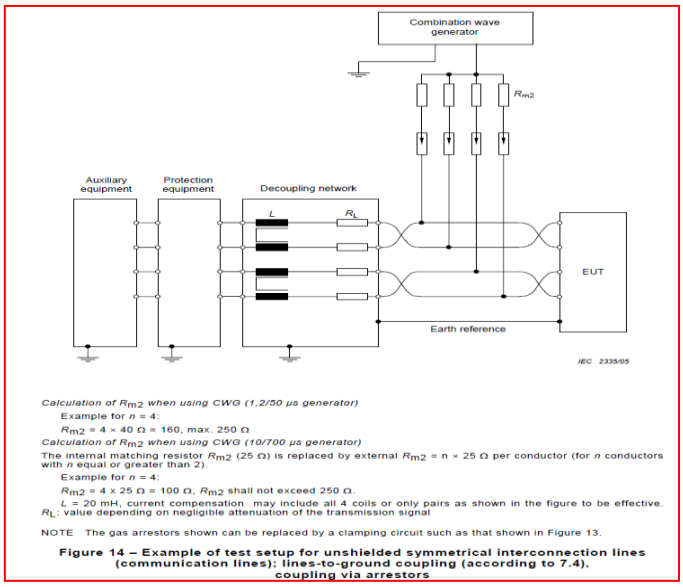

Figure 1

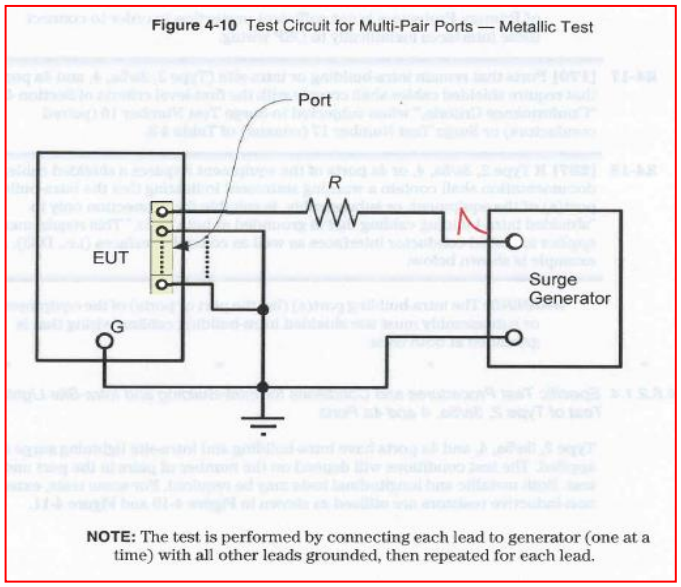

Figure 2

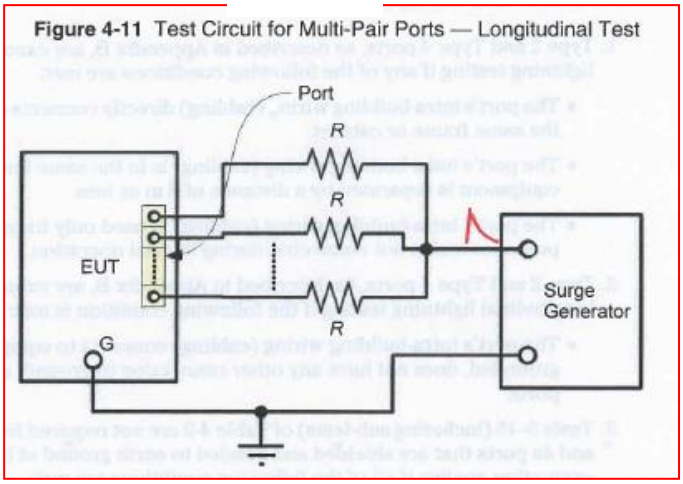

Figure 3

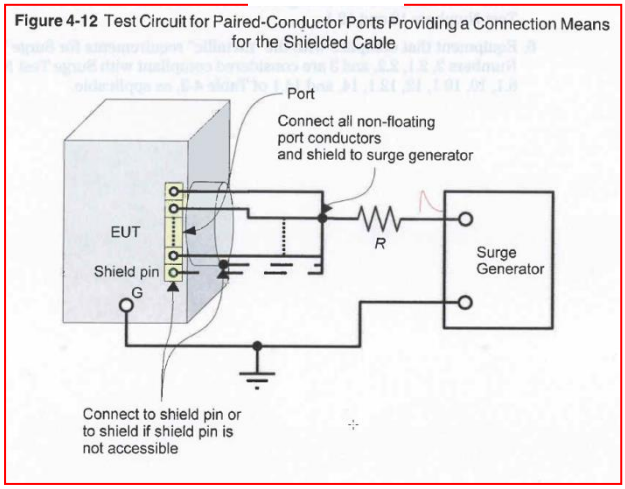

Figure4

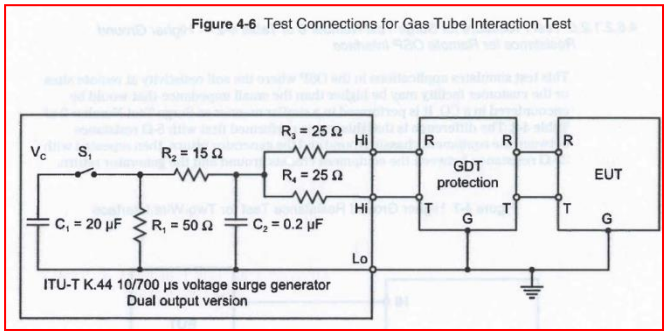

Figure 5

The following circuit complies with the above tests.

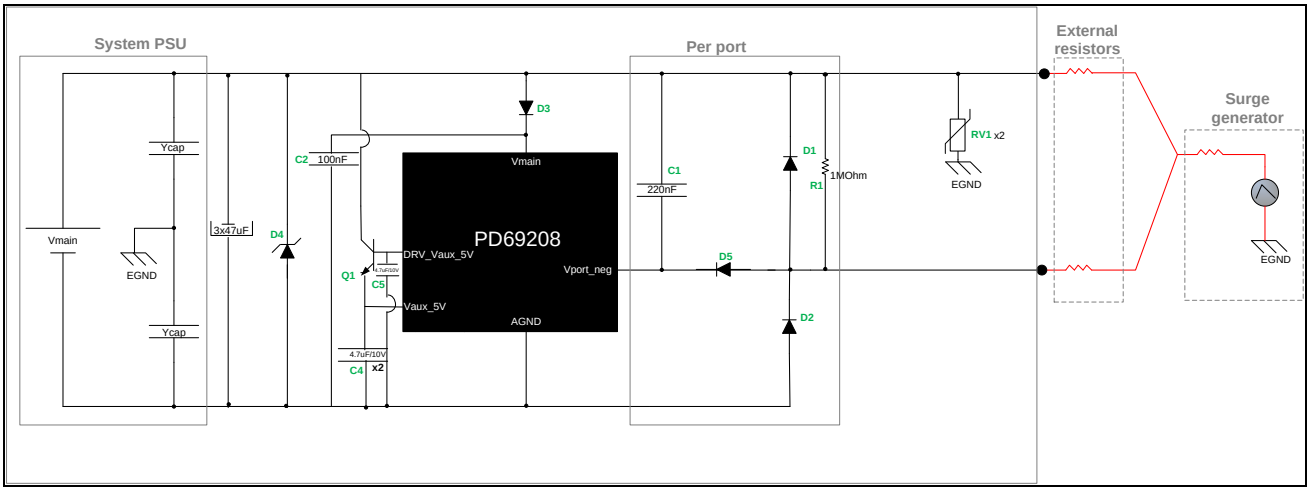

Figure 6 – surge protection circuit

Surge Protection components

Qty	Reference	Description	PCB Foot Print	Manufacturer	
				Brand	Part Number
1 per chip	D3	Schottky Diode 100V	SMA	STMicroelectronics	STPS1H100A
				ON Semiconductor	MBRA1H100T3G
				Vishay	SS1H10-E3/61T
3 per port	D1, D2, D5	Schottky Diode 100V	SMA	STMicroelectronics	STPS1H100A
				ON Semiconductor	MBRA1H100T3G
				Vishay	SS1H10-E3/61T
1 per chip	D4	Unidirectional TVS DIODE 58V	SMC	Fairchild	SMCJ58A
2 per system	RV1	Bidirectional Varistor 275V	TH	EPCOS	B72214S2271K101
1 per port	C1	Capacitor 220nF/100V	1206	TDK	C3216X7R2A224K
1 per Port	R1	Resistor 1MOhm 250mW 1% 1206 SMT	1206	Samsung	RC3216F1004CS
3 per chip	C4,C5	CAP CRM 4.7uF 10V	0603	TDK	C1608X5R1A475K
1 per chip	Q1	TRN NPN 250V 1A 15W D-Pak SMT	D-Pak	ON semi	MJD47

Test setup:

1.

EN55024(2010) +EN61000 4-5 (Europe)	10/700us	+4KV	ON	All lines	Common 15Ω and n x 25Ω + 90V gas arristor per line (n is the number of lines) (Port ON and Port OFF)	All Line to Earth
			OFF			
		-4KV	ON			
			OFF			

Port OFF

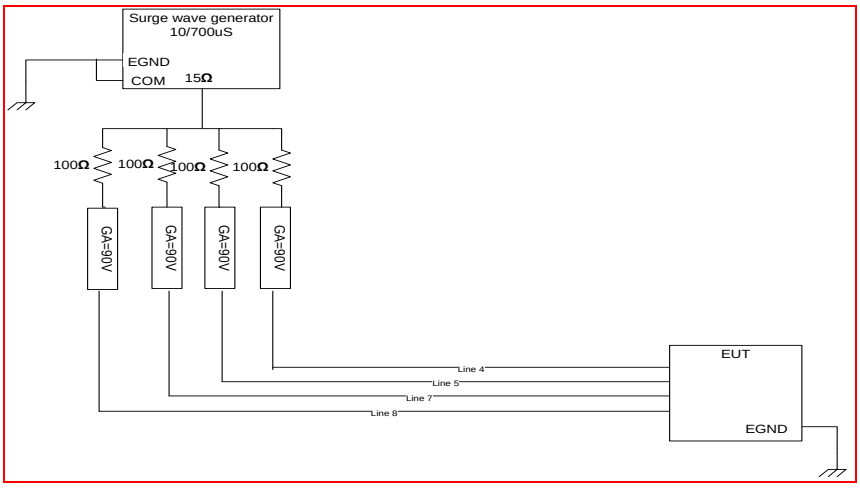

Figure 7

Port ON

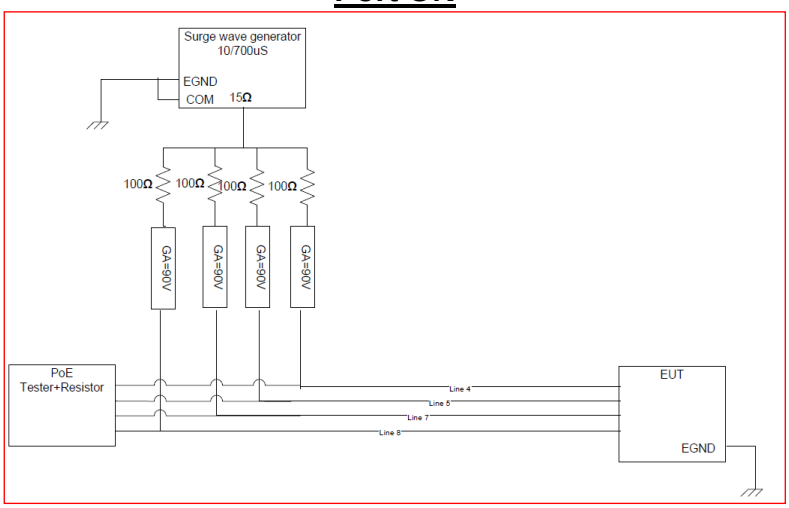

Figure 8

2.

GR-1089 (USA)	1.2/50us	+800V	OFF	Vmain	6 Ω	Line to line (differential)
				Vp_neg		
		-800V	OFF	Vmain		
				Vp_neg		

Surge on Vmain:

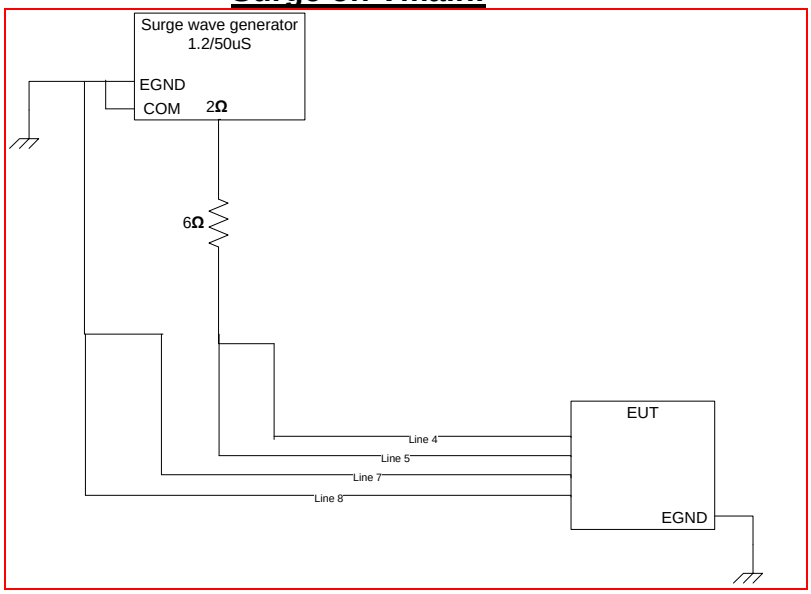

Figure 9

Surge on Vport_Neg:

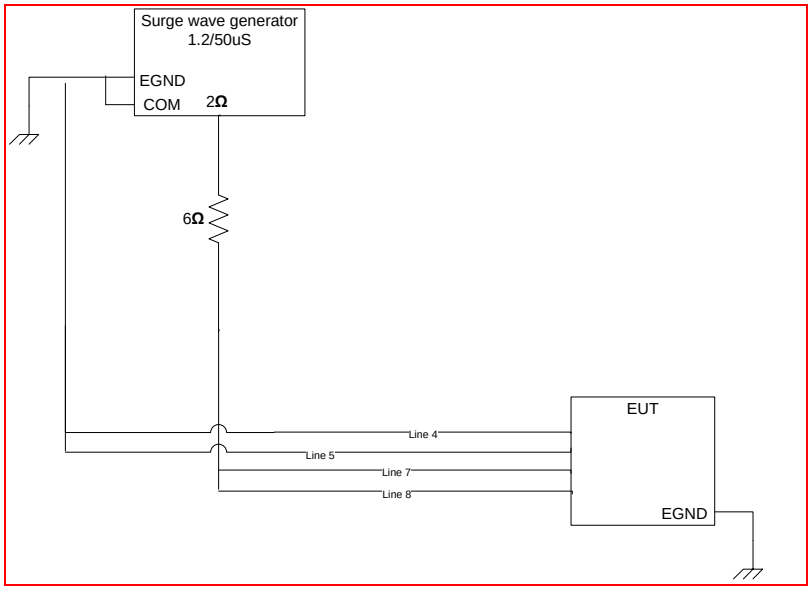

Figure 10

3.

GR-1089 (USA)	1.2/50us	+1.5KV	OFF	All lines	2 pair - 10Ω on each out of 4 lines	Line to Earth (common)
		-1.5KV	OFF			

Test setup

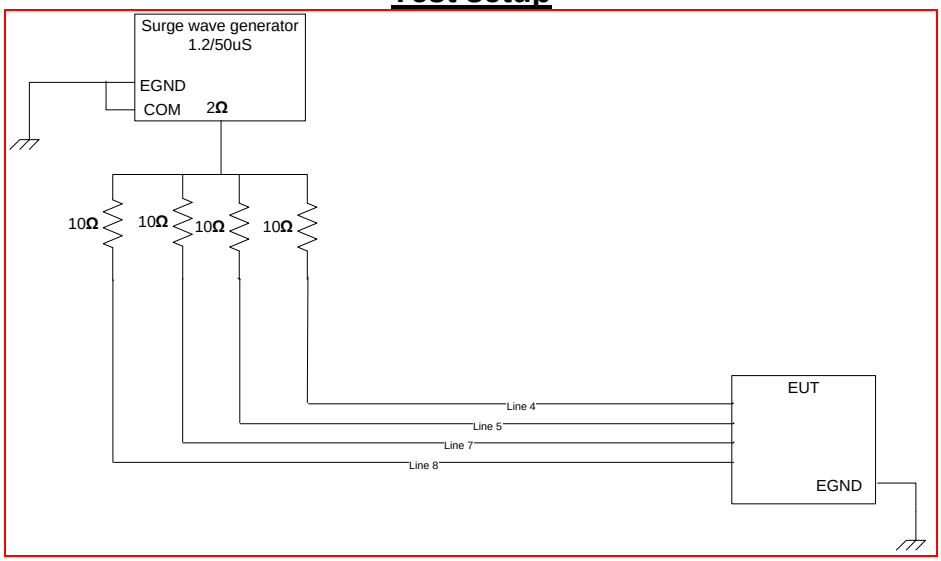

Figure 11

4.

GR-1089 (USA)	2/10us We do 1.2/50us	+1KV	OFF	Vmain	200A (3Ω)	Line to All lines
				Vp_neg		
		-1KV	OFF	Vmain		
				Vp_neg		

Surge on Vmain:

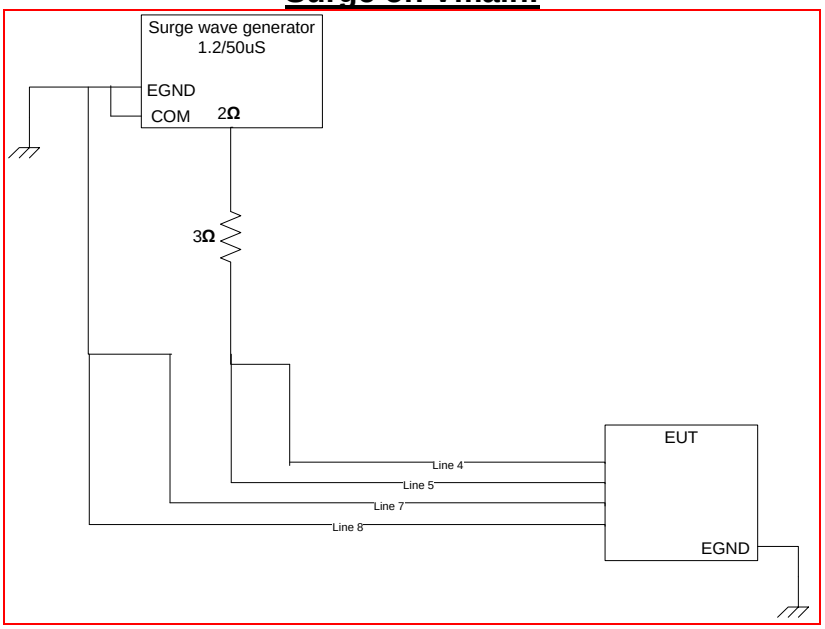

Figure 12

Surge on Vport_Neg:

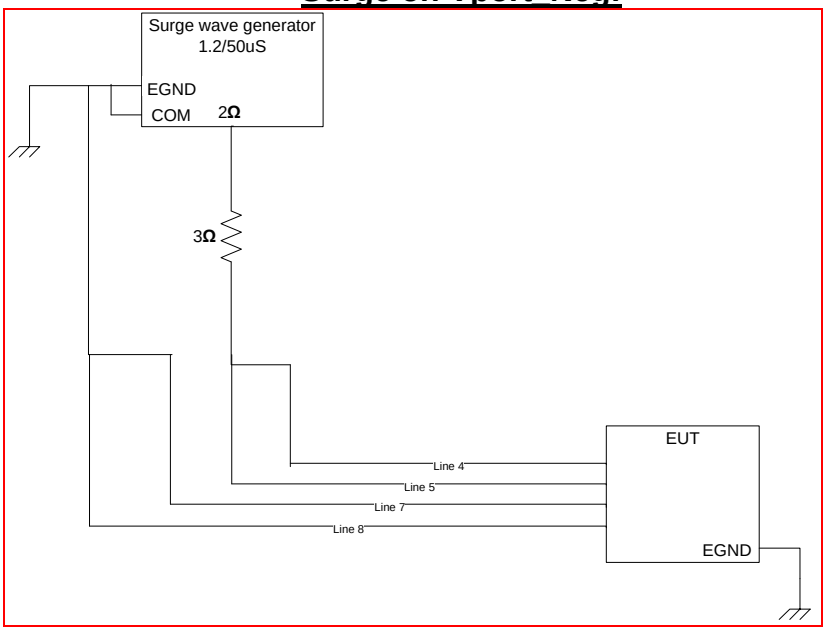

Figure 13

5.

GR-1089 (USA)	2/10us We do 1.2/50us	+1KV -1KV	OFF OFF	All lines	200A (3Ω)	All Lines to Earth

Test setup

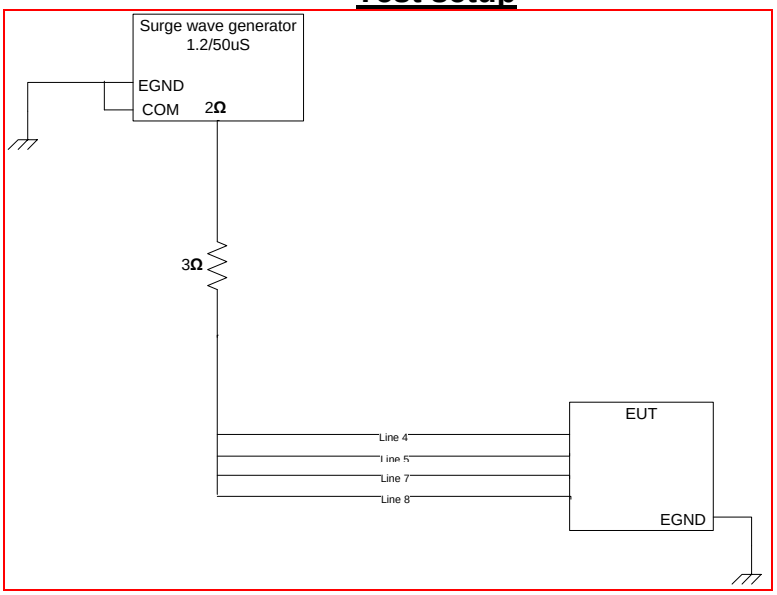

Figure 14

6.

GR-1089 (USA)	10/700us	+4KV -4KV	OFF OFF	All lines	25Ω per line (+15Ω generator internal)	Line to Earth (common)

Test setup

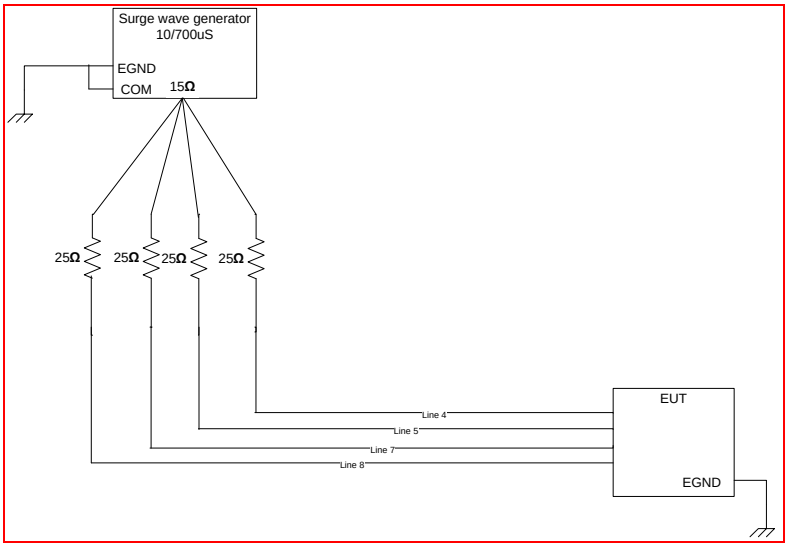

Figure 15

7.

ITU-T K21 (International)	10/700us	+1.5KV	OFF	Vmain	25 Ω (+15Ω generator internal)	Line to line Single port
				Vp_neg		
		-1.5KV	OFF	Vmain		
				Vp_neg		

Surge on Vmain:

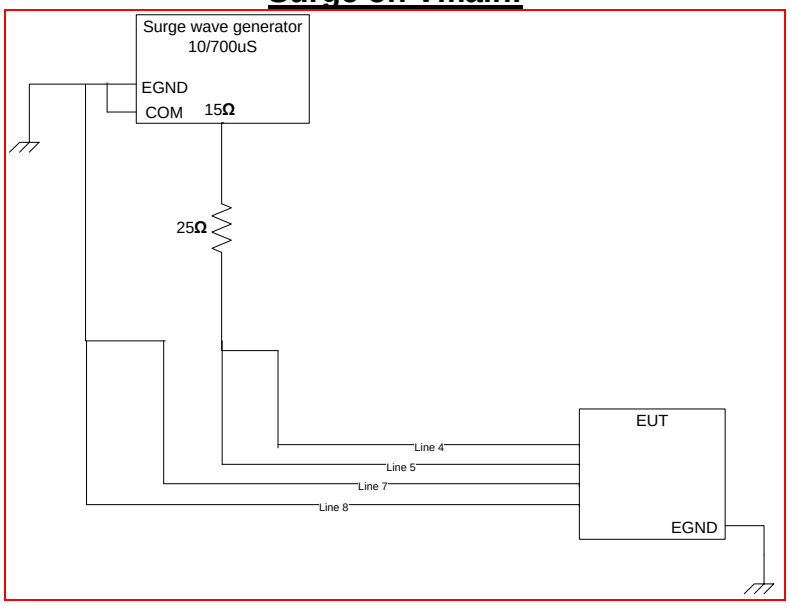

Figure 16

Surge on Vport_Neg:

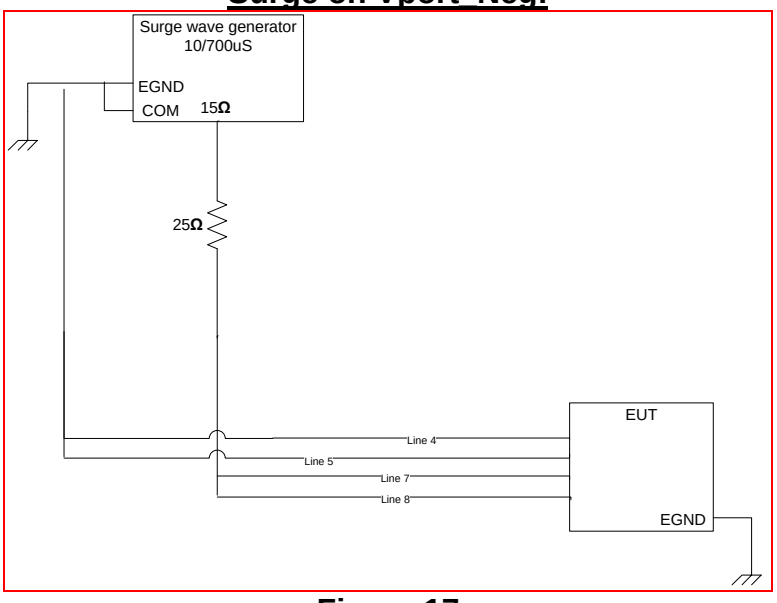

Figure 17

8.

ITU-T K21 (International)	10/700us	+6KV	ON	All lines	25 Ω per line (+15Ω generator internal)	Line to earth Single port
			OFF			
		-6KV	ON			
			OFF			

Port OFF

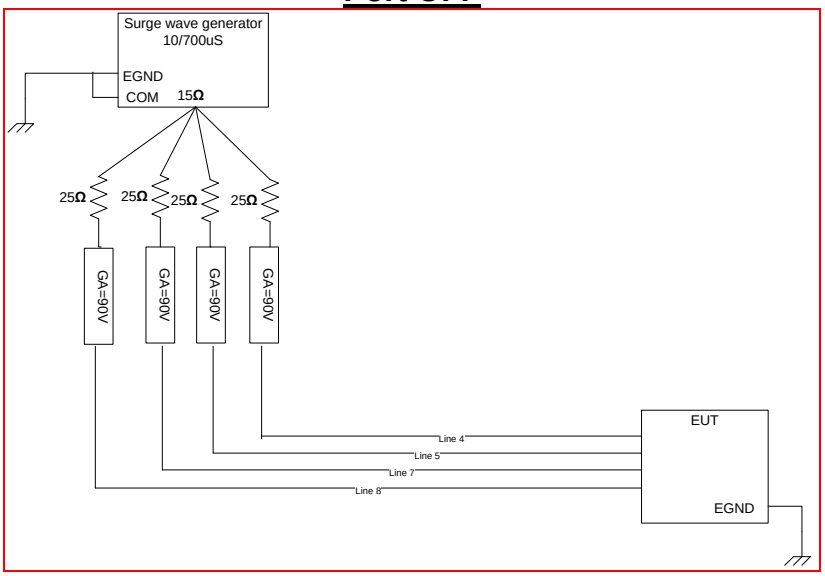

Figure 18

Port ON

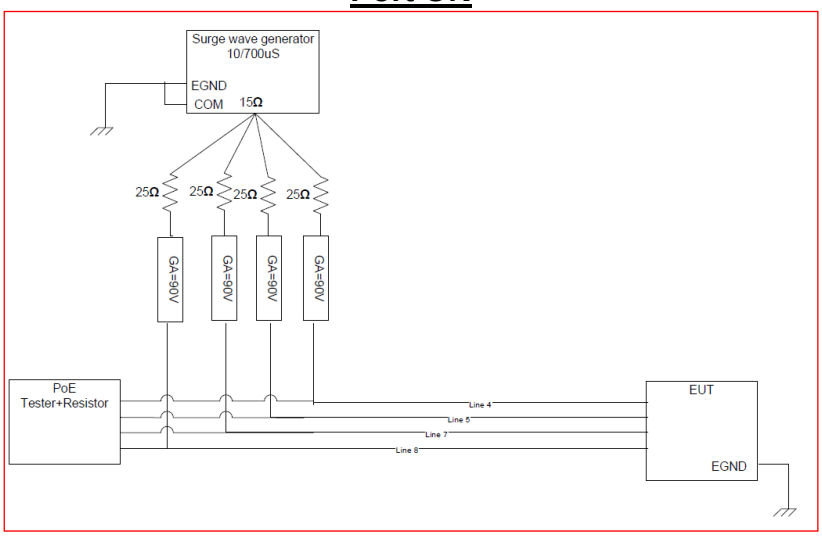

Figure 19

Detailed circuit description

When designing application immunity to surge event there are two concepts to consider:

- Designing isolation mechanism that will prevent the surge from breakthrough to the chassis by keeping clearance distance between the PoE circuitry and chassis. This kind of protection is common for low voltage surge protection of up to 2KV.
- Designing a low impedance current path to chassis and keep the high currents away from the circuitry to be protected. This kind of protection is suitable for low and high voltage surge protection.

In this case, a low impedance current path is leading the currents from the surge source to the chassis and keeps it away from the PD69208/4 circuitry.
The following drawings show the expected current path for each surge event.

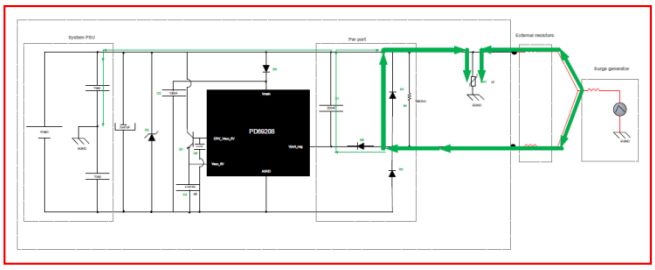

Figure 20: Positive common surge

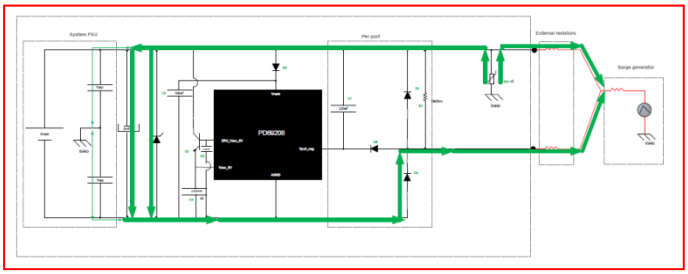

Figure 21: Negative common surge

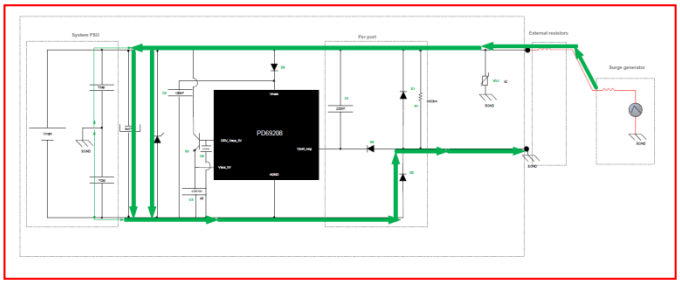

Figure 22: Positive differential surge

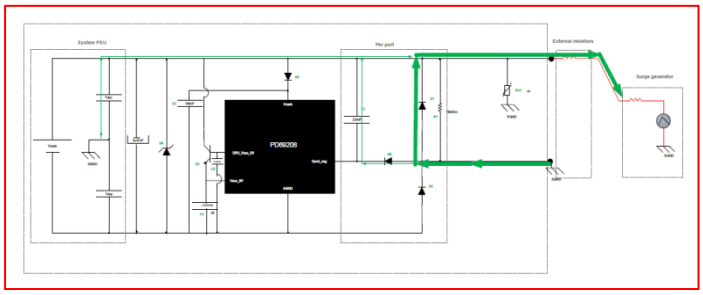

Figure 23: Negative differential surge

- As shown above, the high current path goes through the port diodes D1, D2, Varistor RV1 and TVS D4.
- D5, D3 block the current path thru the PD69208/4.
- In Figures 21 and 22, D4 provids a current path and clamps the voltage to a safe level. The clamped voltage may get up to 80V under the surge current, meaning that the system power supply may be subjected to 80V for about 1.5mS. It is up to the designer to verify that the system PSU is capable of handling this voltage from output components stress point of view and from over voltage protection.
- Q1 is an optional component which help to keep the 3.3V stability.
  It is highly recommended to add it to the PCB layout.
  The decision of assemble it, might be taken during the actual surge test of the final system,

Layout considerations

In order to lead the high current in an efficient way and minimize noise radiation, special care should be taken on PCB layout, following some recommendations for a proper layout (with respect to surge immunity). Any other layout recommendation relating to PoE should also be implemented.

- Keep chassis trace close to RJ45 gang and do not penetrate to PoE environment.
- Chassis trace of 5mm thick should be enough for surge current.
- Make sure chassis trace/plane is well connected to the box screw and that the screw is located close to the RJ45 gang.
- Keep 80mil creepage for each component connecting between chassis and PoE circuitry.
- Do not layout PoE traces in parallel to chassis but orthogonal in order to minimize noise coupling.
- If the layout consists of more than four layers, use internal layers for PoE routing and external layers for plans (V_{main} and GND) in order to have better noise immunity.
- Locate Rv1 (see Figure 6) near the RJ45 gang connected between chassis and V_{main} plane. If vias are needed, use multiple thick VIAs in order to support the high surge currents. It is a good design practice to have a provision to change the RV1 location along the board and to determine the final location by tastings (Usually it will be located at the middle of the RJ45 gang).
- Spread the system electrolytic capacitance along the board connected between analog GND and V_{main}. Use at least 3x47µF per system in order to keep V_{main} overshoot low during the surge.
- Keep D1 and D2 and D5 (See Figure 6) as close as possible to RJ45 gang and keep PoE IC away from it (30mm should be sufficient).
- Place C1 as close as possible to PoE IC
- Place D4 as close as possible to PoE IC

Revision History

Revision Level / Date	Para. Affected	Description
0.1 / 1-Feb-2015		Initial Release
0.2 / 23-Mar-2015		
0.3 / 09-Mar-2016		Add new figures. Add new componenets in the appliacation.
0.4 / 05-June -2016		Fixing figure 23.
0.5 / 18-July -2016		Replace the app shcmeatic. Varistor instead sidactor Repace setup 1 and 8, port ON drawing.

For support contact: **PoEsupport@microsemi.com**

Visit o**u**r web site at: **www.microsemi.com**

Catalog Number: **PD69208/4_TN_205**