AC483
Application Note
PolarFire FPGA Transceiver Signal Integrity

a Microchip company

a Microchip company
Microsemi Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
Microchip Technical Support
www.microchip.com

About Microsemi

Microsemi, a wholly owned subsidiary of Microchip Technology Inc. (Nasdaq: MCHP), offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Learn more at www.microsemi.com.

51900483. 2.0 5/22

Contents

Figures

Tables

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.0

- Added Enhanced Receiver Management options in Libero Flow, page 16.
- Added new Rx CTLE settings, see Table 5, page 13.

1.2 Revision 1.0

The first publication of this document.

2 Transceiver Tuning

This document describes the several PolarFire Transceiver signal integrity settings as well as IBIS-AMI and SmartDebug features.

The document covers the design flow required to perform successful signal integrity tuning at both Transmitter (Tx) and Receiver (Rx) end. For commonly used terminologies, see Glossary, page 23.

Transceiver tuning for PolarFire devices is done three different ways:

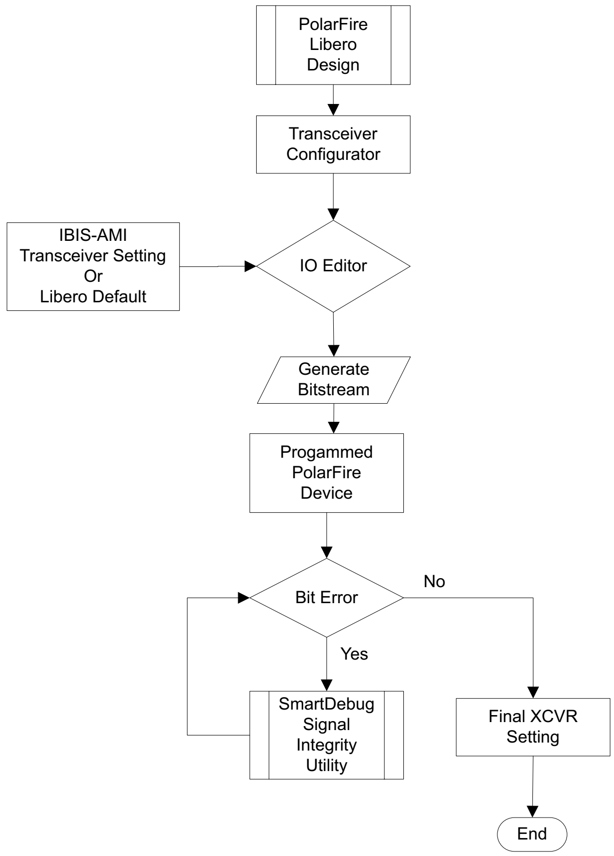
- **Traditional Method (Non-simulation flow)**: Traditional method is based on learnings developed from experience. If costumers know the channel loss, then based on the recommendations provided in this document or on the basis of users experiences, Transceiver attributes are loaded to the device. This method does not guarantee the ideal Transceiver performance.
- **IBIS-AMI Simulations**: Transceiver tuning based on IBIS-AMI Simulations is the best method available. Simulations helps to build confidence on the performance of the hardware. In simulations, both the transmitter and receiver variables can be changed and output is observed. This method provides a clear image on how the different Transceiver attributes impacts the performance of the system. The appropriate Transceiver attributes obtained from the simulation can be applied to the device by two ways:
  - Through Libero: Change the attributes in the design while generating the bit file.
  - Through SmartDebug: The SmartDebug tool provides the facility to vary between the multiple attributes using the same bit file.

  Detailed explanation of tuning using IBIS-AMI Simulations is provided in this document.
- **SmartDebug:** SmartDebug is used for debugging the Transceiver using electrical parameters such as Tx amplitude, De-emphasis, driver impedance, Rx impedance, CTLE and DFE calibration. It gives freedom to the users to play with the signal integrity settings based on the simulations or intuitions. Details of SmartDebug are discussed in the later section of this document. For more information, see *SmartDebug User Guide for PolarFire FPGAs.*

Note: Receiver optimization is disabled in Libero SoC v12.0 SmartDebug. It will be fixed in a future version.

PolarFire transceivers have a memory mapped Dynamic Reconfiguration Interface (DRI) which allows SmartDebug to communicate with the transceiver blocks in real-time. This feature provides debugging capabilities and altering of the transceivers for optimized performance in the system. After the final SmartDebug signal integrity optimization, the user can export the tuned information back into the Libero SoC software for future design regeneration.

Figure 1 • **Transceiver Signal Integrity Tuning Flow**



2.1 Transmitter

High speed transmitter has following capabilities that user can adjust to make the system work. Note that only transmitter tuning alone does not help for high loss channel, receiver tuning is also required to make system work without errors.

- **Amplitude**: Transmitter supports 10 amplitude settings from 100mV to 1000mV in steps of 100mV.
- **De-emphasis**: Transmitter supports six de-emphasis settings. Those are 0dB, -1dB, -2.5dB, -3.5dB, -4.4dB and -6dBmV.
- **Termination impedance**: Transmitter supports four driver terminations. Those are 85 Ω, 100 Ω, 150 Ω and 180 Ω.
- **Jitter**: In the IBIS-AMI simulation, the following Jitter parameters can be used for the transmitter:
  - Tx_DCD (Tx Duty cycle Distortion)
  - Tx_Dj (Tx Deterministic Jitter)
  - Tx_Rj (Tx Random Jitter)

Note: See *PolarFire IBIS-AMI Models* for the worst-case jitter numbers. By default, these jitter numbers are considered while running IBIS-AMI simulations.

The following table describes the recommended Tx settings for different channel lengths.

Table 1 • **Recommended Driver Amplitude, De-emphasis, Impedance Settings**

Amplitude and De-emphasis Setting (mV with dB)	Tx Termination (Ω)	Recommended channel
100mV with 0dB	100	Very Short
200mV with 0dB	100	Very Short
200mV with -1dB	100	Very Short
200mV with -2.5dB	100	Very Short
200mV with -3.5dB	100	Very Short
200mV with -4.4dB	100	Very Short
200mV with -6dB	100	Very Short
300mV with 0dB	100	Short
400mV with 0dB	100	Short
400mV with -1dB	100	Short
400mV with -2.5dB	100	Short
400mV with -3.5dB	100	Short
400mV with -4.4dB	100	Short
400mV with -6dB	100	Short
500mV with 0dB	100	Short
600mV with -3.5dB	150	Short/Medium
600mV with -6dB	150	Short/Medium
800mV with 0dB	150	Short/Medium/Long
800mV with -1dB	150	Short/Medium/Long
800mV with -2.5dB	150	Short/Medium/Long
800mV with -3.5dB	150	Short/Medium/Long
800mV with -4.4dB	150	Short/Medium/Long
800mV with -6dB	150	Short/Medium/Long
1000mV with 0dB	180	Short/Medium/Long
1000mV with -1dB	180	Short/Medium/Long

Table 1 • **Recommended Driver Amplitude, De-emphasis, Impedance Settings**

Amplitude and De-emphasis Setting (mV with dB)	Tx Termination (Ω)	Recommended channel
1000mV with -2.5dB	180	Short/Medium/Long
1000mV with -3.5dB	180	Short/Medium/Long
1000mV with -4.4dB	180	Short/Medium/Long
1000mV with -6dB	180	Short/Medium/Long

Note: Apart from these recommended settings, each driver termination (85,100,150 and 180 Ω) has 29 amplitude and emphasis settings ranging from 100mV with 0dB to 1000mV with -6dB. User can apply any of the recommended or other settings to the silicon according to their applications.

2.1.1 IBIS-AMI

The Tx parameters are accessed in the IBIS-AMI simulation in the following ways:

- Amplitude and De-emphasis is through the variable `TX_AmpEmph`.
- Driver Termination is the through selecting the appropriate pin in the IBIS as listed in the following table.

Table 2 • **Tx Model Pin Description**

Pin	Variable Name	Description
5, 6	microsemi_pf_100_tx	100 to 1000mV with 100 Ω termination
11, 12	microsemi_pf_150_400tx	100 to 400mV with 150 Ω termination
13, 14	microsemi_pf_150_800tx	600 to 800mV with 150 Ω termination
7, 8	microsemi_pf_150_tx	1000mV with 150 Ω termination
15, 16	microsemi_pf_180_400tx	100 to 400mV with 180 Ω termination
17, 18	microsemi_pf_180_800tx	600 to 800mV with 180 Ω termination
9, 10	microsemi_pf_180_tx	1000mV with 180 Ω termination
3, 4	microsemi_pf_85_tx	100 to 1000mV with 85 Ω termination

The PolarFire IBIS-AMI models can be downloaded from link *https://www.microsemi.com/products/fpga-soc/design-resources/ibis-models/ibis-models-polarfire*. The following table shows the IBIS-AMI model files contained in the model package files and its descriptions.

Table 3 • **IBIS-AMI Model File Description**

File Name	Description
microsemi_pf_spisim.ibs	Top-level IBIS models and wrappers for Tx and Rx AMI model.
MPF300T-TX-R085.ami	All Amplitude and de-emphasis settings with 85 Ω termination, full set of settings are present in this transmitter AMI model.
MPF300T-TX-R100.ami	All Amplitude and de-emphasis settings with 100 Ω termination, full set of settings are present in this transmitter AMI model.
MPF300T-TX-R150.ami	1000mv amplitude settings with 150 Ω termination
MPF300T-TX-R150_800.ami	800mv and 600mv amplitude settings with 150 Ω termination
MPF300T-TX-R150_400.ami	100mv to 500mv amplitude settings with 150 Ω termination
MPF300T-TX-R180.ami	1000mv amplitude settings with 180 Ω termination
MPF300T-TX-R180_800.ami	800mv and 600mv amplitude settings with 180 Ω termination
MPF300T-TX-R180_400.ami	100mv to 500mv amplitude settings with 180 Ω termination

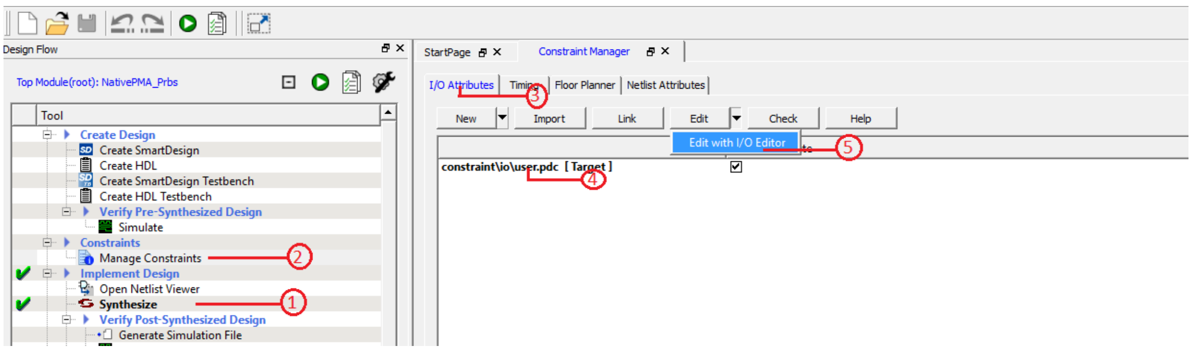
2.1.2 Libero Flow

The Tx and Rx settings obtained from IBIS-AMI simulation can be directly applied to the device through Libero. In this section, settings related to Tx are discussed. Following are the steps to apply Tx signal integrity settings.

To create the transceiver based design:

1. Run the **Synthesize**, this enables the **Manage Constraints**
2. Go to **Manage Constraints**
3. Go to **I/O Attributes**
4. Select the **Target**
5. Click **Edit** > **Edit with I/O Editor** as show in the following figure

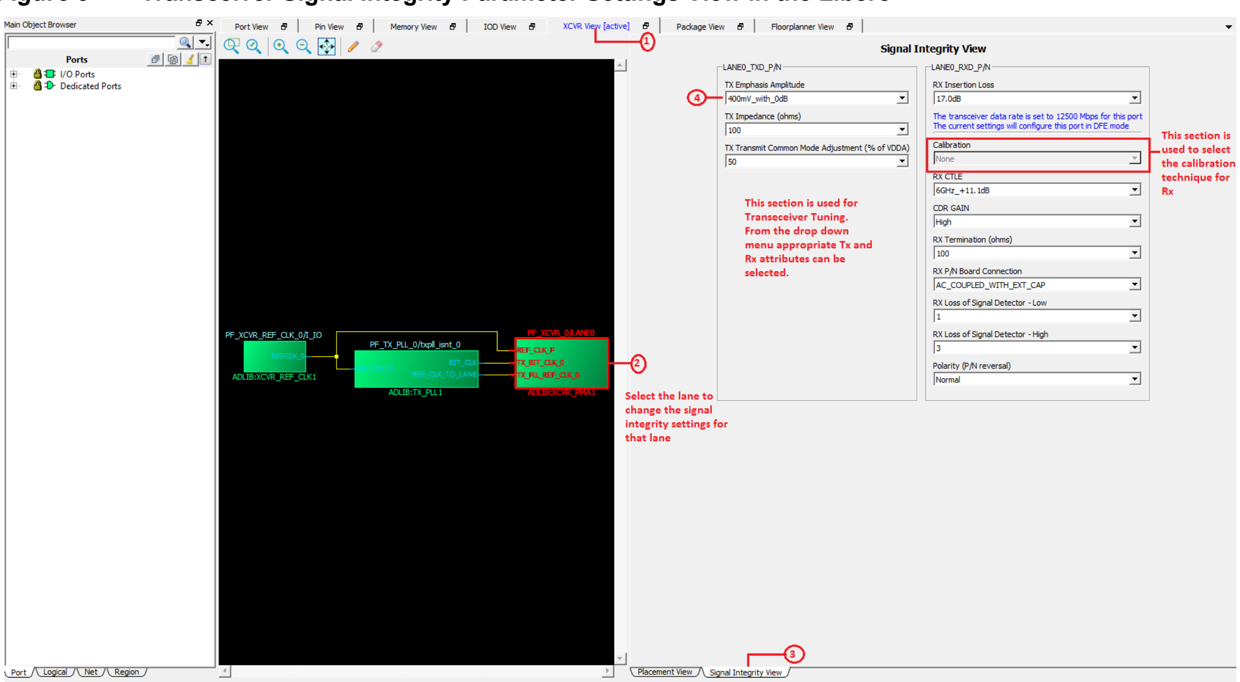
Figure 2 • **Navigating to I/O Attributes in the Libero**



After the I/O Editor is opened, perform the following steps:

1. Select **XCVR** View tab.
2. Select the appropriate lane.
3. Go to **Signal Integrity View** present in the right bottom as shown in the following figure.
4. Set the Tx settings such as, Amplitude with de-emphasis, Tx Impedance as shown in the following figure.

Figure 3 • **Transceiver Signal Integrity Parameter Settings View in the Libero**



XCVR view tab provides options to apply different Tx settings and Termination impedance. Select the appropriate settings and apply. After this step, both Tx and Rx settings are applied to Transceiver.

This fixes the Tx and Rx settings into staple (bit file) file. In-order to debug the design with respect to signal integrity, change the Tx and Rx settings through **SmartDebug** on the fly.

2.1.3 SmartDebug Flow

When the design is not working as expected, SmartDebug is used to debug the design with respect to signal integrity related issues. For more information on SmartDebug, see *SmartDebug User Guide for PolarFire FPGAs*.

For Tx, SmartDebug is used to change the settings such as amplitude, de-emphasis and driver termination settings live on the hardware. There are two ways the hardware can be debugged.

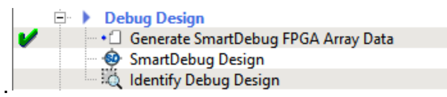
1. Use existing design which sends data.
2. Use in-built PRBS generator from SmartDebug.

Note: Only Tx settings are discussed in this section, however, for successful debug, both Tx and Rx need to be tuned. For Rx setting, see Receiver, page 11

Following steps describe the debugging of the design with respect to Tx.

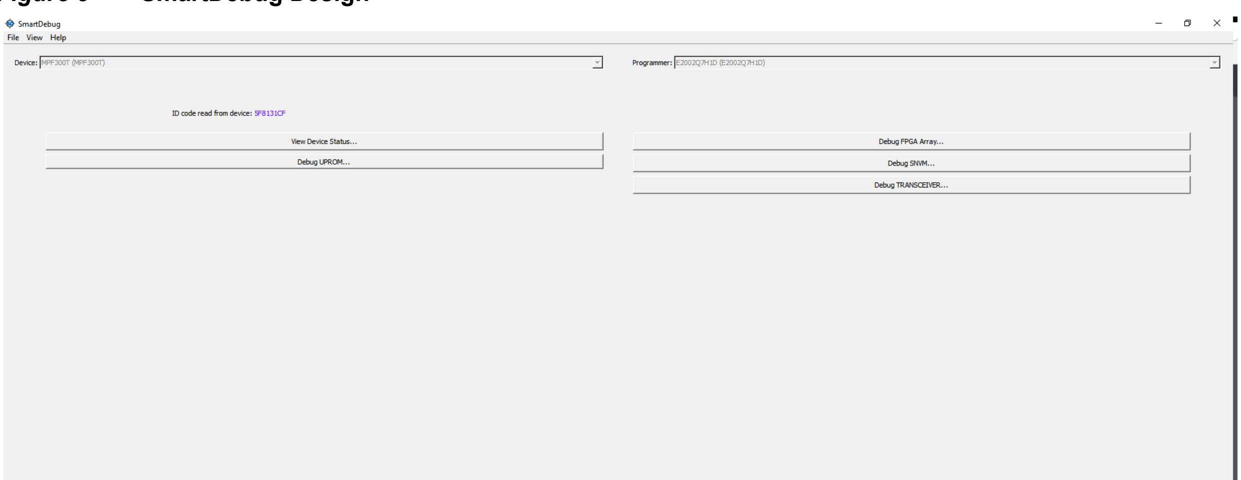
1. Program the bit file (`.stp`) on to the device.
2. Open the corresponding **Libero Project**.
3. Double click the **Generate SmartDebug FPGA Array Data** on Libero Software. Once the array data is generated, a green tick mark appears as shown in the following figure.

Figure 4 • **SmartDebug FPGA Array Data**



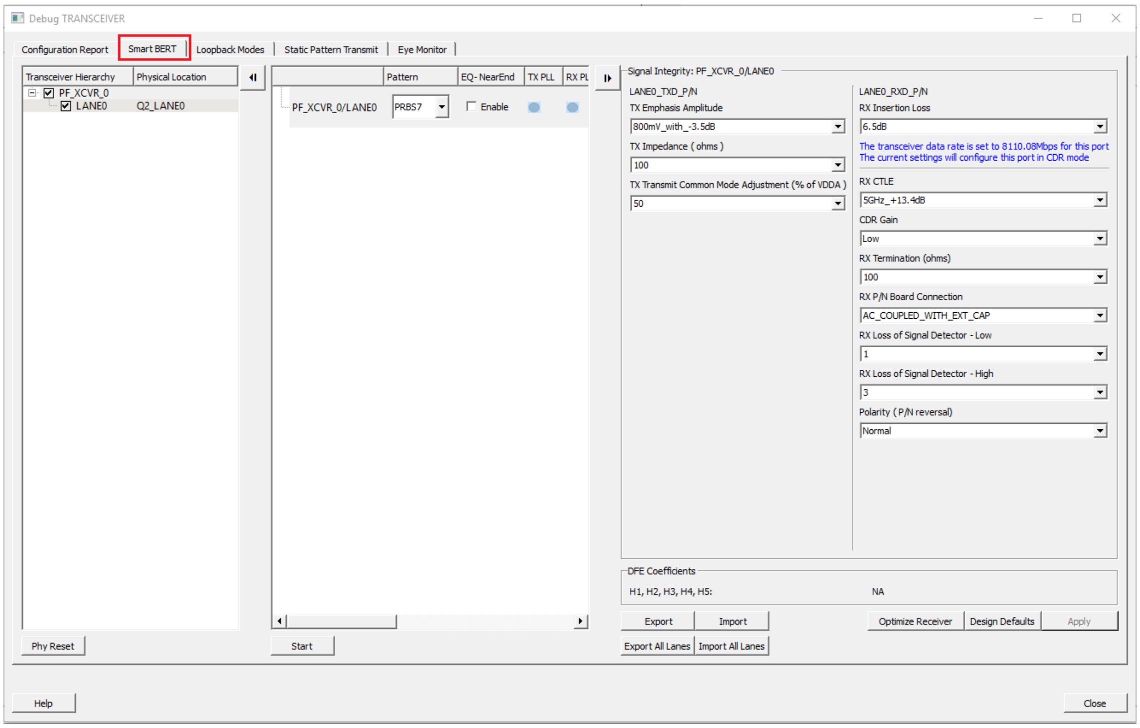
4. After generating the data successfully open the **SmartDebug Design** from the Libero Design Flow. Note that the Hardware has to be connected with FlashPro programmer and power on. If the **SmartDebug** is opened without powering up the hardware, it opens up in Demo Mode. Connect the hardware using FlashPro programmer and open the **SmartDebug** Design from the Libero Design Flow. It opens **SmartDebug** window as shown in the following figure. Click **Debug Transceiver**.

Figure 5 • **SmartDebug Design**



5. Go to **Smart BERT** tab and select the required lane to assign the pattern and Transmitter attributes as shown in the following figure. Select any data pattern or the existing design sends the data pattern.

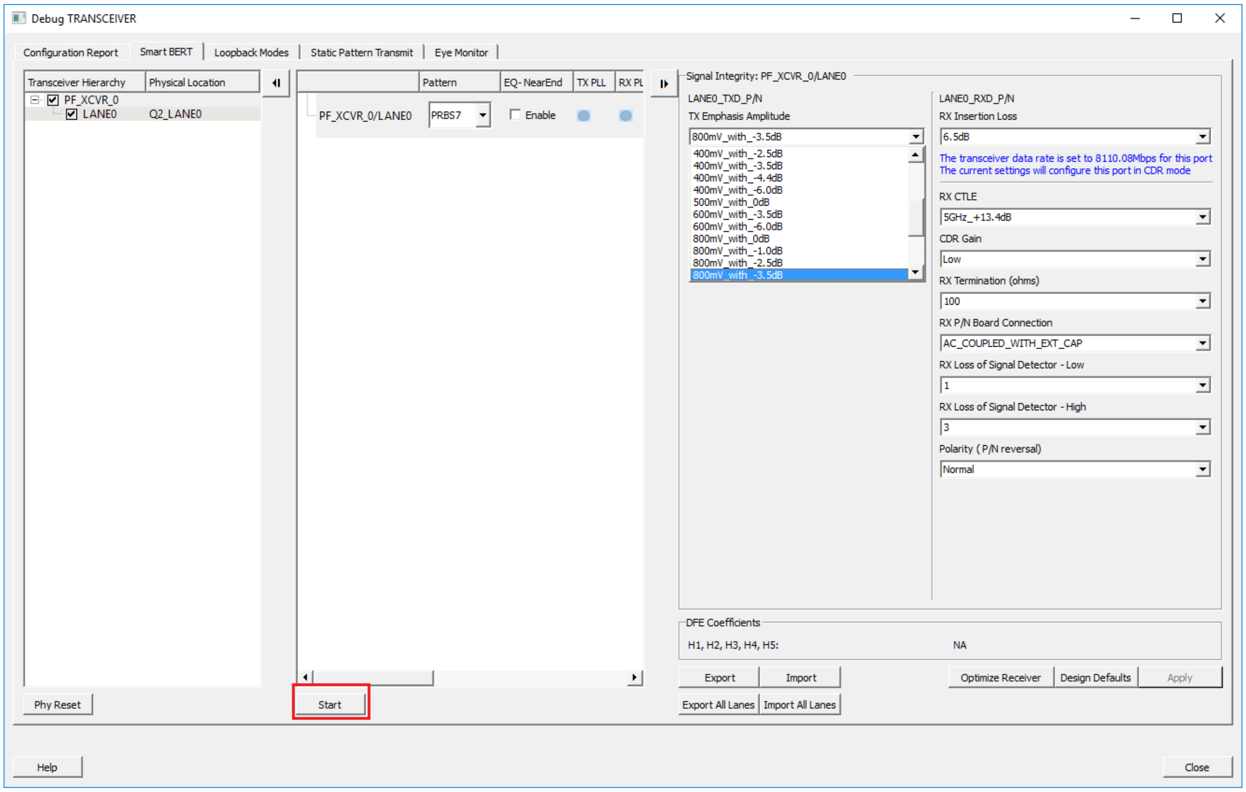
Figure 6 • **Smart Bert**



6. From the drop down menu select the Tx Emphasis amplitude. Selected option sets the device registers to provide the desired de-emphasis for the particular signal amplitude. Tx impedance is also decided based on the signal amplitude.
7. After all the step are completed, click **Apply** for new settings on the device.

8. The inbuilt PRBS generator can be used to send out the data pattern. To enable PRBS generator select appropriate PRBS pattern and click **Start** on the **Smart Bert** window as shown in the following figure.

Figure 7 • **Tx Emphasis Amplitude**



2.1.4 Illustration

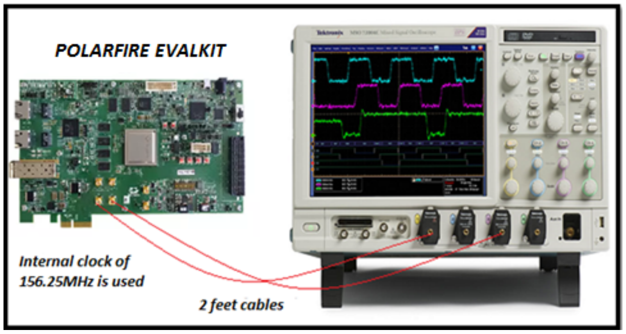
This section describes an example for testing the performance of IBIS-AMI model using PolarFire Evaluation Kit.

Device and Setup Details

- Device Used: MPF300T-1FCG1152.
- Transceiver block: Two Lane 0 is used for measurement.
- Dedicated internal reference clock is used for the SERDES block (156.25MHz).
- LVDS25 IO standard is used to reference clock input.
- 23GHz Tektronix (DPO72304) scope and 100G samples/sec setting is used for measuring jitter and plotting eye.
- Two feet long cable (part# Sucoflex 100 126E) is used for connecting the Tx ports to the scope.
- 2.3 inch long trace is connecting the device and the Tx SMA ports.
- Clock Recovery Configuration:- Method: PLL-Custom BW, PLL Model: Type II, Damping:700m

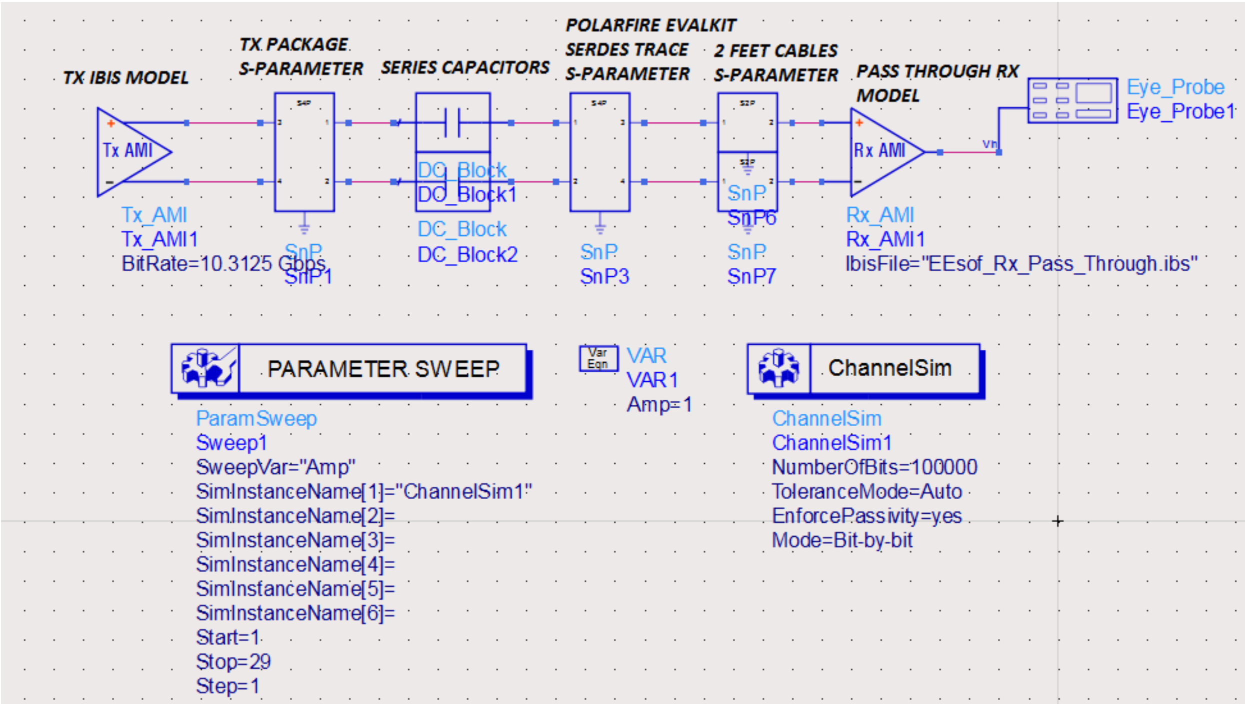
In the measurement the appropriate Tx settings is loaded to the silicon through SmartDebug as explained in SmartDebug Flow, page 7.Use the inbuilt PRBS31 generator to send the data out. Following figure shows the hardware setup used for the measurement.

Figure 8 • **Hardware Setup for Tx**



Design used to test the transmitter performance of the IBIS-AMI model is shown in the following figure. With the help of sweep option different de-emphasis settings is tested and the one which provides the best result is then loaded to SmartDebug. Measurement result is obtained with the best suited settings which is correlated with the simulation to fine tune the model.

Figure 9 • **Design for IBIS-AMI Tx Model**



The IBIS-AMI Tx model is connected to pass through Rx model which is a simple 100 Ω termination through die parasitic, package, board and 24 inch cable s-parameter model. The measurement environment is created virtually through the design in ADS.

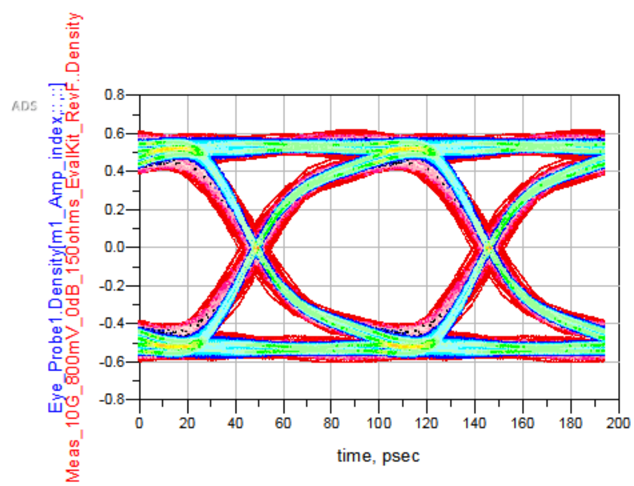
Parameter sweep option is used to test the 29 different de-emphasis setting marked as 1 to 29 with each corresponding to a specific value of signal amplitude and de-emphasis.

Figure 10, page 11 shows the correlation between measurement and IBIS-AMI simulation for following settings:

- Tx Amplitude: 800 mV
- De-emphasis: 0 dB
- Tx Termination: 150 Ω
- Data Rate: 10.3125 Gbps

Simulated Tx Eye correlates well with measurement as shown in following figure.

Figure 10 • **Tx EYE - Measured Vs Simulated**



Note: Blue represents Simulation and Red represents Measurement.

2.2 Receiver

High speed data coming from transmitter passing through a channel can result in degradation of the signals and making it difficult for the receiver to detect it correctly. As the data rate increases, equalization at the receiver becomes a necessity. Equalizers are used to compensate the high frequency losses included by the channel. Analog equalization is done by Continuous Time Linear Equalizers (CTLE) whereas discrete time equalization can be achieved by Decision Feedback Equalization (DFE). For lower data rates CTLE is sufficient, however, for higher data rate DFE is also used along with CTLE.

PolarFire Rx supports 85 Ω, 100 Ω and 150 Ω terminations. The Receiver provides three types of equalizations as explained:

- **CDR Mode**: This option provides users to apply any CTLE setting including the recommended (Default values in the Libero) ones or settings obtained from the IBIS-AMI simulations.
- **CDR Mode with Calibration**: The device internal algorithm optimizes the receiver and applies the best CTLE settings in the device for the given channel and Tx attributes.
- **DFE Mode**: PolarFire transceiver is built with a five tap DFE engine. DFE is used when the data rate is high or loss of the channel is too high. DFE is always used along with CTLE. In CDR Mode with calibration, the device optimizes the receiver and provides best CTLE and associated DFE coefficients. DFE in IBIS-AMI simulations is only used to sign-off the hardware.

For receiver tuning 63 CTLE settings are provided. Libero default CTLE settings are assigned for a particular data rate range and channel however other settings can also be used for the same range as shown in the following table.

Table 4 • **Default Rx CTLE Settings**

Insertion Loss	Data Rate (Mbps)	Mode	RX_CTLE Value
Short (6.5dB)	250-5000	CDR	No Peak +2.8 dB
	5000-6875	CDR	3 GHz +1.4 dB
	6875-8437.5	CDR	5 GHz +1.8 dB
	8437.5-10312.5	CDR	5 GHz +7.3 dB
	10312.5-12700	DFE	5 GHz +10.6dB
Medium (17.0dB)	250-5000	CDR	3 Ghz +5.5 dB
	5000-6875	CDR	3 GHz +1.4 dB
	6875-8437.5	DFE	5 GHz +7.3 dB
	8437.5-10312.5	DFE	5 GHz +7.3 dB
	10312.5-12700	DFE	6 GHz +11.1dB
Long (25.0dB)	250-5000	CDR	3 Ghz +11.4 dB
	5000-6875	CDR	3 GHz +6.8 dB
	6875-8437.5	DFE	5 GHz +7.3 dB
	8437.5-10312.5	DFE	5 GHz +7.3 dB
	10312.5-12700	DFE	6 GHz +11.1dB

The following table contains the information about all 63 CTLE settings and the recommended data rate range in which they are used. Note that user can set any settings for any data rate.

Table 5 • **Rx CTLE Settings**

S.No.	RX_CTLE Settings	DC Gain (dB)	Peak AC Gain (dB)	Data Rate (Mbps)
1	No_Peak_+7.3dB	7.27	7.28	250 - 1600
2	No_Peak_+9.3dB	9.28	9.29	250 - 1600
3	No_Peak_+2.8dB	2.85	3.07	250 - 1600
4	3_Ghz_+5.5dB	-2.28	3.17	250 - 1600
5	3_Ghz_+11.4dB	-7.98	3.46	250 - 1600
6	No_Peak_+2.82dB	2.82	2.84	250 - 1600
7	No_Peak_+0.1dB	0.12	0.13	250 - 1600
8	No_Peak_-2.5dB	-2.57	-2.48	250 - 1600
9	No_Peak_-7.1dB	-7.15	-6.86	250 - 1600
10	3_GHz_+4.62dB	-13.00	-8.38	250 - 1600
11	No_Peak_+4.6dB	4.61	4.62	250 - 1600
12	No_Peak_+1.8dB	1.86	1.88	250 - 1600
13	No_Peak_-0.9dB	-0.94	-0.87	250 - 1600
14	No_Peak_-5.6dB	-5.61	-5.42	250 - 1600
15	3_GHz_+4.6_dB	-11.60	-6.99	250 - 1600
16	3_GHz_+11.0dB	-9.34	1.71	>1600 - 5000
17	3_GHz_+5.6dB	-6.43	-0.77	>1600 - 5000
18	No_Peak_-1.1dB	-1.17	-0.62	>1600 - 5000
19	3_GHz_+12.3dB	-12.77	-0.44	>1600 - 5000
20	3_GHz_+2.3_dB	-6.48	-4.18	>1600 - 5000
21	3_GHz_+9.0dB	-12.96	-3.90	>1600 - 5000
22	3_GHz_+5.9dB	-5.02	0.90	>1600 - 5000
23	No_Peak_+0.3dB	0.37	1.01	>1600 - 5000
24	3_GHz_+12.6dB	-11.37	1.24	>1600 - 5000
25	3_GHz_+2.4dB	-5.07	-2.66	>1600 - 5000
26	3_GHz_+9.1dB	-11.54	-2.37	>1600 - 5000
27	3_GHz_+1.4dB	4.55	5.96	>5000 - 6875
28	3_GHz_+6.8dB	-2.32	4.53	>5000 - 6875
29	3_GHz_+12.9dB	-8.07	4.88	>5000 - 6875
30	3_GHz_+7.8dB	-5.11	2.70	>5000 - 6875
31	3_GHz_+2.2dB	0.29	2.57	>5000 - 6875
32	3_GHz_+14.5dB	-11.50	3.05	>5000 - 6875
33	3_GHz_+4.8dB	-5.16	-0.29	>5000 - 6875
34	3_GHz_+11.8dB	-11.67	0.17	>5000 - 6875
35	5_GHz_+1.8dB	4.56	6.36	>6875 - 8437.5
36	5_GHz_+7.3dB	-2.30	5.03	>6875 - 8437.5

Table 5 • **Rx CTLE Settings *(continued)***

S.No.	RX_CTLE Settings	DC Gain (dB)	Peak AC Gain (dB)	Data Rate (Mbps)
37	5_GHz_+13.4dB	-8.07	5.38	>6875 - 8437.5
38	5_GHz_+8.4dB	-5.11	3.33	>6875 - 8437.5
39	5_GHz_+2.8dB	0.30	3.14	>6875 - 8437.5
40	5_GHz_+15.1dB	-11.50	3.68	>6875 - 8437.5
41	5_GHz_+5.7dB	-5.16	0.58	>6875 - 8437.5
42	5_GHz_+12.7dB	-11.70	1.09	>6875 - 8437.5
43	5_GHz_+9.8dB	-5.43	4.40	>8437.5 - 10312.5
44	5_GHz_+12.4dB	-8.09	4.35	>8437.5 - 10312.5
45	5_GHz_+9.6dB	-5.40	4.22	>8437.5 - 10312.5
46	5_GHz_+10.6dB	-5.38	5.20	>8437.5 - 10312.5
47	6_GHz_+11.1dB	-4.34	6.79	>10312.5
48	6_GHz_+10.1dB	-4.34	5.79	>10312.5
49	6_GHz_+10.13dB	-4.18	5.95	>10312.5
50	6_GHz_+12.2dB	-10.14	2.06	>10312.5
51	6_GHz_+11.0dB	-6.82	4.24	>10312.5
52	6_GHz+12.0dB	-6.97	5.07	>10312.5
53	6_GHz_+11.5dB	-7.25	4.28	>10312.5
54	6_GHz_+13.1dB	-7.17	5.92	>10312.5
55	No_Peak_+9.22 dB	9.22	9.24	>8437.5 - 10312.5
56	No_Peak_+4.53 dB	4.53	4.55	>8437.5 - 10312.5
57	No_Peak_+1.76 dB	1.76	1.78	>8437.5 - 10312.5
58	5_GHz_+3.14 dB	-1.52	1.61	>8437.5 - 10312.5
59	No_Peak_+11.10 dB	11.10	11.13	>10312.5
60	No_Peak_+6.13 dB	6.13	6.15	>10312.5
61	No_Peak_+3.39 dB	3.39	3.41	>10312.5
62	6_GHz_+2.73 dB	0.32	3.06	>10312.5
63	6_GHz_+3.12 dB	1.50	4.62	>10312.5

For higher dates rate, 5 tap DFE is used along with CTLE. Libero sets the default DFE and CTLE settings for given channel and data rate as shown in following table.

Note: These settings are used when auto calibration of DFE is not selected.

Table 6 • **Default Rx DFE Coefficients**

Channel	Data Rate	Ctle Setting	DFE Coefficients
SHORT	10312.5-12700	5_GHz_+10.6dB	6,-3,-2,-1,-1
MEDIUM	6875 - 8437.5	5_GHz_+7.3dB	7,1,2,2,0
MEDIUM	8437.5 - 10312.5	5_GHz_+7.3dB	8,-3,-2,-1,0
MEDIUM	10312.5-12700	6_GHz_+11.1dB	10,0,-2,-1,0

Table 6 • **Default Rx DFE Coefficients**

Channel	Data Rate	Ctle Setting	DFE Coefficients
LONG	6875 - 8437.5	5_GHz_+7.3dB	7,-1,0,0,0
LONG	8437.5 - 10312.5	5_GHz_+7.3dB	8,-5,-1,-1,0
LONG	10312.5-12700	6_GHz_+11.1dB	10,1,0,0,0

2.2.1 IBIS-AMI

This section describes the IBIS-AMI Rx model parameters that needs to be varied in order to obtain proper tuning of the receiver. In Rx model, AMI tab contains four important parameters used for receiver optimization. The following table lists the information about the four key parameters.

Table 7 • **Rx Model Parameter Descriptions**

Rx Variable	Description
RXTERM	Rx Termination. It supports 85 Ω, 100 Ω and 150 Ω
CTLE_ID	This parameter changes the CTLE Settings. Total 63 settings are provided. Detailed description of the complete 63 settings are provided in Table 5, page 13.
DFE_MODE	Determine the DFE calibration mode. 1=off, 2=fixed, 3=adapt. Adapt mode does auto calibration of the device to obtain the best DFE coefficients where as in fixed mode coefficients are added manually.
DFE_TAP	5 Tap DFE is used. Each tap can be manually edited by the costumers in DFE_MODE=2 or DFE_MODE=3. In DFE_MODE=3 the tool takes the value provided in DFE_TAP as initial values to obtain the optimized DFE coefficients.

DFE, when used in adapt mode, calibrates the receiver and gives the best DFE coefficients. These coefficients are then used in the fixed mode in simulation to view the proper eye. Each DFE coefficient in Libero corresponds to 6m in IBIS-AMI DFE tap (tap1 to tap5). Mapping of the coefficients is described in the following table.

Table 8 • **DFE Coefficient Mapping between IBIS-AMI and Libero**

IBIS AMI Value	Libero Value (Hex)	IBIS AMI Value	Libero Value (Hex)
0.006	-1	-0.006	1
0.012	-2	-0.012	2
0.018	-3	-0.018	3
0.024	-4	-0.024	4
0.03	-5	-0.03	5
0.036	-6	-0.036	6
0.042	-7	-0.042	7
0.048	-8	-0.048	8
0.054	-9	-0.054	9
0.06	-a	-0.06	a
0.066	-b	-0.066	b
0.72	-c	-0.72	c
0.78	-d	-0.78	d

Table 8 • DFE Coefficient Mapping between IBIS-AMI and Libero

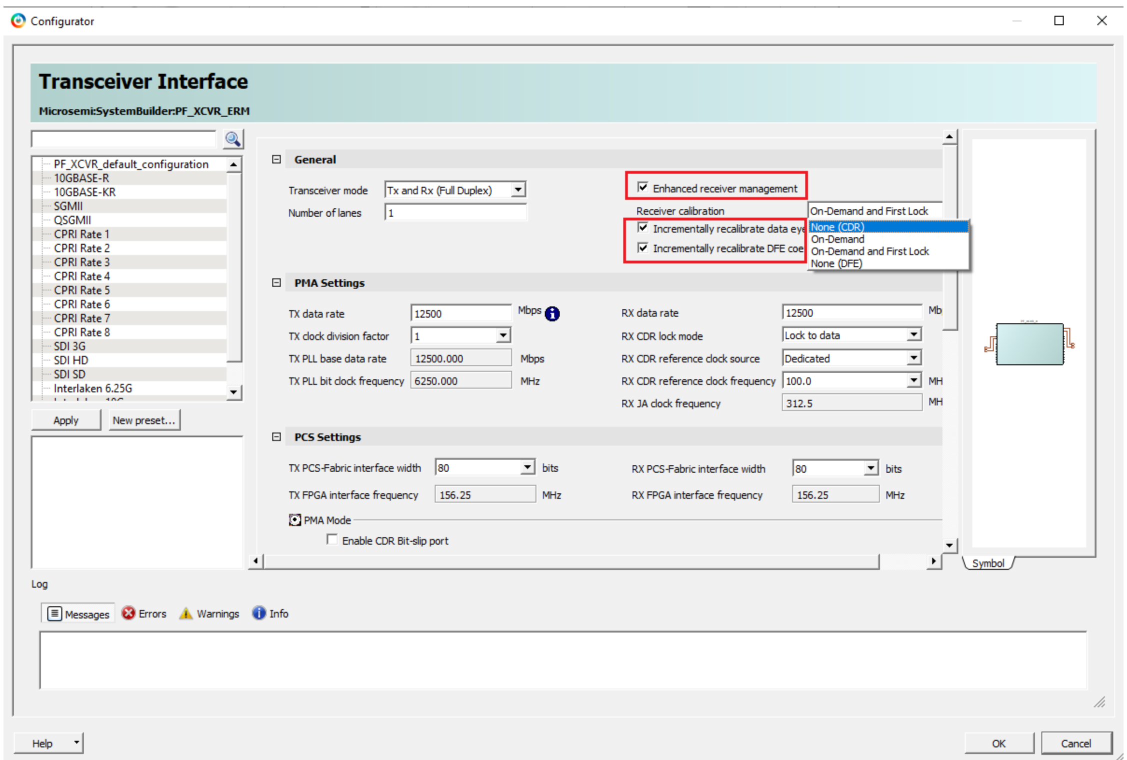
IBIS AMI Value	Libero Value (Hex)	IBIS AMI Value	Libero Value (Hex)
0.084	-e	-0.084	e
0.09	-f	-0.09	f

2.2.2 Libero Flow

Transceiver settings applied using Libero while generating the bit file is explained in IBIS-AMI, page 5. Apart from the earlier explained settings, the Rx model has an additional option for receiver calibration. This feature is available only in Libero SoC 12.0 and above and not supported by Libero version 2.3 or below.

Select the **Transceiver Interface** in the SmartDesign window to open the configurator dialog box as shown in following figure. The Transceiver supports Enhanced Receiver Management (ERM), which adds DFE/CDR calibration management and lock-to-data detection capabilities. The ERM is implemented in the FPGA logic inside the XCVR component. For more information about ERM, see the Enhanced Receiver Management section in *PolarFire and PolarFire SoC FPGA Transceiver User Guide*.

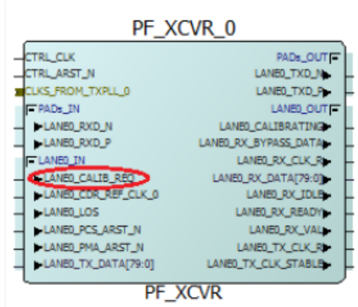
Figure 11 • **Transceiver Interface**



The following receiver calibration options are provided for the ERM operation:

- **None (CDR)**: Select this option if the XCVR is configured as CDR and no CTLE auto-calibration is performed. Static settings are configured by Libero SoC based on data rate and backplane model.
- **On-Demand**: Select this option to perform calibration on-demand. This option is available for both CDR and DFE configuration of the XCVR. You can trigger calibration on-demand using CALIB_REQ port as shown in Figure 12, page 17. The CALIBRATING signal is asserted upon CALIB_REQ assertion and de-asserted when the calibration is completed.

Figure 12 • **Transceiver Interface with On-Demand Calibration**



- On-Demand and First Lock: This method is an extension to On-Demand calibration option. This allows the customers to perform CDR/DFE calibration either by toggling the CALIB_REQ pin or after the power on reset.
- None (Static_DFE): DC Offset Calibration of the CDR is performed, however, the DFE Coefficients are set through PDC commands used from the register rather than from automatic DFE calibration operation. To set the required registers with static values, users must enhance the “set_io” PDC command to add new attributes. The new attributes that need to be added are highlighted in the following example PDC file.

```
set_io -port_name LANE0_RXD_N \
-RX_DFE_COEFFICIENT_H1 20 \
-RX_DFE_COEFFICIENT_H2 20 \
-RX_DFE_COEFFICIENT_H3 20 \
-RX_DFE_COEFFICIENT_H4 20 \
-RX_DFE_COEFFICIENT_H5 20 \
-DIRECTION INPUT
```

The RX_DFE_COEFFICIENT attributes are optional (applied only when Static calibration is selected). These attributes take integer values between 0 and 15. The corresponding register fields are 5 bits wide in all cases with the MSB bit reserved for sign bit. Static_DFE does not use the DFE calibration routine and requires the user to carefully select DFE coefficient values. These values can be gathered by the SmartDebug tool or by simulation. When an initial calibration is completed, the performance of the DFE path can be improved incrementally in the following ways.

- **Incrementally Recalibrate Data Eye**: This recalibration should improve the data eye for most gradients that typically occur from temperature or voltage changes within the system.
- **Incrementally Recalibrate DFE Coefficient**: This recalibration performs the DFE calibration in incremental method. The initially calculated DFE coefficient values are used as the starting values for this algorithm.This results in the reduction of the Calibration time by reducing the number of DFE coefficients that requires recalibration.

Note: Full calibration is always done for DFE. You must select any one of the two options—On-Demand and First Lock or On-Demand—if the transceiver is configured in DFE mode.

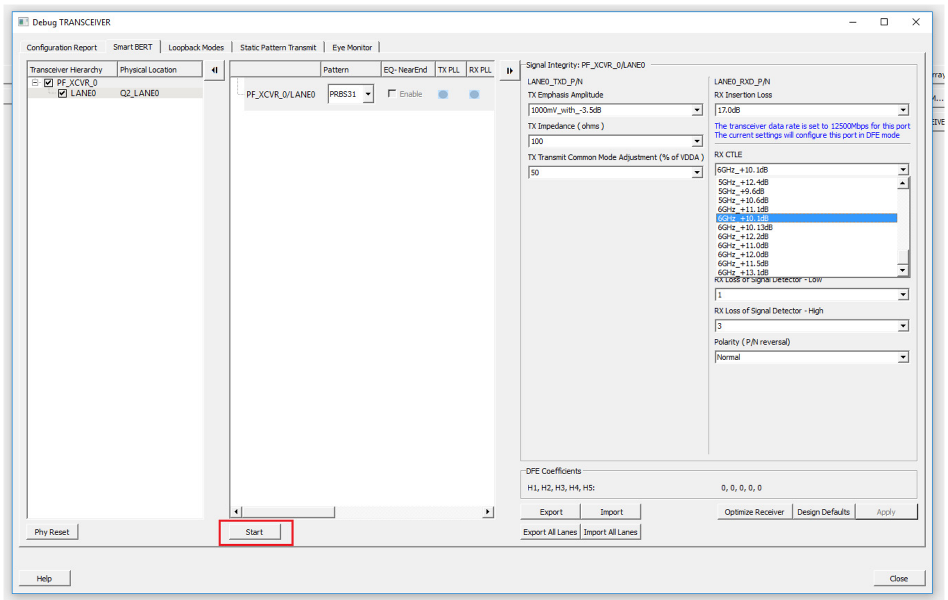
In the **Signal Integrity** View window of **I/O Editor** shown in Figure 3, page 6, the following Rx settings are selected.

1. **Calibration**: None(CDR)/On-Demand/On-Demand and First lock/None(Static DFE) options are provided. Please refer receiver calibration modes described above.
2. **RX_CTLE**: 63 CTLE settings are provided as shown in Table 5, page 13. Users can select any value from IBIS-AMI simulations or recommended values from Table 4, page 12 or from Table 5, page 13.
3. **DFE Mode**: DFE mode is enabled automatically based on the data rate and insertion loss of a channel. DFE values are either auto-tuned in On-demand/On-demand and First Lock mode or set to values recommended in Table 4, page 12 or set by PDC commands in static DFE mode described in the previous section.

2.2.3 SmartDebug Flow

Follow the section SmartDebug Flow, page 7 for invoking the SmartDebug GUI from the Libero. Select the appropriate receiver settings from the menu as shown in following figure. Click **Apply** to apply the settings to PolarFire transceiver.

Figure 13 • **Rx CTLE Settings**



CTLE mode: user can select any of 63 CTLE settings from Rx CTLE tab. After selecting the Transmitter and Receiver attributes.

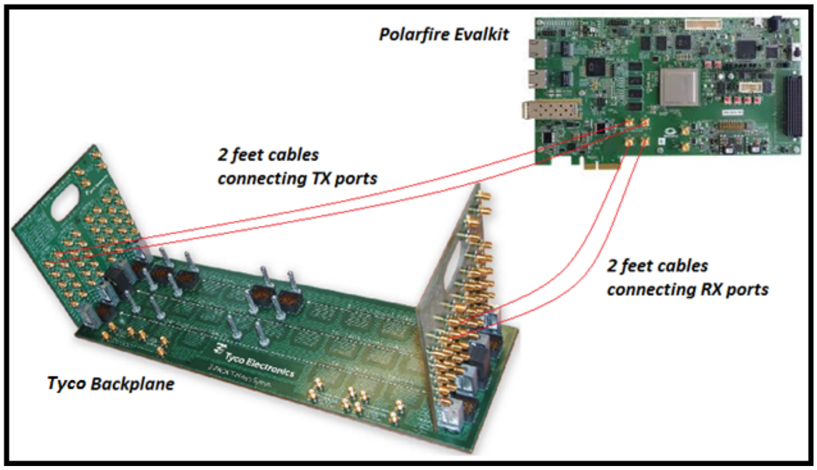
DFE mode: in case the design working in DFE mode, use Optimize Receiver button to auto tune the CTLE and DFE settings. New settings will be displays on the GUI.

In case, user using far end loop back mode, user can generate the PRBS pattern to transfer the data stream. Click **Start** to start the data out as shown in the Figure 13, page 18.

2.2.4 Illustration

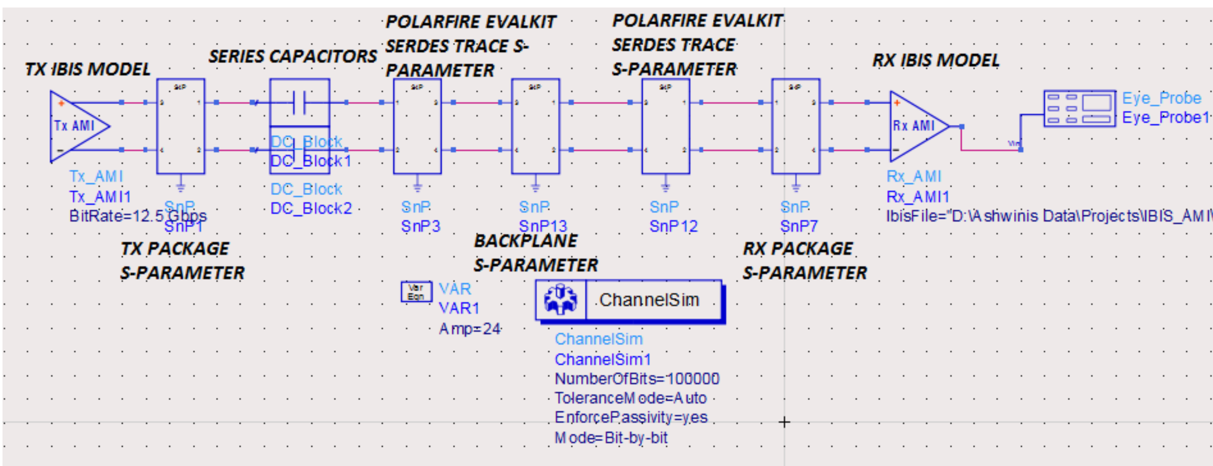
For receiver performance of the IBIS-AMI model, the following design is used as shown in Figure 14, page 19. The Tx is connected to the Rx through, board, 24 inch cables, package and backplane. The output of the backplane is looped back the PolarFire Evaluation kit Rx SMAs. Following figure shows the hardware setup.

Figure 14 • Hardware Setup for Tx



The equivalent IBIS-AMI simulation setup is shown in the following figure.

Figure 15 • Equivalent IBIS-AMI Simulation Setup For Hardware Setup



The different modes are described as follows.

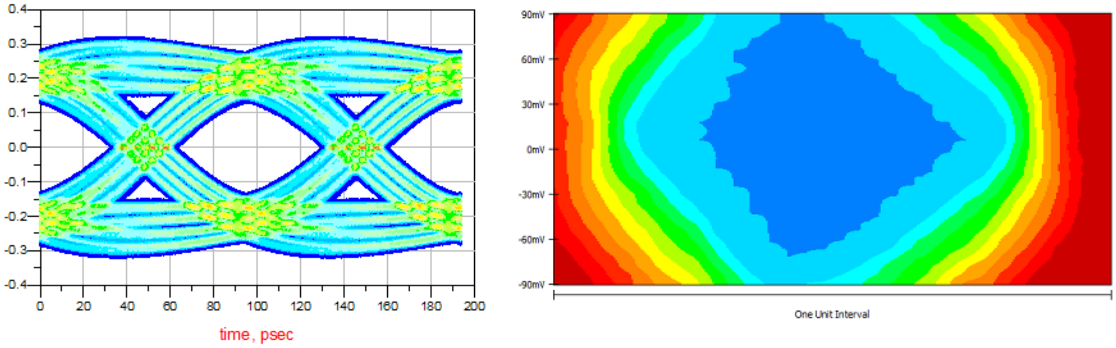
2.2.4.1 CTLE (CDR mode)

CTLE can be used up to 10.3125 Gbps for short channel as shown in the Table 4, page 12. The following example show the data capture with default Libero settings as well as optimal CTLE values from IBIS-AMI simulations at 10.3125Gbps.
The system used for the short reach is 5 inch backplane channel along with cables and PolarFire board traces with following transceiver settings.

- Tx: 400mV, 0dB, 100 Ω
- Rx: 100 Ω
  Libero default CTLE: 5GHz+7.3db and CTLE from Simulation: 5GHz+1.8db
- Data Pattern: PRBS31

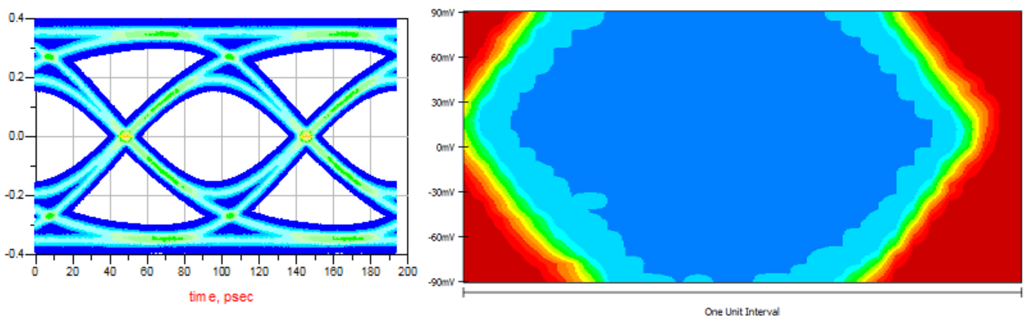
The following figure shows the eye Plot from Simulation with Libero default CTLE setting and corresponding eye from ye monitor on SmartDebug

Figure 16 • Eye Plot and Monitor—Default Setting with Short Reach



The following figure shows eye plot captured with optimal CTLE setting from Simulation and corresponding eye from eye monitor on SmartDebug.

Figure 17 • Eye Plot and Monitor—Optimal Setting with Short Reach



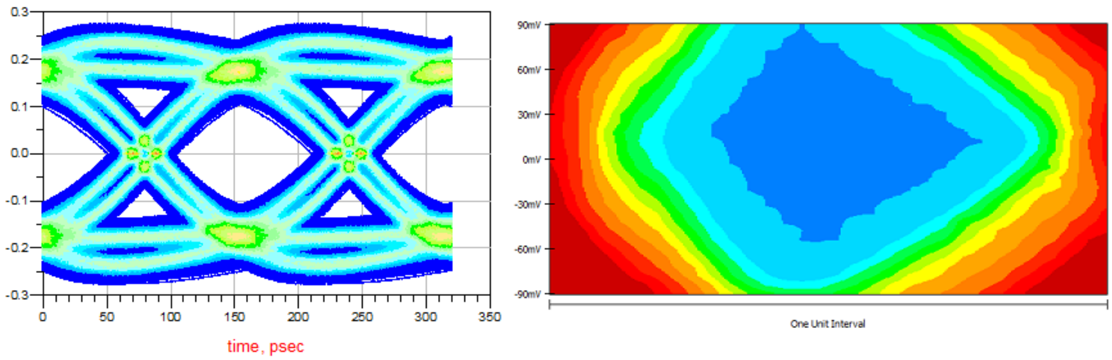
Note that, eye with simulated CTLE values look better than the Libero default CTLE setting since the Libero default CTLE setting is calibrated to have loss of 6.5dB which is higher than the loss used in this example. Default Libero settings works with zero bit error however, best value can be found from the IBIS-AMI simulation. In case of CDR Mode with calibration, Transceiver tunes the best CTLE setting.

CTLE can be used up to 6.8Gbps for long channel as shown in the table 4. Below example show the data capture with default Libero settings as well as optimal CTLE values from IBIS-AMI simulations at 6.25Gbps. The system used for the long reach is 34 inch backplane channel along with cables and PolarFire board traces.

- Tx: 1000mV, -6dB, 180 Ω
- Rx: 100 Ω
  Libero default CTLE: 3GHz+6.8db
  CTLE from Simulation: 5GHz+7.3db
- Data Pattern: PRBS31

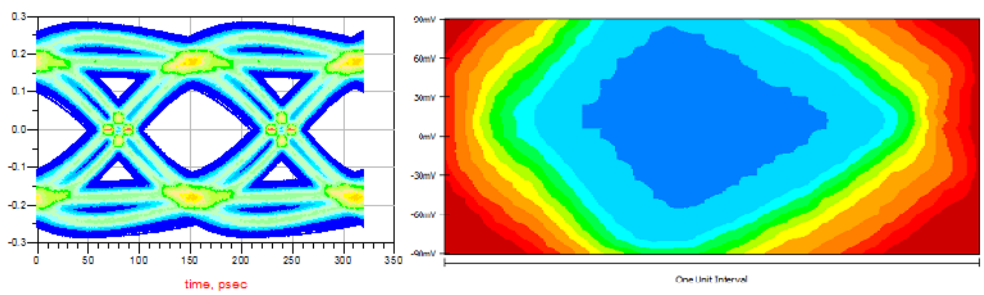
The following figure shows the eye from simulation with Libero default CTLE setting and Corresponding Eye from Eye Monitor on SmartDebug

Figure 18 • **Eye Plot and Monitor —Libero Default CTLE Setting-with long reach**



The following figure shows eye captured with optimal CTLE setting from simulation and corresponding eye from eye monitor on SmartDebug.

Figure 19 • **Eye Plot and Monitor —Optimal CTLE Setting with long reach**



Both the eyes with Libero default CTLE and CTLE from simulation shows similar results.

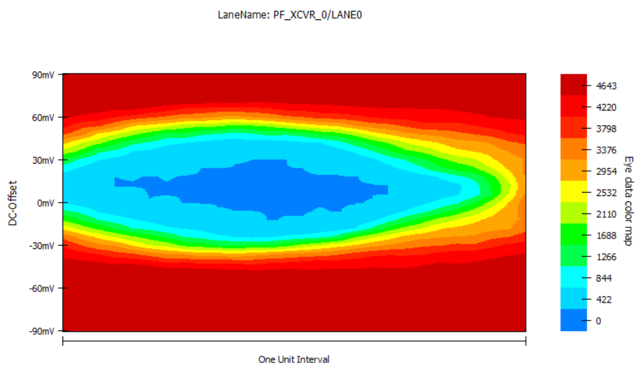
2.2.4.2 DFE Mode

DFE is used above 6.8Gbps for long and medium reach channel, and above 10.3125Gbps for short reach channel. Below example is based on long channel at 12.5Gbps. The transceiver tunes the best value with following system attributes.

- Channel: 34 inch backplane channel and 4 inch PolarFire Evaluation Kit PCB trace
- Tx Amplitude: 800 mV
- De-emphasis: 0 dB
- Tx Termination: 150 Ω
- Data Rate: 12.5 Gbps
- Data pattern: PRBS31

Following figure shows the eye obtained in SmartDebug. The system works with zero bit errors.

Figure 20 • **Eye from SmartDebug at 12.5Gbps, Long Backplane Channel**



The blue portion shows the zero bit error rate region.

3 Glossary

Following are the commonly used terminology in this document.

- **TX**: Transmitter
- **RX**: Receiver
- **Channel**: The connecting medium between Transceiver TX to Transceiver RX is called channel. A channel may contains PCB traces, connectors, cables and backplanes.
- **Insertion Loss**: The Insertion loss is the loss of signal power resulting from the insertion due to a transmission line (Channel) and is usually expressed in decibels. The insertion loss is always expressed with respect to frequency. In this document, the loss is expressed at 5Ghz frequency.
- **Reach**: Reach is a way express the insertion loss of the channel in simple terms. The following terms are used in the document
  - Very Short Channel or Very Short Reach: channel loss is less than 2dB
  - Short length Channel or Short Reach: channel loss is less than 6.5dB
  - Medium length Channel or Medium Reach: channel loss is less than 17dB
  - Long length Channel or Long Reach: channel loss is less than 25dB
- **Libero**: Libero is a software to design and generate the PolarFire FPGA programming bit file.
- **SmartDebug**: A tool in the Libero used for debugging the transceiver online.
- **IBIS-AMI**: IBIS-AMI is a set of files used to simulate the PolarFire transceiver with channel, using simulators such as ADS, Hyperlynx, SystemSI, QCD and so on. IBIS-AMI simulations helps in finalizing the transceiver settings and sign-off its hardware.