

DG0839
Demo Guide
PolarFire FPGA Wireless Radio Digital Front-End
Design



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

The first publication of this document.

2 Wireless Radio Digital Front-End Design

This document describes the Microsemi PolarFire® wireless radio digital front-end (DFE) design and how to run the demo using the PolarFire Evaluation Board, Microsemi Wireless MIMO Daughter Card, and a Remote Radio Head (RRH) Tester.

The demo design features:

- Baseband interface using the CPRI IP
 - Signal processing, Digital Up-Conversion (DUC) and Digital Down-Conversion (DDC)
 - RFIC interface using the JESD204B IP
 - Mi-V soft processor and its peripheral interfaces — SPI, GPIO, and UART
- Microsemi offers the Mi-V processor IP core and software toolchain to support RISC-V processor-based designs.

This fully integrated demo design is created using Microsemi Libero SoC PolarFire® to help customers build prototypes quickly.

The PolarFire Evaluation Board features:

- A 300K LE FPGA (MPF300TS, FCG1152) with 12.7 Gbps transceiver interface
- DDR3 and DDR4 interfaces
- A high pin count FMC connector for plugging in expansion boards

For more information, see the [PolarFire Evaluation Kit](#) page.

The wireless MIMO daughter card features:

- Two AD9371 RFIC chips for four transmit and four receive paths. Each chip supports:
 - 300 MHz to 6 GHz frequency range
 - Dual transmit and Dual receive paths
 - JESD204B digital interface
- AD9528, a two stage PLL with a JESD204B sysref generator
- A high pin count (HPC) FMC connector to connect to an FPGA base board

The RRH tester features:

- One-box solution including a Common Public Radio Interface (CPRI) and Tx/Rx paths
- Send and receive digital IQ data to and from the RRH using CPRI optical connection
- Software options for LTE FDD & TDD signal generation and analysis

For more information, see <http://www.keysight.com/find/E6610A>.

2.1 Design Requirements

The following table lists the design requirements for running the demo.

Table 1 • Design Requirements

Requirements	Description
Host PC	with Windows 10 OS
Serial Terminal Emulation Program	PuTTY
Design Software	
Libero SoC PolarFire	v2.2
SoftConsole	v5.2
Hardware	
PolarFire Evaluation Kit	Rev C
MIMO Daughter Card	
SFP+ transceiver modules	Wavelength: 1310 nm Class 1 DFB laser Connector: LC duplex Max Link Length: 10 KM Max Data Rate: 10.5 Gb/s Temperature Range: -40 °C to +85 °C
Fiber patch	Cable Type: single mode fiber with yellow 2 mm jacket Length: 3 M Connector: LC duplex
RF SMA cables	PASTERNAK SMA Female to SMA Female Cables
Power Splitters	
Test Hardware and Software	
Remote Radio Head Tester	E6610A (700 MHz to 2.7 GHz)
E6610A User Interface	v2.9.5 (2x2 LTE)

2.2 Prerequisites

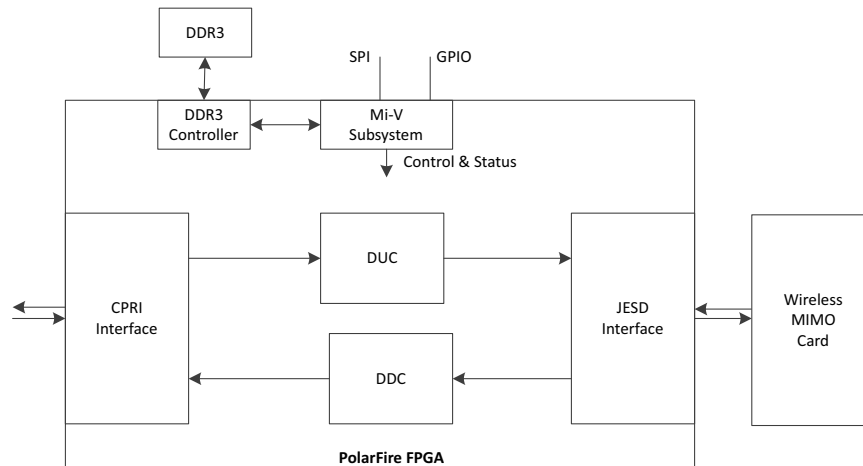
Before you start:

1. Download the design files from:
http://soc.microsemi.com/download/rsc/?f=mpf_dg0839_liberosocpolarfirev2p2_df
2. Download and install Libero SoC PolarFire v2.2 from:
<https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polar-fire#downloads>
3. Download and install SoftConsole v5.2 from:
<https://www.microsemi.com/product-directory/design-tools/4879-softconsole#downloads>
4. Download and install Microsemi PowerMonitor from:
http://soc.microsemi.com/download/rsc/?f=polarfire_power_monitor
5. Download and install KEYSIGHT E6610A User Interface from:
http://www.keysight.com/find/E6610A_Software

2.3 Demo Design Architecture

The demo design supports a 4x4 MIMO, single carrier LTE 20 MHz bandwidth in the FDD mode. The basic system architecture consists of three main data modules—the CPRI IP, DUC and DDC blocks, and the JESD204B IP. The Mi-V soft processor is used for controlling and monitoring functions. The following figure shows the system architecture of the demo design.

Figure 1 • PolarFire Wireless Radio DFE Design Architecture



The following points describe the high-level data flow in the design:

1. The transmit IQ data from the baseband module is received on the Rx port of the CPRI IP and is de-mapped to four antenna carriers. This data is time-division multiplexed in the format required by the DUC chain.
2. The DUC block up-samples and up-converts the received data and then sends it to the JESD204B transmit interface.
3. Similarly, the JESD204B receive interface receives the data from the RFIC module and sends it to DDC for down-conversion and down-sampling.
4. The down-sampled data is then mapped to the four antenna carriers and sent to the Tx port of the CPRI IP.

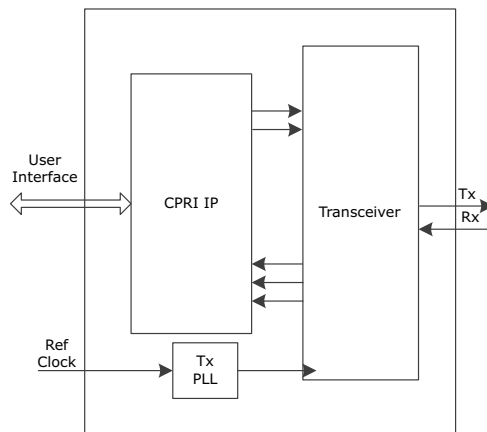
2.3.1 Subsystem Components

The following sections describe the subsystems used in the design.

2.3.1.1 CPRI Interface

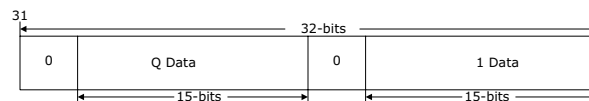
The CPRI IP is configured as a slave at 4.9 Gbps line rate with 4 antenna carriers (AxC), each carrying 20 MHz LTE bandwidth.

Figure 2, page 5 shows the CPRI interface.

Figure 2 • CPRI Interface

The following points describe the port configurations of the CPRI IP:

- The TX and RX AxC data plane ports are enabled.
- The Ethernet TX and RX ports are disabled.
- The vendor specific data and AxC control data ports are looped back.
- The I and Q samples of each AxC are fixed at 15 bits.
- The user interface width is fixed at 32-bits. With zero appending on MSB, 15-bit wide I and Q samples are bit-stuffed in the 32-bit user interface width as shown in the following figure.

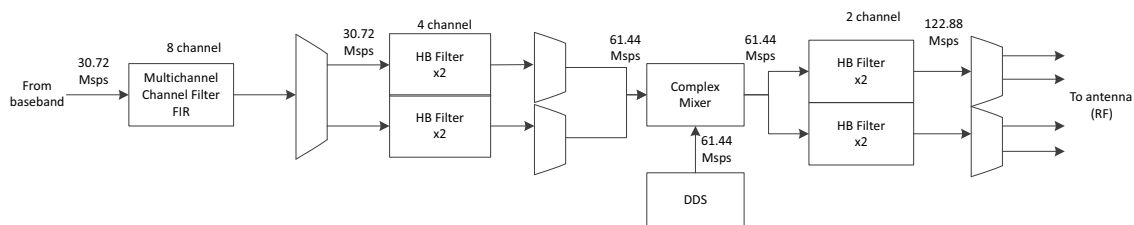
Figure 3 • I and Q Patterns

The transceiver data rate is set to 4.9 Gbps.

For more information about the CPRI IP, see *UG0822: CPRI IP User Guide* from Libero Catalog.

2.3.1.2 DUC and DDC

The DUC and DDC blocks are designed to support a single carrier LTE with 20 MHz bandwidth. These blocks are clocked at 245.76 MHz. The following figure shows the DUC structure for two antenna carriers. The same structure is replicated for the other two antenna carriers.

Figure 4 • DUC

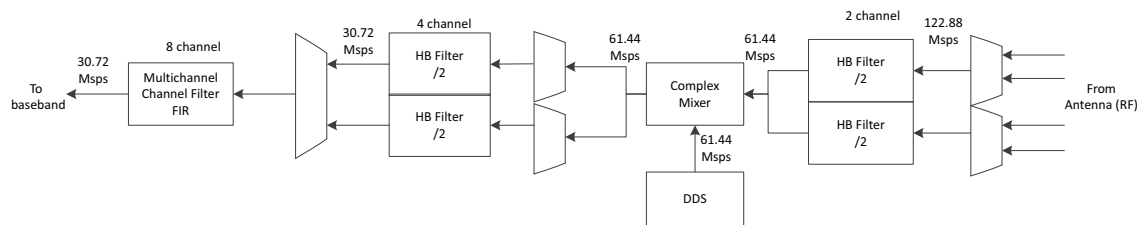
DUC contains a cascaded series of filters, which up-convert a 30.72 Msp/s sample rate to 122.88 Msp/s as per the following process.

1. The channel filter is a multi-channel FIR structure with 8 channels sampled at 30.72 Msp/s.
2. The two 4-channel half-band interpolation filters double the sample rate to 61.44 Msp/s.
3. The complex mixer and direct digital synthesizer (DDS) are used for up-conversion.

- The output of the complex mixer is passed to the two 2-channel half-band interpolation filters to increase the sample rate to 122.88 Msp/s.

The following figure shows the DDC structure.

Figure 5 • DDC



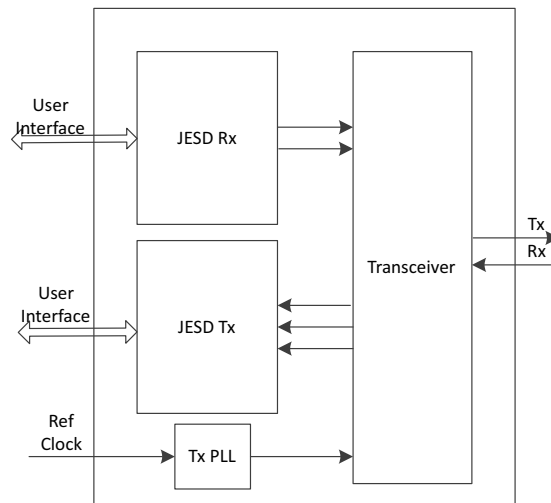
The DDC contains a cascaded series of filters, which down-convert a 122.88 Msp/s sample rate to 30.72 Msp/s as per the following process:

- The two 2-channel half-band decimation filters convert the sample rate from 122.88 Msp/s to 61.44 Msp/s.
- The complex mixer and direct digital synthesizer (DDS) blocks are used for down-conversion.
- The output of the complex mixer is passed to the next two 4-channel half-band decimation filters to reduce the sample rate to 30.72 Msp/s.
- The output of the decimation filters is passed to the multi-channel FIR structure with 8 channels sampled at 30.72 Msp/s.

2.3.1.3 JESD204B Interface

The JESD204B subclass 1 transmit and receive IPs are used at 4.9 Gbps rate. The JESD204B interface is configured to interface with the AD9371 RFIC. The following figure shows the JESD204B blocks.

Figure 6 • JESD204B Interface



For each AD9371, the design includes a pair of JESD204B TX and RX blocks. The transceiver is configured for:

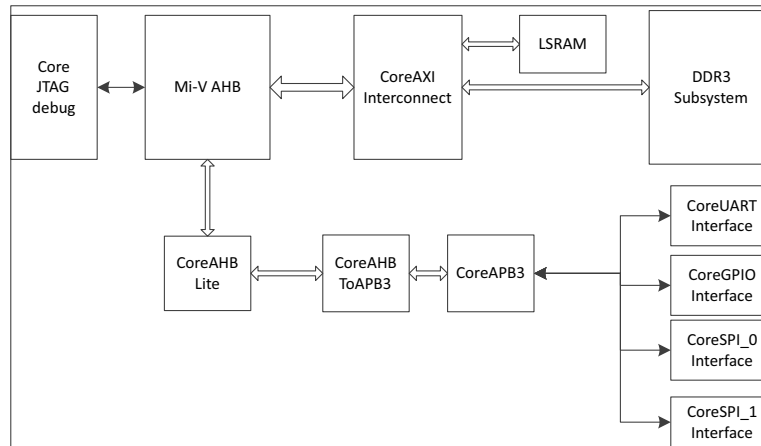
- Two lanes at 122.88 MHz clock— each lane carries 32-bit IQ data for a mixed signal converter.
- A 32-bit PCS interface.

For more information about the JESD204B TX and RX IPs, see [CoreJESD204BTX Handbook](#) and [CoreJESD204BRX Handbook](#).

2.3.1.4 Processor Subsystem

The Mi-V soft processor operates at 111.111 MHz and executes the user application code from an external DDR3. The following figure shows the Mi-V based processor system and its interfaces.

Figure 7 • Mi-V Processor Subsystem



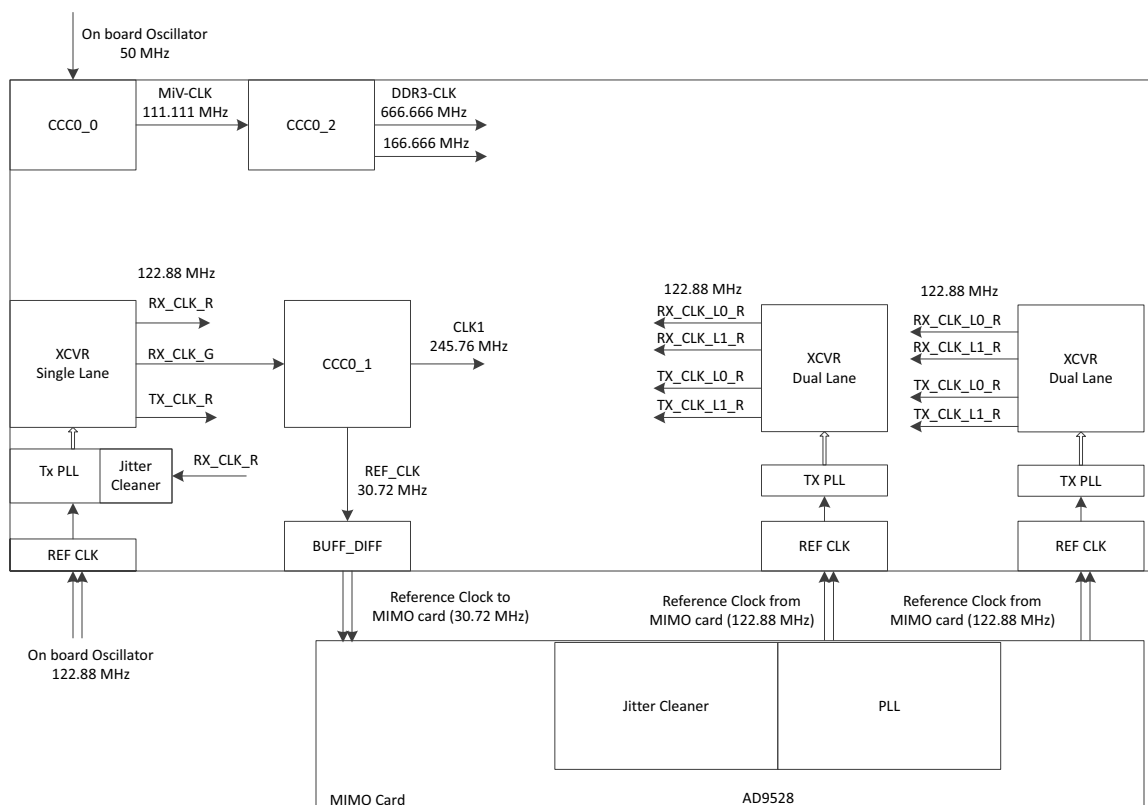
As shown in [Figure 7](#), page 7, the Mi-V subsystem is used to initialize and monitor the CPRI IP via the AHB bus, and the external RFICs via the SPI interface. CoreSPI_0 is used to configure AD9528 and one RFIC chip (AD9371). CoreSPI_1 is used to configure the other RFIC chip. The CoreGPIO interface is used for the soft reset of the JESD204B interface. The CoreUART interface is reserved for internal design debugging.

For more information about how to build the Mi-V subsystem, see [TU0775: PolarFire FPGA: Building a Mi-V Processor Subsystem Tutorial](#).

2.3.2 Clocking Structure

The clocking structure in the demo design is shown in the following figure.

Figure 8 • Clocking Structure



As shown in [Figure 8](#), page 8, the following points summarize the clocking structure:

- In the CPRI interface, the transceiver clock settings are as follows:
 - TX clock is set to Regional (TX_CLK_R) and the RX clock is set to Global (shared). As a result, both the RX regional (RX_CLK_R) and RX global (RX_CLK_G) clocks are enabled.
 - The jitter cleaner feature is enabled in the Tx PLL. The jitter cleaner derives its reference from the transceiver recovered clock to synchronize the TX_CLK clock.
- The global RX clock serves as the reference to all the data modules in the system.
- The CPRI interface uses the RX_CLK_R and TX_CLK_R (122.88 MHz) clocks.
- The DUC and DDC blocks use the 245.76 MHz clock generated from the CCC0_1.
- CCC0_1 also generates a 30.72 MHz fabric clock that is used as the reference clock by AD9528.
- Using the 30.72 MHz reference clock, AD9528 generates the 122.88 MHz reference clock for JESD204B.
- The Mi-V subsystem uses the 111.111 MHz clock generated from CCC0_0.
- Using 111.111 MHz as the reference, the CCC0_2 block generates 666.666 MHz and 166.666 MHz clocks for the DDR3 block.

The following table lists all of the clocks used in the design, their source, frequency, and purpose.

Table 2 • Clocks

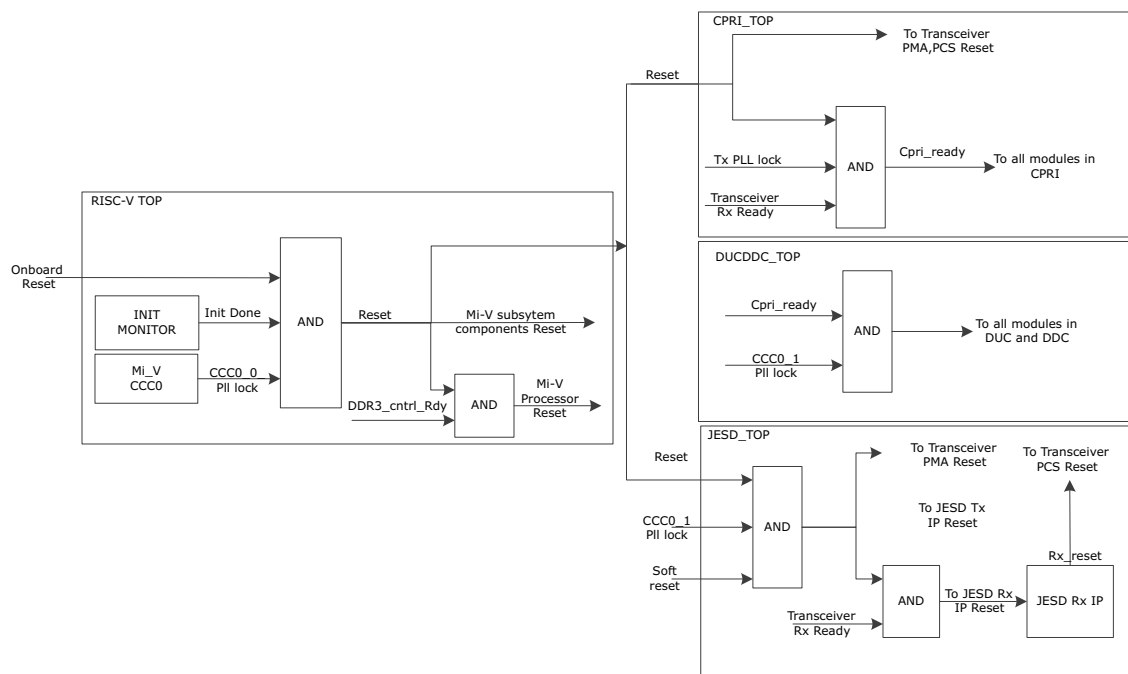
Clock Name	Source	Frequency	Purpose
Mi-V_CLK	CCC0_0	111.111 MHz	Mi-V processor clock
DDR3-CLK	CCC0_2	666.666 MHz 166.666 MHz	DDR3 clocks
RX_CLK_G	Transceiver RX recovered clock	122.88 MHz	CPRI RX
TX_CLK_G	Transceiver TX PLL	122.88 MHz	CPRI TX

Table 2 • Clocks (continued)

Clock Name	Source	Frequency	Purpose
RX_CLK_R	Transceiver RX recovered clock	122.88 MHz	CPRI RX
CLK1	CCC0_1	245.76 MHz	DUC and DDC
REF_CLK	CCC0_1	30.72 MHz	Reference clock to the MIMO card
RX_CLK_L0_R	Transceiver RX recovered clock (Lane 0)	122.88 MHz	JESD204B RX
RX_CLK_L1_R	Transceiver RX recovered clock (Lane 1)	122.88 MHz	JESD204B RX
TX_CLK_L0_R	Transceiver TX PLL (Lane 0)	122.88 MHz	JESD204B TX
TX_CLK_L1_R	Transceiver TX PLL (Lane 1)	122.88 MHz	JESD204B TX

2.3.3 Reset Structure

The reset structure in the demo design is shown in the following figure.

Figure 9 • Reset Structure

As shown in [Figure 9](#), page 9, the following points summarize the reset structure of the design:

- The reset signal from the RISC-V top module drives the reset of all the other modules in the design.
- The onboard push button reset, device initialization init_done, and the PLL lock signals generate the reset signal (Reset) for all the components of the Mi-V subsystem.
- TX_PLL and transceiver RX_Ready signals in CPRI are ANDed with the Mi-V Reset to generate the reset signal (Cpri_ready) for all of the components of the CPRI top module.
- The Mi-V reset signal also resets the CPRI transceiver.
- Cpri_ready and PLL lock signals generate the reset signal for the DDCDUC_TOP module.
- Mi-V reset, PLL lock, and soft reset signals generate the reset for all the components in the JESD_TOP module.

2.3.4 Resource Utilization

The following table lists the resource utilization of the design on the MPF300TS_ES device (FCG1152, speed grade -1).

Table 3 • Resource Utilization

Type	Used	Total	Percentage (%)
4LUT	79298	299544	26.47
DFF	73655	299544	24.59
μSRAM	1315	2772	47.44
LSRAM	116	952	12.18
Math	326	924	35.28
PLL	3	8	37.5
Transceiver Lanes	5	16	31.25

2.3.5 Timing Closure in Libero

In Libero SoC PolarFire, the timing constraints are derived for the top module of the design from **Design Flow > Constraint Manager**. The generated SDC file includes clock definitions based on the PLLs used in the design and constraints specific to IP cores.

Timing issues can be analyzed and cross-probed using SmartTime and ChipPlanner. These applications are integrated in Libero SoC PolarFire.

To close the timing of the wireless radio DFE design at 245 MHz, the following options and guidelines were followed.

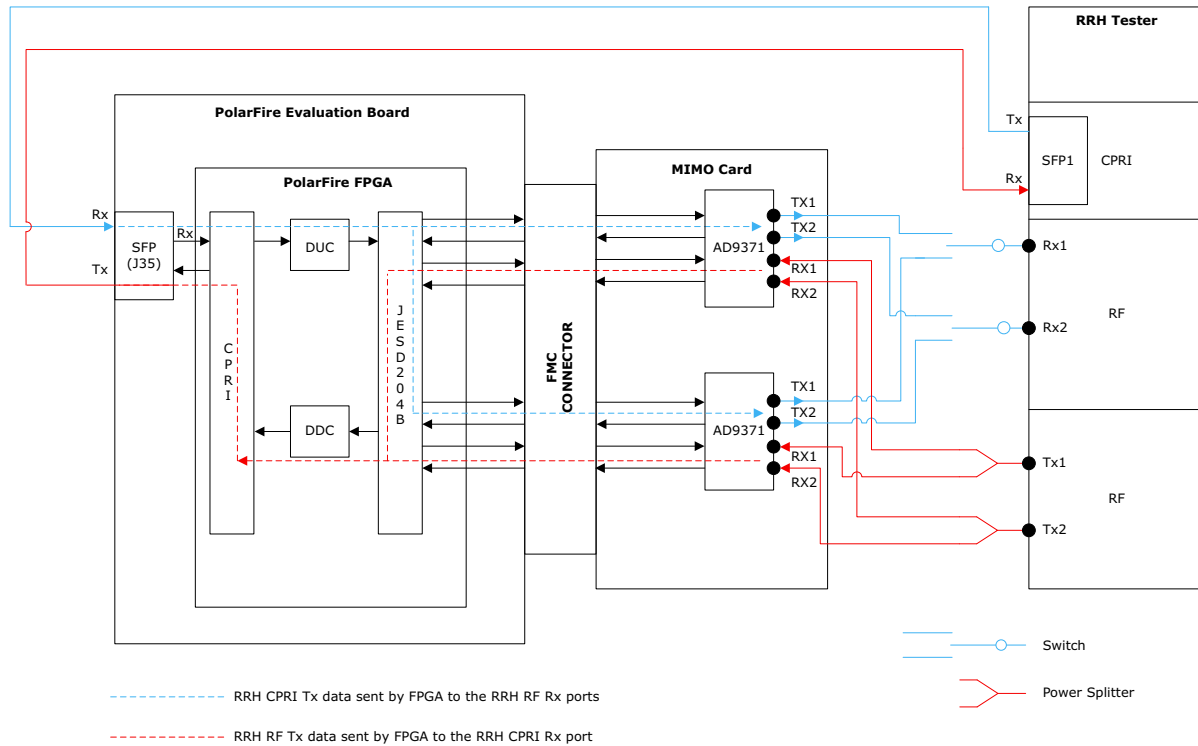
- Input and output data registers of hard blocks such as MACC and RAM were enabled in the RTL. Also, used dedicated CDIN and CDOOUT lines for the MACC blocks.
- The `syn_preserve` directive was used in the RTL of repetitive modules inside DUC and DDC subsystems. This directive avoids the usage of shared nets across modules and duplicates nets for each module to give better timing.
- Asynchronous resets were used in the design.
- The required synchronizer circuitry was used for clock domain crossings. And then, all of the asynchronous clock groups were defined (`set_clock_groups`) in an SDC file for faster Place and Route cycles.
- Using SmartTime results, the maximum fanout limit was set on individual nets instead of setting the fanout for the overall design.

Note: The Place and Route configuration options, **High Effort Layout** and **Repair Minimum Delay Violations** must be enabled only when the timing paths have a lower negative slack with respect to the clock timing constraint. The smart time analysis must be done with these options disabled during initial runs.

3 Hardware Data Flow

The following figure shows the high-level data flow between the RRH tester, MIMO card, and the PolarFire evaluation board.

Figure 10 • Data Flow



4 Setting Up the Demo

This section describes steps to successfully program the FPGA, its Non-volatile memory (sNVM), and run scripts to configure Jitter attenuator PLLs.

Setting up the demo involves the following steps:

1. [Setting up the Hardware](#), page 12
2. [Programming the PolarFire Device](#), page 15
3. [Enabling Jitter Cleaner on CPRI TX PLL](#), page 15

4.1 Setting up the Hardware

This section describes how to connect all of the components required to run the demo.

Follow these steps:

1. Connect the Host PC and the RRH tester to the same LAN using RJ45 cables.
2. Connect the USB cable from the Host PC to J5 (FTDI port) on the evaluation board.
On the evaluation board, DS15, DS24, DS23, DS25, and DS26 LEDs glow.
3. Plug in one SFP module into the SFP1 port of the RRH tester and the other SFP module into J35 (SFP case) on the evaluation board. Connect both these SFP modules using the fiber patch.
4. Connect the MIMO card to the evaluation board using the J34 FMC connector.
5. Connect the two RRH RF Tx ports to the 4 RF Rx ports of the MIMO using power splitters as listed in the following table.

Table 4 • RRH RF Tx to MIMO RF Rx Connections

RRH Tx Port	MIMO Card Rx Port
Tx1	J500 (RX1 of U12) and J522 (RX1 of U15)
Tx2	J501 (RX2 of U12), J519 (RX2 of U15)

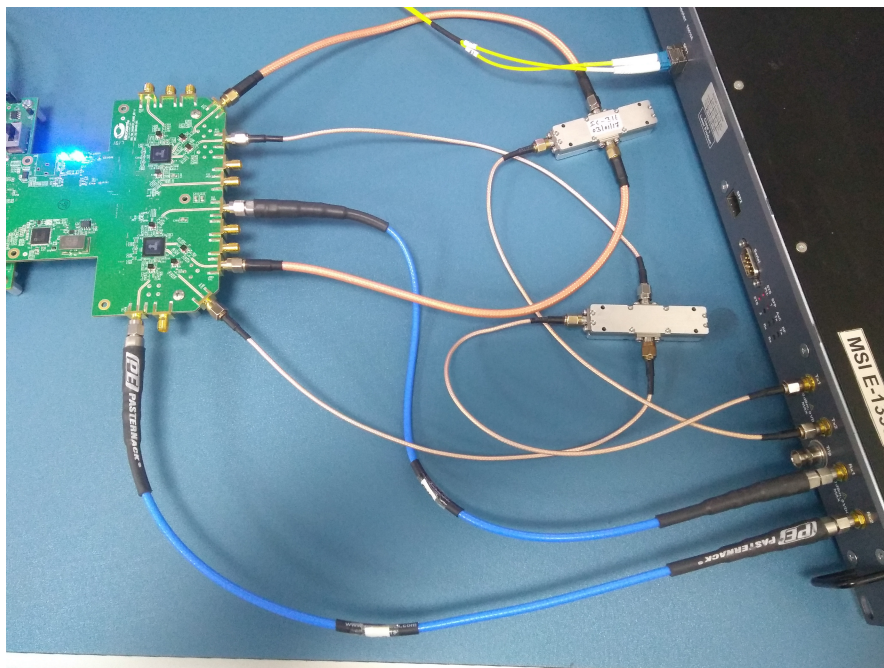
6. Connect the two RF TX ports of the MIMO card to the two Rx ports of the RRH tester as listed in the following table.

Table 5 • MIMO RF Tx to RRH RF Rx Connections

MIMO Card Tx Port	RRH Rx Port
TX1 (J508) of U12	Rx1
TX2 (J509) of U12	Rx2

Note: To see the RF output from the TX1 and TX2 ports U15 of the MIMO card, connect TX1 (J524) and TX2 (J526) to Rx1 and Rx2 ports.

[Figure 11](#), page 13 shows the complete SMA connections.

Figure 11 • SMA Connections

7. Ensure that the following jumper settings are made on the evaluation board.

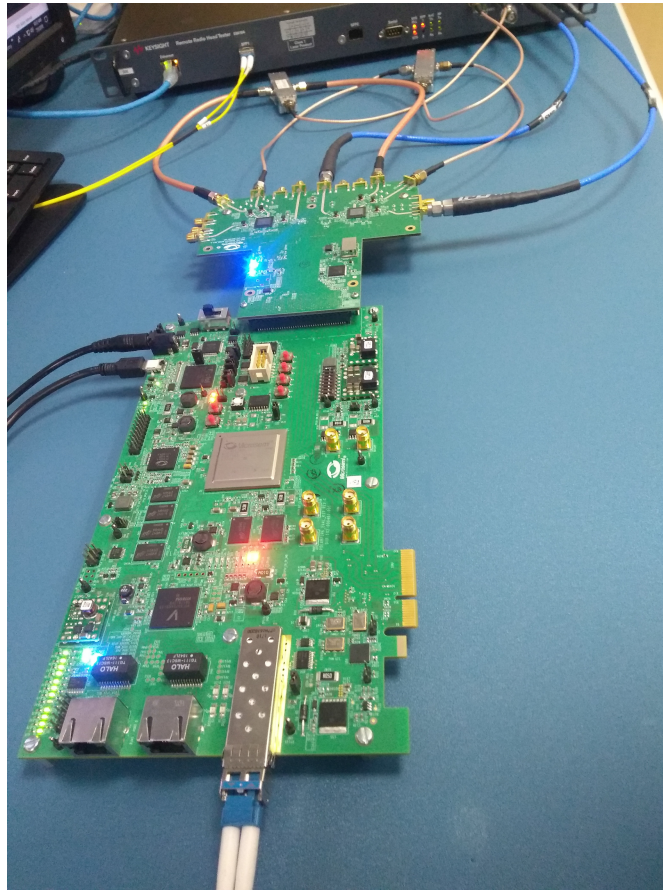
Table 6 • Jumper Settings

Jumper	Setting
J39	Short 1 and 2 for enabling the Tx port of the SFP
J46	Open 1 and 2 for enabling the 122.88 MHz oscillator
J47	Open 1 and 2
J12	short 5 and 6 for 1.8V

8. Connect the power supply cable to the J9 connector on the evaluation board.
9. Connect the RRH tester to the power supply using the power adapter.
10. Power-up the evaluation board using the SW3 slide switch.
On the evaluation board, the power regulator LEDs (DS3 - DS14) glow. And, LEDs DS4 and DS8 on the MIMO card also glow.
11. Power-up the RRH tester using the POWER switch at the back chassis.
After the RRH tester initialization, LEDs SYS PLL, AxC Tx and Rx glow, RF Tx and Rx glow, and STS blinks.

The complete setup is shown in the following figure.

Figure 12 • Hardware Setup



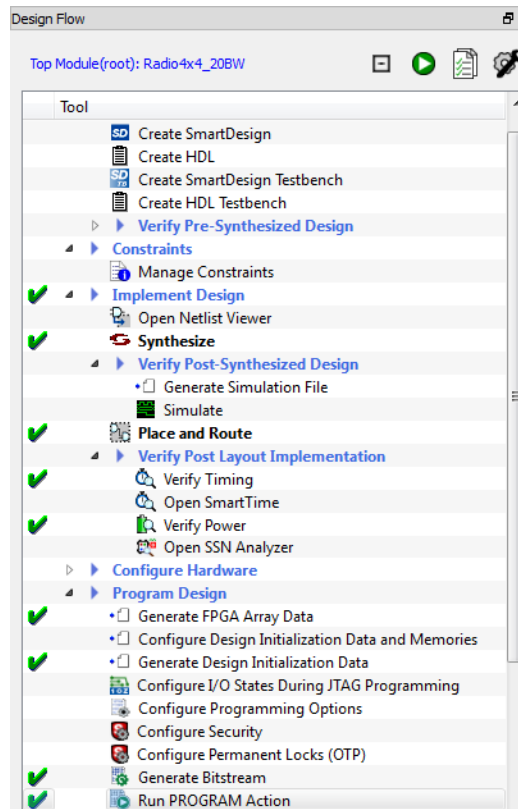
4.2 Programming the PolarFire Device

After setting up the hardware, you must program the device.

To program the device:

1. Start Libero SoC PolarFire v2.2.
2. Open the PRJX file from the following location:
mpf_dg0839_liberosocpolarfirev2p2_df\Libero_Project
3. From the Libero design flow, double-click the **Run PROGRAM Action** option.
The following message appears after the device is successfully programmed.

Figure 13 • Device Programmed



LED 10 glows and LED 11 blinks after the device is successfully programmed.

Note: Keep Libero SoC PolarFire v2.2 open to enable jitter cleaner as described in the following section.

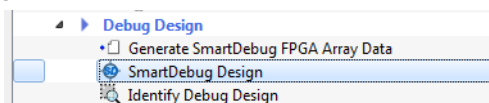
4.3 Enabling Jitter Cleaner on CPRI TX PLL

The design files includes a TCL script file, which enables jitter cleaner on CPRI TX PLL. The script must be executed using SmartDebug.

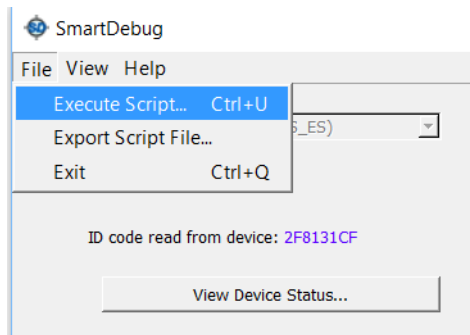
To execute the script:

1. From the Libero design flow, double-click the **SmartDebug Design** option.

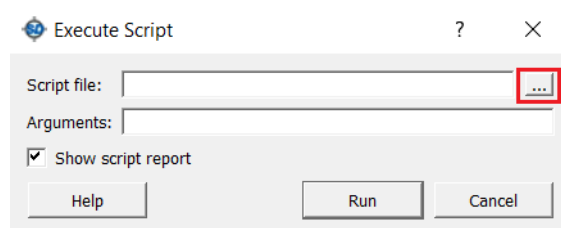
Figure 14 • Starting SmartDebug



2. Select **File > Execute Script** as shown in Figure 15, page 16.

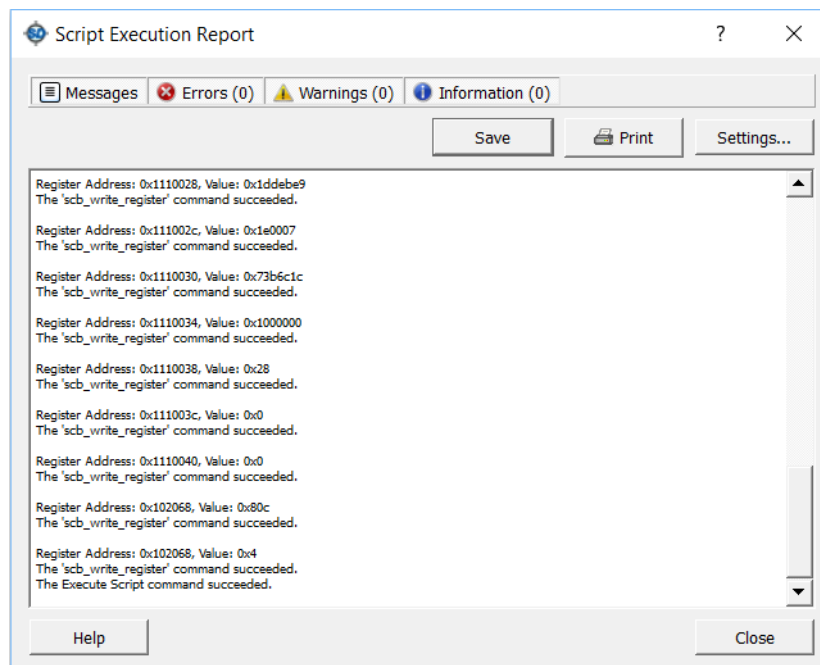
Figure 15 • Execute Script

3. Click the **Import** button to import the TCL file as shown in the following figure.

Figure 16 • The Import button

4. Double-click the `CPRI_JA_Enable.tcl` file from the following location, and click **Run**.
`mpf_dg0839_liberosocpolarfirev2p2\Libero_Project`

After the successful execution of the script, the log window shows the following report.

Figure 17 • Execution Report

5. Close SmartDebug.

Note: Run the script every time the evaluation board is power cycled.

5 Running the Demo

This section describes steps to successfully run the demo and observe the 64 QAM constellation of a 2x2 20 MHz MIMO system.

Running the demo involves the following steps:

1. [Configuring and Monitoring the RRH Tester](#), page 17
2. [Executing the User Application](#), page 23
3. [Monitoring the Performance](#), page 25

5.1 Configuring and Monitoring the RRH Tester

The E6610A user interface is used to configure the carrier technology and bandwidth, CPRI parameters like line rate, bit width, and IQ mapping, and to configure the RF parameters like frequency, waveform, and power levels (for Tx and Rx). The user interface is also used to monitor the RRH tester. Monitoring the tester involves observing the analog and digital data at RF Rx and CPRI Rx respectively.

This section is divided into the following steps:

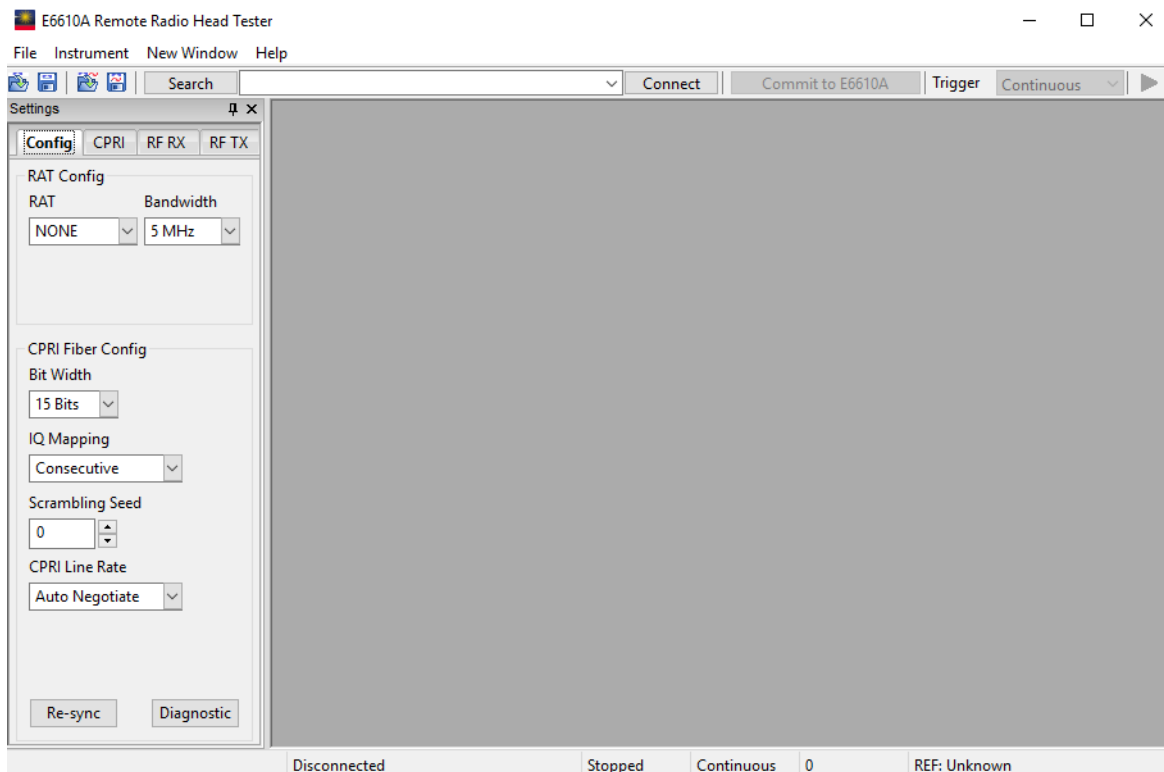
1. [Configuring the Tester](#), page 17
2. [Monitoring the Tester](#), page 20
3. [Enabling Multicast on CPRI](#), page 21

5.1.1 Configuring the Tester

To configure the RRH tester:

1. From the host PC desktop, start the E6610A user interface.
The main window of the user interface is displayed as shown in the following figure.

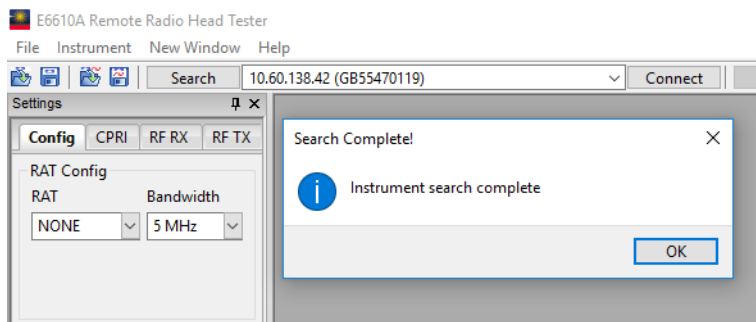
Figure 18 • User Interface



2. Click **Search** to detect the RRH tester connected to the LAN.

The IP address of the RRH tester and the following message is displayed as shown in the following figure.

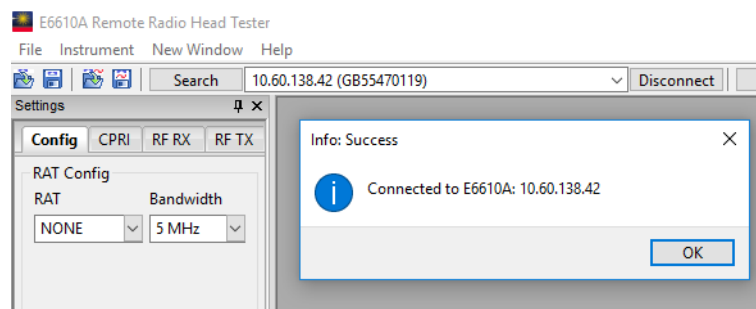
Figure 19 • Instrument Detected



Note: The IP address of the RRH tester varies from one LAN to the other.

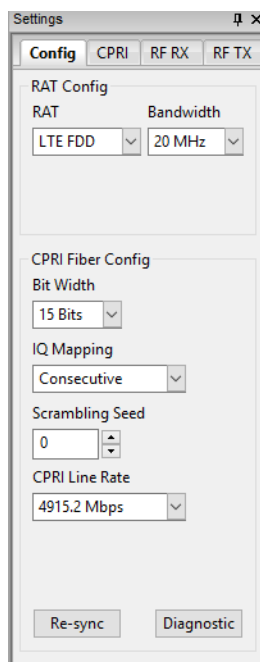
- Click **Connect** to connect to the RRH tester.
The following message is displayed after a successful connection.

Figure 20 • Connection Established

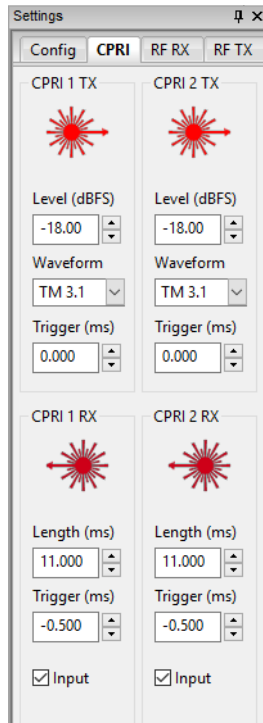


- Configure the carrier technology, bandwidth, and CPRI parameters as shown in the following figure.

Figure 21 • Config Window



- Configure the CPRI Tx and Rx parameters as shown in the following figure.

Figure 22 • CPRI Tx and Rx Config Screen


Settings

Config CPRI RF RX RF TX

CPRI 1 TX CPRI 2 TX

Level (dBFS) -18.00 -18.00

Waveform TM 3.1 TM 3.1

Trigger (ms) 0.000 0.000

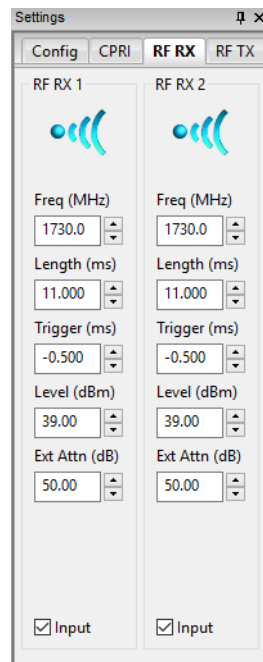
CPRI 1 RX CPRI 2 RX

Length (ms) 11.000 11.000

Trigger (ms) -0.500 -0.500

☒ Input ☒ Input

6. Configure the RF Rx parameters as shown in the following figure.

Figure 23 • RF Rx Config Screen


Settings

Config CPRI RF RX RF TX

RF RX 1 RF RX 2

Freq (MHz) 1730.0 1730.0

Length (ms) 11.000 11.000

Trigger (ms) -0.500 -0.500

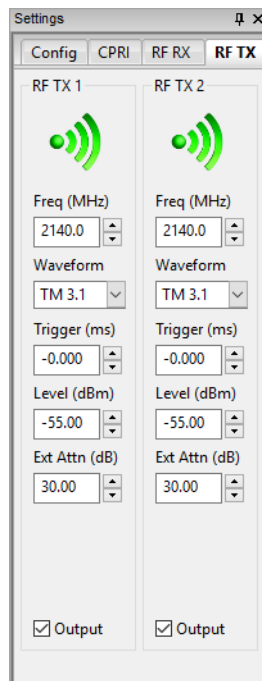
Level (dBm) 39.00 39.00

Ext Attn (dB) 50.00 50.00

☒ Input ☒ Input

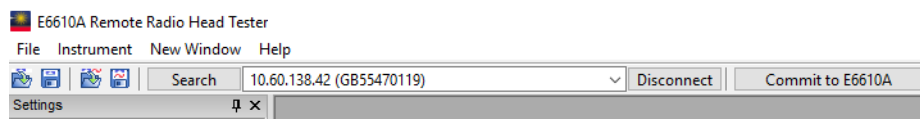
- Configure the RF Tx parameters as shown in the following figure.

Figure 24 • RF Tx Config Screen



- Click **Commit to E6610A** to commit the configuration.

Figure 25 • Commit Configuration



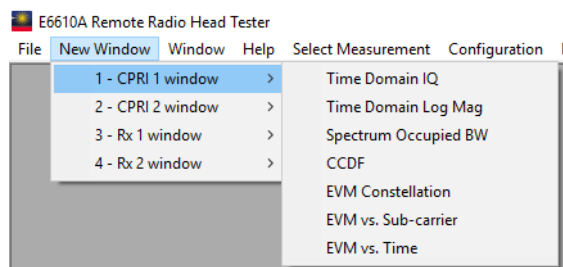
5.1.2 Monitoring the Tester

The time domain, frequency domain, and the EVM constellation plots of the data received at the CPRI Rx and RF Rx ports must be observed. These windows must be opened to view the various plots.

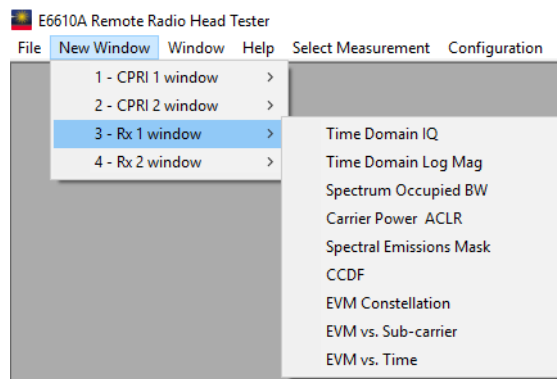
Follow these steps:

- Select **New Window > CPRI 1 > Time Domain IQ** as shown in the following figure.

Figure 26 • CPRI 1 Rx Plot Window



- Similarly, open the CPRI 1 Rx frequency domain, and EVM constellation plot windows.
- Similarly, open the CPRI 2 Rx time and frequency domain, and EVM constellation plot windows.
- Select **New Window > RF Rx1 > Time Domain IQ** as shown in the following figure.

Figure 27 • RF Rx Plot Window

5. Similarly, open the RF Rx1 frequency domain, and EVM constellation plot windows.
6. Similarly, open the RF Rx2 time and frequency domain, and EVM constellation plot windows.
7. Select **New Window > CPRI Diagnostics** to monitor the CPRI link.

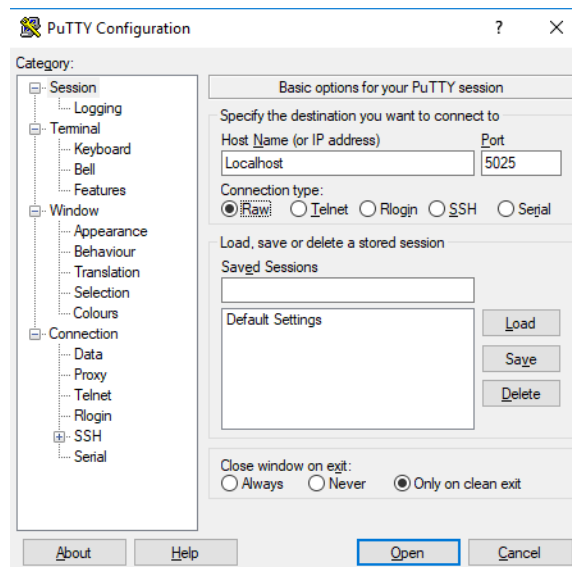
5.1.3 Enabling Multicast on CPRI

The RRH tester supports Multicast in the down link. The multicast feature creates copies of the CPRI 1 and CPRI 2 IQ data streams and places them in the additional antenna containers that the RRH can use to map to other antenna ports. Multicast is used in the demo to get the CPRI 1 and 2 IQ data on the other 2 antennas.

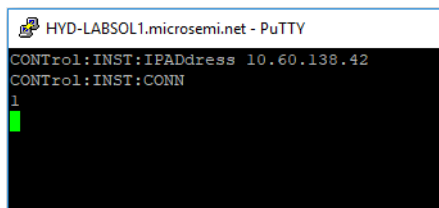
From the host PC, PuTTY must be used to connect to the tester. After connecting, multicast must be enabled on CPRI.

To enable multicast:

1. From the host PC desktop, start PuTTY.
2. Enter the hostname, port number, and select the **Connection Type** as shown in the following figure.

Figure 28 • PuTTY Connection Config

3. Type the commands shown in the following figure and click **Enter** to connect to the Tester. After connecting, the return code 1 is displayed as shown in the following figure.

Figure 29 • Connection Established


```
HYD-LABSOL1.microsemi.net - PuTTY
CONTROL:INST:IPADdress 10.60.138.42
CONTROL:INST:CONN
1
```

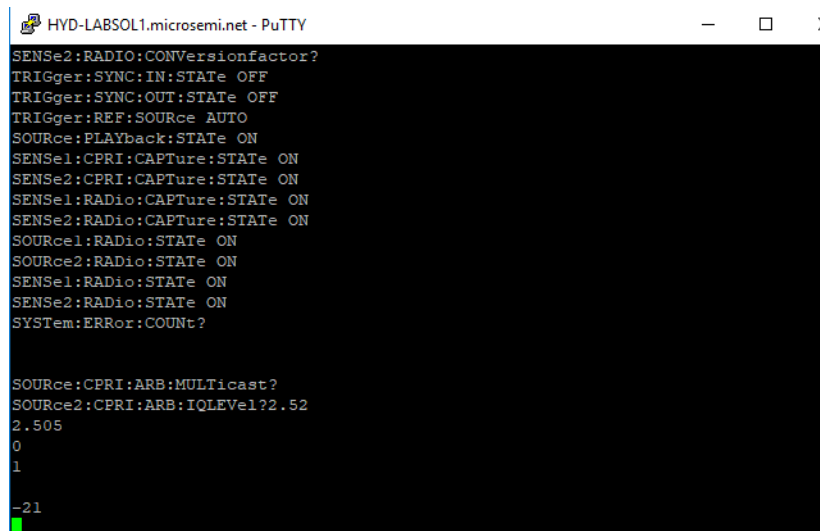
4. Copy multicast commands shown in the following figure and paste it on PuTTY.

Figure 30 • Multicast Commands

```
*CLS
SOURCE:PLAYback:STATE OFF
CONFigure:RAT:TYPE LTE
CONFigure:RAT:MODE FDD
CONFigure:RAT:Bw 20,consecutive
CONFigure:CPRI:BITwidth 15
SOURCE:CPRI:MODE consecutive
SOURCE:CPRI:ARB:MULTicast ON
SOURCE1:RADio:ARB:TModel TM31
SOURCE1:RADio:MODE modulated
SOURCE1:RADio:ARB:STATE ON
CONFigure:SEMask CATBOPT2
SOURCE1:RADio:ARB:TRIGger -0.000000
SOURCE1:RADio:CORRection 30.000000
SOURCE1:RADio:FREquency 2140000
SOURCE1:RADio:Power -55.000000
CONFigure:TXSpurious1:RBW 1
SENSe1:RADio:FREquency 1730000
SENSe1:RADio:CORRection 50.000000
SENSe1:RADio:Leve1 39.000000
SENSe1:RADio:CAPTure:DEPTH 11.000000
SENSe1:RADio:CAPTure:TRIGger -0.500000
SENSe1:RADio:CAPTure:TModel TM31
SOURCE1:CPRI:ARB:IQLeve1 -21.000000
SOURCE1:CPRI:ARB:TRIGger 0.000000
SOURCE1:CPRI:ARB:TModel TM31
SOURCE1:CPRI:ARB:STATE ON
SENSe1:CPRI:CAPTure:DEPTH 11.000000
SENSe1:CPRI:CAPTure:TRIGger -0.500000
SENSe1:RADio:CONVersionfactor?
SOURCE2:RADio:ARB:TModel TM31
SOURCE2:RADio:MODE modulated
SOURCE2:RADio:ARB:STATE ON
CONFigure:SEMask CATBOPT2
SOURCE2:RADio:ARB:TRIGger -0.000000
SOURCE2:RADio:CORRection 30.000000
SOURCE2:RADio:FREquency 2140000
SOURCE2:RADio:Power -55.000000
CONFigure:TXSpurious2:RBW 1
SENSe2:RADio:FREquency 1730000
SENSe2:RADio:CORRection 50.000000
SENSe2:RADio:Leve1 39.000000
SENSe2:RADio:CAPTure:DEPTH 11.000000
SENSe2:RADio:CAPTure:TRIGger -0.500000
SENSe2:RADio:CAPTure:TModel TM31
SOURCE2:CPRI:ARB:IQLeve1 -21.000000
SOURCE2:CPRI:ARB:TRIGger 0.000000
SOURCE2:CPRI:ARB:TModel TM31
SOURCE2:CPRI:ARB:STATE ON
SENSe2:CPRI:CAPTure:DEPTH 11.000000
SENSe2:CPRI:CAPTure:TRIGger -0.500000
SENSe2:RADio:CONVersionfactor?
TRIGger:SYNC:IN:STATE OFF
TRIGger:SYNC:OUT:STATE OFF
TRIGger:REF:SOURce AUTO
SOURCE:PLAYback:STATE ON
SENSe1:CPRI:CAPTure:STATE ON
SENSe2:CPRI:CAPTure:STATE ON
SENSe1:RADio:CAPTure:STATE ON
SENSe2:RADio:CAPTure:STATE ON
SOURCE1:RADio:STATE ON
SOURCE2:RADio:STATE ON
SENSe1:RADio:STATE ON
SENSe2:RADio:STATE ON
SYSTEM:ERRor:COUNT?

SOURCE:CPRI:ARB:MULTicast?
SOURCE2:CPRI:ARB:IQLeve1?
```

The following figure shows the status and return codes displayed after multicast is successfully enabled.

Figure 31 • Multicast Enabled


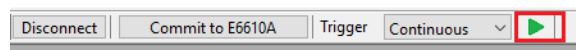
```

SENSe2:RADIO:CONVersionfactor?
TRIGger:SYNC:IN:STATe OFF
TRIGger:SYNC:OUT:STATe OFF
TRIGger:REF:SOURce AUTO
SOURce:PLAYback:STATe ON
SENSe1:CPRI:CAPTure:STATe ON
SENSe2:CPRI:CAPTure:STATe ON
SENSe1:RADIO:CAPTure:STATe ON
SENSe2:RADIO:CAPTure:STATe ON
SOURce1:RADIO:STATe ON
SOURce2:RADIO:STATe ON
SENSe1:RADIO:STATe ON
SENSe2:RADIO:STATe ON
SYSTem:ERRor:COUNt?

SOURCE:CPRI:ARB:MULTICAST?
SOURCE2:CPRI:ARB:IQLEVel72.52
2.505
0
1
-21

```

5. Click **Run** to start the CPRI and RF traffic from the tester.

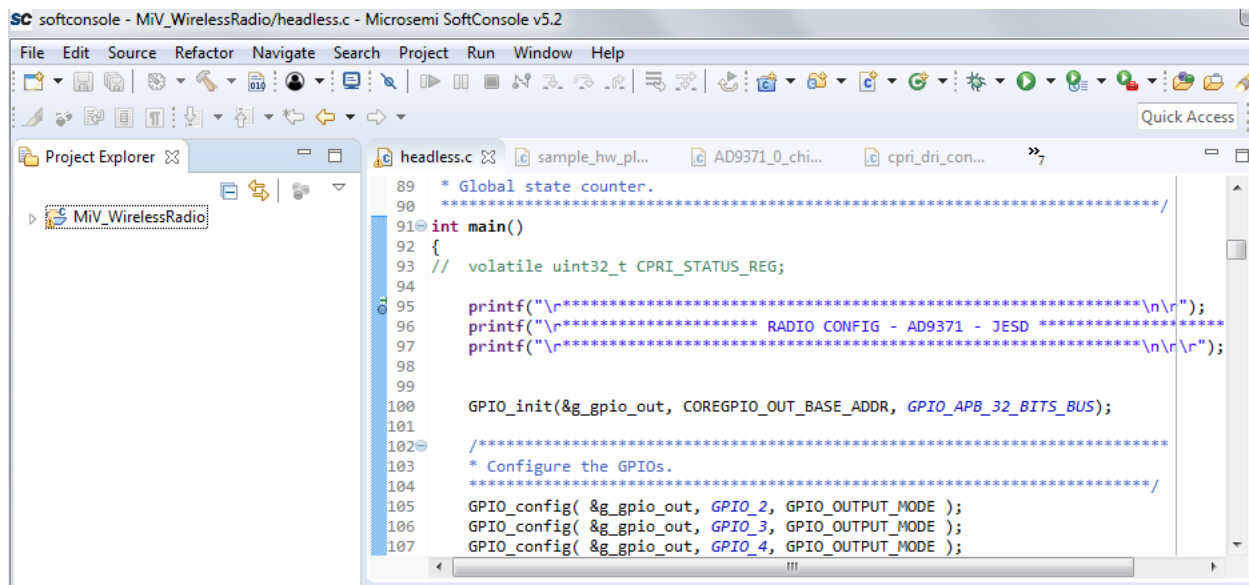
Figure 32 • Start Tester traffic

5.2 Executing the User Application

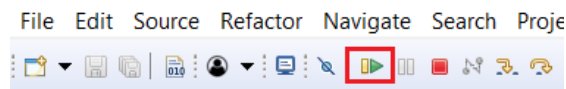
Using SoftConsole, the user application must be launched in the debug mode. CPRI registers and devices on the MIMO card are initialized after the debugger executes the main function. The main function also monitors the CPRI link.

To execute the user application:

1. From the host PC desktop, start SoftConsole v5.2.
2. In the workspace launch window, enter the following location and click **Launch**.
mpf_dg0839_liberosocpolarfirev2p2\Libero_Project\SoftConsole
3. The user application is launched in the debug mode.
4. Click the debug option as shown in the following figure.

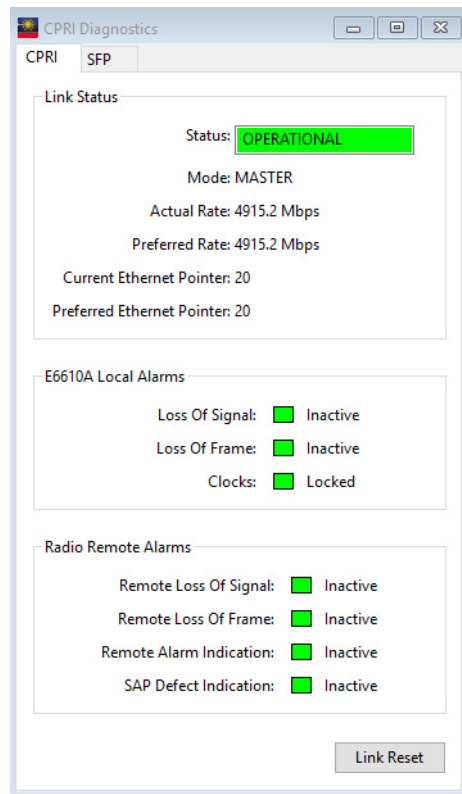
Figure 33 • Launch Debugger

5. In the debug window, click the Resume option to execute the main function.

Figure 34 • Resume Application Execution

The application is executed and LED 4, 5, 6, 7, 8, and 9 on the evaluation board glow. On the MIMO card LEDs, DS6 and DS7 glow. This indicates that the wireless radio DFE design is up and running.

The CPRI diagnostics window shows the link up status as shown in the following figure.

Figure 35 • CPRI Diagnostics

5.3 Monitoring the Performance

After the wireless design is up and running, the RF and baseband plot windows display the data as shown in [Figure 36](#), page 26 and [Figure 37](#), page 26.

The plots show the 20 MHz occupied bandwidth data correctly decoded for the 64 QAM constellation on LTE TM3.1.

Figure 36 • CPRI 1 and 2 Windows

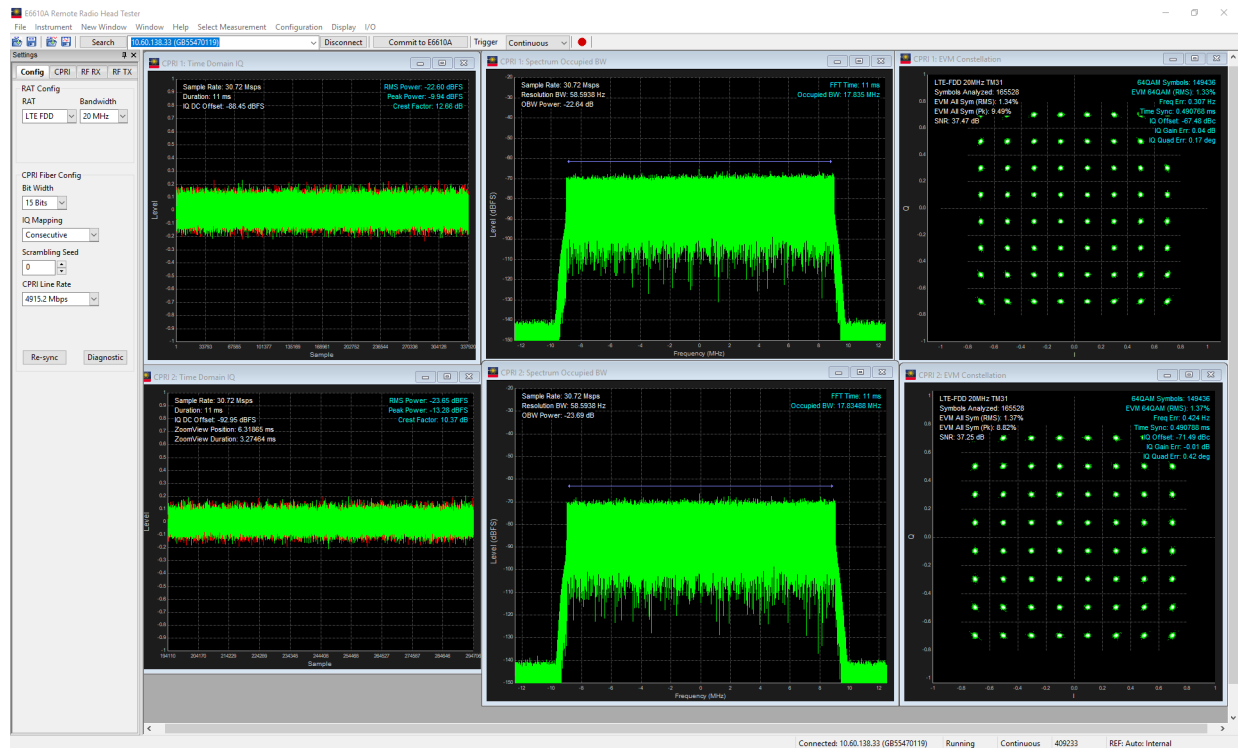
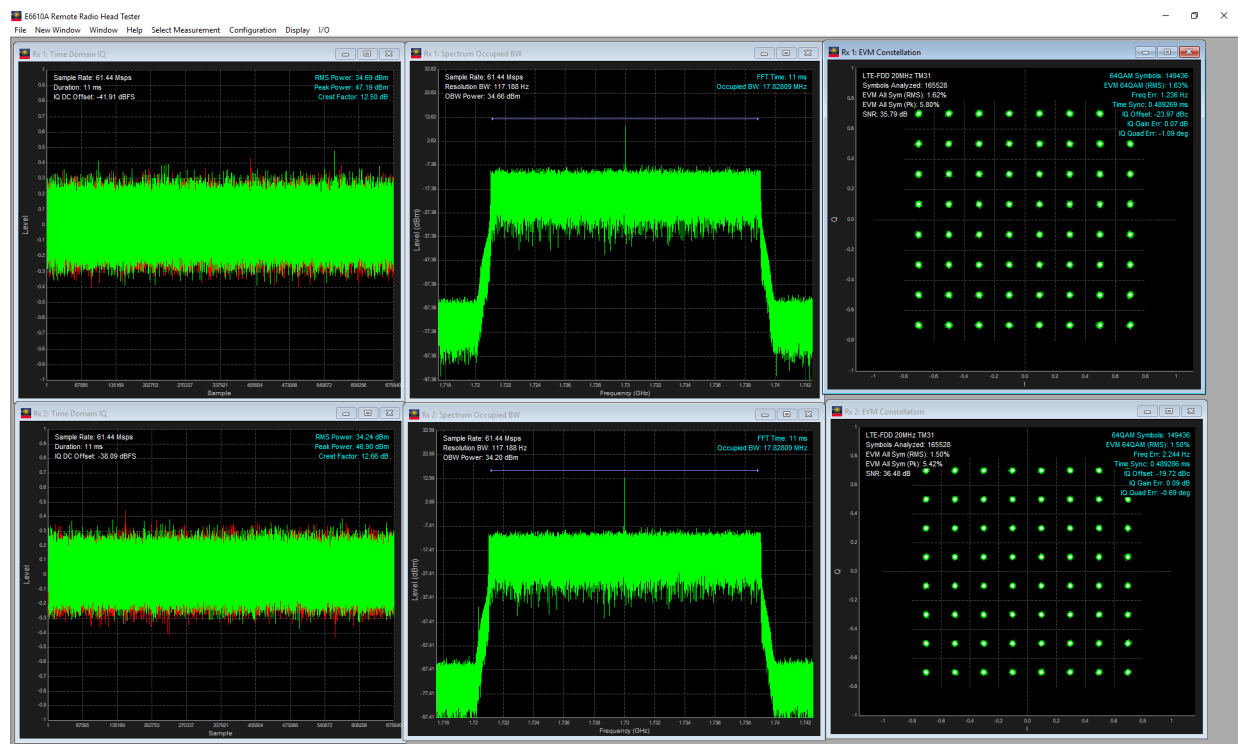


Figure 37 • RF Rx1 and Rx2 Windows



6 Power Measurements

This section describes how to monitor the real-time power consumption of the wireless radio DFE design using PowerMonitor.

PolarFire Evaluation Board comes with a power monitoring solution implemented using the on-board SmartFusion A2F 200 device and the PowerMonitor application. The PowerMonitor application connects to the power monitoring program running on the A2F 200 device to measure power.

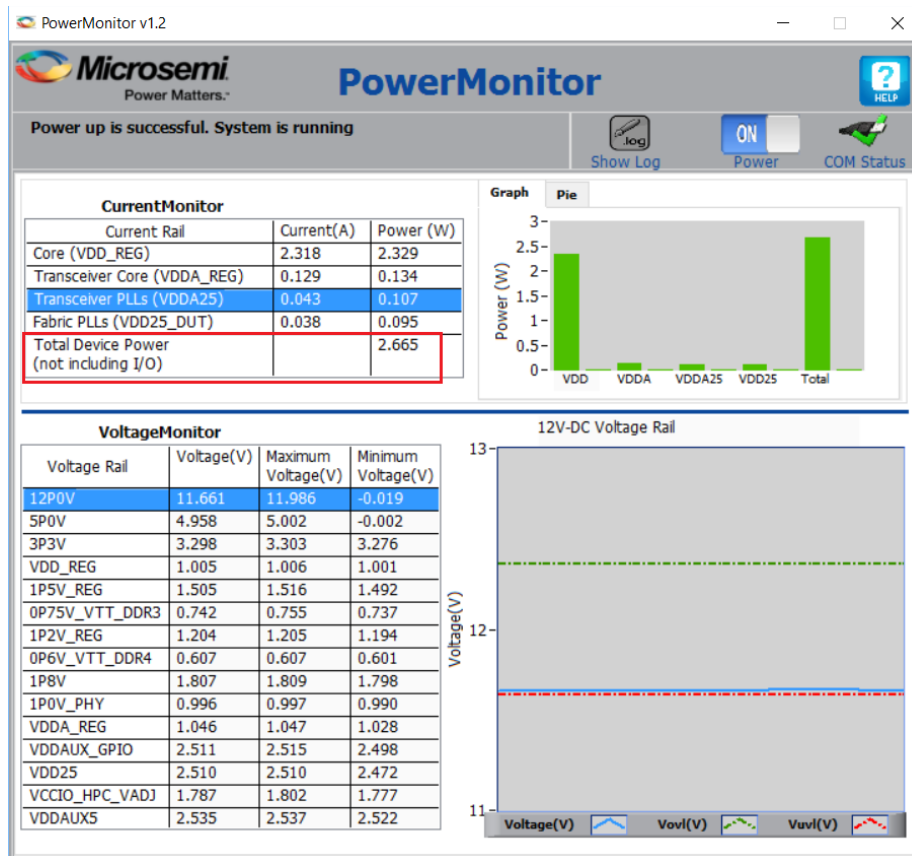
For more information about PowerMonitor, see [UG0747: PolarFire FPGA Evaluation Kit User Guide](#).

Follow these steps:

1. On the host PC desktop, click Start and select PowerMonitor.
2. In the **COMPort SetUp** dialog box, select the highest COM port from the drop-down and click **Connect**.

The PowerMonitor application successfully connects to the board and starts displaying the Core Fabric (VDD) power, Fabric PLL (VDD25) power, Transceiver Core (VDDA) power, and Transceiver PLL (VDDA25) power as shown in the following figure.

Figure 38 • Power Consumption of the DFE Wireless Radio



As shown in Figure 38, page 27, the power consumed by a 2x2 20 MHz MIMO application running on a PolarFire device is only 2.66 W.

6.1 Conclusion

This demo shows that PolarFire FPGA designs can be successfully used in wireless communication applications such as small cell and RRH. The demo also demonstrates the low power advantages of using PolarFire FPGAs in such applications.