UG0830
User Guide
PolarFire FPGA Low Voltage Differential Signaling 7:1

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 2.0

The following is a summary of the changes made in revision 2.0 of this document.

- Updated Low Voltage Differential Signaling 7:1, page 2, LVDS 7:1 Transmit Module, page 3, and LVDS 7:1 Receive Module, page 4
- Added LVDS 7:1 Top SmartDesign, page 3
- Updated Table 1, page 6
- Replaced Figure 8, page 6

1.2 Revision 1.0

The first publication of this document.

2 Low Voltage Differential Signaling 7:1

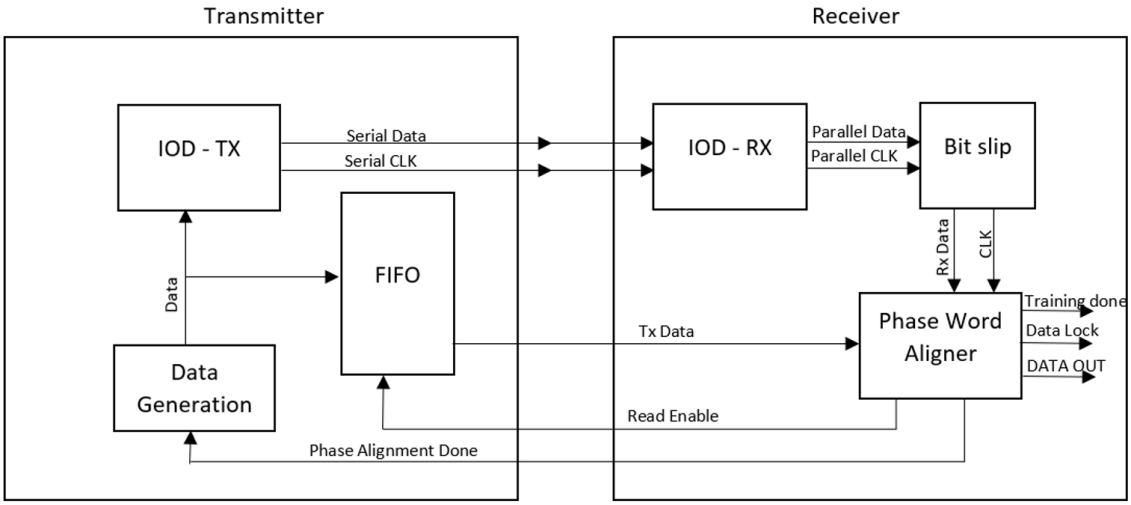
Low-voltage differential signaling (LVDS) is a high-speed, low-power, general-purpose interface standard. Also known as the ANSI/TIA/EIA-644 standard, LVDS was approved in March 1996. LVDS data is dual data rate transmission, that is, both the edges of the serial CLK. It is a source synchronous transmission, which means all the data lanes are synchronized to a common clock sent by the source. LVDS uses differential signaling with a nominal signal swing of 350 mV differential. The low signal swing decreases rise and fall times to achieve the maximum transmission rates specified in the LVDS standard. LVDS signal swing does not depend on the voltage of any specific supply. LVDS uses current mode drivers, which limit power consumption. The differential signals are immune to ±1 V common voltage noise. The Channel-Link technology was originally developed as a solution for flat panel displays, using LVDS for the physical layer (PHY). The technology was then extended into a method for general purpose data transmission. Channel-Link consists of a driver pair and a receiver pair. The application note describes the loopback test in simulation mode for PolarFire FPGA to validate the LVDS 7:1 functionality.

The LVDS 7:1 solution uses PF_IOD_GENERIC_TX and PF_IOD_GENERIC_RX macros from Libero catalog to handle parallel to serial and serial to parallel conversion respectively. IOD configured for transmit, serializes the parallel data and transfers low-speed parallel data from the fabric to high-speed output clock domain. IOD configured for receive, receives high-speed clock domain serial data and de-serializes the data.

The Transmit data_gen module generates sync codes for phase and lane alignment followed by counter data. The phase sync code is used by receive logic to achieve phase alignment, and the word sync code is used by receive logic to achieve word alignment (lane alignment). Each cycle of the transmit clock output includes seven bits of serialized data.

The following figure depicts a high-level functional block diagram.

Figure 1 • **LVDS 7:1 Block Diagram**



The LVDS 7:1 transmit and receive blocks perform the following functions:

1. The transmit data_gen is interfaced to PF_IOD_GENERIC_TX, which serializes the data. Transmit IOD transmits serial bits at HS_CLK (serial clock), which is 3.5 times the parallel clock.
2. PF_IOD_GENERIC_RX receives differential RX_CLK, serialized data, and de-serializes the received data. Bit slip module receives the data from PF_IOD_GENERIC_RX for the phase alignment.
3. After the phase alignment, the Phase Word alignment module auto checks and provides the lock signal. The counter data lock and training done signals are promoted to top-level for monitoring.

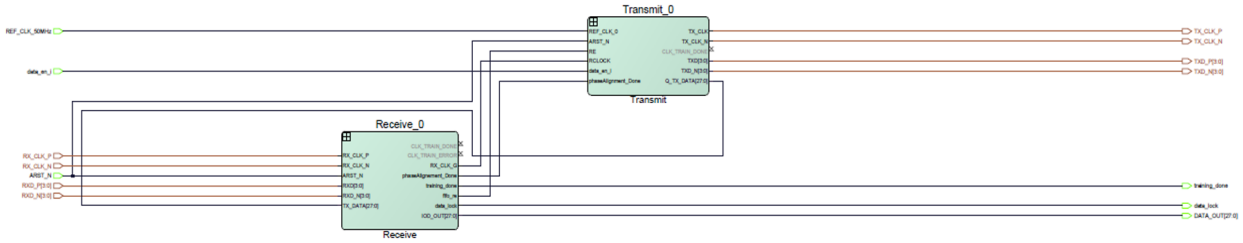
3 SmartDesign and Configurations

This section describes the LVDS 7:1 top, transmit and receive smart designs and their configurations.

3.1 LVDS 7:1 Top SmartDesign

The following figure depicts the LVDS 7:1 Top SmartDesign.

Figure 2 • **LVDS 7:1 Top SmartDesign**



LVDS 7:1 top is a four lanes simulation model. The LVDS 7:1 top has transmitter and receiver modules. Transmit outputs TX_CLK and TXD connected to receiver RX_CLK and RXD in the testbench. Reference CLK 50 MHz frequency is used in this design. The receive module asserts training done signal after phase and word alignment. The transmitter then transmits data that the receiver compares to validate the received data.

3.2 LVDS 7:1 Transmit Module

The LVDS 7:1 transmit module generates the phase and word patterns followed by counter data. The clock generator logic generates serial and parallel clocks. Transmit module output consists of one clock pair and four data pairs. Transmit IOD transmits serial bits at HS_IO_CLK (serial clock), which is 3.5 times the parallel clock. The IO features are set by Libero configurator with in Libero SoC PolarFire. PF_IOD_GENERIC_TX is configured for two outputs, one for data and one for the clock.

Figure 3 • **LVDS 7:1 Transmitter SmartDesign**

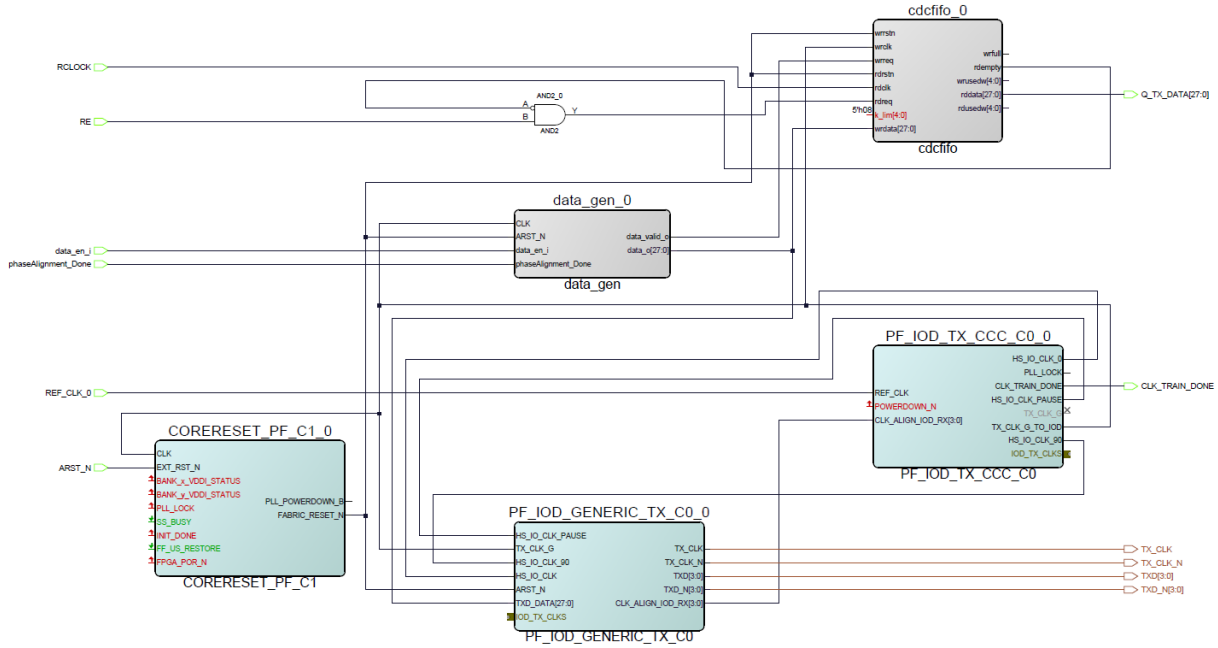


Figure 4 • **PF_IOD_GENERIC_TX Configurator**

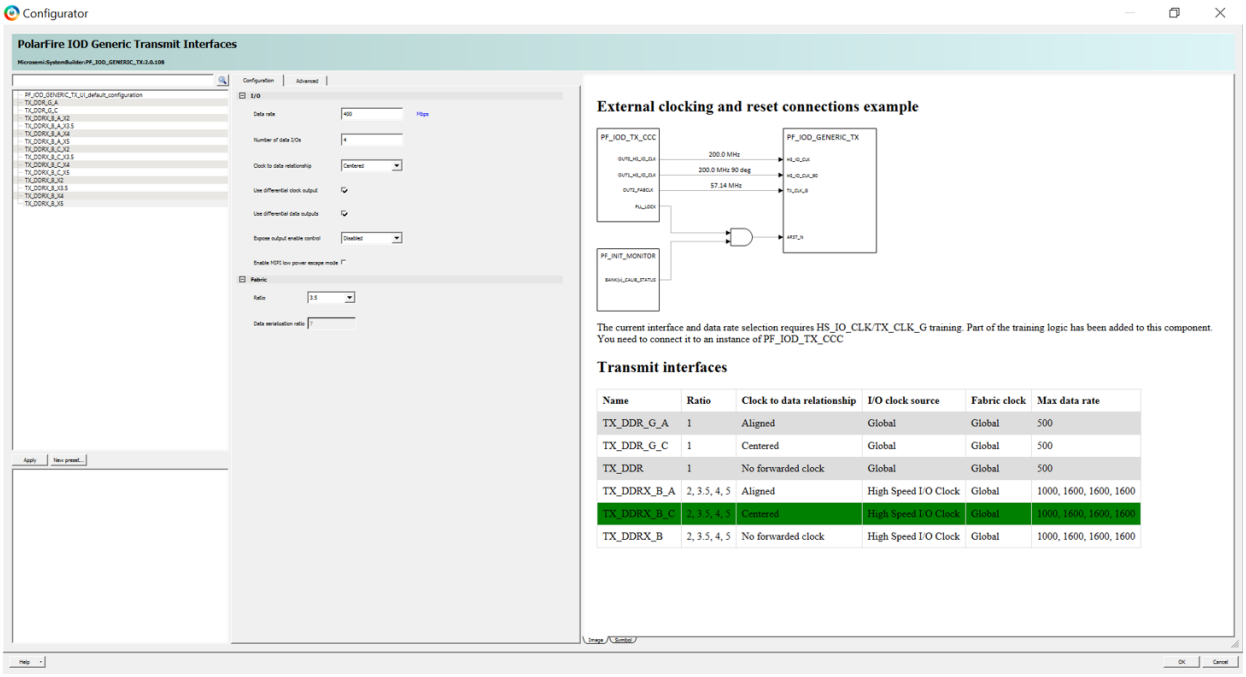
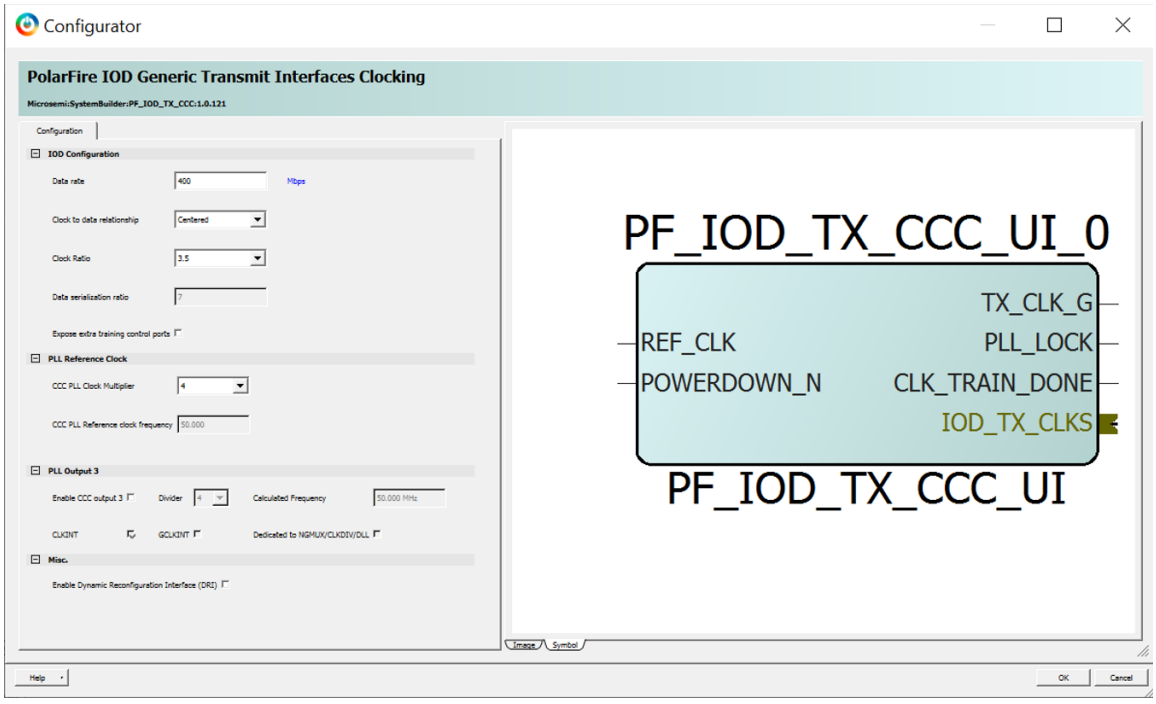


Figure 5 • **PF_IOD_TX_CCC Configurator**



3.3 LVDS 7:1 Receive Module

The LVDS 7:1 receive module receives serial data and a source synchronous parallel clock. The serial data is input to receive PF_IOD_GENERIC_RX. The serial data is received on an IOA pair and sent to the associated IOD block. For more information, see *UG0686: PolarFire FPGA User I/O User Guide*.

The bit slip module in receive block accepts the parallel data from receive IOD and uses it to generate bit slip pulses to achieve phase alignment with respect to the transmit phase pattern. After achieving phase

alignment, the data_gen module transmits word sync code. After achieving phase and word alignment, read enable signal is asserted high which is connected to transmit CDC FIFO read enable. The phase word aligner starts auto-checking after the word alignment signal is asserted. Training done signal is asserted high after phase and word alignment. The training is done and data lock signals are promoted to the top for observing the signal on functional simulation.

Figure 6 • **LVDS 7:1 Receiver SmartDesign**

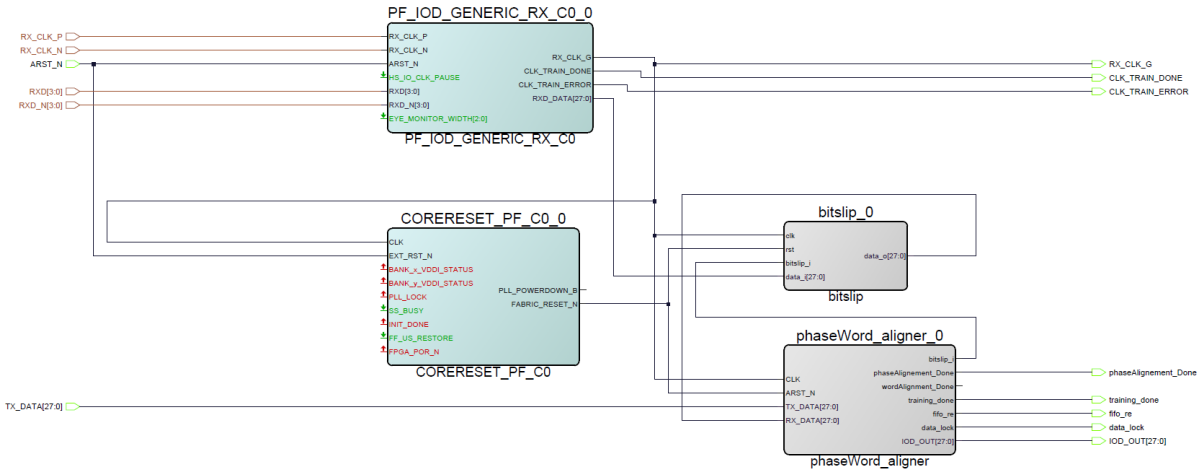
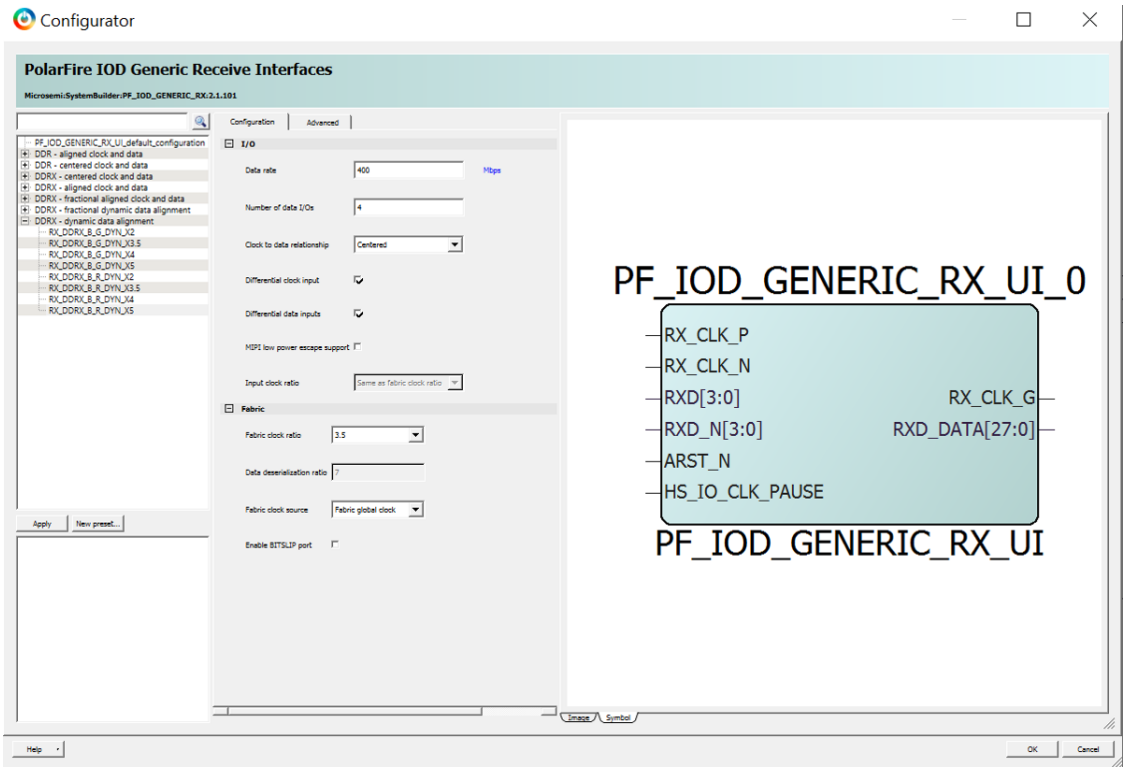


Figure 7 • **PF_IOD_GENERIC_RX Configuration**



3.4 Inputs and Outputs

The following table lists the LVDS 7:1 top interface input and output ports.

Table 1 • **LVDS 7:1 Top Interface Ports**

Signal Name	Direction	Width (bits)	Description
REF_CLK_50MHz	Input	1	Reference Clock 50 MHz
data_en_i	Input	1	Data enable signal for transmitter data generation
RX_CLK_P	Input	1	Differential IOD receiver serial CLOCK - P
RX_CLK_N	Input	1	Differential IOD receiver serial CLOCK - N
RXD_P	Input	4	Differential IOD receiver 4 lanes serial DATA - P
RXD_N	Input	4	Differential IOD receiver 4 lanes serial DATA - N
TX_CLK_P	Output	1	Differential IOD transmitter serial CLOCK - P
TX_CLK_N	Output	1	Differential IOD transmitter serial CLOCK - N
TXD_P	Output	4	Differential IOD transmitter 4 lanes serial DATA - P
TXD_N	Output	4	Differential IOD transmitter 4 lanes serial DATA - N
training_done			Phase and Word Align Signal. Asserted when IOD RXD_DATA [6:0] is phase and word aligned with transmit phase and word patterns
data_lock	Output	1	Asserted when receiver data matches with transmitter data

3.5 Functional Simulation Timing Diagram

The following figure shows the functional simulation timing diagram for the LVDS 7:1 top.

Figure 8 • **LVDS 7:1 Top Functional Simulation Timing Diagram**