Total Ionizing Dose Test Report

August 6th, 2015

Nadia Rezzak, J.J. Wang, Alex Cai, Kevin Chou, Mike Traas, Amal Zerrouki

Table of Contents

I. SUMMARY TABLE

The TID tolerance for each tested parameter is summarized below in Table 1.

Table. 1. Tolerances for Each Tested Parameter

Parameter	**Tolerance**
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current (I_{DD}/I_{DDI}/I_{PP_PLL})	Passed 125 krad(SiO_2)
3. Input Threshold (V_{TIL}/V_{IH})	Passed 125 krad(SiO_2)
4. Output Drive (V_{OL}/V_{OH})	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded.

Table. 2. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	UMC
Technology	65 nm
DUT Design	Inverter string
Die Lot Number	KLYQH
Quantity Tested	3
Serial Number	1203 (S43), 1204 (S44), 1205 (S45)
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	5 krad(SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (V_{DD}/$V_{DDI\_2.5}$/$V_{DDI\_3.3}$/V_{PP_PLL})	Static at 1.2 V/2.5 V/3.3 V/3.3 V
IO Configuration	Single ended Differential pair

B. Test Method

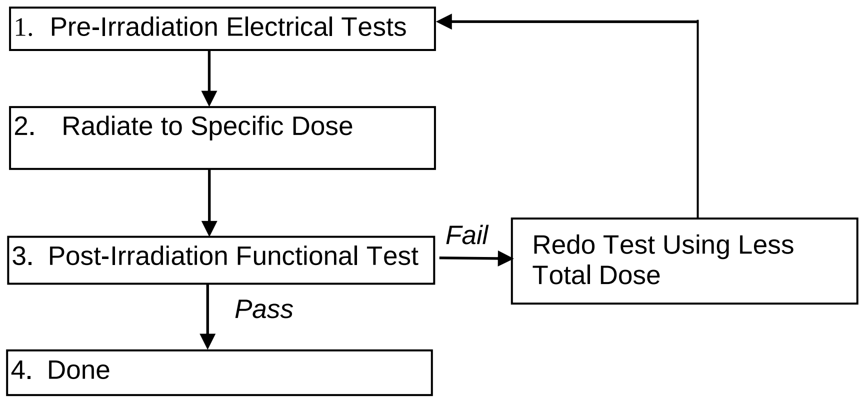

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre- and post-irradiation.

The functionality is measured on the output pin (Out) of an inverter string with 6000 inverters.

The core power supply current I_{DD}, the I/Os power supply currents ($I_{DDI\_2.5}$/$I_{DDI\_3.3}$) and the charge pump/PLL power supply current (I_{PP_PLL}) are monitored during irradiation.

The input logic threshold (V_{IL}/V_{IH}) is measured on all single-ended inputs as well as all differential inputs, and is reported as pass or fail. The output-drive voltage (V_{OL}/V_{OH}) is measured on the LVCMOS 3.3V and reported.

The propagation delay is measured on the output of the inverter string; the propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output of the inverter string design, are shown as oscilloscope captures is section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests. The irradiated DUT is functionally tested on the output of the inverter chain.

B. Power Supply Current

The core power supply current (I_{DD}) is 1.2 V, the I/O bank power supply currents (I_{DDI}) are 2.5 V ($I_{DDI\_2.5}$) and 3.3 V ($I_{DDI\_3.3}$). The charge pump and PLL power supply current (I_{PP_PLL}) is 3.3 V. Figures 2-12 illustrate the plot of in-flux standby I_{DD}, $I_{DDI\_2.5}$, $I_{DDI\_3.3}$ and I_{PP_PLL} versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation I_{DD}, $I_{DDI\_2.5}$, $I_{DDI\_3.3}$ and I_{PP_PLL}.

Table. 3. Pre-irradiation and Post Irradiation I_{DD}

DUT	Total Dose	Pre-Irradiation (A)	Post-irradiation (A)	Increase (%)
S43	125 krad	0.293	0.323	10.23
S44	125 krad	0.332	0.364	9.76
S45	125 krad	0.210	0.223	6.42

Table. 4. Pre-irradiation and Post Irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-Irradiation (A)	Post-irradiation (A)	Increase (%)
S43	125 krad	0.010	0.013	27.57
S44	125 krad	0.011	0.013	25.86
S45	125 krad	0.011	0.014	25.71

Table. 5. Pre-irradiation and Post Irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-Irradiation (A)	Post-irradiation (A)	Increase (%)
S43	125 krad	0.006	0.008	26.56
S44	125 krad	0.007	0.009	24.83
S45	125 krad	0.007	0.009	24.23

Table. 6. Pre-irradiation and Post Irradiation I_{PP_PLL}

DUT	Total Dose	Pre-Irradiation (A)	Post-irradiation (A)	Increase (%)
S43	125 krad	0.0036	0.0037	4.17
S44	125 krad	0.0035	0.0036	2.03
S45	125 krad	0.0035	0.0036	1.05

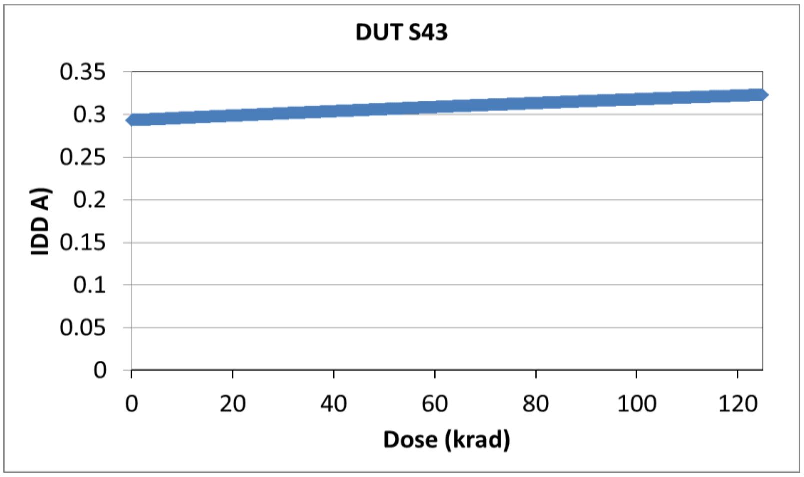

Fig. 2. DUT S43 core power supply current (I_{DD}) versus TID

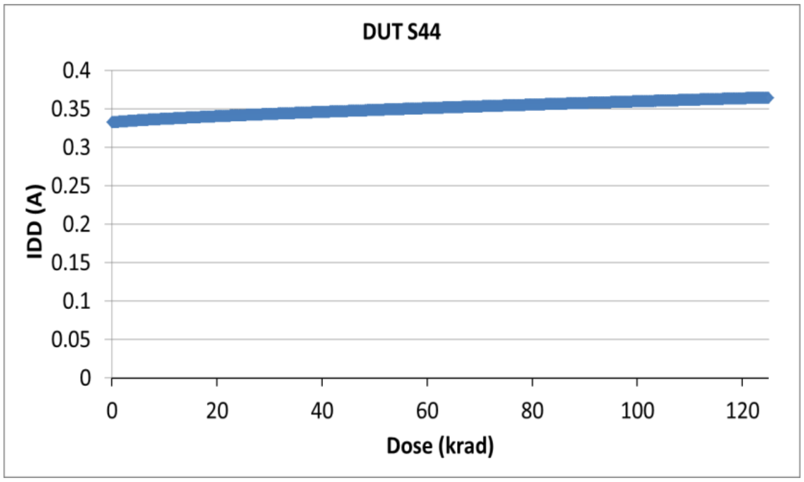

Fig. 3. DUT S44 core power supply current (I_{DD}) versus TID

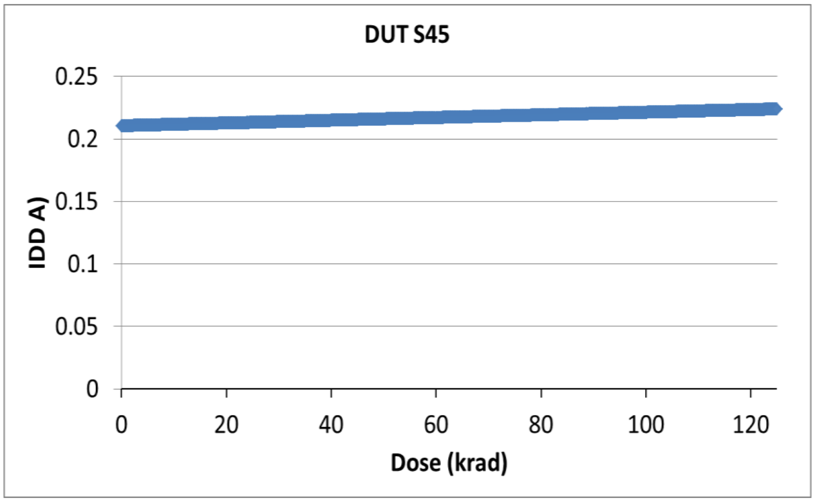

Fig. 4. DUT S45 core power supply current (I_{DD}) versus TID

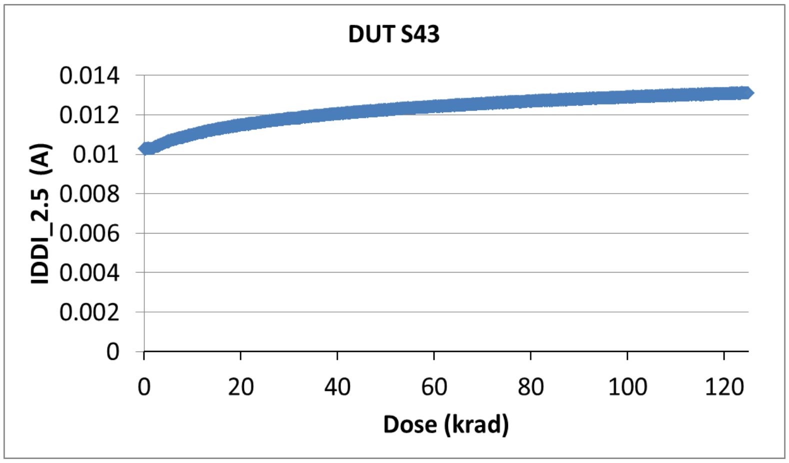

Fig. 5. DUT S43 I/O bank 2.5 V power supply current ($I_{DDI\_2.5}$) versus TID

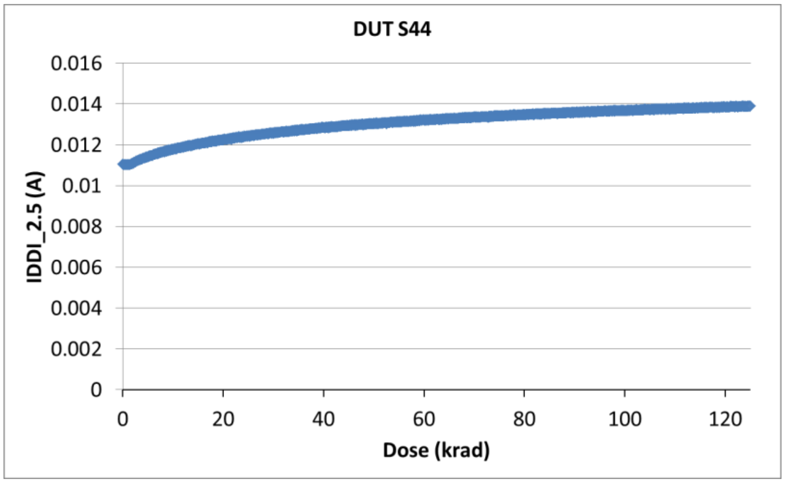

Fig. 6. DUT S44 I/O bank 2.5 V power supply current ($I_{DDI\_2.5}$) versus TID

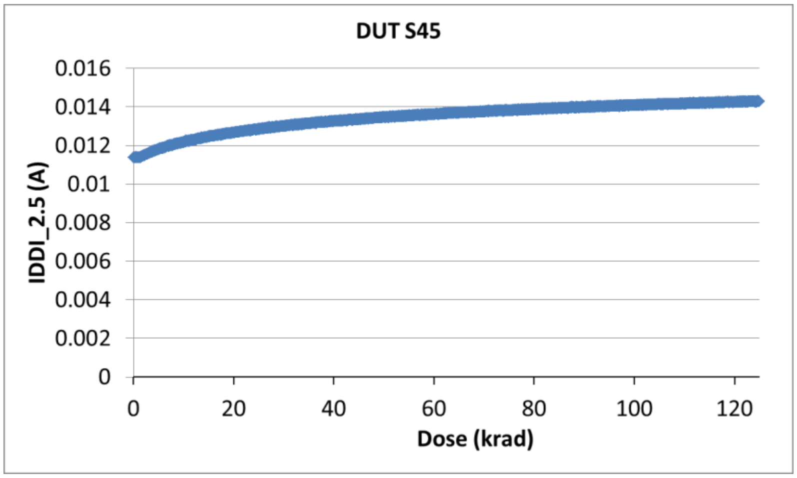

Fig. 7. DUT S45 I/O bank 2.5 V power supply current ($I_{DDI\_2.5}$) versus TID

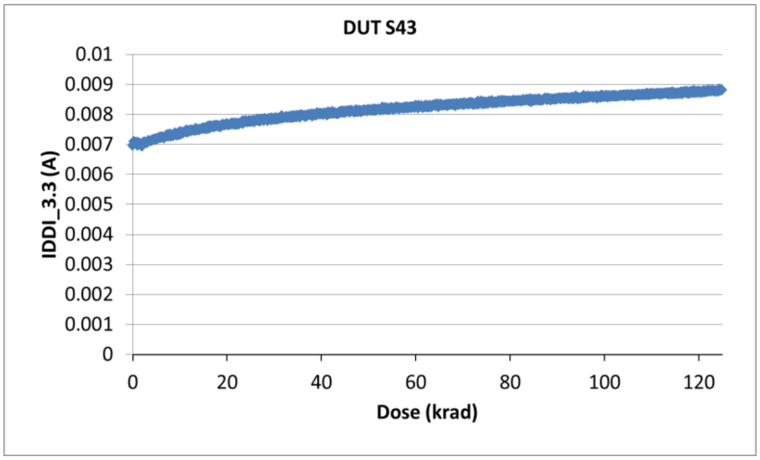

Fig. 8. DUT S43 I/O bank 3.3 V power supply current ($I_{DDI\_3.3}$) versus TID

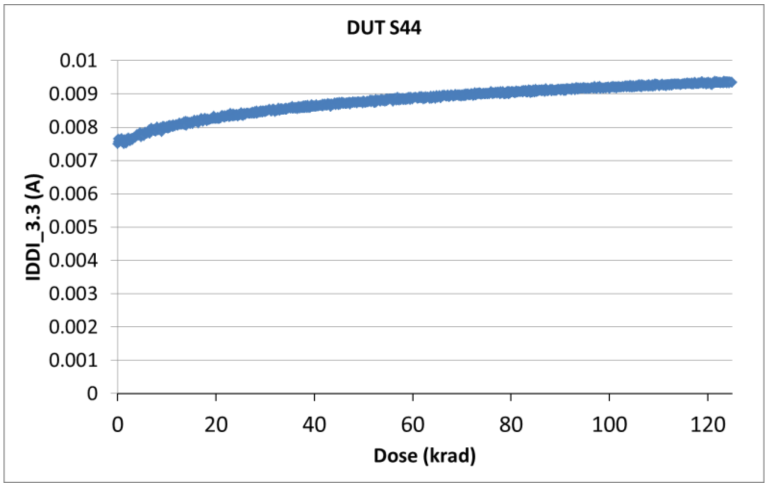

Fig. 9. DUT S44 I/O bank 3.3 V power supply current ($I_{DDI\_3.3}$) versus TID

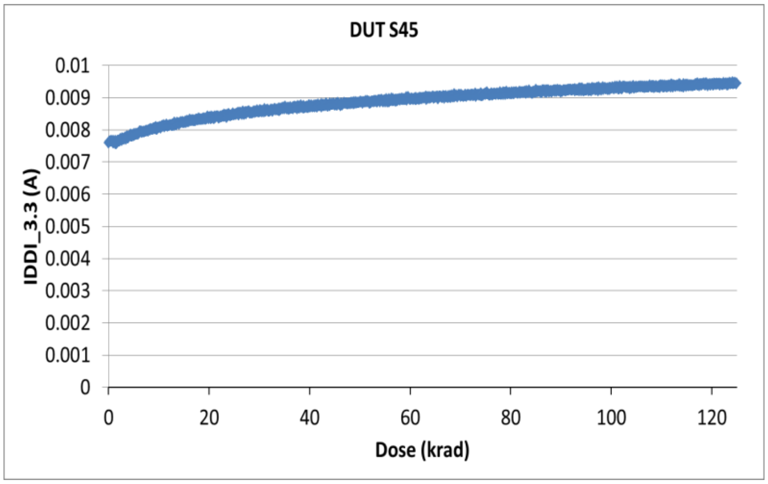

Fig. 10. DUT S45 I/O bank 3.3 V power supply current ($I_{DDI\_3.3}$) versus TID

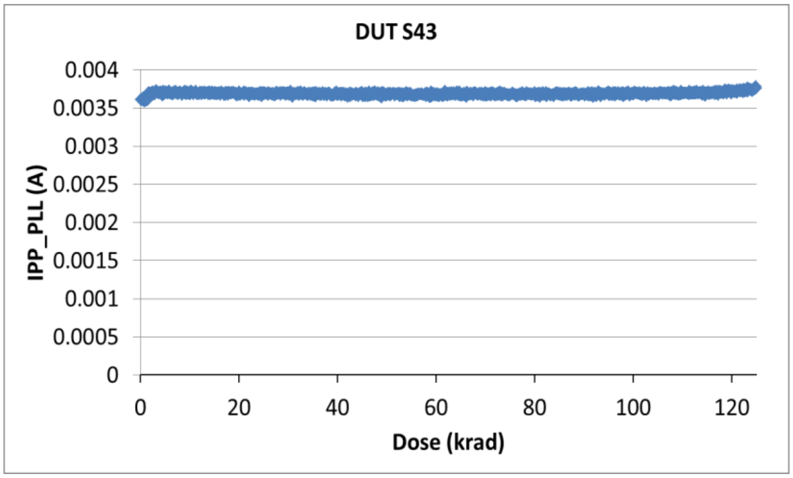

Fig. 11. DUT S43 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

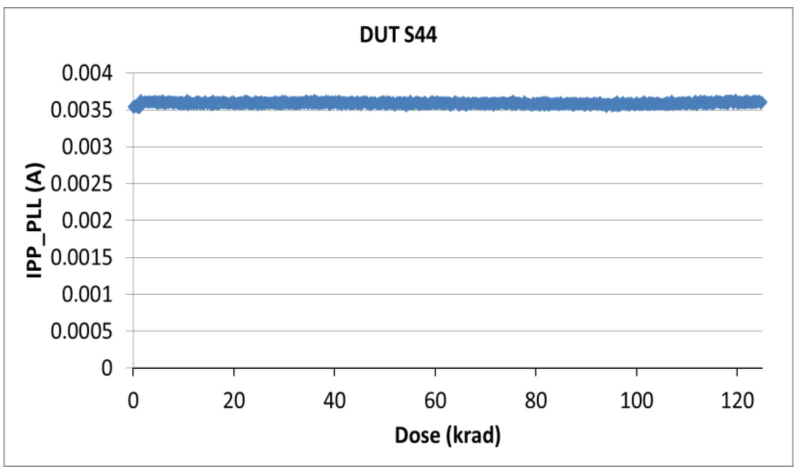

Fig. 12. DUT S44 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

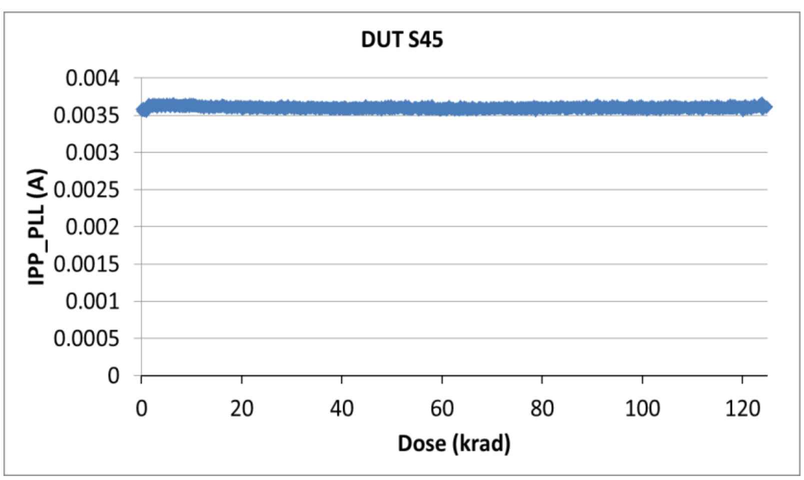

Fig. 13. DUT S45 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. V_{IH} is the input trip point when the input is going high to low and V_{IL} is the input trip point when the input is going low to high. The difference between the pre-irradiation and post-irradiation data is usually negligibly small. The input logic threshold (V_{IL}/V_{IH}) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail.

In each case, both the pre-irradiation and post-irradiation passed with respect to the specification.

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are listed in Tables 7 and 8. The post-irradiation data are within the specification limits; in each case, the radiation-induced degradation is within 10%.

Table. 7. Pre-irradiation and Post Irradiation V_{OL} (mV)

Pin\DUT(Dose)	S43 (125 krad)		S44 (125 krad)		S45 (125 krad)	
	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
In	267.66	267.68	257.82	258.36	262.81	262.88
Out	257.33	257.85	271.53	271.71	275.66	275.63
Clk	271.38	271.26	274.69	274.85	278.86	278.70
Reset	269.22	269.35	272.77	273.29	276.54	276.69
SERDES_Enable	264.34	264.44	267.02	267.24	271.13	271.14
Burn_In_Enable	264.36	264.16	266.78	266.80	270.87	270.66

Table. 8. Pre-irradiation and Post Irradiation V_{OH} (V)

Pin\DUT(Dose)	S43 (125 krad)		S44 (125 krad)		S45 (125 krad)	
	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
In	2.1743	2.1733	2.1747	2.1734	2.1712	2.1705
Out	2.1654	2.1644	2.1632	2.1624	2.1608	2.1600
Clk	2.1658	2.1650	2.1640	2.1630	2.1618	2.1609
Reset	2.1672	2.1665	2.1655	2.1646	2.1633	2.1623
SERDES_Enable	2.1705	2.1699	2.1693	2.1686	2.1669	2.1662
Burn_In_Enable	2.1709	2.1703	2.1698	2.1689	2.1673	2.1664

E. Propagation Delay

Table 9 lists the pre-irradiation, post-irradiation propagation delay and percentage change (degradations) for each DUT. Every DUT passes the 10% degradation criterion.

Table. 9. Radiation-Induced Propagation Delay Degradation

DUT	Total Dose	Pre-Irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
S43	125 krad	1.142	1.133	-0.856
S44	125 krad	1.132	1.128	-0.345
S45	125 krad	1.186	1.182	-0.293

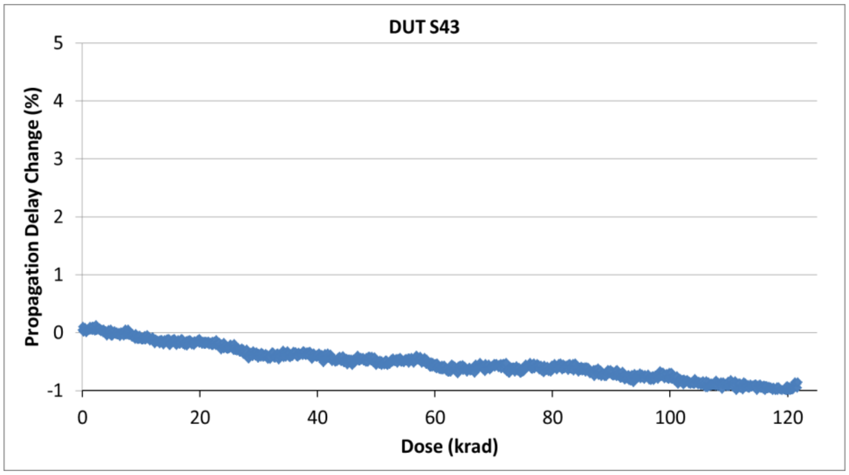

Fig. 14. DUT S43 propagation delay degradation versus TID

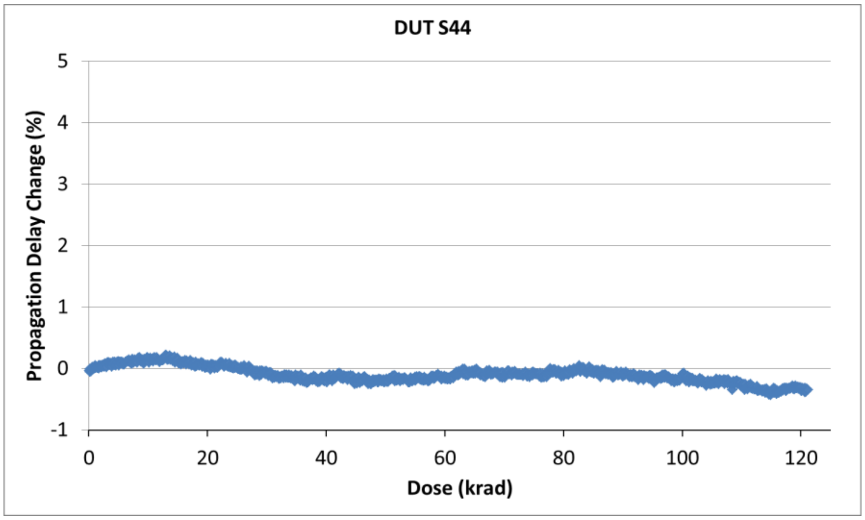

Fig. 15. DUT S44 propagation delay degradation versus TID

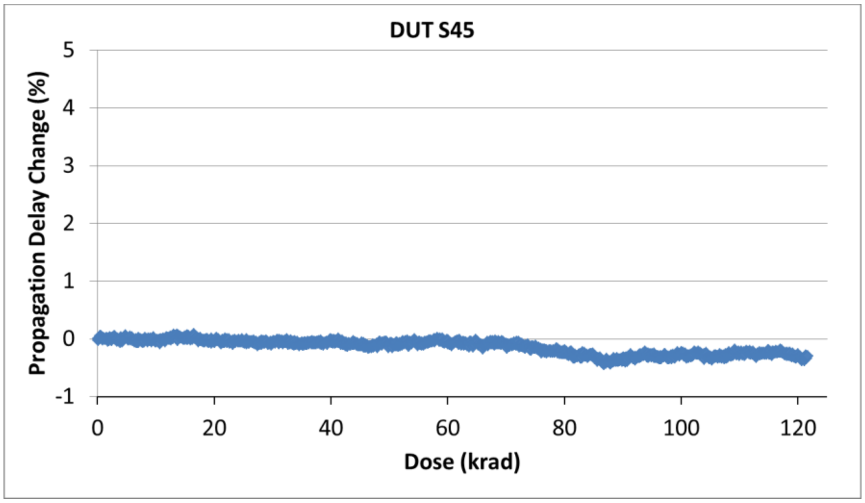

Fig. 16. DUT S45 propagation delay degradation versus TID

F. Transition Time

Figures 17 to 19 show the pre-irradiation and post-irradiation transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

Fig. 17(a). DUT S43 pre-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.

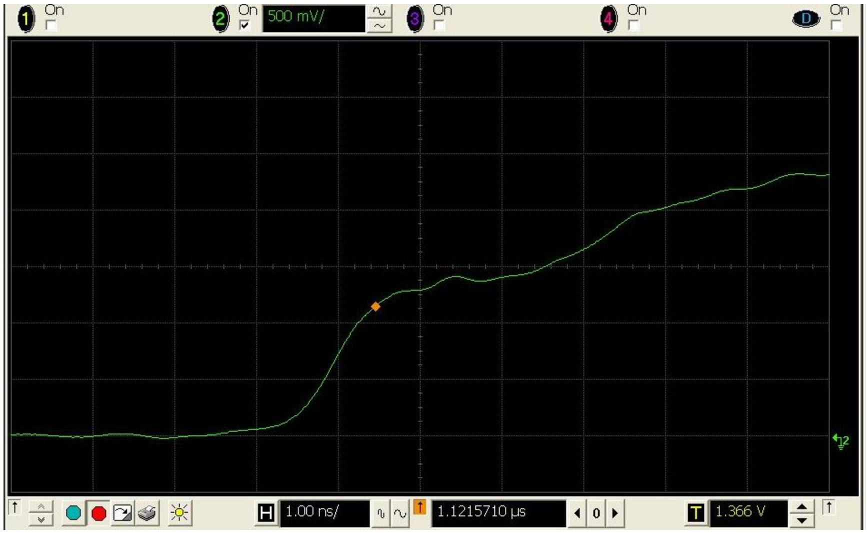

Fig. 17(b). DUT S43 post-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.

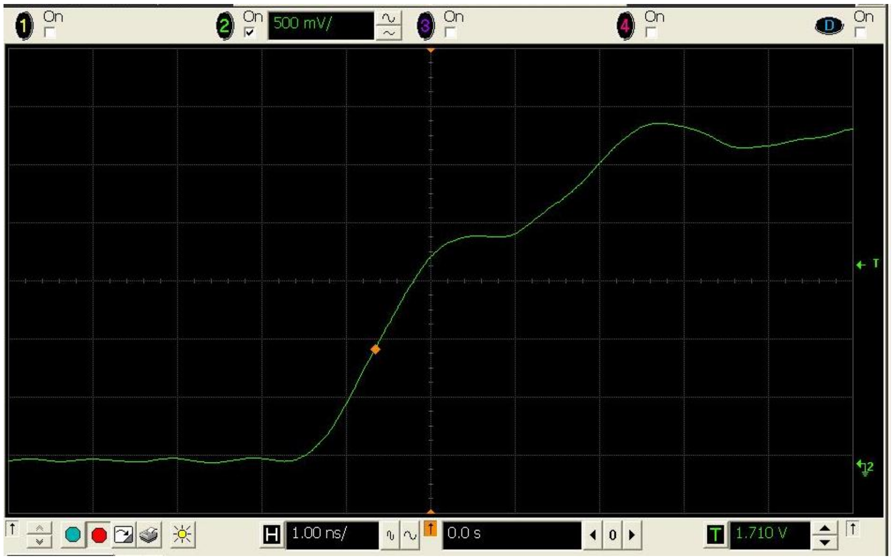

Fig. 18(a). DUT S44 pre-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.

Fig. 18(b). DUT S44 post-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.

Fig. 19(a). DUT S45 pre-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.

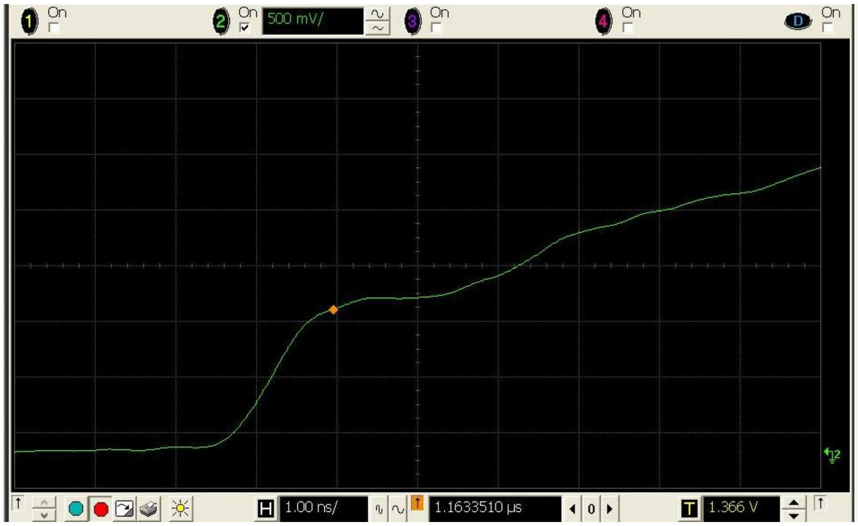

Fig. 19(b). DUT S45 post-irradiation rising edge, abscissa scale is 500 mV/div and ordinate scale is 1 ns/div.