RELIABILITY REPORT

FOR

MAX3678UTN+

PLASTIC ENCAPSULATED DEVICES

August 22, 2011

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Approved by
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Conclusion

The MAX3678UTN+ successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. ....Device Description

II. ....Manufacturing Information

III. ....Packaging Information

.....Attachments

IV. ....Die Information

V. ....Quality Assurance Information

VI. ....Reliability Evaluation

I. Device Description

A. General

The MAX3678 is a low-jitter frequency synthesizer with intelligent dynamic clock switching optimized for systems where redundant clock failover switching is needed. It contains a monolithic phase-locked loop (PLL) that accepts two reference clock inputs and generates nine phase-aligned outputs. The device continuously monitors the signal status for both reference clock inputs. In the event that the primary clock fails, the PLL automatically switches to the secondary clock input without generating a phase bump at the clock outputs, using a glitchless switchover mechanism. A manual switch mode is also provided for user-controlled switching. The device features ultra-low jitter generation of 0.3psRMS (integrated 12kHz to 20MHz) and excellent power-supply noise rejection. The MAX3678 operates from a single +3.3V supply and typically consumes 400mW. The operating temperature range is from 0°C to +85°C, and is available in a 8mm x 8mm, 56-pin TQFN package.

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II. Manufacturing Information

A. Description/Function:	Low-Jitter Frequency Synthesizer with Intelligent Dynamic Switching
B. Process:	MB3
C. Number of Device Transistors:	
D. Fabrication Location:	California
E. Assembly Location:	Thailand
F. Date of Initial Production:	May 21, 2008

III. Packaging Information

A. Package Type:	56-pin TQFN 8x8
B. Lead Frame:	Copper
C. Lead Finish:	100% matte Tin
D. Die Attach:	Conductive
E. Bondwire:	Au (1.3 mil dia.)
F. Mold Material:	Epoxy with silica filler
G. Assembly Diagram:	#05-9000-1938
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 3
J. Single Layer Theta Ja:	35°C/W
K. Single Layer Theta Jc:	1°C/W
L. Multi Layer Theta Ja:	21°C/W
M. Multi Layer Theta Jc:	1°C/W

IV. Die Information

A. Dimensions:	111 X 111 mils
B. Passivation:	BCB
C. Interconnect:	Al with top layer 100% Cu
D. Backside Metallization:	None
E. Minimum Metal Width:	0.35µm
F. Minimum Metal Spacing:	0.35µm
G. Bondpad Dimensions:	
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

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V. Quality Assurance Information

A. Quality Assurance Contacts: Richard Aburano (Manager, Reliability Engineering)
Don Lipps (Manager, Reliability Engineering)
Bryan Preeshl (Vice President of QA)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4340 \times 176 \times 2}$$

(Chi square value for MTTF upper limit)

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$\lambda = 6.2 \times 10^{-9}$

λ = 6.2 F.I.T. (60% confidence level @ 25°C)

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at http://www.maxim-ic.com/qa/reliability/monitor. Cumulative monitor data for the MB3 Process results in a FIT Rate of 0.08 @ 25C and 1.33 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SZH0MZ001 0813)

The HT59 die type has been found to have all pins able to withstand a HBM transient pulse of +/-1000V per JEDEC JESD22-A114. Latch-Up testing has shown that this device withstands a current of +/-250mA.

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Table 1
Reliability Evaluation Test Results

MAX3678UTN+

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)					
	Ta = 135°C	DC Parameters	80	0	SZH0MZ001E, D/C 0813
	Biased	& functionality	96	0	SZH0G2008D, D/C 0646
	Time = 192 hrs.				

Note 1: Life Test Data may represent plastic DIP qualification lots.

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