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## 1.0 Introduction

In order to help customers quickly integrate the new Microsemi clock distribution buffers into existing designs, selected clock buffer devices are footprint compatible with other devices. This application note lists the compatible parts and highlights the differences between the Microsemi devices and their footprint compatible parts. The devices and their industry counterparts are listed here:

Microsemi Device	Industry Counterpart
ZL40203	SY58021U
ZL40203	ADCLK944
ZL40211	SY89837U

**Table 1 - Compatible Devices**

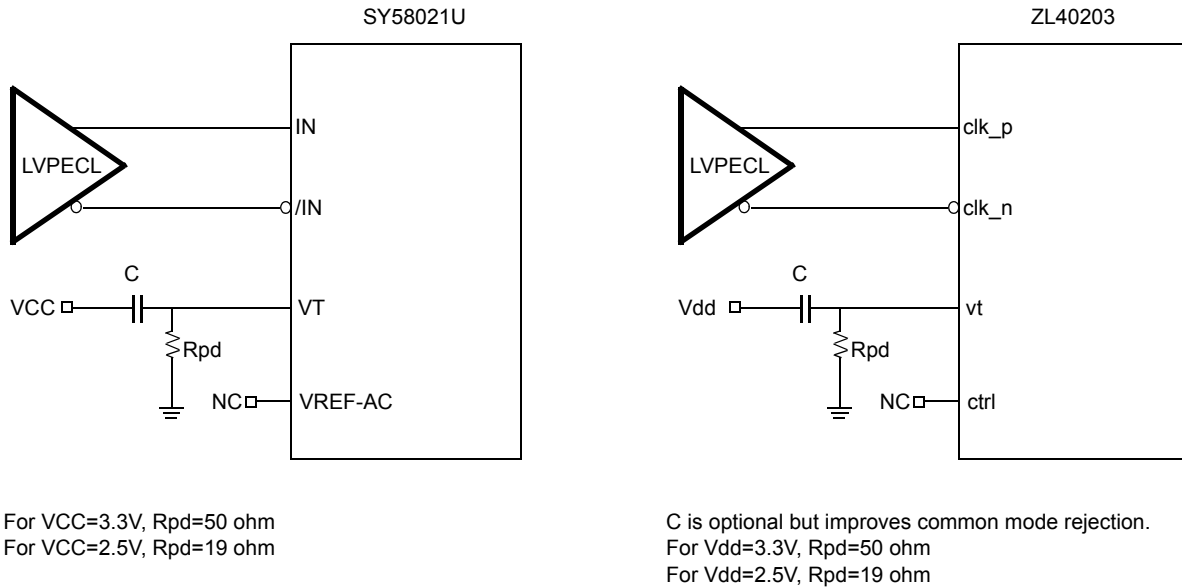
## 2.0 Footprint Compatibility of ZL40203 with Micrel SY58021U

The ZL40203 has been designed to be footprint compatible with the Micrel SY58021U. The following table shows the similarity of the pin map and also highlights the slight differences.

Pin	ZL40203 Pin Name	SY58021U Pin Name	Comment
1	clk_p	IN	
2	vt	VT	
3	ctrl	VREF-AC	See differences
4	clk_n	/IN	
5	gnd	GND	
6	out3_n	/Q3	
7	out3_p	Q3	
8	vdd	VCC	
9	out2_n	/Q2	
10	out2_p	Q2	
11	out1_n	/Q1	
12	out1_p	Q1	
13	vdd	VCC	
14	out0_n	/Q0	
15	out0_p	Q0	
16	gnd	GND	

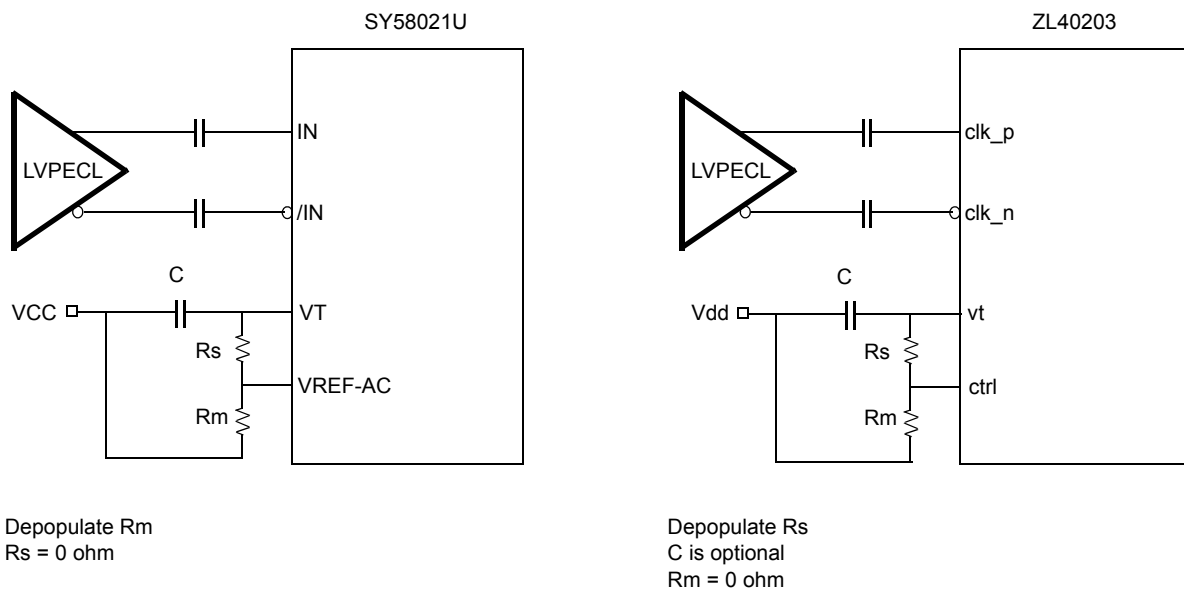
**Table 2 - Pin Commonality between ZL40203 and SY58021U**

For a DC coupled LVPECL input on pin 1 and 4, the SY58021U and the ZL40203 should be configured identically as shown in Figure 1. Note that for the ZL40203, pin 3 (ctrl) is a control pin which engages the internal biasing network when asserted. It is internally pulled to gnd (i.e logic 0) when unconnected. This pin could optionally be pulled down externally. Pin 3 (VREF-AC) on SY58021U is a voltage reference and should be left floating.



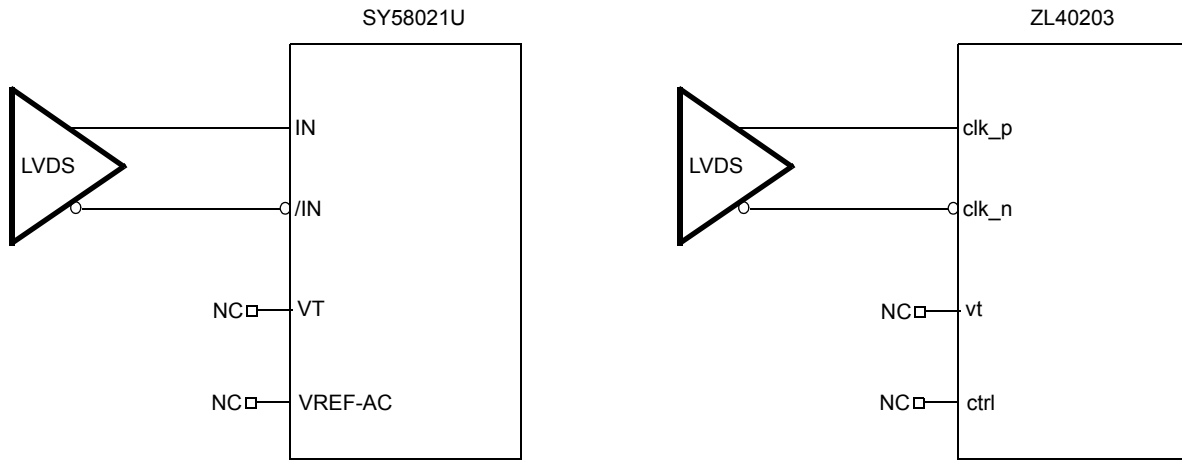
**Figure 1 - DC-Coupled LVPECL input**

For an AC-coupled LVPECL input, the devices should be configured as shown in Figure 2.



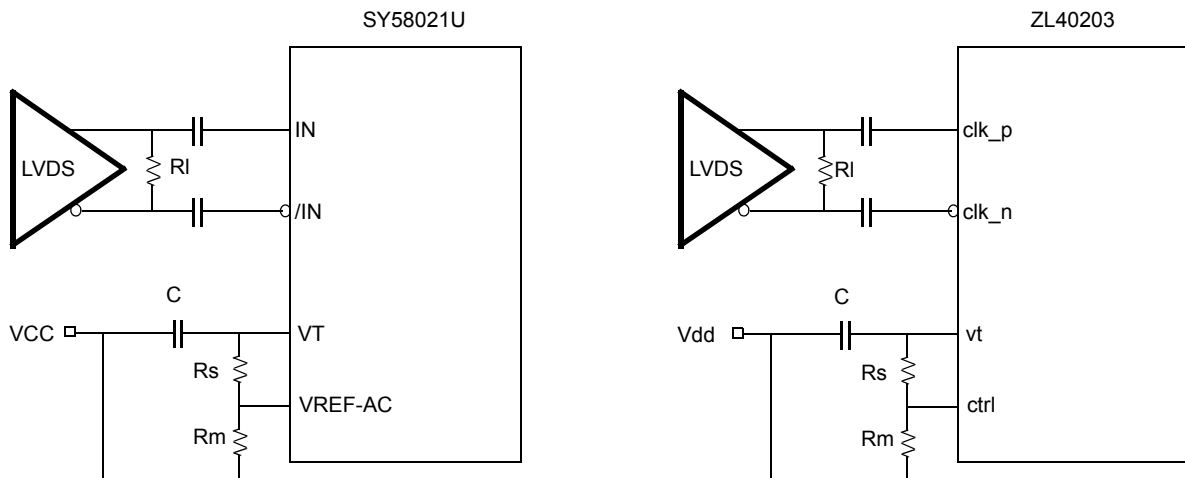
**Figure 2 - AC-coupled LVPECL input**

For a DC-coupled LVDS input signal, the devices should be configured identically as shown in Figure 3. Note again that the ctrl pin on the ZL40203 is pulled down internally.



**Figure 3 - DC-coupled LVDS input**

For AC-coupled LVDS, the devices should be configured as shown in Figure 4.



Depopulate Rm  
 Rs = 0 ohm  
 For VCC=3.3V, RI = 900 ohm  
 For VCC=2.5V, RI = 600 ohm

Depopulate Rs  
 C is optional  
 Rm = 0 ohm  
 For Vdd=3.3V, RI = 900 ohm  
 For Vdd=2.5V, RI = 600 ohm

**Figure 4 - AC-Coupled LVDS input**

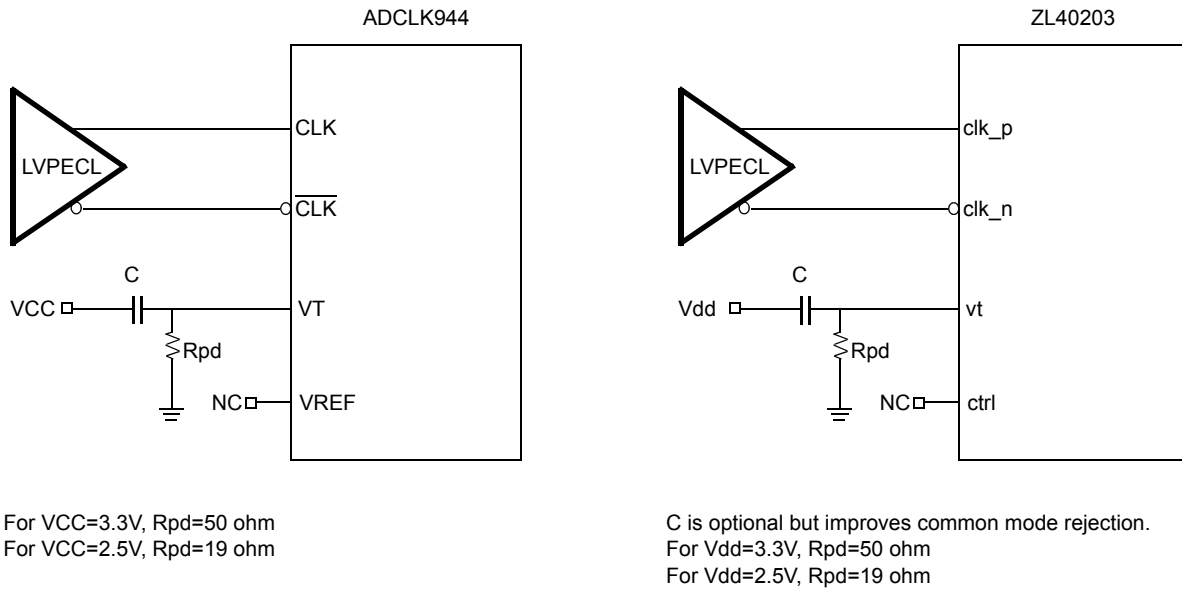
### 3.0 Footprint Compatibility of ZL40203 with ADI ADCLK944

The ZL40203 has been designed to be footprint compatible with the ADI ADCLK944. The following table shows the similarity of the pin map and also highlights the slight differences.

Pin	ZL40203 Pin Name	ADCLK944 Pin Name	Comment
1	clk_p	CLK	
2	vt	VT	
3	ctrl	VREF	See differences
4	clk_n	$\overline{\text{CLK}}$	
5	gnd	VEE	
6	out3_n	$\overline{\text{Q3}}$	
7	out3_p	Q3	
8	vdd	VCC	
9	out2_n	$\overline{\text{Q2}}$	
10	out2_p	Q2	
11	out1_n	$\overline{\text{Q1}}$	
12	out1_p	Q1	
13	vdd	VCC	
14	out0_n	$\overline{\text{Q0}}$	
15	out0_p	Q0	
16	gnd	VEE	

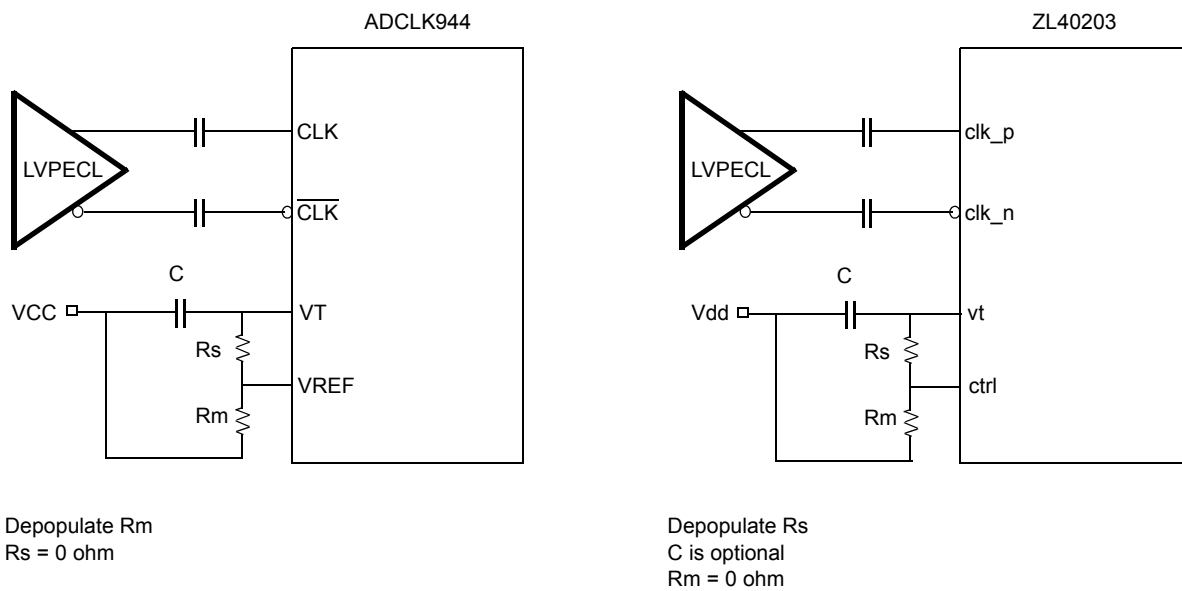
**Table 3 - Pin Commonality between ZL40203 and ADCLK944**

For a DC-coupled LVPECL input on pin 1 and 4, the ADCLK944 and the ZL40203 should be configured identically as shown in Figure 5. Note that for the ZL40203, pin 3 (ctrl) is a control pin which engages the internal biasing network when asserted. It is internally pulled to gnd (i.e logic 0) when unconnected. This pin could optionally be pulled down externally. Pin 3 (VREF) on ADCLK944 is a voltage reference and should be left floating.



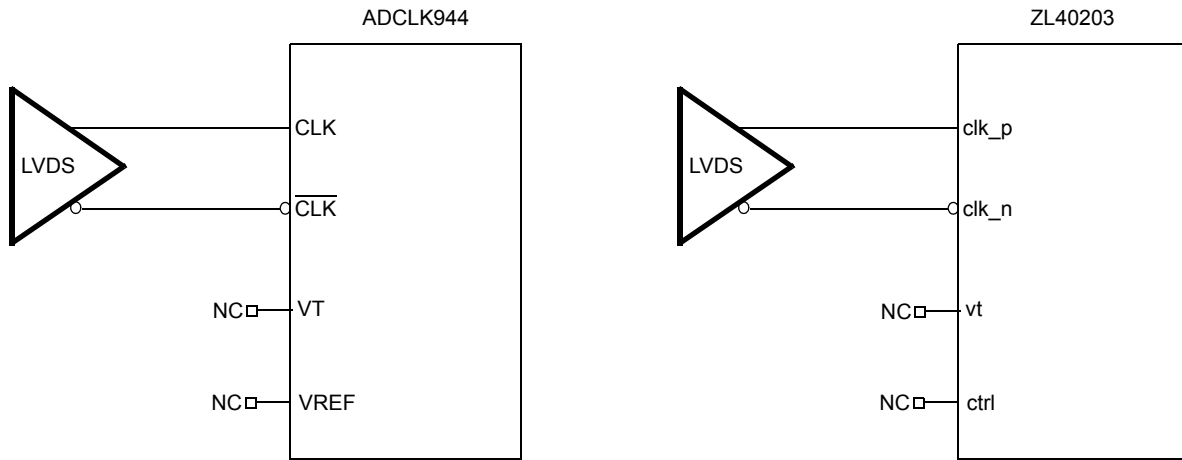
**Figure 5 - DC-coupled LVPECL input**

For an AC-coupled LVPECL input, the devices should be configured as shown in Figure 6.



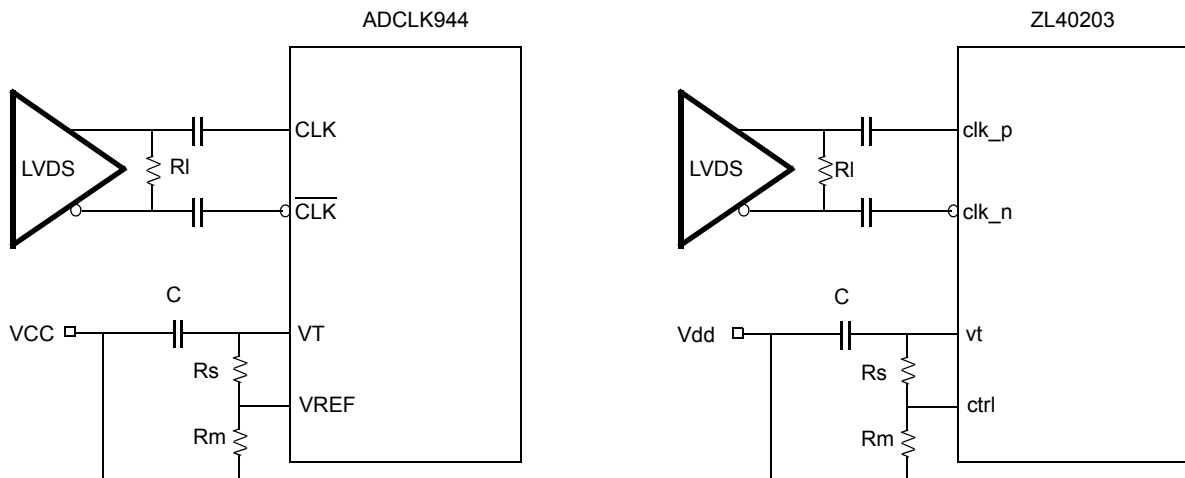
**Figure 6 - AC-coupled LVPECL input**

For a DC coupled LVDS input signal, the devices should be configured identically as shown in Figure 7. Note again that the ctrl pin on the ZL40203 is pulled down internally.



**Figure 7 - DC-coupled LVDS input**

For AC coupled LVDS, the devices should be configured as shown in Figure 8.



Depopulate Rm  
 Rs = 0 ohm  
 For VCC=3.3V, RI = 900 ohm  
 For VCC=2.5V, RI = 600 ohm

Depopulate Rs  
 C is optional  
 Rm = 0 ohm  
 For Vdd=3.3V, RI = 900 ohm  
 For Vdd=2.5V, RI = 600 ohm

**Figure 8 - AC Coupled LVDS input**

#### 4.0 Footprint Compatibility of ZL40211 with SY89837U

The ZL40211 is a 2:8 LVPECL buffer that has been designed to be footprint compatible with the Micrel SY89837U. The following table shows the similarity of the pin map and also highlights the slight differences.

Pin	ZL40203 Pin Name	SY58021U Pin Name	Comment
1	clk0_p	IN0	
2	vt0	VT0	
3	clk0_n	/IN0	
4	ctrl0	VREF-AC0	See differences
5	ctrl1	VREF-AC1	See differences
6	clk1_p	IN1	
7	vt1	VT1	
8	clk1_n	/IN1	
9	vdd	VCC	
10	NC	CAP	See differences
11	out7_n	/Q7	
12	out7_p	Q7	
13	out6_n	/Q6	
14	out6_p	Q6	
15	out5_n	/Q5	
16	out5_p	Q5	
17	out4_n	/Q4	
18	out4_p	Q4	
19	vdd	VCC	
20	gnd	gnd	
21	gnd	gnd	
22	vdd	VCC	
23	out3_n	/Q3	
24	out3_p	Q3	
25	out2_n	/Q2	
26	out2_p	Q2	
27	out1_n	/Q1	
28	out1_p	Q1	
29	out0_n	/Q0	
30	out0_p	Q0	
31	sel	SEL	
32	vdd	VCC	

**Table 4 - Pin Commonality between ZL40211 and SY89837U**

The difference in VREF-AC on the SY89837U and "ctrl" ZL40211 are the same as highlighted for the 1:4 devices. That is, VREF-AC provides a reference voltage that can be used in conjunction with the VT pin to set the bias point for the device. Ctrl is different in that it is a control pin that when asserted engages an internal biasing network. In addition to this difference, the SY89837U requires a capacitor to be connected to pin 10 to correctly initialize the Runt Pulse Elimination (RPE) circuit. The pin can be connected directly to Vcc to disable the RPE circuit. This pin is a No-connect on the ZL40211.

Refer to Figures 1 to 4 for guidelines on how to connect vt and ctrl vs VT and VREF-AC on these devices. The treatment of these pins is identical on the 1:4 devices and the 1:8 devices.





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