Intelligent Power Solutions

User Guide

IPS Evaluation Kit

Released

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Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 was published in April 2018. In Revision 2.0 of this document, the following changes were made:

- Appendix A—Communications Protocol (see page 25) was added.
- Section 4.1 (see page 5) was updated with new text.
- Section 8.3 (see page 20) was updated with new text.
- Section 7.1 (see page 18) was added.
- Table 1 (see page 2) was updated with LVTTL.
- Table 6 (see page 10) was updated with new values and a note was added below the table.
- Table 8 (see page 11) was updated with new values.
- Table 9 (see page 11) was updated with new values.
- Table 10 (see page 12) was updated with new values.
- Table 11 (see page 14) was updated with new values and a note was added below the table.
- Table 17 (see page 18) was updated with a new Manufacturer column.
- Table 18 (see page 21) was updated with new values.
- Figure 2 (see page 5) was updated with new text.
- Figure 3 (see page 7) was updated.

1.2 Revision 1.0

Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Glossary

The following table defines some common acronyms used throughout this document.

Table 1 • Glossary

Acronym	Description
AC	Alternating current
ADC	Analog-to-digital converter
COM	Control module
CRC	Cyclic redundancy checking
DC	Direct current
FPGA	Field programmable gate array
HES	Hall effect sensor
HPD	Hybrid power drive
HVDC	High voltage direct current
IDC	Insulation displacement contact
IGBT	Insulated gate bipolar transistors
IPS	Intelligent power solutions
LED	Light emitting diode
LVDS	Low-voltage differential signals
LVTTL	Low-voltage transistor-transistor logic
MON	Monitoring module
MOSFET	Metal oxide semiconductor field effect transistor
PCM	Power core module
PDE	Power drive electronics
PECU	Power electrical control unit
PSDI	PCM serial digital interface
PWA	Printed wiring assembly
PWM	Pulse width modulation
SBD	Schottky barrier diodes
STE	Special test equipment

3 Introduction

The Intelligent Power Solutions (IPS) evaluation kit is designed to assist users in evaluating the Power Core Module (PCM) (https://www.microsemi.com/existing-parts/parts/137208) and Hybrid Power Drive (HPD) (https://www.microsemi.com/existing-parts/parts/137209) for motor control. The IPS evaluation kit provides a common platform to test PCM and HPD with the following features:

- Digital isolation for low-voltage signal lines to provide noise immunity
- User-selectable operation options
- Flexible hardware configuration options per application requirements
- Cables provided in the kit for integration

This user guide includes the installation settings, operational procedures, design guidelines, and evaluation tutorial for the evaluation kit.

3.1 Kit Contents

Tables 2, 3, and 4 show the contents of the IPS evaluation kits for each of the three following order selections:

- Evaluation kit standalone (without PCM or HPD) EVAL-MAI-PWA
- Evaluation kit with HPD EVAL-MAIPDMC40X120A
- Evaluation kit with PCM EVAL-MAICMMC40X120A

The following table shows the contents of the standalone evaluation kit.

Table 2 • Evaluation Kit Standalone Contents

Part Description	Quantity
IPS evaluation board	1
2.00 mm IDC ribbon cable assembly, socket, 2-inch cable	1
2.00 mm IDC ribbon cable assembly, socket, 12-inch cable	1
IPS evaluation kit cable—evaluation board (D-type) to controller board (condensed board type)	1
Microsemi IPS Evaluation Kit User Guide	1

The following table shows the contents of the evaluation kit with HPD.

Table 3 • Evaluation Kit with HPD Contents

Part Description	Quantity
IPS evaluation board	1
2.00 mm IDC ribbon cable assembly, socket, 2-inch cable	1
2.00 mm IDC ribbon cable assembly, socket, 12-inch cable	1
IPS evaluation kit cable—evaluation board (D-type) to controller board (condensed board type)	1
Microsemi IPS Evaluation Kit User Guide	1
Hybrid power drive, MAIPDMC40X120A	1

The following table shows the contents of the evaluation kit with PCM.

Table 4 • Evaluation Kit with PCM Contents

Part Description	Quantity
IPS evaluation board	1

Part Description	Quantity
2.00 mm IDC ribbon cable assembly, socket, 2-inch cable	1
2.00 mm IDC ribbon cable assembly, socket, 12-inch cable	1
IPS evaluation kit cable—evaluation board (D-type) to controller board (condensed board type)	1
Microsemi IPS Evaluation Kit User Guide	1
Power core module, MAICMMC40X120A	1

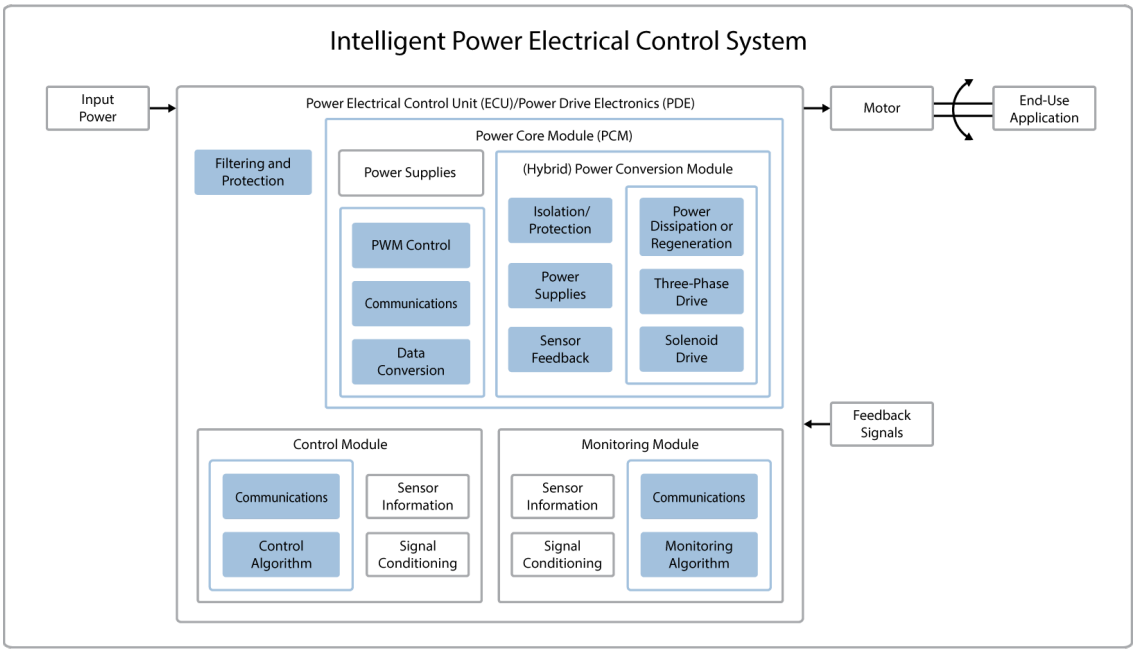
3.2 Power Core Module Architecture Summary

The PCM is an intelligent power conversion unit comprising of an HPD integrated with a controller board. The HPD is the sub-assembly integrated with the power stage and the driver PWA. The power conversion stage comprises of a three-phase bridge with embedded SiC MOSFETs or IGBTs and SiC Schottky Barrier Diodes (SBD). The driver sub-assembly comprises of isolated gate drive circuitry with telemetry functions to control the three-phase bridge. Additionally, SiC MOSFETs or IGBTs with isolated gate drivers are embedded on the driver sub-assembly to support high-voltage, low-current, solenoid drives. The controller sub-assembly comprises of low-voltage circuitry, primarily digital circuits for pulse-width modulation (PWM) generation and communication bus interfaces with local bias power supplies.

The primary application areas for the PCM include actuation systems such as primary and secondary flight control actuators, landing gear, and braking systems. Secondary applications include engine control systems such as starter generator, fuel management, and power conversion and distribution systems.

The following image shows the system architecture of the higher assembly called the power drive electronics (PDE) or the power electrical control unit (PECU). The PDE comprises the PCM, control (COM), and monitoring (MON) modules. The COM and MON are algorithm processing blocks for control and health monitoring of the PDE. The PCM communicates with the COM to generate the motor drive voltages. The PCM communicates with the MON to transfer the system critical information for safety and monitoring. For more information on the PCM and HPD, such as datasheets and application notes, refer to References (see page 24).

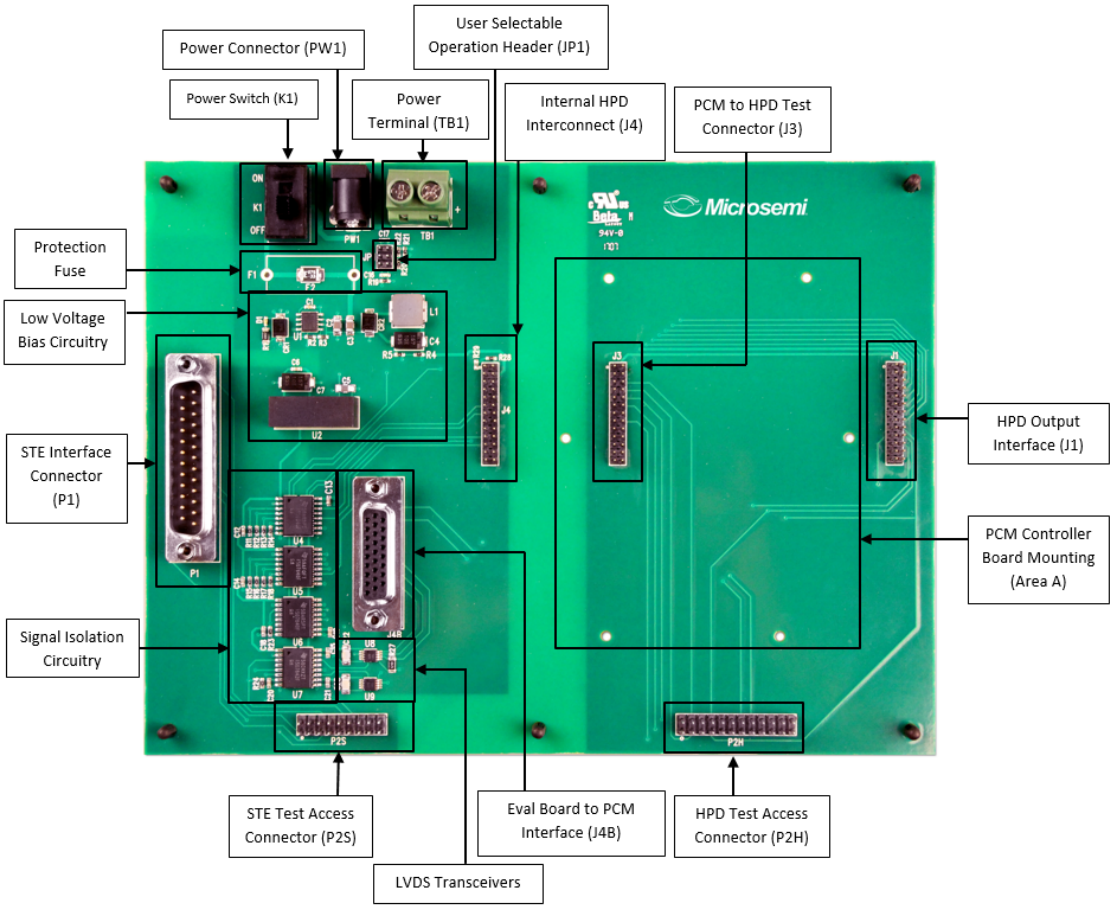
Figure 1 • Power Electrical Control Unit Architecture



4 Functional Description

The evaluation board provides isolated signal interfaces with simplified interconnects and configuration options to support both the PCM and HPD. The following image shows the evaluation board hardware. The board callouts highlight the features supporting different test configurations.

Figure 2 • Evaluation Board Hardware Illustration



4.1 PCM Test Configuration

The PCM test configuration allows users to test the PCM with the controller board mounted in Area A, as shown in Figure 2 (see page 5). Connector P1 transmits the input data from the user's input interface referenced as the special test equipment (STE). For the PCM evaluation, the STE input signals are grouped into COM and MON data, discrete input signals, and motor position signals. All the input signals except the motor position signals are buffered through the isolators to provide noise immunity for single-ended interfaces. The motor position signals (3×) are differential inputs that measure the rotor position information and transmit the data from J4B to the PCM via P5 located on the controller board. Refer to Section 5.1 (see page 8) for hardware installation settings.

The COM and MON data are converted from single-ended to LVDS through LVDS drivers for the PCM communication bus to process the information. See Appendix A (see page 25) for more information on PCM serial digital interface.

The user can run the PCM in pre-programmed modes that can be triggered on the controller board using Jumper header JP1. Refer to Firmware Programming Settings (see page 9) for more information on programming configurations.

The PCM controller board processes the input signals and transmits the output data from J3 to J1 (through board traces). The HPD is connected to J1 through the 12-inch ribbon cable.

The output signals from the PCM to the STE are communicated through COM and MON transmission outputs (COM_TX and MON_TX). The user can decode the information to read the telemetry information according to the communication protocol definitions.

All I/O signals on the evaluation board for the PCM test configuration can be monitored through designated test access connectors P2S and P2H.

4.2 HPD Configuration

The HPD can be evaluated using either of the two test configuration options listed below.

Option 1: With Controller Card

The PCM configuration instructions should be followed for setup when the HPD is used with the controller card. Refer to the PCM Test Configuration (see page 5) section for more information.

This configuration allows the user to evaluate the HPD unit using the pre-programmed firmware options on the controller card. The user is not required to decode the telemetry information through the PSDI protocol. All the HPD evaluation parameters can be accessed using HPD test access connector P2H. Refer to Section 5.1 (see page 8) for hardware installation settings.

Similar to the configuration of the PCM, the user can trigger a pre-programmed mode in the FPGA on the controller board using Jumper JP1. Refer to Firmware Programming Settings (see page 9) for more information on programming configurations. The controller board transmits the output data from J3 to J1 (through board traces). The HPD is connected to J1 through the 12-inch ribbon cable.

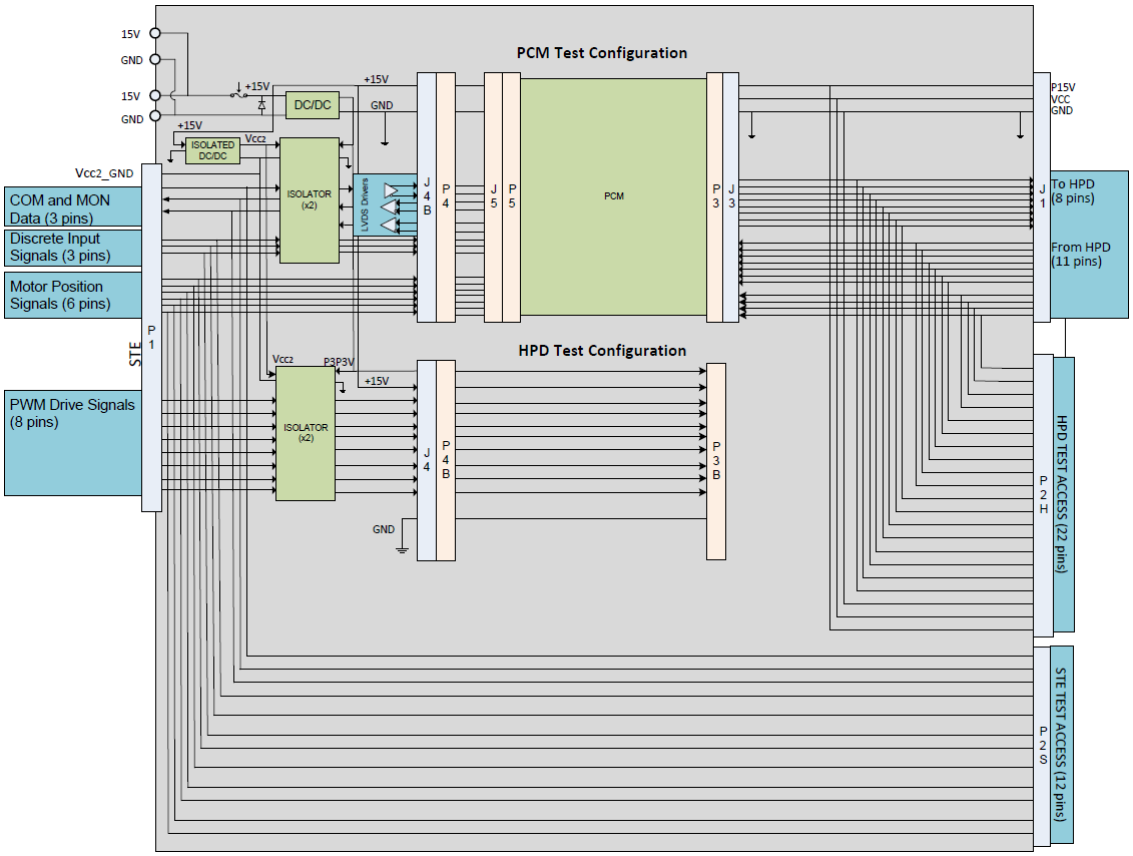
Option 2: Without Controller Card

This option allows the user to test the HPD with an STE that generates the PWM signals based on the user's control algorithm. The PWM drive input signals are transmitted from the STE to connector P1. They are buffered through the isolators to provide noise immunity for single-ended interfaces. The buffered signals are connected from J4 to J3 through the 2-inch ribbon cable interface. The HPD is connected to J1 through the 12-inch ribbon cable interface. Refer to Section 5.2 (see page 8) for hardware installation settings.

All I/O signals on the evaluation board for the HPD test configuration can be monitored through designated test access connectors P2S and P2H.

The following image shows the functional block diagram of the evaluation board for the various configurations.

Figure 3 • Functional Block Diagram



5 Installation and Configuration Settings

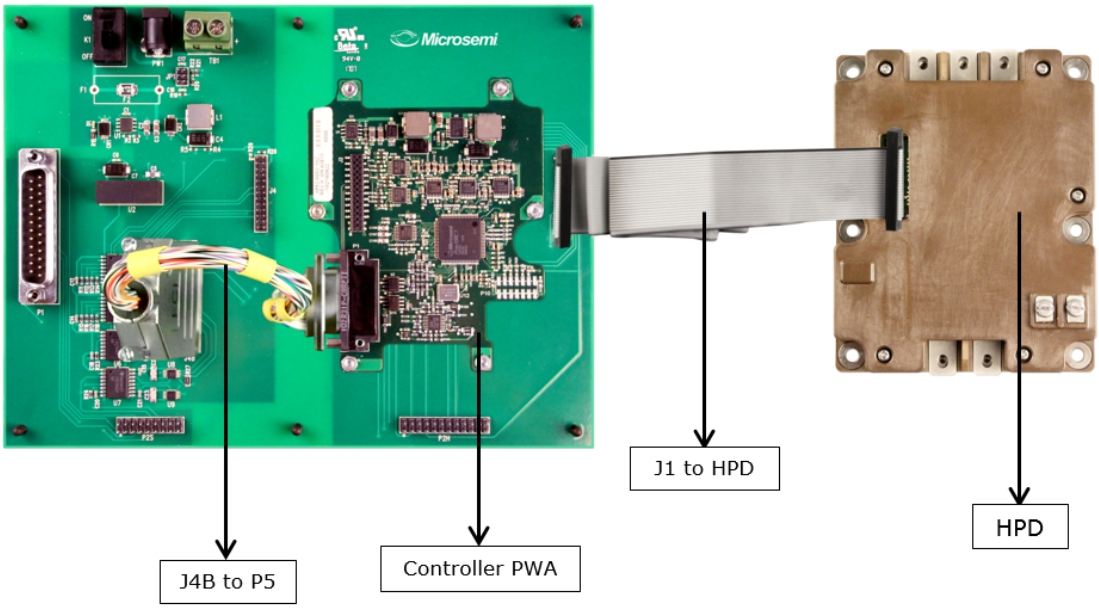
This section describes the hardware installation and firmware programming configurations for the evaluation kit.

5.1 Evaluation Board with PCM

In this configuration, the PCM Controller PWA has to be mounted onto the evaluation board using the mechanical hardware provided in the kit. The hardware setting for the PCM is shown in the following image.

Note: The controller board is mounted on the evaluation board prior to installation of the interconnect cables.

Figure 4 • PCM Test Configuration

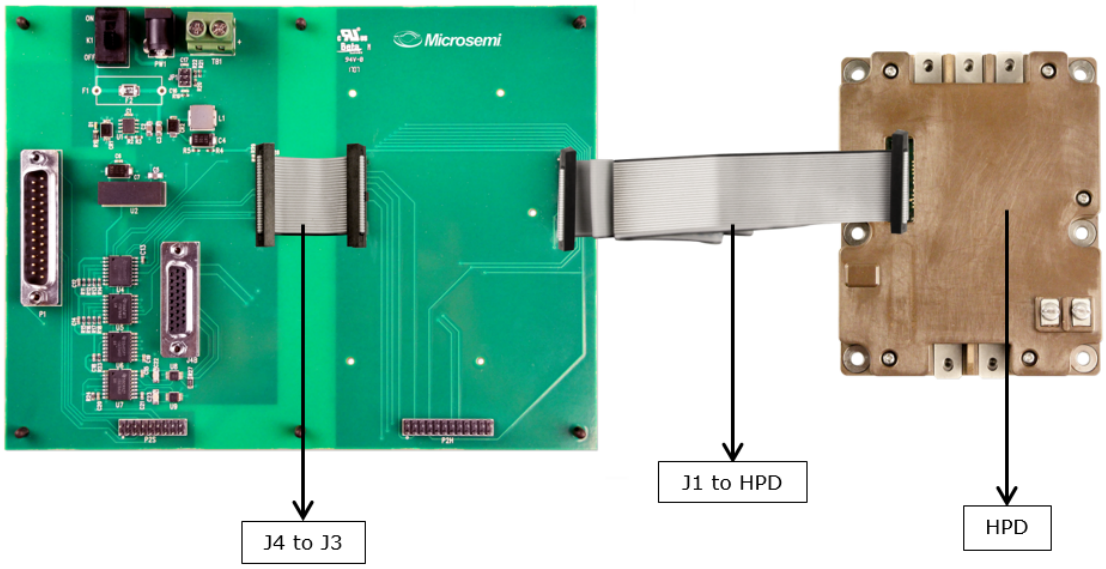


5.2 Evaluation Board with HPD

The HPD can be evaluated either with or without a controller card as described previously. The hardware setting for the HPD with the controller card is shown in Figure 4 (see page 8).

The hardware setting for the HPD without the controller card is shown in the following image.

Figure 5 • HPD Test Configuration



5.3 Firmware Programming Settings

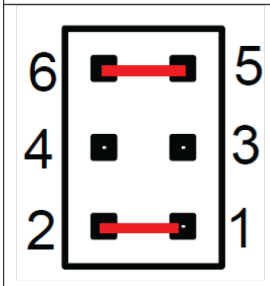
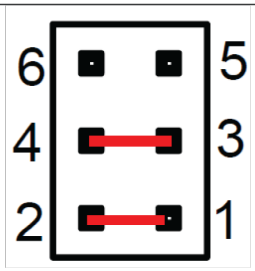
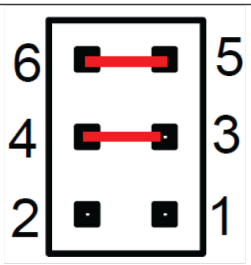
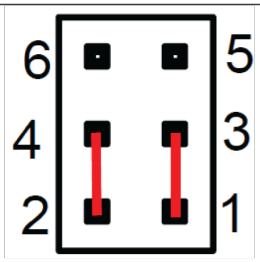
The firmware programming settings are applicable to the PCM and HPD with controller card test configurations. The following table lists the firmware configurations with the corresponding jumper settings and program status. See Figure 6 (see page 10) for JP1 pin references.

Table 5 • Firmware Configuration

Pin Position—JP1	Firmware Status	Program Description
Installed between pins 1-2; pins 5-6 (By default)	'00'	Default setting represents standard PCM configuration. User shall send the commands through COM_RX input line per the communication protocol settings (see Appendix A (see page 25)).
Install between pins 1-2; pins 3-4	'01'	This program executes three-phase bridge control with nominal current setting of 12.5 A peak phase amplitude and solenoid control. Refer to Table 6 (see page 10) for load settings.
Install between pins 5-6; pins 3-4	'10'	This program executes three-phase bridge control with maximum current setting of 25 A peak phase amplitude and solenoid control. Refer to Table 6 (see page 10) for load settings.
Install between pins 1-3; pins 2-4	'11'	This program executes standalone solenoid control. The three-phase bridge control is disabled. Refer to Table 6 (see page 10) for solenoid settings.

The following figure illustrates the jumper pin positions for each firmware status. Note pins 3 and 4 are not connected to the board. Refer to Figure 7 (see page 13) for the reference pin orientation on the evaluation board.

Figure 6 • Jumper Position Representing the Firmware Status

Firmware Status '00'	Firmware Status '01'	Firmware Status '10'	Firmware Status '11'
			

The following table summarizes the load settings recommended for testing the PCM and HPD for the previously mentioned firmware configurations at an ambient temperature of 25 °C. The user shall ensure that the current and voltage limits do not exceed the maximum allowable ratings for PCM and HPD. Refer to References (see page 24) for PCM and HPD specifications.

Table 6 • Load Settings for PCM and HPD

Parameter	Value	Description
Nominal Current Settings		
Current rating	12.5 A	Peak value per phase at 400 Hz
Three-phase switching frequency	10 kHz	Typical
HVDC rating	540 VDC	At 12.5 A
Inductive load	2.5 mH	Maximum per phase
High Current Settings		
Current rating	25 A	Peak value per phase at 400 Hz
Three-phase switching frequency	10 kHz	Typical
HVDC rating	540 VDC	At 25 A
Inductive load	2.5 mH	Maximum per phase
Solenoid Settings		
Current rating	1 A	Peak value (steady state)
Current rating	5 A	Peak value (transient state) for < 100 ms
Switching frequency	10 kHz	Typical
HVDC rating	540 VDC	
Load inductance	5 H	Typical load range is from 2.5 H–10 H
Load resistance	100 Ω	Maximum 1 kW power rating, in series with the load inductance

Note: In order to eliminate the phase current offsets, it is recommended to connect an external load resistance of 2.2 Ω in series with the load inductors per phase.

6 Operation and Interface Characteristics

This section describes the power-up procedure, electrical characteristics, and mechanical characteristics of the evaluation board.

6.1 Powering Up the Board

The PCM Evaluation Board is powered by a 15 V power source using either of the two power input terminals: Power Connector Jack (PW1) (center point of the power jack is the positive terminal) or Power Terminal Block (TB1). The user shall ensure that only one power source is applied at any given instant. Switch control (K1) is provided at the input to deliver power to the circuit board. The switch settings are given in Table 7. A LED (D1) is used to indicate the status of the 15V power to the board.

The following table shows the switch settings of the PCM Evaluation Board.

Table 7 • Power Switch K1 Settings

Switch K1 Position	Power Status	LED Status—D1
ON	ON	Yellow—Indicates 15 V power
OFF	OFF	No color—Indicates no power

6.2 Electrical Characteristics

The electrical characteristics of the input and output signals are listed in the following tables. The signals are categorized based on their connector assignment on the evaluation board. All ratings are specified at 25 °C ambient temperature (T_A) unless otherwise noted.

The following table lists the power connector PW1/TB1 electrical characteristics.

Table 8 • Power Connector PW1/TB1

Parameter	Signal Reference	Min	Typ	Max	Unit
15 V bias power supply	+15 V	12	15	18	V
15 V bias power current	$I_{15V\text{-}IN}$		31		mA

The following table lists the STE P1 connector signals electrical characteristics.

Table 9 • STE P1 Connector Signals

Parameter	Signal Reference	Min	Typ	Max	Unit	Notes
COM transmit channel	COM_TX	0	5	5.025	V	COM and MON data
COM receive channel	COM_RX	0	5	5.025	V	COM and MON data
MON receive channel	MON_RX	0	5	5.025	V	COM and MON data
Drive enable	DR_EN	0	5	5.025	V	Discrete input signals
Program 1	PRG1	0	5	5.025	V	Discrete input signals
Program 2	PRG2	0	5	5.025	V	Discrete input signals
Rotor position input per phase	EXT_HES_IN	0		24	mA	HES motor position signals; differential input
Phase drive signal, low level	PH_DR_L	0		1.5	V	PWM drive input signals for three-phase and solenoid bridge from STE

Parameter	Signal Reference	Min	Typ	Max	Unit	Notes
Phase drive signal,high level	PH_DR_H	3.51		5.025	V	PWM drive input signals for three-phase and solenoid bridge from STE

The following table lists the HPD J1 connector signals electrical characteristics.

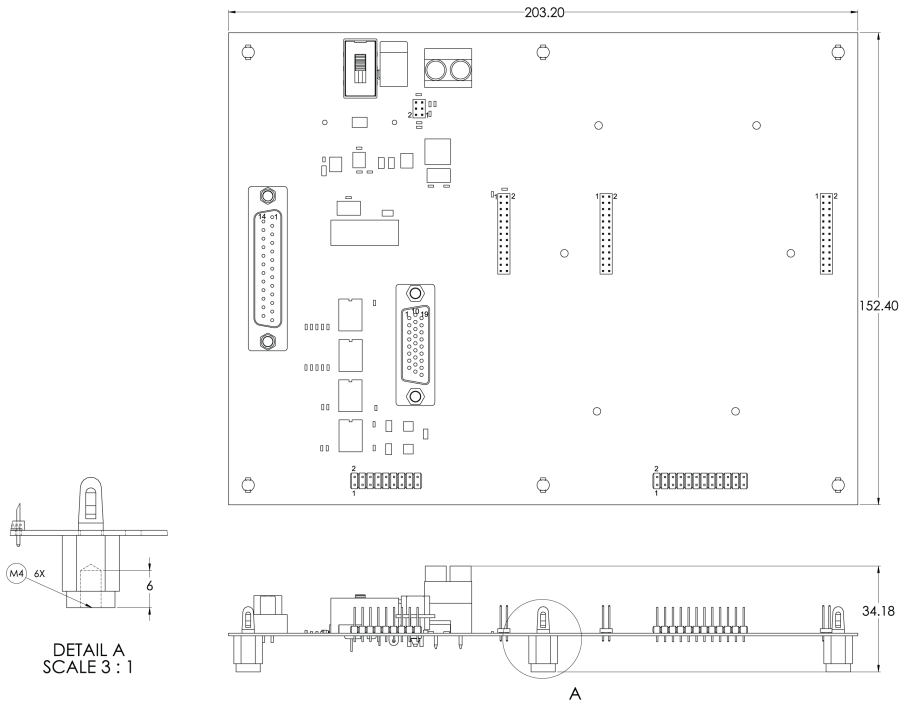
Table 10 • HPD J1 Connector Signals

Parameter	Signal Reference	Min	Typ	Max	Unit	Notes
15 V bias power supply	P15V	12	15	18	V	
3.3 V	VCC	3.29	3.3	3.31	V	
Phase sense current	IPHASE	0.825	1.65	2.475	V	Peak phase current range = ±25 A
Temperature sensor	RT		1000		Ω	
Phase drive signal, low level	PH_DR_L	0		0.99	V	PWM drive signals for three-phase and solenoid bridge to HPD
Phase drive signal, high level	PH_DR_H	2.31		3.3	V	PWM drive signals for three-phase and solenoid bridge to HPD
Scaled HVDC voltage	TM_VBUS	0	1.08	2	V	HVDC range = 0 V to 1000 V
DC bus current sense	IBUS			3.3	V	Maximum DC bus current
Solenoid current sense	ISOL	1.65	1.78	2.31	V	Maximum solenoid current = 5 A (transient)

6.3 Mechanical Characteristics

The evaluation board dimensions are shown in the following figure. All dimensions are in millimeters.

Figure 7 • PCM Assembly Drawing



7 Pin List

The following tables list the pin descriptions for the evaluation board interface connectors.

Table 11 • Connector P1 Signal Pins

P1 Singal Pin #	STE Connector P1 Pin Description	Signal Type	Signal Group	Signal Reference
1	Phase 1 top switch drive	Input	PWM drive	PH_DR_1T
2	Phase 1 bottom switch drive	Input	PWM drive	PH_DR_1B
3	Phase 2 top switch drive	Input	PWM drive	PH_DR_2T
4	Phase 2 bottom switch drive	Input	PWM drive	PH_DR_2B
5	Phase 3 top switch drive	Input	PWM drive	PH_DR_3T
6	Phase 3 bottom switch drive	Input	PWM drive	PH_DR_3B
7	Solenoid top switch drive	Input	PWM drive	SOLENOID_DR_1T
8	Solenoid bottom switch drive	Input	PWM drive	SOLENOID_DR_1B
9	External HES phase 1 input	Input	Motor position	EXT_HES_IN1
10	External HES phase 1 input return	Input	Motor position	EXT_HES_IN1_RTN
11	External HES phase 2 input	Input	Motor position	EXT_HES_IN2
12	External HES phase 2 input return	Input	Motor position	EXT_HES_IN2_RTN
13	External HES phase 3 input	Input	Motor position	EXT_HES_IN3
14	External HES phase 3 input return	Input	Motor position	EXT_HES_IN3_RTN
15	Drive enable	Input	Discrete inputs	DR_EN
16	Program 1	Input	Discrete inputs	PRG1
17	Program 2	Input	Discrete inputs	PRG2
18	Control receive	Input	COM and MON data	COM_RX
19	Control transmit	Output	COM and MON data	COM_TX
20	Monitor transmit	Output	COM and MON data	MON_TX
21	Vcc2 power ground	Output		Vcc2_GND
22	No connect			NC
23	No connect			NC
24	Vcc2 power ground	Output		Vcc2_GND
25	Vcc2 power ground	Output		Vcc2_GND

Note: The evaluation board generates an internal 5 V bias power referenced as Vcc2 (See Figure 3 (see page 7)). A 3.3 V bias power option is available upon request.

Table 12 • Connector J4B Signal Pins

JB4 Singal Pin #	PCM Connector JB4 Pin Description	Signal Type	Signal Reference
1	External HES phase 2 input	Input	EXT_HES_IN2
2	Ground	Input	GND
3	External HES phase 2 input return	Input	EXT_HES_IN3_RTN
4	Ground	Input	GND
5	No connect		NC
6	Ground	Input	GND

JB4 Singal Pin #	PCM Connector JB4 Pin Description	Signal Type	Signal Reference
7	No connect		NC
8	Ground	Input	GND
9	Monitor transmit positive	Output	MON_TX_P
10	No connect		NC
11	Drive enable	Input	DRIVE_EN
12	Program 1	Input	PROG1
13	Program 2	Input	PROG2
14	No connect		NC
15	No connect		NC
16	No connect		NC
17	External HES phase 2 input return	Input	EXT_HES_IN2_RTN
18	Monitor transmit negative	Output	MON_TX_N
19	External HES phase 3 input	Input	EXT_HES_IN3
20	15 V bias power	Input	+15V
21	External HES phase 1 input	Input	EXT_HES_IN1
22	External HES phase 1 input return	Input	EXT_HES_IN1_RTN
23	Control receive negative	Input	COM_RX_N
24	Control receive positive	Input	COM_RX_P
25	Control transmit negative	Output	COM_RX_N
26	Control transmit positive	Output	COM_RX_P

Table 13 • Connector J4 Signal Pins

J4 Singal Pin #	HPD Board Interface Connector J4 Pin Description	Signal Type	Signal Reference
1	Ground reference	Input	GND_REF
2	P3P3V ground	Input	VCC_GND
3	No connect		NC
4	3.3 V supply power	Input	VCC
5	No connect		NC
6	No connect		NC
7	No connect		NC
8	No connect		NC
9	Phase 3 bottom switch isolated drive	Input	PHASE_DR_3B_O
10	No connect		NC
11	Phase 2 bottom switch isolated drive	Input	PHASE_DR_2B_O
12	No Connect		NC
13	Phase 1 bottom switch isolated drive	Input	PHASE_DR_1B_O
14	No connect		NC
15	Phase 3 top switch isolated drive	Input	PHASE_DR_3T_O
16	No connect		NC
17	Phase 2 top switch isolated drive	Input	PHASE_DR_2T_O
18	No connect		NC
19	Phase 1 top switch isolated drive	Input	PHASE_DR_1T_O

J4 Singal Pin #	HPD Board Interface Connector J4 Pin Description	Signal Type	Signal Reference
20	No connect		NC
21	Solenoid bottom switch isolated drive	Input	SOL_DR_1B_O
22	Solenoid top switch isolated drive	Input	SOL_DR_1T_O
23	15 V bias power	Input	+15V
24	Ground	Input	GND
25	15 V bias power	Input	+15V
26	Ground	Input	GND

Table 14 • Connector J1 Signal Pins

J1 Singal Pin #	HPD Output Interface Connector J1 Pin Description	Signal Type	Signal Reference
1	Power ground reference	Input	GND_REF
2	3.3 V power ground	Input	VCC_GND
3	Phase 3 sense current	Output	IPHASE_3
4	3.3 V power	Input	VCC
5	Phase 2 sense current	Output	IPHASE_2
6	Temperature sensor (1) +	Output	RT1+
7	Phase 1 sense current	Output	IPHASE_1
8	Temperature sensor (1) –	Output	RT1-
9	Phase 3 gate drive bottom switch	Input	PHASE_DR_3B
10	Temperature sensor (2) +	Output	RT2+
11	Phase 2 gate drive bottom switch	Input	PHASE_DR_2B
12	Temperature sensor (2) –	Output	RT2-
13	Phase 1 gate drive bottom switch	Input	PHASE_DR_1B
14	Scaled HVDC voltage (+)	Output	TM_VBUS+
15	Phase 3 gate drive top switch	Input	PHASE_DR_3T
16	Scaled HVDC voltage (–)	Output	TM_VBUS-
17	Phase 2 gate drive top switch	Input	PHASE_DR_2T
18	DC bus current sense	Output	IBUS
19	Phase 1 gate drive top switch	Input	PHASE_DR_1T
20	Solenoid current sense	Output	ISOL
21	Solenoid gate drive bottom switch	Input	SOL_DR_1B
22	Solenoid gate drive top switch	Input	SOL_DR_1T
23	15 V bias power	Input	P15V
24	Power ground	Input	PGND
25	15 V bias power	Input	P15V
26	Power ground	Input	PGND

Table 15 • Connector P2H Signal Pins

P2H Singal Pin #	P2H Test Access Connector Pin Description	Signal Reference
1	Temperature sensor (2) –	RT2-
2	Temperature sensor (2) +	RT2+

P2H Singal Pin #	P2H Test Access Connector Pin Description	Signal Reference
3	Temperature sensor (1) –	RT1-
4	Temperature sensor (1) +	RT1+
5	Scaled HVDC voltage (–)	TM_VBUS-
6	Scaled HVDC voltage (+)	TM_VBUS+
7	DC bus current sense	IBUS
8	Solenoid current sense	ISOL
9	Phase 2 sense current	IPHASE_2
10	Phase 1 sense current	IPHASE_1
11	Solenoid gate drive bottom switch	SOL_DR_1B
12	Solenoid gate drive top switch	SOL_DR_1T
13	Phase 3 gate drive bottom switch	PHASE_DR_3B
14	Phase 3 gate drive top switch	PHASE_DR_3T
15	Phase 2 gate drive bottom switch	PHASE_DR_2B
16	Phase 2 gate drive top switch	PHASE_DR_2T
17	Phase 1 gate drive bottom switch	PHASE_DR_1B
18	Phase 1 gate drive top switch	PHASE_DR_1T
19	Power ground	PGND
20	3.3 V power	VCC
21	15 V bias power	P15V
22	Power ground reference	GND_REF
23	Phase 3 sense current	IPHASE_3
24	Power ground	PGND

Table 16 • Connector P2S Signal Pins

P2S Singal Pin #	P2S Test Access Connector Pin Description	Signal Reference
1	External HES phase 1 input	EXT_HES_IN1
2	External HES phase 1 input return	EXT_HES_IN1_RTN
3	External HES phase 2 input	EXT_HES_IN2
4	External HES phase 2 input return	EXT_HES_IN2_RTN
5	External HES phase 3 input	EXT_HES_IN3
6	External HES phase 3 input return	EXT_HES_IN3_RTN
7	Drive enable	DR_EN
8	Program 1	PRG_1
9	Program 2	PRG_2
10	Control receive	COM_RX
11	Control transmit	COM_TX
12	Monitor transmit	MON_TX
13	No connect	NC
14	No connect	NC
15	No connect	NC
16	No connect	NC
17	No connect	NC

P2S Singal Pin #	P2S Test Access Connector Pin Description	Signal Reference
18	No Cconnect	NC

7.1 Suggested Mating Connector List

The following table lists the mating connector references for the user to interface with the I/Os on the evaluation board.

Table 17 • Mating Connector Reference Part Numbers

Connector Reference Designator	Part Number	Manufacturer	Description
J1 to HPD	TCSD-13-D-04.00-01-F-N	Samtec	Ribbon cable, IDC receptacle, 26 ways, 4 in, 101.6 mm, 2 mm
J4 to J3	TCSD-13-D-02.00-01-F-N	Samtec	Ribbon cable, IDC receptacle, 26 ways, 2 in, 50.8 mm, 2 mm
P1 (for COM and MON signals)	TTL-232R-3V3	Future Technology Devices International Ltd.	TTL-232R-3V3—cable, USB to TTL level, serial converter, 1.8 m
JP1	2SN-BK-G	Samtec	2SN-BK-G—jumper (Busbar), shunt, Samtec TMMH, TMM, MTMM, MMT, TW, LTMM, ZLTMM, TSH, and EHT series connectors
TB1, positive	934160101	Hirschmann Test and Measurement	Test lead, 0.64 mm square pin socket to 4 mm banana plug, red, 60 V, 3 A, 1 m
TB1, negative	934160100	Hirschmann Test and Measurement	Test lead, 0.64 mm square pin socket to 4 mm banana plug, black, 60 V, 3 A, 1 m
P2S, P2H	PSG-JMP150MF	pro-SIGNAL	Jumper cable, Raspberry Pi breakout, male-to-female connector, 150 mm length
P2S, P2H	PSG-JMP150FF	pro-SIGNAL	Jumper cable, jumper wires for Gertboard headers, female-to-female connector, 150 mm length
P1	5-747913-2	TE Connectivity	D sub connector, 25 contacts, receptacle, AMPLIMITE HDP-20 series, metal body, solder
J4B	L77HDA26S	Amphenol	D sub connector, high density, 26 contacts, receptacle, HD series, steel body, solder
PW1	SPC21361	Multicomp	DC power connector, plug, 5 A, 9.5 mm, cable mount, 2.5 mm
P5 (on controller PWA)	MWDM2L-31SSB	Glenair	D-sub micro-D connectors MICRO D SLDRCUP CON 31CNT SZ #26 SKT

8 Tutorial

The following tutorial demonstrates the evaluation of the PCM and HPD (with controller card) in pre-programmed mode for a nominal load condition of 12.5 A peak magnitude and maximum load condition of 25 A peak magnitude, as described in Table 6 (see page 10).

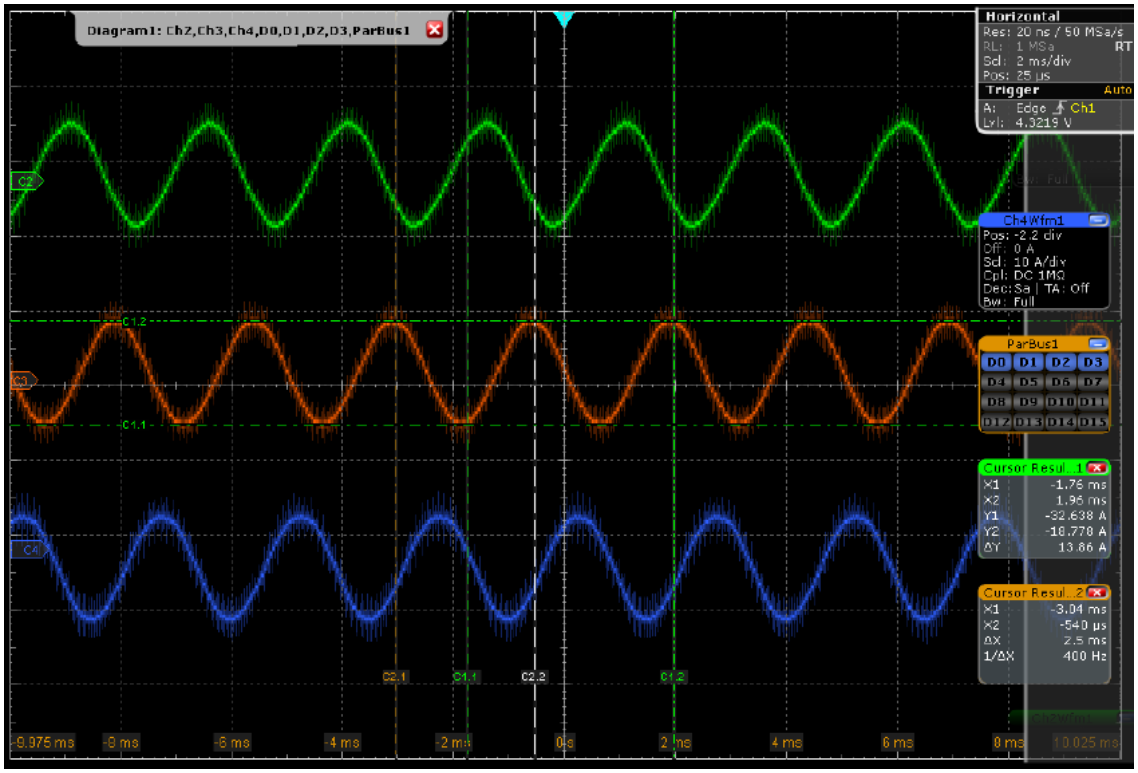
8.1 Evaluation of PCM in Pre-Programmed Mode

The following steps describe how to perform the evaluation of the PCM using the pre-programmed configuration for 12.5 A load condition:

1. Connect the PCM unit for evaluation as shown in Figure 4 (see page 8). Refer to the MAICMMC40X120 datasheet for PCM Power terminal assignment.
   a. Connect the HVDC input across terminals S1 (+) and S2 (–) of the HPD.
   b. Connect the three-phase load (inductive or motor load) to the output terminals S3, S4, and S5 (Phase A, Phase B, and Phase C, respectively).
2. Install the Jumper JP1 between pins 1–2 and pin 3–4 for mode '01'.
3. Apply the 15 V power to the PCM evaluation board.
4. Monitor the PWM signals at connector P2H: pins 11–18 generated through the pre-programmed mode '01'.
5. Increase HVDC input voltage from 0 VDC to 540 VDC.
6. Measure the three-phase AC output current, solenoid output current, and telemetry signals for the PCM.

The following image shows a typical three-phase output current measured on the PCM at the three phases (S3, S4, and S5). The following measurements are recorded at 533 VDC input with a peak-to-peak magnitude of 13.86 A.

Figure 8 • PCM Three-Phase Output Current



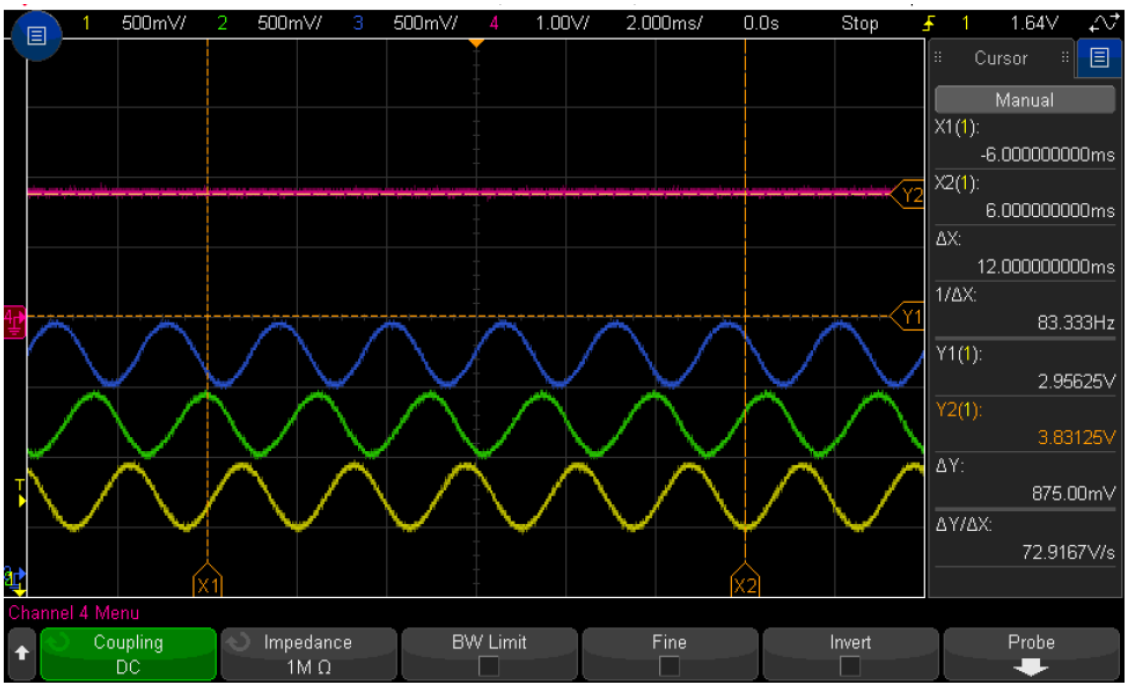
8.2 Evaluation of HPD with Controller Card in Pre-Programmed Mode

The following steps describe how to perform the evaluation of the HPD with controller card using the pre-programmed configuration for 25 A load condition:

1. Connect the HPD with the controller card for evaluation as shown in Figure 4 (see page 8). Refer to the MAIPDMC40X120 datasheet for HPD Power terminal assignment.
   a. Connect the HVDC input across terminals S1 (+) and S2 (–) of the HPD.
   b. Connect the three-phase load (inductive or motor load) to the output terminals S3, S4, and S5 (Phase A, Phase B, and Phase C, respectively).
2. Install the Jumper JP1 between pins 5–6 and pin 3–4 for mode '10'.
3. Apply the 15 V power to the PCM evaluation board.
4. Monitor the PWM signals at connector P2H: pins 11–18 generated through the pre-programmed mode '10'.
5. Increase HVDC input voltage from 0 VDC to 540 VDC.
6. Measure the three-phase AC output current, solenoid output current, and telemetry signals for HPD.

The following image shows the telemetry signal measurements of the three-phase output current and input HVDC voltage on the HPD. The scaled measurement of 500 mVpp for the three-phase current corresponds to 13.86 A and 1.78 V, and the HVDC input voltage corresponds to 533 VDC.

Figure 9 • Three-Phase Current and Input HVDC Telemetry Measurements on HPD



8.3 Reading Digital Data from the Evaluation Board

The following data format is applicable to firmware programming modes: '01', '10', and '11'. The digitized data from the evaluation board is transmitted to the STE through single-ended LVTTL signals for the COM_TX and MON_TX signals. Similarly, the user shall transmit single-ended LVTTL signals for COM_RX to the evaluation board. Internally on the evaluation board, these LVTTL signals are converted into LVDS format for PSDI communication with the PCM.

The STE is the master while the PCM is in the slave mode. The communication protocol consists of the master sending one command byte and the slave returning 1000 bytes of telemetry data. Upon receiving a telemetry request command, the digitized telemetry data—such as HVDC bus voltage, three-phase output current, HES rotor position current, and PCM operation status—is transmitted to the telemetry port. Full duplex series communication with 921,600 bps baud rate and LVTTL single-ended signals are used. The transmit and receive words comprise a start bit, eight data bits, two stop bits, and no parity bit.

The following table shows the master command and the corresponding telemetry data being sent out.

Table 18 • Request Command Word Definition

Master Command	Return Data Type	Total Return Byters	Number of Sets	Data Format
0x01	Three-phase current	1000	166	6 bytes each set Byte 0: Phase A lower byte Byte 1: Phase A upper byte Byte 2: Phase B lower byte Byte 3: Phase B upper byte Byte 4: Phase C lower byte Byte 5: Phase C upper byte
0x02	Solenoid current	1000	500	2 bytes each set Byte 0: Lower byte Byte 1: Upper byte
0x04	HVDC bus voltage	1000	500	2 bytes each set Byte 0: Lower byte Byte 1: Upper byte
0x08	HES position	1000	166	6 bytes each set Byte 0: Phase A lower byte Byte 1: PhaseA upperbyte Byte 2: Phase B lower byte Byte 3: Phase B upper byte Byte 4: Phase C lower byte Byte 5: Phase C upper byte
0x10	PCM status	1000	500	2 bytes each set Byte 0: Lower byte Byte 1: Upper byte
Others	Reserved—do not use			

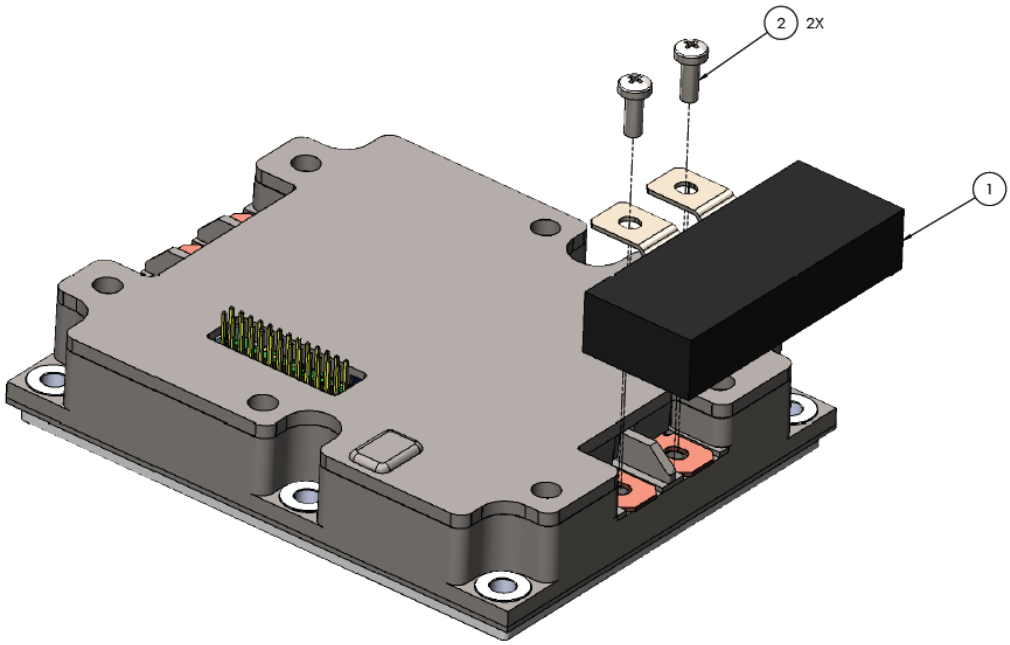
Note: For more information on PSDI, refer to Appendix A (see page 25).

9 Design Guidelines

The following recommendations allow the user to realize the best performance of PCM and HPD.

- Ensure that all low-level input and output signals have minimum cable length to reduce noise propagation.
- Circuit parasitics can cause high dv/dt in SiC MOSFETs while switching at high frequency for high-power applications. Hence, stray inductance should be minimized between the HVDC input terminals of the PCM (S1 and S2) and the DC link capacitor.
    - Microsemi suggests using a nominal snubber capacitance of 0.22 uF (±10%), 1200 VDC mounted directly across the HVDC input terminals: S1-S2. This capacitor minimizes the effect of the residual DC inductance between the DC link capacitor and the PCM. The following image shows the suggested mounting for the input snubber capacitance on the HPD.

Figure 10 • Snubber Capacitor Mounting



1. Align the center of the holes in the snubber cap terminals with the holes in the input terminals on the HPD as shown in the diagram.
2. Tighten the M3 screws to 0.35±0.05 Nm to fasten the snubber cap to the HPD.

10 Ordering Information

The following table lists the ordering information for the PCM and HPD.

Table 19 • Ordering Information

Part Number	Description
EVAL-MAI-PWA	Evaluation kit (no HPD or PCM)
EVAL-MAIPDMC40X120A	Evaluation kit (including HPD)
EVAL-MAICMMC40X120A	Evaluation kit (including PCM)

11 References

This section lists references cited in this user guide.

1. Datasheet: Power Core Module, MAICMMC40X120, Rev 1.2, A150-0002 https://www.microsemi.com/document-portal/doc_download/136391-maicmmc40x120-aviation-power-core-module-datasheet
2. Datasheet: Hybrid Power Drive, MAIPDMC40X120, Rev 1.1, A150-0001 (https://www.microsemi.com/document-portal/doc_download/136394-maipdmc40x120-hybrid-power-drive-datasheet)
3. Power Core Module Thermal Characteristics Application Note, Rev 1.0, A160-0002 (https://www.microsemi.com/document-portal/doc_download/136393-maicmmc40x120-power-core-module-thermal-characteristics-application-note)
4. Power Core Module Mounting Application Note, Rev 1.0. A160-0001 (https://www.microsemi.com/document-portal/doc_download/136392-maicmmc40x120-power-core-module-mounting-application-note)
5. Commercial Aviation Solutions (https://www.microsemi.com/document-portal/doc_download/132179-commercial-aviation-solutions)
6. Aviation Intelligent Power Solutions (https://www.microsemi.com/document-portal/doc_download/136016-aviation-intelligent-power-solutions)
7. Aviation Products Directory (https://www.microsemi.com/product-directory/non-radiation-hardened-devices/3803-high-reliability-intelligent-power-solutions)

12 Appendix A—Communications Protocol

The protocol in Appendix A defines the communication standard for users to evaluate the PCM using the PCM evaluation board. The PCM communication protocol is referred to as the PSDI (PCM serial digital interface).

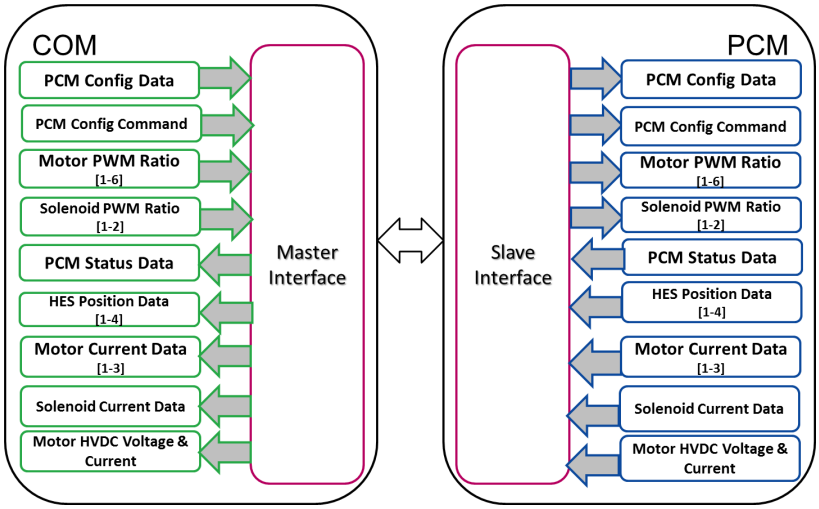
12.1 Functional Description

The PSDI system is designed to communicate between the PCM and COM. This communication bus provides a serial digital interface to control the three-phase bridge and the solenoid driver of the PCM from the external master control unit called the command module (COM).

The COM transmits the commands to the PCM to generate the PWM controls for the three-phase bridge and solenoid driver. The PSDI is designed to replace the conventional discrete analog and digital interfaces by a single serial digital channel. The functional block diagram of the PSDI implementation is shown in the following figure. As illustrated below, the PCM implementation is defined between the PCM and COM modules only for the preliminary design. Later stages of PSDI development shall also include unidirectional transmit channel from the PCM to the MON.

The three-phase bridge and solenoid PWM ratios are commanded from the COM through the PSDI bus. The real-time digitized telemetry data such as HVDC bus voltage, three-phase output current, HES rotor position current, and PCM operation status is transmitted to the COM at an update rate controlled by the COM bus cycle rate in the active mode.

Figure 11 • PSDI Preliminary Functional Block Diagram



12.1.1 PSDI Operation

This section details the PSDI operation of the PCM device.

12.1.1.1 PSDI Bus Characteristics

This following are PSDI bus characteristics of the PCM device:

- The physical layer is based on point-to-point transmit and receive links at the LVDS level using Manchester encoding.
  - The LVDS receivers shall provide a load impedance of 100 Ω.
- Data bit rate is at 20 MHz. Data exchange is periodic with a cycle time of 100 µs.
- A "0" data bit is represented by a LOW for 25 ns followed by a HIGH for 25 ns.
- A "1" data bit is represented by a HIGH to LOW transition.

- Each message is composed of three header words and eleven payload words followed by one CRC word.
- The last word in the payload message is the CRC word for error detection of the transmitted message.
- The CRC polynomial being used for the CRC calculation is 1021h.

12.1.1.2 PSDI Functional Definitions

This following are the PSDI functional definitions of the PCM device:

- The COM is defined as the master module while the PCM is defined as the slave module.
- All data exchanges are initiated by the master through master messages.
- The slaves transmit slave messages only when commanded by the master.

12.1.1.3 PSDI Operating Modes

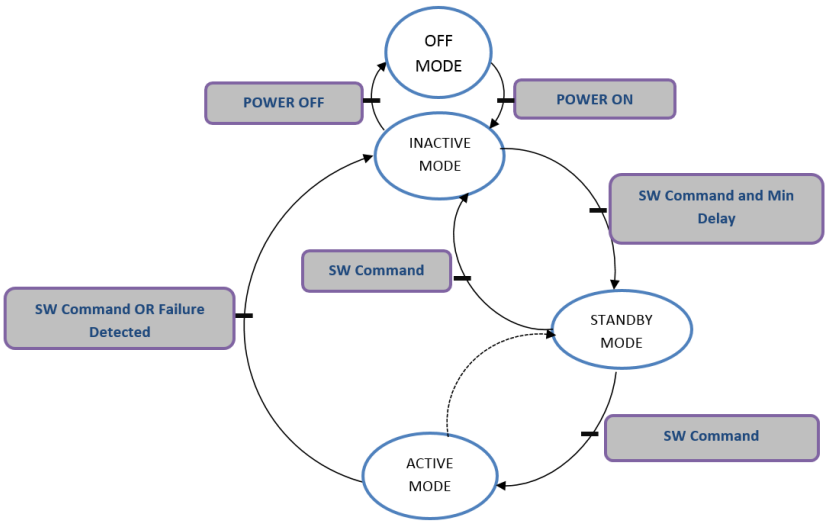
The four PSDI operating modes consist of the following: OFF Mode, INACTIVE Mode, STANDBY Mode, and ACTIVE Mode. The design transition state flow diagram is shown in the PSDI State Flow Chart (see page 26).

The following list describes the PSDI operating modes:

- OFF MODE: In OFF mode, there is no communication between the PCM and COM.
- INACTIVE MODE: In INACTIVE mode, power is applied but there is no communication between the PCM and the COM. After power-up, the PCM is in an inactive state waiting for the master-initialization message.
- STANDBY MODE: The COM generates the initialization message to the PCM. Upon receiving the initialization message, the PCM transitions into the STANDBY mode and transmits back the slave descriptor message. The COM validates the slave descriptor message and transmits the PWM command message to the PCM.
- ACTIVE MODE: Upon receiving the PWM command message from the COM, the PCM enters the ACTIVE state and sends back the data acquisition message. This process is repeated every time a new PWM command message is received.
- If consecutive transmission errors are detected, the PCM returns to the inactive mode. A master command is needed to bring the PCM out of INACTIVE mode.

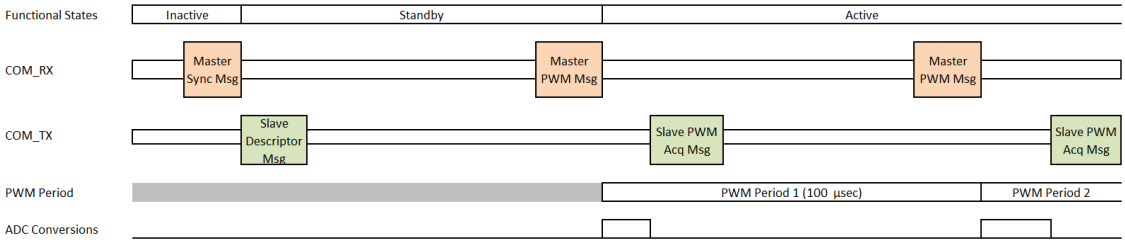
The following image shows the PSDI state flow chart of the PCM device.

Figure 12 • PSDI State Flow Chart



The operating timeline of the PSDI bus is described in the following image.

Figure 13 • PSDI Operating Timeline



Source	Frame Type	Frame Sub-Type	Message
Master	0	001	Sync
Master	0	010	PWM
Slave	1	001	Descriptor
Slave	1	010	PWM Acquisitions

12.1.1.4 PSDI Message Definitions

There are two types of master command messages and two types of slave return messages being transmitted on the PSDI in the following sequence:

1. The Master Sync message commands the PCM operating mode and initialization message.
2. The PCM will return the Slave Description message back to the master once the Master Init message is received.
3. The other command message being sent to the PCM is the Master PWM message. This message informs the PCM of the PWM ratios that should be applied to the switches to generate the three-phase and solenoid current. Note that the PCM shall generate the complementary PWM ratios for all bottom switches and insert dead time on the output transitions.
4. Upon receiving the Master PWM message, the PCM starts the next PWM cycle, performs ADC conversions to gather telemetry data, and sends out the Slave Acquisition message that contains telemetry and status information.

The following figures show detailed descriptions of the four PSDI message types.

Figure 14 • Master Sync Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	1	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0
		Source ID				↑ Master frame type	Frame Subtype			Start of cycle indication				Frame destination			
3	Header word 3	1	0	0	0	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		Slave message request				PICOL cycle count								Slot number			
4	Payload word 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Initialization message															
5	Payload word 2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
6	Payload word 3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
7	Payload word 4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
8	Payload word 5	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
9	Payload word 6	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
10	Payload word 7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
11	Payload word 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Payload word 9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 2 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 15 • Master PWM Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	1	1	1	0	0	0	1	0	0	0	0	0	1	0	X	X
		Source ID				Master frame type	Frame Subtype			Start of cycle indication				Frame destination			
3	Header word 3	1	0	0	0	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		Slave message request				PICOL cycle count								Slot number			
4	PWM1 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PWM ratio {"000h" => 0%, "FA0h" => 100%)															
		PWM signal polarity {"0' => Inverted, "1" => Normal)															
		PWM shape {"0" => Asymmetric, "1" => Symmetric)															
		Dead time {"0" => No dead time, "1" => Inserted dead time)															
		Safe state {"0" => Inverter/Solenoid open, "1" => Normal operation)															
5	PWM1 low side	To be Ignored															
6	PWM2 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
7	PWM2 low side	To be Ignored															
8	PWM3 high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
9	PWM3 low side	To be Ignored															
10	Solenoid high side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
11	Solenoid low side	1	1	1	1	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
12	Bridge dynamic config	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
		Provision												Max # of consecutive error			
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 2 – 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 16 • Slave Descriptor Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	0	0	0	1	1	0	0	1	X	X	X	X	X	X	X	X
		Source ID				↑ Slave frame type	Frame Subtype			PCM status							
3	Header word 3	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		PCM status				PICOL cycle count								Slot number			
4	Payload word 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
		Provision												PCM module size			
5	Payload word 2	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		OTAN code															
6	Payload word 3	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		PCM part number															
7	Payload word 4	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		PCM serial number															
8	Payload word 5	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0
		PWM2 dead time (1 LSB => 10ns)								PWM1 dead time (1 LSB =>10ns)							
9	Payload word 6	0	0	1	1	0	0	1	0	0	0	1	1	0	0	1	0
		Solenoid dead time (1 LSB => 10ns)								PWM3 dead time (1 LSB => 10ns)							
10	Payload word 7	0	0	0	1	1	0	0	1	0	0	0	0	1	0	1	0
		PCM max output current (12A to 100A, LSB = 1A)								PCM max output power (5KW to 41KW, LSB = 500W)							
11	Payload word 8	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
12	Payload word 9	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
13	Payload word 10	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
15	CRC of words 2 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Figure 17 • Slave PCM Acquisition Message

#	Word Description	MSB b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	LSB b0
1	Start of frame	1	1	1	1	0	0	0	0	1	1	0	0	1	1	0	0
2	Header word 2	0	0	0	1	1	0	1	0	X	X	X	X	X	X	X	X
		Source ID				↑ Slave frame type	Frame Subtype			PCM status							
3	Header word 3	X	X	X	X	Y	Y	Y	Y	Y	Y	Y	Y	0	0	0	0
		PCM status				PICOL cycle count								Slot number			
4	Payload word 1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
		N/A															
5	Payload word 2	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM HVDC Voltage (3.2768LSB/V, 0V to 1250V, "X000h" to "XFFFh")															
6	Payload word 3	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 1 Current { 40.65LSB/A, -50A to 50A, "X000h" to "XFFFh")															
7	Payload word 4	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 2 Current { 40.65LSB/A, -50A to 50A, "X000h" to "XFFFh")															
8	Payload word 5	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM Phase 3 Current {40.65LSB/A, -50A to 50A, "X000h" to "XFFFh")															
9	Payload word 6	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Solenoid Current { 163LSB/A, -12.5A to 12.5A, "X000h" to "XFFFh")															
10	Payload word 7	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 1 (LSB = 1mV)															
11	Payload word 8	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 2 (LSB = 1mV)															
12	Payload word 9	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		Rotor Position 3 (LSB = 1mV)															
13	Payload word 10	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y
		PCM status (TBD)															
14	Payload word 11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		Provision															
15	CRC of words 2 - 14	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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